Chips to Startup Programme

इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
सत्यमेव जयते

Implementation Agency	Academic Partners	MSME partner	End User

Ref. No. CRG/2023/001 **10-10-2023**

Advertisement for Junior Research Fellow (JRF), Senior Research Fellow (SRF) and Research Assistant (RA)

Applications are invited for the position of Junior Research Fellow (JRF) Senior Research Fellow (SRF) and Research Assistant (RA), in a research and development project **(under CHIPS TO START-UP PROGRAMME (C2S) CATEGORY – I PROPOSALS)** for the duration of **2 years (2023-2025)** with the following details:

Title of the project:

"DESIGN AND DEVELOPMENT OF GROUND PENETRATING RADAR WITH ON-FIELD RECONFIGURATION CAPABILITY APPLICABLE TO SUSTAINABLE INDUSTRIAL AND AGRICULTURAL PURPOSES"

Candidates with experience or knowledge in the following domains can apply:

1. PCB design
2. Analog & mixed signal design
3. RF CMOS
4. Antenna design
5. CMOS layout design and schematic capture
6. FPGA design
7. Microcontrollers and embedded systems

Familiarity with programming languages:

1. HDL
2. MATLAB
3. Embedded C
4. C/C++
5. Python

Job description:

1. System level design of GPR system
2. Design and development of image processing software for ground penetrating radar
3. System in Package of GPR system
4. RF front end design (LNA, Mixers, Power Amplifiers, Buffers) of GPR and Antenna Design
5. ASIC design of base band system
6. FPGA development and prototyping

7. Analog design and mixed signal design (data converters)

Research staff will be working from Cambridge Institute of Technology campus and visiting collaborating Institute as per the need basis. Fresher's (with UG/PG/PhD) qualification can apply for the above positions. The core team will be able to train the team members and then deployed on the project. Software familiarity – SYNOPSYS, CANDENCE, Mentor Graphics (Siemens), Ansys, MATLAB, PCB Design

Job positions:

Name of the Position	No. of positions/ vacancies	**Qualification**
Junior Research Fellow (JRF)	4	BE – ECE M.Tech – ECE, VLSI or any other equivalent discipline
Senior Research Fellow (SRF)	1	M.Tech – ECE, VLSI or any other equivalent discipline PhD - ECE
Research Assistant (RA)	2	M.Tech – ECE, VLSI or any other equivalent discipline – 5 years experience PhD - ECE

Terms and Conditions for JRF, SRF & RA are as follows

Age Limit: - Not more than 28 Years for JRF, 35 years for SRF and RA. Age relaxation as per DST, GOI norms

Salary: - As per DST norms + HRA

Qualification:

Essential Qualifications: - M.Tech./M.E. in Electronics &Communication Engineering with a minimum of 60% aggregate score (6.5/10 CGPA) for JRF & RA, Ph. D degree from reputed University for SRF. Candidate must have qualified GATE examination (old gate score is also considered). Proof of M.Tech/ M.E/ Ph. D certificate has to be provided during the interview.

Duration: 01 year or up to the termination of the project, subject to annual performance review. The candidate is encouraged to apply for PhD at Cambridge Institute of Technology or BMSCE or Reva University, Bangalore or SNS college of Technology, Coimbatore, Tamil Nadu.

Roles and Responsibilities: The candidate is required work on the project assigned and will be reporting to respective principal investigators of respective colleges. Project progress will be monitored and the candidate needs to participate in all review meetings. All the team members will be responsible for successful completion of project. Product development, testing and field studies need to be carried out. Report preparation, publication, patenting and technical documentation will be part of the project.

How to apply: Interested candidates must apply by filling out the attached application form along with the following documents (1) Cover letter (2) Bio-data with passport-sized photograph, (3) Scanned copies of educational certificates and mark sheets (class-X onwards) (4) GATE qualified certificate and (5) Scanned copies of Proof for research experience, special achievements and publications, if any.

The soft copies of the application form and required documents (pdf format) must be **emailed to girish.ece@cambridge.edu.in by 17th October 2023**. The email address for correspondence is given above. Only shortlisted candidates will be intimated by email and called for an interview. The position is available immediately. The appointment will be on a purely temporary basis co-terminus with the project.

APPLICATION FOR THE POST OF JUNIOR RESEARCH FELLOW / SENIOR RESEARCH FELLOW (SRF) / RESEARCH ASSISTANT

For Office Use:	Paste your recent Passport size photo
Serial Number:	
Eligible for Written exam/Interview: Yes / No	
Verified the Certificates:	

1. Name:	
2. Father's Name:	
3(a). Date of Birth: (DD/MM/YYYY)	**3(b).** Nationality:

4. Contact information:

(i) Address for communication:	
(ii) Mobile No:	
(iii) Email ID:	

5. Educational Qualifications*

Class	**Subject/ Stream**	**Board/ University**	**Name of Institute**	**Marks/ CGPA**	**Year of Passing**
X					
XII					
B.E/B.Tech.					
M.E/M.Tech.					
Ph. D					

Competitive Exam	Qualified	Marks / Rank	Year
CSIR-UGC NET	Yes / No		
GATE	Yes / No		

***Attach self-attested copies of all certificates.**

6. Work Experience, if any (in years) ……

Organization	Designation	Duration	Responsibilities

7. Number of Publications: (Attach a separate list of publications with full details)

National	International

8. Workshop/Training programs attended*:

Sl. No.	Details

***Attach separate sheet (if required)**

9. Other Achievements*:

Sl. No.	Details

***Attach separate sheet (if required)**

Declaration: All the above particulars provided by me are true to the best of my knowledge and I understand that, if found incorrect, I may be disallowed to appear in the interview/test.

Date:

Place:

Signature of the Candidate

Note: Attach the list of enclosures along with the application.