B.M.S. COLLEGE OF ENGINEERING, BENGALURU-19

Autonomous Institute, Affiliated to VTU

Department of Medical Electronics Engineering

Title:

Two-week Value-Added course
on
VLSI DIGITAL: THINK, DESIGN & SIMULATE- 1.0

VLSI Digital: Think, Design & Simulate- 1.0 was a two-week value-added course organized by the Department of Medical Electronics Engineering of BMS College of Engineering, in collaboration with BMSCE IEEE. The course was a walk-through of VLSI design, Verilog and their diverse applications.

Objective:

This Value added course on Digital Design covers the complete digital design and explains the concepts of combinational, sequential and FSM designs and coding for synthesis and simulation. It comprehends the concepts of hardware description language and basic concepts like data types and operators. Then it explains the advanced concepts like assignments, procedural blocks, synthesis coding style and test bench coding, in detail with various examples. Doing the labs will make you a hands-on RTL programmer.
The concepts discussed included digital design, combinational circuits and coding for synthesis and simulation. An introduction to Hardware Description Language, data types and operators was given. The course enlightened the students about the ever-evolving world of chip design, and enhanced the skills required for a career in the same.

Outcome:

At the end of the course, the students will be able to:

1. To understand the digital fundamentals and approach any kind of real time digital designs.
2. Appreciate the constructs and conventions of the Verilog HDL programming.
3. Develop digital circuits using gate level, data flow and behavioral modeling.
4. Perform functional verification of above designs using Test Benches.
5. It trains the students extensively on the Verilog HDL programming and makes them a hands-on RTL designer, which can be an aid in future growth.

Target Audience:

Students and research scholars from BMSCE and other institutions.

Resource Persons:

1. Dr. Suma M. S.
   Professor, Department of Medical Electronics
2. Dr. Jisha P.
   Assistant Professor, Department of Medical Electronics
3. Mrs. Namita Palecha
   Research Scholar, BMSCE
4. Mr. Chandrashekar Patil
   Sr. ASIC Design Engineer, CISCO.

Brochure:

Attached as Annexure -1

Financial Model:

Model -III:

Resource persons from department, industry, other academic Institutions.
To treat the event on the model of consultancy.
Hence:

30% of revenue generated to college
70 % of revenue for to be used for:

Honorarium to external resource persons, as per college norms
Internal resource persons for professional activities/gadgets (webcam, speaker, laptop, professional body membership, registration and travel for presenting paper in National/ International conference/ any other)

Association with Industry/ Alumni if applicable:

Mr. Chandrashekar Patil,
Sr. ASIC Design Engineer, CISCO.

Any Other : NIL

Course schedule and details:

Day 1- 2nd November 2022 (2PM - 5PM)
An introduction to all the concepts to be discussed in the following 10 days of the VAC was given. An overview of the VLSI chip design procedure was given. The steps in VLSI Design Flow were discussed, along with the types of design.

Day 2- 3rd November 2022 (2PM - 5PM)
The theoretical design of basic gates and combinational circuits was discussed. The students were given an introduction to multiplexers. Mux-based design of logical gates and combinational circuits were discussed.

Day 3- 4th November 2022(2PM - 5PM)
An introduction to Verilog HDL Programming was given. Data types and operators were explained. The concepts of Data Flow modelling were discussed.

Day 4- 5th November 2022 (2PM - 5PM)
The students were introduced to ModelSim software and had hands-on experience in digital design using Verilog programming. Students designed basic gates and mux-based circuits using Verilog.

Day 5- 6th November 2022 (2PM - 5PM)
Students worked on online assignments related to topics discussed in the course.

Day 6- 7th November 2022 (2PM - 5PM)
Students learnt the concepts of conditional operators and applied them to design mux-based circuits, decoders and encoders.

Day 7- 8th November 2022 (2PM - 5PM)
Students studied the design of comparator and adder circuits and programmed the same using Verilog.

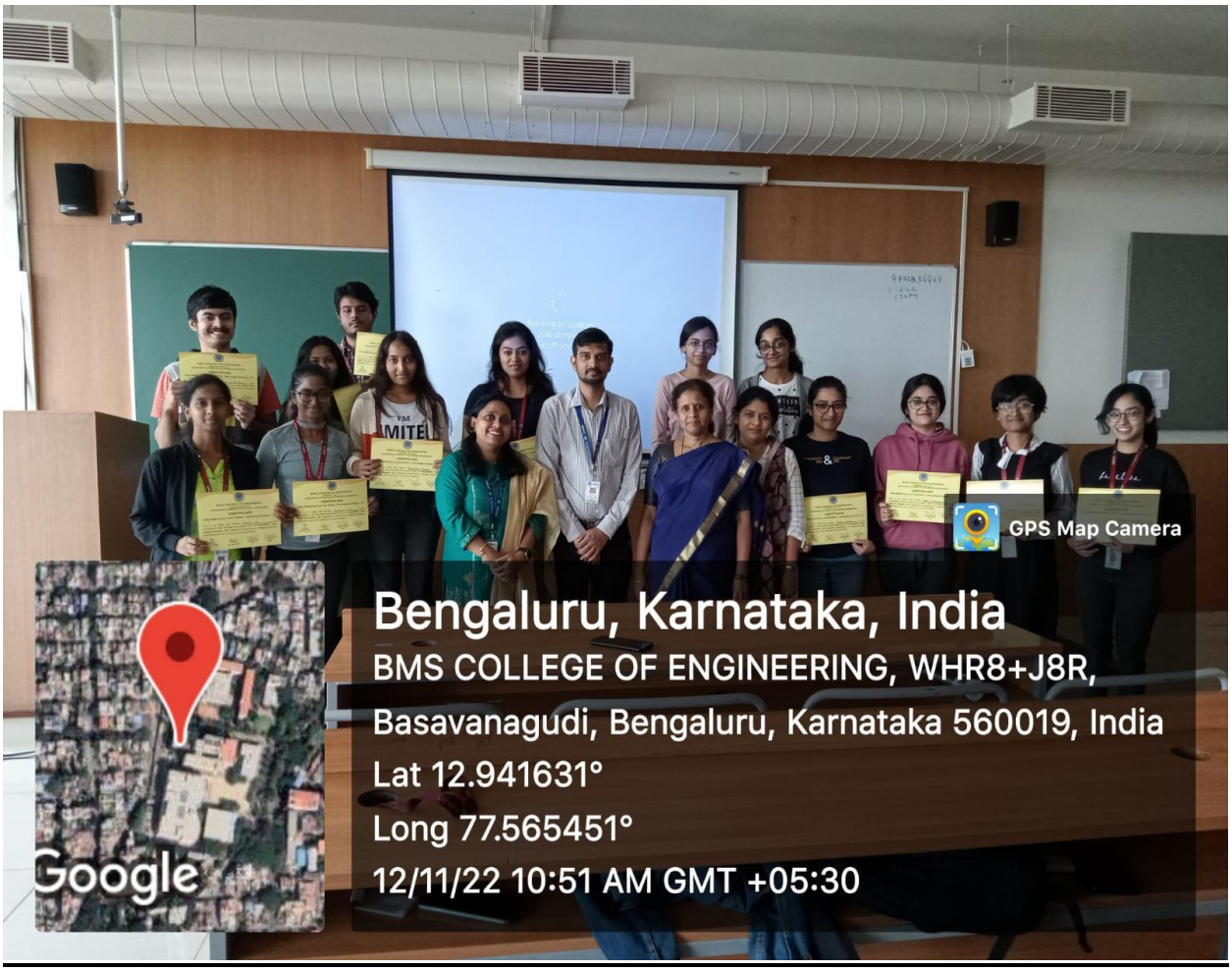
Day 8- 9th November 2022 (2PM - 5PM)
An interactive session was conducted by Mr. Chandrashekar Patil, Sr. ASIC Design Engineer, CISCO on VLSI chip design in the industry. He discussed the real world applications of concepts discussed in the course.

Day 9- 10th November 2022 (2PM - 5PM)
Students learnt the concepts of structural modeling and applied them for operations involving a larger number of bits.

Day 10- 11th November 2022 (2PM - 5PM)
The application of VLSI Design in the biomedical sector was discussed, along with an evaluation of the students. Their feedback was also collected.

Day 11- 12th November 2022
The course was concluded with the Valedictory.

<u>Pictures of the Event</u>

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Chip design – ASIC and CAD tools
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List of Participants

1. Vani S Ramachandran
2. Chinmaya R Bhat
3. Ashwathi S
4. Apoorva M S
5. Ananya Namratha
6. Nauman Ahmed
7. Sakshi Marodia
8. Lekha M
9. Harshitha Jampala
10. Aaditya Balakrishna
11. Harshith P
12. Prathiksha Harish
13. Dhwani Sanjai
14. Sahana S
15. Prathita Gowri A K Rao
16. Umme Hani Gadiwan
17. Varshini Manjunath
18. Pravallika Swaraj
19. Saphonia Aaron. H
20. Keerthana B R
21. Ruchira Srinidhi
22. Shreyaa. P. J
23. Madhu M
24. Mohammed Ibaad

Sample certificate

B.M.S. COLLEGE OF ENGINEERING

(Autonomous under VTU)

DEPARTMENT OF MEDICAL ELECTRONICS ENGINEERING

CERTIFICATE

Value Added Course on "VLSI DIGITAL : Think, Design & Simulate – 1.0"

This is to certify that Mr./Ms. _____ has participated in the Two Week Value Added Course on **"VLSI DIGITAL : Think, Design & Simulate – 1.0"**, conducted by Department of Medical Electronics Engineering from 02-11-2022 to 12-11-2022 at BMSCE.

Dr. Jisha P Assistant Professor Dept. of ML , BMSCE	**Dr. Suma M S** Professor Dept. of ML , BMSCE	**Dr. Joshi Manisha S** Professor & HOD BMSCE	**Dr. S. Muralidhara** Principal, BMSCE