BMS College of Engineering

(Autonomous College under VTU)
Bull Temple Road, Basavanagudi, Bangalore-560019

The Department of Medical Electronics Engineering and
The Department of Electronics and Telecommunication Engineering
in association with **Angstromers Engineering Solutions Private Limited**
cordially invites you to the

Online Faculty Development Program (FDP)

Adaptability of RISC-V in Academia Research and Labs

Empowering Educators to Embrace the Future of Processor Design, RISC-V in Research and Labs.

Department of Medical Electronics Engineering,
Department of Electronics and Telecommunication Engineering

28th July 2025 - 1st August 2025
10:00 AM to 4:00 PM

Mode: **Online**

Registration Fee: ₹500/- only
Registrations close on 25th July 2025

Organised by:

Dr. R. Jayagowri
HOD, Medical Electronics Engineering

Dr. Balachandra K
HOD, Electronics and Telecommunication Engineering

Coordinated by:

Dr. Vijaylakshmi
Prof., Electronics and Communication Engineering
80508 72783

Dr. Vani
Asst. Prof., Medical Electronics Engineering
96865 75771

Dr. C. Gururaj
Prof., Electronics and Telecommunication Engineering
9986069831

Target Audience

Who Can Attend:

- **Faculty members**
- **Research scholars**
- **Postgraduate students interested in processor design and RISC-V.**

Resource persons from:
Angstromers Engineering Solutions Private Limited, Bangalore.

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Department of Medical Electronics Engineering

Department of Electronics and Telecommunication Engineering

FDP Report

Topic: "Adaptability of RISC-V in Academia Research and Labs"

Empowering Educators to Embrace the Future of Processor Design, RISC-V in Research and Labs

Program Details:

- **Organizing Departments:** The Department of Medical Electronics Engineering and the Department of Electronics and Telecommunication Engineering.
- **In Association With:** Angstromers Engineering Solutions Private Limited.
- **Dates:** July 28, 2025, to August 1, 2025.
- **Mode:** Online.
- **Timings:** 10:00 AM to 4:00 PM.

Organizing and Coordinating Team:

- **Organized By:**
  - Dr. R. Jayagowri, HOD, Medical Electronics Engineering.
  - Dr. Balachandra K, HOD, Electronics and Telecommunication Engineering.
- **Coordinated By:**
  - Dr. Vijaylakshmi K, Professor, Electronics and Communication Engineering.
  - Dr. Vani A, Assistant Professor, Medical Electronics Engineering.
  - Dr. C. Gururaj, Professor, Electronics and Telecommunication Engineering.

Target Audience

The FDP was intended for faculty members, research scholars, and postgraduate students who are interested in processor design and RISC-V.

Program Schedule & Resource Persons

- **Resource Persons:** The speakers were from Angstromers Engineering Solutions Private Limited, Bangalore. The instructors for the sessions included Dr. Cyril PrasannaRaj P, Kavinesh, Dr. Girish , Dr Gangadhar and Apoorva.
- **Daily Schedule:**
  - **Session 1:** 10:00 AM – 12:30 PM.
  - **Session 2:** 1:30 PM – 4:00 PM

Session Details:

- **Day 1:** The inauguration started at 10am. The first day of the FDP featured a session on "RISC Intro" in the morning. Dr. Girish was the instructor for this session. The afternoon session was "SPIKE Installation & Demonstration". This session was led by Kavinesh and Apoorva. The total duration of the sessions on this day was from 10:00 AM to 4:00 PM.

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- **Day 2:** The morning session on the second day focused on "ISA – Single Cycle Pipeline". The instructor for this session was Dr. Cyril PrasannaRaj P. The afternoon session was about "Implementation Examples". Kavinesh and Apoorva were the instructors for this afternoon session. The sessions ran from 10:00 AM to 4:00 PM, with a break in between.

- **Day 3:** Day three began with a morning session on "ISA – Multicycle Pipeline". This session was instructed by Dr Gangadhar. In the afternoon, Kavinesh and Apoorva presented on "Implementation Examples".

- **Day 4:** The morning session on day four was titled "Case Study in RISC-V Optimization" and was conducted by Dr. Cyril PrasannaRaj P. In the afternoon, there was a session on "Research Avenues". The instructors for the afternoon session were Dr. Cyril PrasannaRaj P, Kavinesh, and Apoorva. The sessions, like the other days, were from 10:00 AM to 4:00 PM.

- **Day 5:** The final day's morning session was on "RISC-V SoC Design" with Dr. Cyril PrasannaRaj P as the instructor. The afternoon session was a continuation of "Research Avenues". Dr. Cyril PrasannaRaj P, Kavinesh, and Apoorva were the instructors for the final session. The FDP concluded on this day, August 1st, 2025 at 4PM.

The FDP was intended to benefit faculty members, research scholars, and postgraduate students. The program aimed to empower these educators to embrace the future of processor design. The FDP focused on the "Adaptability of RISC-V in Academia Research and Labs," which would be of interest to anyone in these fields. Participants would have gained knowledge on RISC-V topics ranging from introductory concepts to case studies in optimization and SoC design. They would have also been exposed to research avenues in the field

Signature of Coordinators:

Dr. Vijaylakshmi K, Professor, Electronics and Communication Engg.

Dr. Vani A, Assistant Professor, Medical Electronics Engg.

Dr. C. Gururaj, Professor, Electronics and Telecommunication Engg.

Dr. R. Jayagowri,
HOD, Medical Electronics Engg.

Dr. Balachandra K,
HOD, Electronics and Telecommunication Engg.