Dr. Kiran Bailey

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OBJECTIVE

Provide Education and Mentorship to Engineering Students so as to enable them to achieve their goals.

WORK EXPERIENCE

5/1998 – till date

Assistant Professor

Responsibilities:

- To train the students in the latest cutting edge technology by framing suitable curriculum.
- Establish Labs and Innovation centers to encourage students to develop their products.
- Mentor and Guide UG and PG students in their research and motivate them to publish papers.
- Establish Industry interaction through various bodies.
- Procure government funding to set up infrastructure in the department.
- Author Text books in VLSI domain.
- Paper setting, Valuation and Invigilation duties.
- Examiner to other academic Institutions.
- Co-ordinate for NBA activities and other administrative activities.
- Member of First year Academic Audit Committee.
- Internship/Seminar Coordinator.
- Perform data analysis for CO and PO attainments.

EDUCATION

2008 - 2012

PhD in Electronics Engineering, VLSI Domain, Bangalore University, Bangalore

1999 - 2001

M.Tech in Digital Communication, BMSCE,VTU, Belgaum

1993 - 1997

B.E in Electronics, DSCE, Bangalore University, Bangalore

ADDITIONAL SKILLS

Cadence EDA Tools: ncverilog, simvision, genus, Innovous, virtuoso
Synopsys EDA Tools: Sentaurus TCAD, sdevice, SDE and inspect
OS: Windows, Linux
Programming: C++, Python, Verilog, System Verilog

PAPERS PUBLISHED

Kiran Bailey, K.S. Gurumurthy "Low Power Semiconductor devices at 65 nm technology node", INTERNATIONAL JOURNAL OF CIRCUITS, SYSTEMS AND SIGNAL PROCESSING , Volume 4, Issue 2, 2010, pp. 43-51,ISSN: 1998-4464.

Kiran Bailey, K.S. Gurumurthy "Modeling and Performance evaluation of UTB SGOI Devices scalable to 22 nm Technology node", WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS, Volume 9,Issue 10, October 2010, pp. 607-616, ISSN: 1109-2734.

Kiran Bailey, K.S. Gurumurthy, "3D device modeling and assessment of Triple gate SOI FinFET for LSTP applications", International Journal of Computer Theory and Engineering, IJCTE, Vol. 4, No. 5, October 2012,pp. 831-834, ISSN: 1793-8201.

Kiran Bailey, K.S. Gurumurthy and A. Prathima, "IMPACT OF DEVICE PARAMETERS OF TRIPLE GATE SOI-FINFET ON THE PERFORMANCE OF CMOS INVERTER AT 22 nm", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.5, October 2012, pp.79- 91. ISSN: 0976 - 1357 (Online); 0976 - 1527 (print).

Kiran Bailey, JhnaneshSomayaji, "Optimization of Gate Leakage for 22nm MOSFETs through Alternate High-k Materials using T-CAD simulations", International Journal of VLSI and Embedded Systems-(IJVES) ISSN: 2249 – 6556, Vol 04, Issue 02; April 2013.

Kiran Bailey, K.S. Gurumurthy, "Analysis and Modeling of High Performance and Low Power UTB SGOI Devices Scalable to sub 30 nm". 4th International conference on Latest Trends on Circuits, Systems and Signals (CSS'10), Corfu Island, Greece, July-22-25, 2010, pp. 120-123.

Kiran Bailey, K.S. Gurumurthy, "3D device modeling

and assessment of Triple gate SOI FinFET for LSTP applications", 4th IEEE International Conference on Computer Science and Information Technology, Chengdu, China during June 10 - 12, 2011.

Kiran Bailey, K.S. Gurumurthy, "Device characterization and analysis of Triple gate SOI and Bulk FinFET structures for low standby power applications", International conference on frontiers of computer science, ICFoCS 2011, JN TATA convention center, IISC, Bangalore, August 7-9, 2011

Kiran Bailey, Vijayalakshmi. V, K.S. Gurumurthy, "Effect of Fin doping on Static power dissipation and gate delay for triple gate bulk FinFET", International conference on frontiers of computer science, ICFoCS 2011, held at JN TATA convention center, IISC, Bangalore, August 7-9, 2011.

PATENTS FILED

Application No: 201941025817
"Radio Frequency Identification based user database management system"- 2019
