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Formalizing Feature Model Integrity: A Typing System and Refactoring Approaches for Improving Software Product Line Design

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Abstract

Feature modeling plays a pivotal role in the development of Software Product Lines (SPL), enabling the systematic representation of common and variant features across a family of products. However, despite its widespread use, there is a lack of formalization in the typing and well-formedness rules for feature models, leading to potential design flaws and inconsistencies. This paper introduces a comprehensive formalization of feature model typing rules and identifies a catalog of "bad smells" that indicate suboptimal designs in feature models. An automated toolchain is introduced for detecting bad smells and ensuring adherence to defined typing constraints in feature models. Additionally, a set of refactoring techniques is proposed to address detected issues and enhance the overall design of feature models. The work provides a solid foundation for ensuring that feature model transformations, such as refactorings, preserve model integrity, and supports scalable, maintainable, and error-free feature model management in SPLs.

1. Introduction

Feature modeling is a widely used technique for representing concepts within a software domain. Various systematic reuse and domain-driven approaches, such as Software Product Line [1], [2], Generative Programming [3], and Software Factories [4], incorporate feature-based notation as a fundamental component.

Despite recent advancements in defining semantics [5] and reasoning about feature models, there remains a lack of formal definitions for *type-checking* and *well-formedness rules*. Even when correctly typed, a feature model may exhibit structural issues. Similar to software programs [6], certain patterns, referred to as bad smells, can indicate potential structural weaknesses.

The figure illustrates a feature model. No formal definition explicitly states the properties that a well-typed model must satisfy, which is crucial when performing feature model transformations. Transformations should ensure that a well-typed model remains well-typed, avoiding the introduction of type errors.

As feature models scale to hundreds of features, their structural integrity may deteriorate. For instance, in the model shown in Figure 1, a mandatory feature B implies an optional feature D. This type of constraint raises concerns, as it effectively alters the cardinality of feature D, making it mandatory under specific conditions. Such constraints are considered indicators of suboptimal design (*bad smells*) and should be identified and refactored to enhance the feature model's integrity.

This study formalizes a type system for feature models and introduces a catalog of bad smells associated with their structure. Additionally, refactoring techniques are proposed to mitigate these issues. The formalization presented herein serves multiple purposes, two of which are explored in Section 5.

A type-checking process for feature models is essential before applying transformations such as those introduced by Bonifa´cio and Borba [7]. Moreover, this framework is beneficial for other automated product line engineering methodologies. Furthermore, the formalization aids in validating that feature model refactorings [8] do not introduce type errors. In addition to preserving all configurations of the original model, this approach guarantees that a well-formed feature model remains well-formed after refactoring.

Beyond type correctness, this study investigates structural patterns indicative of design deficiencies. Detecting bad smells is crucial in the reactive approach to Software Product Line (SPL) development, as it facilitates the identification of recurring faults during the modeling and evolution of large-scale feature models containing numerous features and constraints.

In summary, the contributions of this research are threefold:

- Establishing well-formedness rules and a type system that define the criteria for a well-typed feature model (Section 2).
- Developing a catalog of bad smells within feature modeling to assist business analysts in identifying common faults during feature model design and evolution (Section 3).
- Presenting a tool for verifying feature model type correctness, detecting bad smells, and applying refactorings to mitigate these issues (Section 4).

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2. Type System

Ensuring *type safety* in feature models is essential to prevent erroneous or undesirable analysis outcomes. A feature model is considered well-typed if it satisfies a set of well-formedness constraints. This section presents these rules both informally and through a formalization language that integrates conventional notation with the PVS language [9]. The constraints defined represent a minimal set derived from fundamental requirements for verifying the validity of feature selections within a feature model.

A formal definition of feature models is introduced, consisting of a root feature, relations, features, and formulae. The `Feature` component is an uninterpreted type associated with a name, whereas `Relation` is defined as a PVS datatype comprising four distinct categories: optional (`OPT_REL`), mandatory (`MAND_REL`), alternative (`ALT_REL`), and Or-feature (`OR_REL`). The first two relation types associate two features, while the latter involve a parent feature and a set of child features. Additionally, a set of formulae is considered to define constraints within the feature model, utilizing core logical constructs such as negation, conjunction, and implication.

```
FM: type = [#
  root: Feature,
  relations: set[Relation]
  features: set[Feature],
  formulae: set[Formula]
#]

Relation: datatype
begin
_REL(p,c: Feature):OPT?:Relation
_REL(p,c: Feature):MAND?:Relation
_REL(p: Feature,c:set[Feature]):
^  ALT?:Relation
_REL(p: Feature,c:set[Feature]):
^  OR?:Relation
Relation

Formula : datatype
 TRUE_FORMULA:TRUE?:Formula
 FALSE_FORMULA:FALSE?:Formula
 NAME_FORMULA(n: Name):NAME?:Formula
 NOT_FORMULA(f: Formula):NOT?:Formula
 AND_FORMULA(f0,f1: Formula):
     AND?:Formula
 IMPLIES_FORMULA(f0,f1:Formula):
     IMPLIES?:Formula
 end Formula
```

A feature model is well-typed if its feature tree is well-formed and its constraints are correctly defined. The well-formedness rules for a feature tree include:

- The existence of exactly one root feature (already incorporated in the `FM` definition);
- Formation of a tree structure, ensuring connectivity and the absence of cycles;
- Unique feature names;
- Properly structured relations.

```
wellTyped(fm: FM): boolean =
  wellFormednessRules(fm) ∧
  wellTypedFormulae(fm)

wellFormednessRules(fm: FM): bool =
  tree(fm) ∧ uniqueFeatureNames(fm) ∧
  wellFormedRelations(fm)
```

For the `tree` predicate, two auxiliary predicates must hold: the model must be both *acyclic* and *connected*. These predicates rely on the `children` function, which determines the transitive closure of the feature model's set of relations. Additionally, a relation is well-formed if it connects the appropriate number of features corresponding to its type. For example, an alternative relation must include at least one parent and one child feature.

```
tree(fm: FM): bool =
    acyclic(fm) ∧ connected(fm)

acyclic(fm:FM): bool =
^∀f : Feature · f ∈ features(fm) ⇒
^f≠children←f←

connected←fm.FM←.bool/
^∀f : Feature · f ∈ features(fm) ⇒
^f≠children←root←fm←←

uniqueFeatureNames←fm.FM←.bool/
∀f1‹f2.Feature·
f1=f2ANDf1∈features←fm←∧
f2∈features←fm←⇒f1/f2

wellFormedRelations←fm.FM←.bool/
∀r.Relation·r∈relations←fm←∧
←ALT⋆←r←ORor⋆←r←←⇒
∃f.Feature·
f∈features←fm←∧f∈children←r←
```

Type correctness for formulae is determined by ensuring they refer exclusively to features explicitly defined within the feature tree (as seen in the `NAME_FORMULA` clause). These formula typing predicates are conditioned upon the well-formedness of the feature tree, as indicated by the PVS predicate subtypes included in the function header.

```
wellTypedFormulae(fm: {featMod: FM |
  wellFormednessRules(featMod)}): boolean =
    ∀f:Formula: f ∈ formulae(fm) ⇒
        wellTyped(fm,f)

wellTyped(fm:{featMod:FM |
  wellFormednessRules(featMod)},
  f:Formula):boolean =
  cases f of
    TRUE_FORMULA: true,
    FALSE_FORMULA: true,
    NAME_FORMULA(n): n ∈ names(fm),
    NOT_FORMULA(f1): wellTyped(fm,f1),
    AND_FORMULA(f1,f2):
```

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```
      wellTyped(fm,f1) ∧
      wellTyped(fm,f2),
    IMPLIES_FORMULA(f1,f2):
      wellTyped(fm,f1) ∧
      wellTyped(fm,f2)
endcases
```

3. Bad Smells

Bad smells in feature models represent structural issues that may indicate opportunities for refinement and improved design. Fowler introduced the concept of bad smells in software programs [6].

This section presents a catalog of bad smells specific to feature models. It is important to note that this list is not exhaustive. Identifying bad smells enables domain analysts to enhance the quality of feature models by revealing incorrect or missing constraints and suggesting opportunities for restructuring. However, the presence of a bad smell does not necessarily imply inconsistency within the feature model.

Bad smells can be addressed through feature model (FM) refactoring, which involves transforming one FM into another while ensuring that all valid configurations of the original model are preserved [8]. The following subsections introduce several bad smells, each described using a structured approach: an explanation of its relevance, an illustrative example, and a corresponding refactoring inspired by the catalog presented by Alves et al. [8] to improve the model's design.

3.1. Expecting Multiple Alternatives

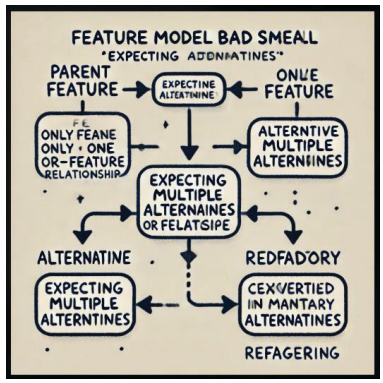
In some cases, a feature model may define a relationship as an *Alternative Feature* or an *Or Feature* between a parent feature and a single child feature. This configuration may indicate a design flaw, as the semantics of both relationships imply that the child feature is mandatory. A more appropriate approach is to redefine the relationship as *Mandatory*.

A common occurrence of this issue arises when a feature A is classified as an *Or Feature* or an *Alternative Feature* but has only one child feature B. Detecting this pattern may indicate an erroneous modeling decision, where an alternative grouping was mistakenly chosen instead of a direct mandatory relationship. This issue has been identified in several feature models available on the FeatureIDE platform [10].

To address this bad smell, Refactoring 1 is introduced, replacing an alternative relation with a mandatory relation. Refactoring strategies can be systematically applied using template matching techniques. Each general FM refactoring consists of two templates, representing feature models before (LHS) and after (RHS) the transformation.

A refactoring is applicable whenever the FM matches the LHS template. This matching process involves assigning concrete values to the meta-features occurring in the LHS

Refactoring 1: ⟨replace alternative to mandatory⟩



template. Elements not explicitly depicted in the templates remain unchanged, ensuring that only the intended modifications are applied. Features connected by dashed lines in the diagrams indicate possible parent-child relationships that may exist beyond the immediate scope of the refactoring.

Additionally, an alternative refactoring approach can transform an *Or* relation into a mandatory relation. The correctness of these refactorings can be demonstrated through formal verification methods, including encodings of feature models in Alloy [11] or the application of the Prototype Verification System (PVS) [9] framework [12].

3.2. Constraint Imposing the Selection of an Alternative

In some cases, a constraint within a feature model may enforce the selection of a specific child within an alternative relationship. This issue arises when a global constraint mandates the selection of an *Alternative Feature* or *Or Feature*.

Since one child is always selected, the remaining children in the alternative relationship cannot be chosen. Identifying this bad smell may reveal inconsistencies between constraints and the relationships defined within the feature model.

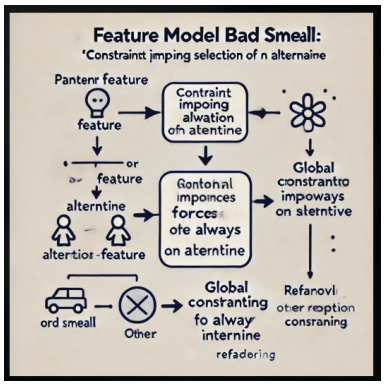
For instance, if the constraint $B \Rightarrow D'$ is introduced in the feature model of Figure, feature B, being a mandatory feature of A, must be selected. Consequently, due to the added constraint, feature D' must also be selected, leaving D" as an invalid choice. This scenario suggests a possible design flaw.

Refactoring 2 addresses this issue by eliminating the restrictive constraint.

A similar refactoring can be applied to an *Or* relationship. In this and subsequent cases involving constraints (formulae), Refactoring 3 can be utilized to prepare the feature

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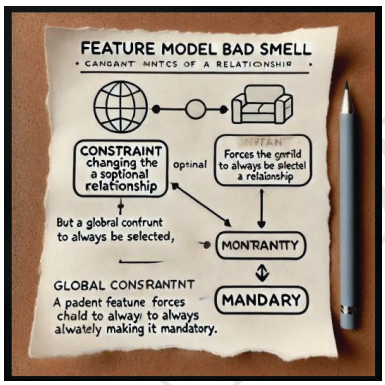
Refactoring 2: ⟨change alternative constraint⟩



model to match a specific refactoring template, such as Refactoring 2. The variable *fs* represents a set of features.

Within the feature model example in Figure 3, Refactoring 3 is first used to deduce the constraint D'. After this step, Refactoring 2 can be applied to correct the model.

Refactoring 3: ⟨add deducible formula⟩



(↔) f can be deduced from *forms* and *fs*.

3.3. Constraint Changing the Semantics of a Relationship

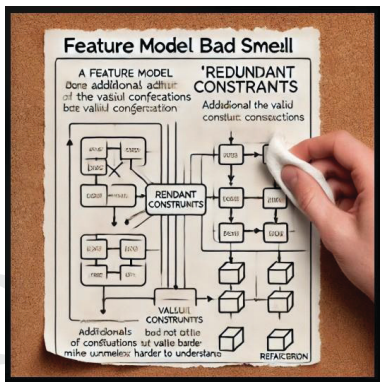
A feature model may sometimes include constraints that unintentionally make the semantics of a relationship more restrictive.

This issue can complicate the understanding of the model, requiring additional effort from domain analysts. A more effective approach is to modify the relationship itself, ensuring that constraints are incorporated directly into the graphical notation, thereby improving readability.

An example of this bad smell is found in the feature model depicted in Figure given below. As discussed in Section 1, the presence of the global constraint $B \Rightarrow D$ alters the optional relationship between features A and D, effectively making it mandatory. Identifying this bad smell helps determine whether the issue lies in an improperly defined constraint or an inadequate feature model relationship.

Refactoring 4 resolves this issue by converting the optional relationship into a mandatory one.

Refactoring 4: ⟨replace optional to mandatory⟩



This type of issue can also occur with other relationships. In some cases, an *Or* relationship can be replaced with an *Alternative* relationship. Several refactoring techniques are available to address these cases effectively [13].

3.4. Redundant Constraints

Including redundant constraints in a feature model can enhance readability and aid comprehension. A redundant constraint does not reduce the number of valid configurations within a feature model, meaning it does not impose any additional restrictions. The total number of valid configurations remains unchanged.

However, excessive redundant constraints may complicate the model, making it more difficult for domain analysts to interpret. Analysts might spend unnecessary time examining constraints that do not contribute meaningful restrictions to the model. In such cases, removing redundant constraints may improve clarity and usability.

For instance, consider the introduction of the constraint $C \Rightarrow B$ in the feature model of Figure 4. This constraint is redundant since feature B is already included in every valid configuration of the model. Identifying this type of bad smell may indicate that a constraint has not been well specified.

This issue can be resolved by applying Refactoring 3 from right to left, thereby eliminating redundant constraints from the model.

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3.5. Dead Features

A dead feature is a feature that can never be selected in any valid configuration of a feature model due to an imposed global constraint [14]. This situation may arise when multiple constraints interact in ways that unintentionally render certain features unusable, increasing model complexity and the likelihood of errors.

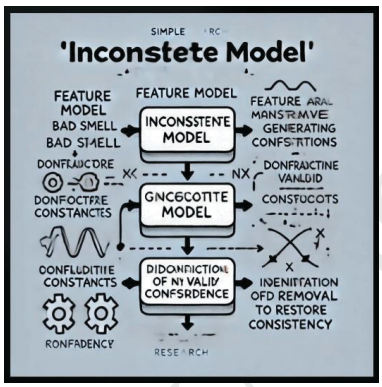
The presence of dead features often suggests an issue with the model's design.

For example, introducing the constraint $B \Rightarrow \neg C$ in the feature model of Figure 5 results in feature C becoming a dead feature, as it will never appear in any valid configuration of the model.

If a feature is dead, it may no longer serve a functional purpose within the model and should either be removed or reviewed for potential overconstraint issues. If the model is overly constrained, certain constraints may need to be relaxed or removed to restore proper functionality.

Two refactoring approaches can address this issue. Refactoring 5 eliminates excessive constraints contributing to overconstraint issues.

Refactoring 5: ⟨remove formula⟩



Alternatively, if the dead feature must be removed, Refactoring 6 can be applied. This process eliminates the feature from the model and replaces its occurrences within constraints with *false*, ensuring consistency.

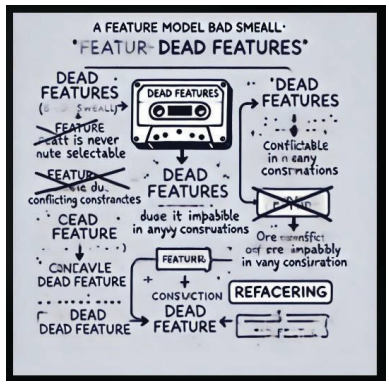
3.6. Inconsistent Model

An inconsistent feature model occurs when contradicting constraints prevent any valid configuration. Overconstraint issues often contribute to this problem, making the model difficult to analyze and prone to errors.

In general, an inconsistent model indicates poor design and the presence of logical errors.

For example, adding the constraint $C \Rightarrow \neg D$ to the feature model in Figure 5 creates an inconsistency, as feature D is required to always be selected. This contradiction renders the model unusable, as no valid configuration can be generated. If a model is inconsistent, it often signifies a fundamental design issue. A model without valid configurations does not serve its intended purpose.

Refactoring 6: ⟨remove dead feature⟩



To resolve inconsistencies, an analysis tool such as the one proposed by Benavides [15] can be used to identify the minimal set of conflicting constraints causing the inconsistency. Once identified, a domain analyst should evaluate which constraints need to be removed. Refactoring 5 can then be applied to eliminate these constraints and restore consistency within the model.

4. Tool Support

A Haskell library and a set of tools have been developed to detect errors and bad smells in feature models. This contribution extends support to the Haskell community, as no similar libraries or tools have been previously developed in functional programming languages. The provided libraries and tools offer the following capabilities:

- Data types for feature modeling in Haskell;
- Functions for verifying whether a feature model is well-typed;
- Functions for identifying bad smells in feature models;
- Functions for checking feature model satisfiability;
- Functions for validating whether a selection of features constitutes a valid instance of a feature model; and
- Integration with existing tools, such as Feature Modeling Plugin and FeatureIDE.

This section begins by discussing key design decisions made during the development of the feature model library. Additionally, an analysis of benchmarking results is presented, based on evaluations conducted on three publicly available feature models: *eShop feature model* (325 features), *Model Transformation* (113 features), and *Web Portal* (49

features) [16]. These models have been extensively studied in the literature. Moreover, satisfiability functions were tested on models containing up to 1000 features.

4.1. Design Decisions

To verify satisfiability, two approaches have been implemented. The first approach is a purely functional implementation utilizing the Funsat Haskell library. This approach not only determines whether a feature model is satisfiable but also retrieves a valid instance of the model when possible. However, the library is not optimized for complex feature models. Consequently, an interface with the Minisat SAT solver, an open-source tool developed in C, has been developed to enhance efficiency.

4.2. Benchmark Analysis

The toolset was evaluated using small and medium-sized feature models that are publicly accessible. These models have been widely referenced in the literature, making them suitable for analysis. The primary objective was to assess whether the tools accurately detect errors and bad smells within a reasonable execution time. Some of the tested feature models already contained structural errors, primarily related to duplicated features. Additionally, bad smells were intentionally introduced into the models to evaluate the detection capabilities.

Three operations were evaluated for each feature model: type checking (TC), satisfiability checking (SC), and bad smell detection (BSD). To minimize bias, each operation-feature model pair was evaluated 50 times. The tests were conducted on a Mac OS-X system with a 2.16 GHz processor and 2 GB of RAM. Execution time, measured in milliseconds, was recorded using the *BenchPress* library [17]. The average execution time for each evaluation pair is presented in Table 1.

Feature Model	Features	TC	SC	BSD
Web Portal	49	4.8	4.5	125.78
Model Transformation	113	4.5	20.70	1339.03
eShop	325	15.27	125.76	25806.05

Table 1. Benchmark results

The results indicate that the execution time required for bad smell detection increases significantly as the number of features grows. For instance, detecting bad smells in the *eShop* feature model took approximately 25 seconds, which is nearly 20 times longer than the execution time for the *Model Transformation* feature model. However, even in such cases, the execution time remains acceptable, as the tool significantly reduces the effort required to manually identify poor design decisions.

The current implementations of the detection functions were developed without a primary focus on performance optimization. For example, the function for detecting dead features, shown in Listing 1, is computationally expensive. For each optional feature, the function makes a separate call to the satisfiability checker, increasing execution time. Optimizing these functions is an area for future improvement.

Listing 1. Function for checking dead features.

```
checkDeadFeatures :: FeatureModel -> [Feature]
checkDeadFeatures fm =
 let fm' = addImplies fm
 in
  [ f | f <- features fm
  , isOptional f
  , not (isSatisfiable fm' f)
  ]
```

5. Evaluation

This section presents various applications of the type system introduced in Section 2.

5.1. Checking Feature Model Refactorings

A feature model refactoring [8] must (i) preserve or improve configurability and (ii) maintain well-formedness and typing rules. Therefore, proving the validity of each refactoring involves demonstrating compliance with both conditions. Previous work has established the correctness of refactorings concerning configurability [12]. The focus here is to verify their correctness with respect to type preservation.

To ensure that a transformation maintains well-formedness, the following theorem must hold. If the theorem is valid for a given transformation, it ensures that no type errors are introduced and that well-formedness rules remain intact.

typingRulesPreservation: THEOREM
∀ m1, m2: FM, ... |
syntax(...) ∧ conditions(...) ∧
wellFormed(m1) ⇒ wellFormed(m2)

The predicate *wellFormed* defines when a feature model meets structural requirements, as detailed in Section 2. The predicates *syntax* and *conditions* describe the syntactic elements of the refactoring transformation and any conditions it must satisfy. Each transformation is mapped to its corresponding elements in feature model semantics.

To illustrate, consider Refactoring 2. Let *m1* and *m2* represent the feature models before and after transformation, respectively. If *m1* is well-typed, the structural properties of *m2* ensure that it remains a tree. The introduction of new

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relations (alternative and mandatory) maintains the requirement that each must have exactly one child. Additionally, the transformation does not introduce naming conflicts, as no new names are declared. Finally, all constraints from *m1* are retained in *m2*, ensuring that the resulting constraints remain well-typed. Consequently, Refactoring 2 preserves typing rules.

Other refactorings can be proven correct using similar reasoning.

6. Related Work

Several tools assist developers in creating and maintaining feature models. Feature Modeling Plugin (FMP) [18] does not detect incorrect constraints during modeling but does so when creating configurations for a specific product. The techniques proposed in this work offer early-stage constraint validation. Similarly, pure::variants [19] can detect some irregularities in feature models but does not cover the cases discussed in this paper. However, it includes a validation framework that allows for the implementation of additional checks and automated fixes, which could support the proposed techniques.

Benavides et al. [20] propose an automated approach for analyzing feature models, covering aspects such as configuration enumeration, counting possible configurations, and verifying model consistency. Their work transforms feature models into Constraint Satisfaction Problems (CSPs) for formalization. However, their analyses do not incorporate type checking, making the approach complementary to the work presented here.

White et al. [21] introduce a method using constraint solvers to determine the minimal set of feature selection modifications needed to correct an invalid configuration. Their work focuses on resolving configuration conflicts rather than preventing them through type correctness, making it a subsequent step to the analysis presented in this paper.

Trujillo et al. [22] conduct a case study on feature model refactoring within the AHEAD Tool Suite. Their work focuses on restructuring feature models but does not account for type soundness. Similarly, Segura et al. [23] automate the merging of feature models using graph transformations without ensuring well-formedness and type correctness.

Thum et al. [24] introduce an automated reasoning approach for feature model edits using SAT solvers. They categorize edits as either *refactorings*, which maintain the same set of products, or *generalizations*, which add new products without removing existing ones. This classification aligns with the objectives of detecting and addressing bad smells in feature models.

Regarding bad smells, Trindad et al. [14] describe dead (isolated) features and propose methods for their detection in feature models using three alternative implementations. This work extends that concept by presenting a broader catalog of bad smells and providing type-sound refactorings for their elimination.

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Smart Health Monitoring System

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***Abstract*— This project introduces a Smart Health Monitoring System designed to provide real-time health data monitoring for individuals. The system utilizes a Raspberry Pi 3B+ as the central processing unit, incorporating a Heart Rate Sensor, AD8232 ECG Sensor, and LM35 Temperature Sensor to gather vital health information. The Raspberry Pi 3B+ processes and analyzes the sensor data efficiently, with the Heart Rate Sensor capturing pulse rate, the AD8232 sensor recording the Electrocardiogram (ECG), and the LM35 measuring body temperature. These sensors operate in combination to provide a comprehensive overview of the user's health status. The system design also includes an Internet of Things (IoT) component for remote access, with data transmission to a cloud platform for online storage and visualization. In this study, the system was implemented and tested in a Proteus simulation environment to validate its design, data acquisition, and communication flow prior to hardware deployment. The results demonstrate the feasibility of combining embedded hardware, biomedical sensors, and IoT technologies to create a scalable remote health monitoring solution suitable for future real-world applications.**

Keywords*— *Smart Health Monitoring, Raspberry Pi 3B+, Heart Rate, Electrocardiogram (ECG), Temperature

I. INTRODUCTION

Smart health monitoring systems leverage a combination of advanced sensors, embedded processing platforms, and Internet of Things (IoT) connectivity to provide continuous, real-time tracking of vital physiological parameters. By integrating multi-sensor data acquisition with efficient processing and cloud-based visualization, these systems enable early detection of anomalies, rapid clinical decision-making, and improved patient outcomes. Unlike traditional bedside monitoring solutions that restrict patient mobility, smart health monitoring devices can be portable, cost-effective, and accessible from remote locations, allowing healthcare providers to observe patient health without direct physical presence. The proposed Raspberry Pi–based system aligns with this paradigm by acquiring electrocardiogram (ECG), body temperature, and heart rate data, digitizing them via a high-resolution ADC, and transmitting the results to the ThingSpeak IoT platform for remote access and visualization.

Body temperature, electrocardiogram (ECG), and heart rate are fundamental physiological parameters for assessing an individual's health status. Body temperature reflects the body's thermoregulatory balance and can serve as an indicator of infections, metabolic disturbances, or inflammatory conditions. The ECG records the heart's electrical activity over time, offering detailed insights into cardiac rhythm, conduction pathways, and potential arrhythmias, thereby playing a vital role in cardiovascular diagnostics. Heart rate, measured in beats per minute, provides a direct indication of cardiovascular performance and can reveal stress, fitness levels, or early signs of cardiac dysfunction. Together, these parameters form a comprehensive basis for continuous health monitoring in both clinical and remote care settings.

Cardiovascular diseases (CVDs) remain one of the leading causes of morbidity and mortality worldwide, necessitating accurate, continuous, and cost-effective monitoring solutions. Electrocardiography (ECG) plays a central role in diagnosing heart conditions, as it provides detailed information about the heart's electrical activity and rhythm patterns[1]. Traditional hospital-based ECG machines are often bulky, expensive, and tethered to stationary monitoring stations, limiting mobility and patient comfort. Furthermore, routine hospital visits for monitoring impose logistical and financial burdens, particularly in resource-constrained settings.

The adoption of Internet of Things (IoT) technologies has been accelerating at an unprecedented pace, offering transformative benefits across industries, particularly in healthcare. Projections indicate that by 2025, the number of IoT-connected devices worldwide will surpass 75 billion, generating massive volumes of data. The economic potential of IoT is estimated to range from USD 3 to 6 trillion, with smart healthcare contributing the largest share—between USD 1 and 2.5 trillion. In the healthcare domain alone, the IoT market was valued at approximately USD 180 billion in 2022 and is forecasted to grow to nearly USD 962.21 billion by 2032, representing a compound annual growth rate (CAGR) of 18.3% over the 2023–2032 period. This rapid expansion is fueled by the integration of connected medical devices and IoT-based systems in hospitals, clinics, and home healthcare, highlighting the growing importance of developing secure, efficient, and scalable smart health monitoring solutions [2].

Recent advances in personalized health monitoring systems have demonstrated the potential to improve elderly wellness management through real-time vital sign tracking and intelligent data analysis. For example, a community-level implementation in Hong Kong integrated data from wearable trackers and all-in-one health monitoring stations, enabling reliable, stable, and convenient real-time data sharing. Such systems not only allow continuous monitoring but also enable predictive analytics for personalized coaching and early intervention, thereby reducing the likelihood of critical health events. [3]

Existing smart home health monitoring technologies leverage IoT-enabled sensors to track vital physiological, functional, safety, and cognitive parameters, enabling remote healthcare support and improved patient outcomes[4].

This research proposes a multi-parameter health monitoring system based on the integration of an AD8232 ECG module, LM35 precision temperature sensor, and a dedicated heart rate sensor. The analog outputs from these sensors are routed to an MCP3208 12-bit Serial ADC, ensuring high-resolution digitization. The digitized signals are then processed by a Raspberry Pi, which serves as the central

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processing unit (“brain”) of the system. The Raspberry Pi coordinates sensor data acquisition, executes real-time signal processing, and manages data display or transmission. The overall design emphasizes reliability, high signal integrity, and cost-effectiveness, making it suitable for both clinical and remote monitoring scenarios without reliance on machine learning or complex cloud-based analytics.

II. METHODOLOGY

A. System Overview

The proposed health monitoring system is designed to acquire, process, and display three physiological parameters: ECG, body temperature, and heart rate. The selection of sensing modules prioritizes accuracy, low noise, and ease of integration, drawing on established designs in prior work[5].

B. Signal Acquisition stage

(a) ECG Measurement – AD8232 Module

In the proposed design, the ECG signal is modelled and processed using the AD8232 ECG module in a simulated environment (Proteus 8.12). The AD8232 is an integrated signal conditioning block optimized for ECG applications [6]. In the simulation, the ECG waveform is generated programmatically to emulate realistic cardiac electrical activity, which is then amplified and filtered to produce a clean analog signal suitable for digitization.

(b) Temperature Measurement – LM35 Sensor

The LM35 precision temperature sensor is included in the simulation to measure body temperature. It produces a linear output of 10 mV/°C with typical accuracy of ±0.5°C, making it highly reliable for biomedical applications [6]. The sensor’s analog voltage is directly proportional to the modelled temperature value and is easily interfaced with the ADC.

(c) Analog-to-Digital Conversion – MCP3208

The MCP3208 is selected for its 12-bit resolution, SPI communication capability, and low power consumption. In simulation, it digitizes the analog outputs from the ECG module, LM35 sensor, and heart rate sensor. This resolution ensures that subtle variations in simulated ECG morphology and temperature changes are captured with high fidelity, allowing for accurate downstream processing.

The digitized data is intended to be processed by a Raspberry Pi and transmitted over the Internet to ThingSpeak, an IoT cloud platform for real-time visualization and analysis. This enables remote monitoring capabilities, where authorized users can access live physiological data through a web dashboard.

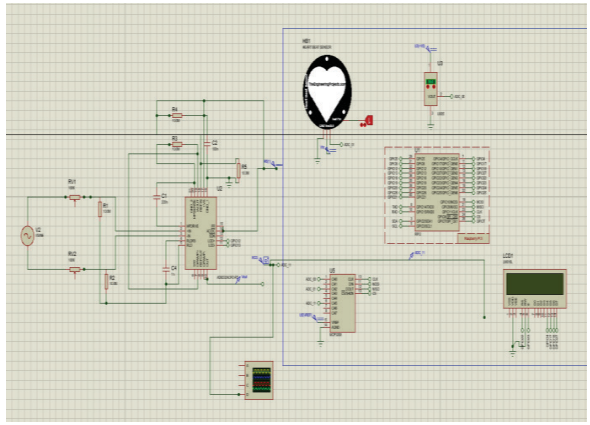


Fig 1. Circuit diagram

Fig 1 illustrates the complete simulated circuit schematic, including the ECG module, temperature sensor, heart rate sensor, MCP3208 ADC, and Raspberry Pi interface. The Raspberry Pi, acting as the system’s processing unit, was programmed to read sensor data via SPI, process the readings and to display them on an LCD.

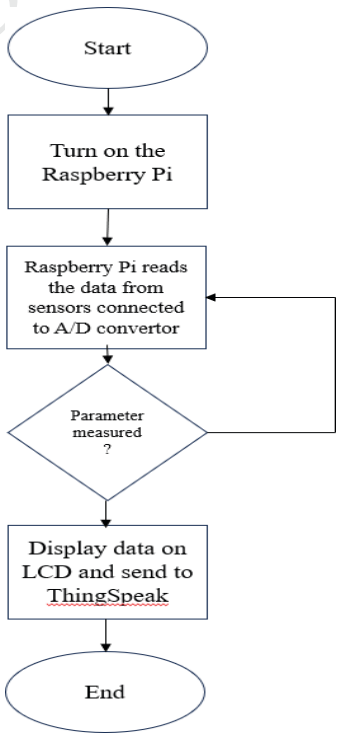


Fig 2. Flowchart depicting system operations

Figure 2 presents the system flowchart, outlining the data acquisition and transmission sequence. After initialization, the Raspberry Pi continuously polls the connected sensors via the MCP3208, verifies parameter readings, displays them on the LCD, and uploads the data to ThingSpeak for real-time visualization.

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C. Algorithm

Step 1: Import the required Python libraries for interfacing with the LCD (lcd123), Raspberry Pi GPIO (RPi.GPIO), handling time (time), SPI communication (spidev), and sending HTTP requests (requests).
Step 2: Define Thingspeak Parameters
Step 3: Set the GPIO mode to BOARD. Initialize the SPI interface using the spidev library. Open the SPI connection on channel 0 and CE0 (Chip Enable 0) for communication with the ADC.
Step 4: Define Sensor Channels. Define channels for temperature, ECG, and heart rate readings to streamline data acquisition from the sensors. They are channel 0 for temperature, channel 1 for heart rate and channel 5 for electrocardiogram.
Step 6: Define Sensor Reading Functions
Step 7: Initialize LCD
Step 8: heartb() func - Read analog data from the heart rate channel, displaying pulse information on the LCD. Calculate the heart rate over a 10-second interval and display the result on the LCD.
Step 9: Infinite loop:
Read temperature and ECG data. Display temperature and ECG values on the LCD. Call the heartb() function to measure and display heart rate. Send the collected data to Thingspeak using the send_to_thingspeak function. Repeat the loop with a 1-second delay.
Step 10: Clean Up GPIO. Close the SPI connection to release system resources. Clean up GPIO resources to ensure proper shutdown.

III. RESULTS

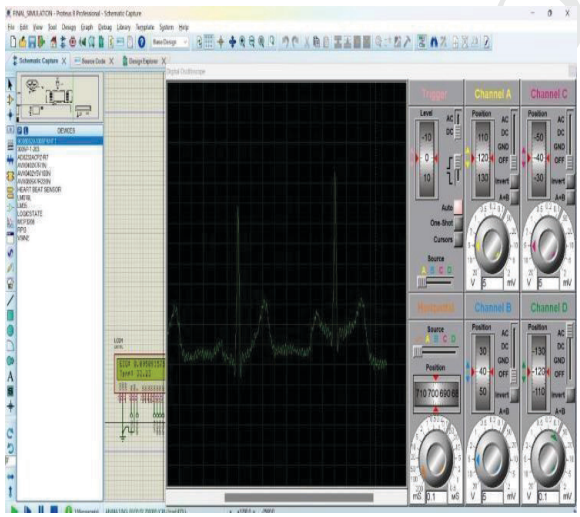


Fig 3. Output presented on Proteus

The proposed health monitoring system was modeled and tested in **Proteus 8.11** simulation software. The ECG signal acquisition module (AD8232) was interfaced with the MCP3208 12-bit ADC, along with LM35 and a simulated heart rate sensor, to verify proper analog-to-digital conversion and data handling by the Raspberry Pi.

TABLE I. SAMPLE READINGS OBTAINED ON THE LCD

Trial	Respective health parameters		
	Electrocardiogram	*Temperature*	*Heart rate*
1	0.022	33.68	72
2	0.024	32.65	75
3	0.026	32.19	78

[a.] The ECG values are generated and are displayed on the oscilloscope in addition to LCD display

IV. FUTURE SCOPE AND CONCLUSION

The Smart Health Monitoring System developed in this work demonstrates the successful integration of biomedical sensors with a Raspberry Pi platform and IoT-based remote monitoring capabilities in a simulated environment. Future developments will focus on implementing the system in a real hardware setup to enable continuous, real-time health monitoring under actual operating conditions. The IoT functionality, currently configured in simulation with ThingSpeak integration, will be fully deployed in hardware to provide live cloud-based data access, storage, and analytics. Additional enhancements may include advanced algorithms for accurate heart rate detection, ECG noise filtering, and anomaly detection to assist in early diagnosis.

The system can also be extended with wireless connectivity modules such as Wi-Fi or GSM for greater portability and use in remote areas. Integration with mobile or web applications can improve user accessibility, while incorporating more sensors (e.g., SpO_2, blood pressure) will expand the range of monitored health parameters. Security measures such as data encryption and authentication protocols will be added to ensure patient privacy and compliance with healthcare data standards.

These advancements will enhance the system's robustness, scalability, and applicability in telemedicine, elderly care, and personal health tracking.

This system could also be adapted for continuous remote patient monitoring, where healthcare professionals can access real-time vital parameters from anywhere in the world, as suggested in prior research [7].

According to recent reviews in the field of remote patient health monitoring systems future research should prioritize the development of secure and energy-efficient solutions[8]. While several studies have addressed various aspects of remote health monitoring, there remains a need to integrate these advancements into comprehensive and secure systems. Emerging technologies such as IoT, cloud computing, and blockchain offer significant potential for creating scalable, flexible, and energy-efficient platforms.

Several studies highlight that while IoT offers significant potential in elderly healthcare, critical challenges remain in areas such as standardization, interoperability, security, privacy, performance, big data management, scalability, trust, federated learning, and edge computing, requiring focused research to enable reliable, secure, and scalable healthcare solutions. [9]

CONFERENCE PROOF

As suggested by M. Ghafurian, K. Wang, I. Dhode, M. Kapoor, P. P. Morita and K. Dautenhahn, despite the great potential of smart homes in improving older adults' lives, research in this area remains in its infancy, and further studies are needed to better understand their effects, benefits, and contributing factors for effectiveness [10].

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Design of a Comprehensive Tyre Health Management System with Predictive Analytics Using STM32

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***Abstract*— Tire failures are still one of the most common causes of car problems, and they are frequently brought on by surface fatigue, misalignment, overheating, or undetectable pressure drops. Reliability and safety are increased through ongoing monitoring of these factors. The STM32 microcontroller has been used to create a real-time diagnostic framework that assesses vibration, alignment accuracy, temperature, and tire pressure. Important parts include the MPU6050 for motion and impact detection, the BMP180 for temperature and pressure sensing, and infrared sensors for wheel alignment. With the use of a pre-trained VGG19 model, tire wear is evaluated through image-based classification, allowing for predictive alerts based on visual degradation. An ESP32 module is used to detect engine-side wiring issues by monitoring voltage levels. Data is sent via UART for external logging and analysis, and it is shown on a graphical LCD. This combined strategy reduces the need for manual inspections, encourages preventative maintenance, and improves operational safety for all kinds of vehicles.**

Keywords— STM32, Tyre Condition Monitoring, Predictive Analytics, Sensor-Based Diagnostics, Infrared Alignment, Vibration Detection, Image Classification, ESP32 component.

I. INTRODUCTION

Tires have a direct impact on a vehicle's handling, fuel economy, braking, and overall performance, making them one of the most crucial safety features. But tire-related issues like under-inflation, overheating, misalignment, and excessive wear are frequently ignored until they cause major damage or accidents. Conventional tire inspection techniques rely on manual checks, which are labor-intensive and prone to human error. The need for automated tire health monitoring systems that offer real-time data and early fault warnings is growing along with the demand for smart and secure transportation systems. Compact and effective monitoring systems that can continuously track tire condition while a vehicle is in motion have been made possible by advancements in sensor and embedded systems technology. Such systems can gather important parameters like tire pressure, temperature, alignment, and vibration by combining a number of sensors with a microcontroller. They can also notify the driver when any of these values surpass a certain threshold. Predictive maintenance, made possible by these smart systems, not only helps to decrease unplanned breakdowns but also increases tire longevity and boosts vehicle dependability. The main goal of this project is to use the STM32 microcontroller to create a complete tire health management system. Motion tracking (MPU6050), wheel alignment (IR sensors), and temperature and pressure (BMP180) sensor modules are all part of the system. The system can identify tires that require replacement based on their surface condition thanks to a machine learning model that uses MATLAB image processing in addition to real-time data monitoring. To further improve safety, an ESP32 module monitors voltage continuity to identify engine wiring flaws. The STM32 processes the gathered data and shows it on a graphical LCD. It also sends the data via serial communication to a computer for logging and analysis. Both remote visibility and on-board alerts are provided by this integrated system, which is intended to function in real time. Personal transportation, fleet management, and commercial logistics can all benefit from the system's scalability and adaptability to different vehicle types. This solution makes a substantial contribution to road safety and economical vehicle maintenance through its capacity to identify early warning indicators and offer predictive insights. To ensure quick and precise identification of any abnormal conditions, the system is built to read data from all sensors several times per second. The system immediately displays a warning on the LCD screen if the temperature rises above the threshold or if the tire's pressure falls below the safe limit. Similarly, the driver receives an alert if any of the infrared sensors identify wheel misalignment. The MPU6050 sensor aids in monitoring sharp vibrations, bumps, or abrupt movements that may be signs of road conditions causing tire damage. The system uses MATLAB-processed tire images to check for surface wear. Each image is categorized as either "Good" or "Defective" by a pre-trained VGG19 deep learning model. As a result, the system can recommend replacement before the tire is completely worn out. UART serial communication is used to store and transmit all sensor readings and alerts to a computer. The computer's Eltima Serial Port Monitor program aids in viewing and recording the data for later examination. By assessing the condition of engine wires, the ESP32-WROOM module adds an additional layer of security. The ESP32 recognizes the issue and notifies the STM32 system if any wire is broken or disconnected. By integrating engine and tire monitoring, this increases the system's dependability. A 12V DC source provides power to the entire system, with each component being safely powered by the source. The system is appropriate for long-term vehicle use because the microcontroller and sensors use little power. Because of its small size and low weight, the hardware is simple to install in a variety of car models. This system helps drivers make better maintenance decisions and lessens the need for frequent manual checks. It offers precise readings under both typical and challenging driving circumstances when the sensor is calibrated properly. In later iterations, it can also be extended to incorporate GPS or IoT modules for cloud-based monitoring. All things considered, it provides an affordable, real-time, and clever way to increase traffic safety and prolong tire life. In the future, the

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system can be enhanced to remotely alert drivers by connecting via Bluetooth or Wi-Fi to a mobile application. Fleet managers could use this to schedule maintenance in advance and keep an eye on several vehicles at once. Additionally, the system has the capacity to store historical data, which aids in the analysis of tire usage trends over time. This type of information can help reduce needless tire replacements and improve driving habits. Each sensor or feature can be added or removed depending on the type of vehicle because the current setup is modular. For instance, only simple sensors may be required in small personal vehicles, but all modules, including engine wire fault detection, can be utilized in large trucks. The STM32 microcontroller has sufficient speed and memory to effectively process all sensor data. The overall goal of the system is to make car maintenance safer, quicker, and more intelligent for all kinds of users.

II. LITERATURE REVIEW

It focuses on enhancing vehicle health monitoring through the use of Internet of Things-based communication systems. The study examines issues with current TCP/IP protocols such as data loss, transmission delays, and network congestion. It suggests a multi-layered structure to improve better data delivery through communication between various protocol layers. Additionally, the study offers a structured understanding of contemporary issues by introducing taxonomies to categorize communication protocols and optimization techniques. This strategy emphasizes the necessity of optimized protocols to increase the dependability and effectiveness of vehicle monitoring systems [1].

It focuses on enhancing model predictive control (MPC) algorithms for STM32 microcontroller-based fast dynamic systems. The study looks at Generalized Predictive Control(GPC) and Dynamic Matrix Control (DMC), and it presents faster versions, FDMC and FGPC, which expedites computations by using straight forward formulas. These enhanced algorithms are perfect for applications that need fast responses because they run in microseconds. This method demonstrates how quick MPC algorithms can be used for embedded systems in robotics and automotive applications [2].

To maximize performance and energy use, the IoT-enabled Smart Street Lighting System combines LED lights, ESP32, STM32, LDR, and IR sensors. The IR sensor modifies brightness in response to object detection, while the LDR makes sure lights only turn on in complete darkness. Data Thing-Speak's visualization offers information on system dependability and energy efficiency. This creative solution provides an economical and environmentally friendly method of street lighting in urban areas [3].

To enhance plant care, particularly in regions with poor air quality, the paper proposes an intelligent irrigation system utilizing the STM32 microcontroller. It addresses obstacles to China's adoption of contemporary technologies and emphasizes the value of indoor plants for air purification. The system promotes plant health and reduces manual care by automating irrigation using temperature and humidity sensors. The study highlights how these systems living conditions and people's quality of life. The STM32 microcontroller determines when to water the plants by analysing data from the sensors. The system automatically activates the water pump when the soil is dry or the temperature is high. This lessens the need for daily hand watering of the plants. These intelligent systems increase indoor space health, enhance plant growth, and conserve water [4].

In this paper, the C8051F005 microcontroller is used to design and implement a Tire Pressure Monitoring System (TPMS). The system uses wireless communication to efficiently monitor tire pressure time data collection. By preventing tire-related accidents caused by incorrect tire pressure, the proposed TPMS improves vehicle safety. For real-time monitoring, the pressure data is wirelessly transmitted to a central unit from each tire. The system instantly notifies the driver if the tire pressure falls below the safe threshold. This enhances driving safety by lowering the likelihood of tire blowouts. Because a microcontroller is used, the system is dependable, small, and appropriate for a variety of vehicle types [5].

The MSP430 microcontroller with SPI communication protocol is used in this paper to investigate the design of a Tire Pressure Monitoring System (TPMS). The system uses the SPI interface to send data in real-time to a central unit while tracking tire pressure. System performance and reliability are improved for automotive safety applications through the use of MSP430 and SPI. The microcontroller receives the tire pressure readings from the pressure sensor. The data is accurately and swiftly sent to the control unit or display via the SPI protocol. If the tire pressure drops too much, this configuration guarantees prompt notifications. The entire system promotes safer driving practices and accident prevention [6].

The design and deployment of a wireless tire pressure management system for automobiles are covered in this paper. To track tire pressure and send information to a central receiver, it makes use of wireless sensors. By giving real-time warnings of low tire pressure, the system seeks to improve vehicle safety. This technology provides a workable way to increase fuel efficiency and reduce tire-related accidents [7].

The design and testing of an electronic control system for wireless transmission and sensor data detection in a single-seat Formula SAE car using the STM X-Nucleo board are covered in the paper. It focuses on combining multiple sensors to track important vehicle parameters, then wirelessly transmitting the data for in-the-moment analysis. The method offers insightful information about how automotive control systems for motorsport applications are developed [8].

The design and deployment of a tire pressure monitoring system (TPMS) are the main topics of this paper. In order to increase vehicle safety, the system continuously checks tire pressure and notifies the driver if it is underinflated. It measures tire pressure using sensors and sends information to a central unit for in the moment tracking [9].

The paper presents a wireless communication-based Tire pressure Monitoring System (TPMS) designed to monitor tire pressure in real-time and alert the driver when pressure falls below a safe threshold. The system uses wireless sensors placed on the tires to transmit data to a central unit, enabling efficient and accurate monitoring. This approach

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enhances vehicle safety by preventing tire-related accidents and improving fuel efficiency[10].

III. METHODOLOGY

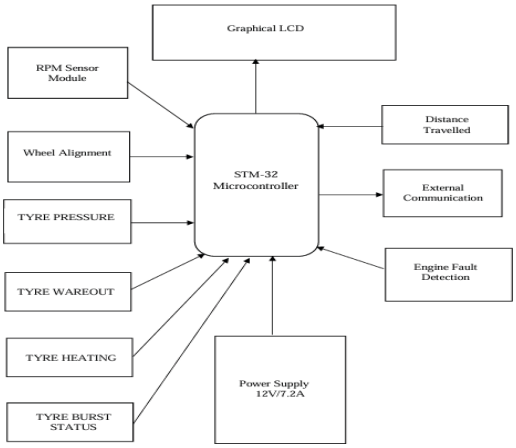


Fig 1: Block Diagram of the proposed system

An STM32F407VGT6 microcontroller is used in this project's structured approach to real-time tire health monitoring. For the purpose of monitoring vehicle safety, the system design incorporates sensor interfacing, data collection, threshold-based decision making, and external communication. Numerous sensors, including temperature, pressure, accelerometers, and infrared (IR) sensors, were interfaced with STM32 to guarantee thorough tire health detection. Additionally, MATLAB was used to implement image-based classification for tire wear detection using an SVM classifier and a deep learning model based on VGG19. Eltima software was employed to monitor serial communications. Sensor integration, data reading and display, fault condition checking, machine learning for image classification, and external communication setup.

The purpose of the tire health monitoring system is to continuously assess the condition of the tires by connecting a number of sensors to an STM32 microcontroller. Finding tire problems like low pressure, overheating, wheel misalignment, surface wear, and abrupt vibrations is the primary goal. Through a graphical LCD display, the system operates in real time and provides the driver with prompt warnings. First, the temperature and tire pressure are measured using a BMP180 sensor. The I2C communication protocol is used by the sensor to transmit digital data to the STM32. The microcontroller determines whether the temperature is higher than 32°C or if the pressure is less than 20 kPa. If so, the screen displays a warning about danger. Second, to verify that the wheels are correctly aligned, infrared (IR) sensors are positioned close to each tire. Infrared light is reflected by the sensors, if this reflection is not properly detected, the wheel is out of alignment. After reading this signal, the STM32 modifies the alignment status displayed on the screen.

Third, movement and vibration are detected by an MPU6050 sensor. Three directions of acceleration are measured by it: X, Y, and Z. Any unexpected movements or shocks are noted as they could be signs of tyre damage, potholes, or bumps.

Fourth, image classification is used to detect tire wear. Images of the tire surface are gathered and processed in MATLAB using the VGG19 deep learning model. Based on apparent wear, the model assigns a "Good" or "Defective" rating to the tire condition. This aids in anticipating when a tire replacement is necessary. Fifth, engine wiring is monitored by an ESP32-WROOM module. It determines the voltage across a few chosen wires and indicates whether any of them are disconnected or broken. After receiving this fault signal, the STM32 displays an engine warning on the LCD. Additionally, all sensor data is sent to a computer via serial communication (UART). The data is viewed and logged using Eltima Serial Port Monitor software. This facilitates debugging and the tracking of prior readings. The entire system is powered by a 12V supply and is designed to run continuously while the vehicle is moving. Its modular design makes it easy to use in a range of vehicle types, and it can be expanded in the future with Internet of Things or GPS features for remote monitoring.

IV. HARDWARE REQUIREMENTS

The key hardware components of this tire health monitoring system are the ESP32-WROOM module, graphical LCD, BMP180 sensor, IR sensors, MPU6050 sensor, and STM32 microcontroller. The BMP180 sensor measures temperature in degrees Celsius and tire pressure in kilopascals. Based on reflected infrared signals, the IR sensors are positioned close to each wheel to verify wheel alignment. To detect shocks or unusual movement, the MPU6050 sensor measures acceleration and vibration in three different directions. Engine wire connections are monitored and any issues are found using the ESP32-WROOM module. The STM32 microcontroller, which gathers data and displays the status on the graphical LCD, is connected to all of the sensors. Additionally, serial communication is used to send the data to a computer for real-time viewing and logging.

A. BMP180

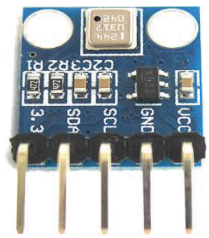


Fig2:BMP180

Tire temperature and pressure are measured by the BMP180 sensor. It can detect temperatures between -40°C and 85°C and pressures between 30 and 110 kPa. Via the I2C interface, the sensor transmits the measured values to the STM32 microcontroller. For real-time monitoring, the temperature and pressure readings are transmitted to the

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computer via serial communication in addition to being shown on the graphical LCD.

B. IR Sensor

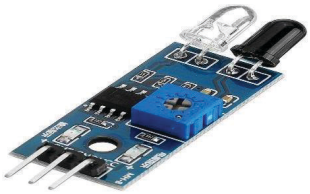


Fig 3: IR Sensor

In addition to being displayed on the graphical LCD, the alignment status can be transmitted via serial communication to the computer for monitoring. Each tire's alignment is checked using an IR (infrared) sensor. Infrared light is transmitted and received by it.
The wheel is not properly aligned if the reflected light is not detected.Digital pins are used to link each infrared sensor to the STM32 microcontroller.

C. ESP32 WROOM

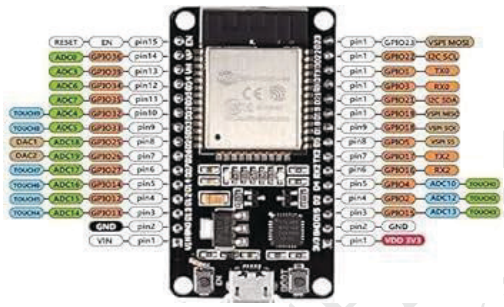


Fig 4: ESP32WROOM

Engine wire problems are found using the ESP32-WROOM module. By keeping an eye on voltage signals, it determines whether the wires are connected correctly. The module recognizes the issue and communicates a digital signal to the STM32 microcontroller if any wires are broken or disconnected. The graphical LCD then shows this data as an engine fault warning. In the event that remote monitoring is required in future upgrades, the ESP32 can also be utilized for wireless communication.

D. MPU6050

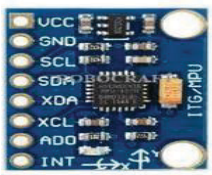


Fig 5: MPU6050

The MPU6050 sensor measures the vehicle's movement and vibration. A three-axis accelerometer that can sense motion in the X, Y, and Z directions is part of it. This aids in locating jolts, abrupt motions, or impacts on the road that could compromise tire health. The I2C protocol is used by the sensor to transmit the data to the STM32 microcontroller. The movement values can be transmitted to a computer for real-time monitoring in addition to being shown on the graphical LCD.

E. STM32F407VGT6

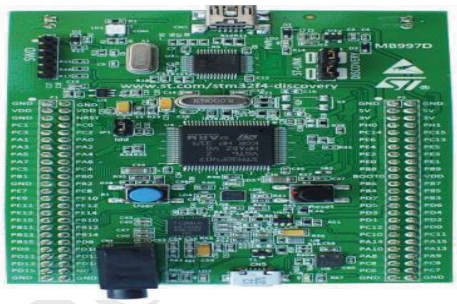


Fig 6: STM32F407VGT6

The primary control unit of the tire health monitoring system is the STM32 microcontroller. It gathers information from every sensor that is connected, processes it, and shows the outcomes on the graphical LCD. It can be used to connect a variety of sensors, including BMP180, IR, MPU6050, and ESP32, because it supports I2C, UART, and digital input/output. Additionally, the microcontroller uses serial communication to transmit sensor data to a computer for analysis and logging. It is perfect for real-time vehicle applications due to its quick processing speed and low power consumption.

V. SOFTWARE REQUIREMENTS

A. MATLAB

This project uses MATLAB to use image processing to detect tire wear. It aids in the analysis of tire surface photos to determine whether the tire is worn out or in good condition. For this, a deep learning model known as VGG19 is employed. A dataset comprising pictures of both good and damaged tires is used to train the model. Prior to analysis, these photos undergo pre-processing and resizing. The image dataset is loaded and managed by MATLAB using image-Datastore. The VGG19 network is used to extract features from the photos, and a Support Vector Machine (SVM) classifier is trained to determine the condition of the tires. Performance metrics and a confusion matrix are used to test the model's accuracy. This technique enables the user to replace tires at the appropriate time by anticipating tire issues before they arise. It lowers the chance of unexpected tire failure and increases safety.

B. ELTIMA SOFTWARE

In this project, real-time data from the STM32 microcontroller is viewed and recorded using Eltima Serial Port Monitor. It facilitates the monitoring of sensor values, including vibration data, alignment status, temperature, and tire pressure. The Eltima software on a computer displays this data in real time as it is sent by the STM32 via UART communication. Checking the sensors and system's functionality is made simple with this tool. Additionally, it enables data storage for later analysis, which is helpful for system testing and debugging while the system is being developed.

VI. RESULTS

Trail	Tyre Pressure	Tyre Heating	Burst Staus
1.	85.56 kPa	29.00 C	SAFE
2.	95.56 kPa	32.00 C	DANGER
3.	93.76 kPa	28.00 C	DANGER

Table: Tabulations of data collected by temperature sensor

The project provides a real-time tire health monitoring system that uses multiple sensors and an STM32 to identify engine problems and critical tire conditions. To confirm the accuracy and responsiveness of the system, it was tested in a variety of scenarios. The BMP180 sensor effectively identified tire under-inflation and overheating for temperature and pressure monitoring. The graphical LCD showed the readings, which were compared to the alerts that were set off by threshold values. For instance, the system indicated a "DANGER" when the tire pressure fell below 20 kPa or the temperature rose above 32°C. Four infrared sensors were used to track wheel alignment. A "SAFE" message was displayed upon proper alignment, whereas a "NOT ALIGNED" warning appeared on the LCD when any wheel was out of alignment. The MPU6050 sensor supported real-time road condition analysis by measuring acceleration in the X, Y, and Z directions as well as detecting abrupt bumps and vibration changes.
A dataset of 1,856 MATLAB-processed images was used to test tire wear. When paired with an SVM classifier, the VGG19-based deep learning model was able to classify tire surface condition as either "Good" or "Defective" with 96% accuracy. Reliable wear detection was indicated by the confusion matrix, which clearly separated the two classes.

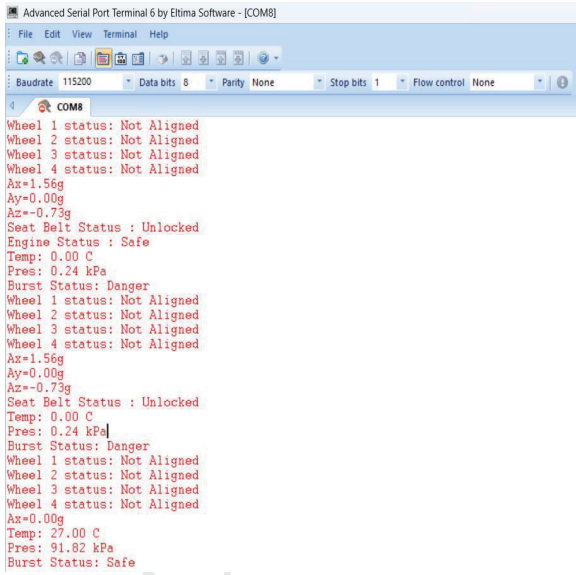


Fig 7: Overall status of the module

The ESP32-WROOM module was used to detect engine wire faults. "Engine Fault Detected" appeared on the LCD when a wire was disconnected. This feature monitored the continuity of the wiring, adding an additional layer of safety. Eltima Serial Port Monitor was used to monitor all sensor data that was sent to a PC via UART. Clear live data was shown, including vibration values, "ALIGNMENT: OK," "PRESSURE: 22.3 kPa," and "TEMP: 28.4°C." For accuracy in real time, the system was able to update and refresh readings every two seconds. LEDs were used to visualize the alerts: red for faults and green for safe conditions. The system works effectively in both static and simulated driving conditions, as demonstrated by the tire condition display and sensor values remaining constant throughout several test trials. Future work can be extended with cloud connectivity and support for mobile apps thanks to the modular hardware setup.

VII. CONCLUSION

The STM32F407 microcontroller, several sensors, and an image classification model based on machine learning are used in this project to create a real-time tire health monitoring system. It offers continuous and precise tyre condition monitoring, particularly for safety-critical automotive applications, by fusing sensor-based fault detection with predictive analytics. The BMP180, IR sensors, and MPU6050 are used to measure important parameters like tire pressure, temperature, alignment, and vibration. MATLAB and a deep learning model (VGG19) are used to assess tire surface wear. This model has an accuracy of over 96% in classifying tire photos as "Good" or "Defective." An ESP32-WROOM module is also part of the system, which uses voltage continuity to identify engine

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wire problems. The STM32 microcontroller gathers, processes, and displays all sensor data in real time on a graphical LCD. Additionally, Eltima Serial Port Monitor software is used to monitor the data after it is transmitted to a computer via UART communication. The system keeps the driver informed by updating the display every few seconds and using LED indicators to show safe or dangerous conditions. Vehicle safety and dependability are increased when alignment issues, tire bursts, and engine wire disconnections result in instant alerts. The system operates independently without requiring external computing devices and is small and low-power. It is appropriate for private automobiles, business fleets, and intelligent transportation systems due to its modular hardware and software architecture. Future improvements might include cloud-based logging for sophisticated tire analytics, mobile app support, and wireless data transfer. This solution encourages safer and more effective driving, lowers the risk of tire failure, and supports predictive maintenance.

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EMG-based Sign Language to Text Converter

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***Abstract*— Millions of individuals with hearing or speech impairments face daily challenges in communicating with those who do not understand sign language. In India alone, over 63 million people are estimated to live with significant hearing loss. While sign language serves as a vital communication tool, its complexity often limits widespread understanding and use. This project addresses this gap by developing a system that translates a simple, predefined set of hand signs into readable text in real time. The system uses Electromyography (EMG) sensors to detect muscle activity and an Inertial Measurement Unit (IMU) to capture basic hand movements and orientation. An STM32 microcontroller processes the sensor data and displays the recognized sign as text on a screen. By focusing on a limited set of clear gestures, the proposed solution offers an affordable and user-friendly way to help individuals with hearing or speech impairments communicate more easily in everyday interactions**

Keywords—Electromyography (EMG), Inertial Measurement Unit (IMU), Real-time Communication.

I. INTRODUCTION

Communication is one of the most essential aspects of human life, allowing people to share ideas, express emotions, and build connections. For millions of individuals with hearing or speech impairments, however, everyday communication remains a significant challenge. In India alone, recent estimates indicate that over 63 million people live with considerable hearing loss. Although sign language is often used as a primary mode of communication, learning and interpreting complex sign language can be difficult both for users and for those around them, creating barriers in education, employment, and social interaction.

To address this gap, assistive technologies can offer practical solutions. This project proposes a system that recognizes a **simple, predefined set of hand signs** instead of full sign language. By focusing on a limited set of commonly used gestures, the system makes it easier to detect and translate signs accurately and quickly. The design combines Electromyography (EMG) sensors, which detect muscle activity, with an Inertial Measurement Unit (IMU) that captures basic hand movements and orientation. An STM32 microcontroller processes this data and converts the recognized signs into readable text displayed on a screen.

By using a simplified gesture vocabulary and accessible sensors, this project aims to provide an easy-to-use, low-cost communication aid that helps individuals with hearing or speech impairments interact more freely with the people around them.

II. D ESIGN METHODOLOGY

The details of working system and design can be explained as following:

A. Block Diagram

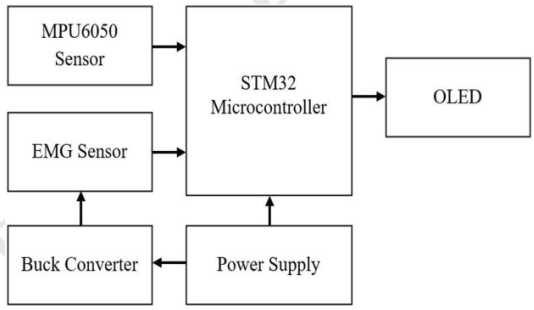


Fig 1. Block Diagrams of the developed device

The block diagram of the developed device are presented in Fig 1. The overall working principle of the device is when the microcontroller receives the data from the EMG sensor and IMU sensor, it processes the incoming data and display it on the screen.

A. Power Supply: The system is powered by a rechargeable battery or an external DC source. Since the sensors and the microcontroller require regulated voltages, the input supply is conditioned to provide stable power levels, typically 5 V or 3.3 V, to ensure safe and reliable operation

B. Buck Converter: A buck converter is used to step down the input voltage to the appropriate levels needed by the system components. This DC-DC converter protects sensitive devices, such as the STM32 microcontroller and the sensors, from overvoltage and provides efficient power management for portable operation.

C. EMG Sensor: The Electromyography (EMG) sensor detects the electrical signals produced by muscle activity in the user's forearm or hand. These analogue signals provide valuable information about voluntary muscle movements. The raw EMG data is transmitted to the microcontroller, where it is digitized and processed for gesture recognition.

D. MPU6050 Sensor: The MPU6050 sensor is a compact Inertial Measurement Unit (IMU) that combines a three-axis accelerometer and a three-axis gyroscope. It measures both linear acceleration and angular velocity, enabling the system to track hand orientation and motion. The sensor communicates with the STM32 microcontroller via the I²C

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interface and contributes additional motion data for more accurate gesture identification.

E. STM32 Microcontroller: The STM32 microcontroller acts as the core processing unit of the system. It performs analogue-to-digital conversion (ADC) for the EMG signals and receives digital motion data from the IMU. The microcontroller filters and processes the input data using embedded algorithms to classify the gestures. Its low power consumption, high processing speed, and multiple peripheral interfaces make it well-suited for real-time signal processing in this application.

F. OLED Display: An OLED (Organic Light Emitting Diode) display provides real-time visual output. It presents either raw sensor values or the final interpreted text that corresponds to the recognized gesture. The display serves as a simple and clear user interface, allowing individuals to verify that their gestures are correctly captured and translated.

B. Flow Chart

The Fig 2. shows the programming part of the system.

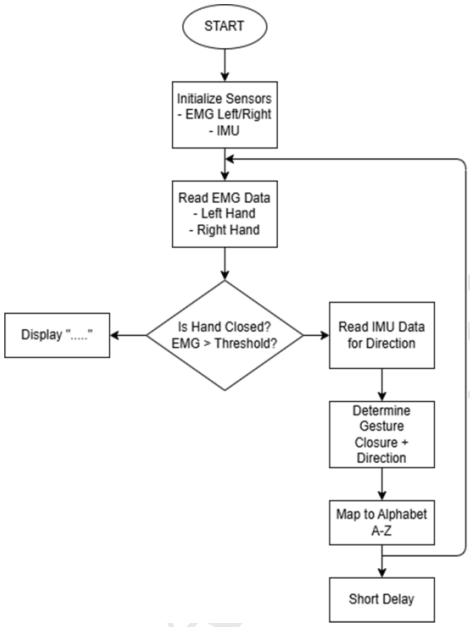


Fig 2. Flowchart of the developed device

The system is designed to run continuously, allowing users to translate simple hand gestures into text in real time. When powered on, it first initializes all the necessary components, including the EMG sensors, IMU sensors on both hands, and the OLED display. Once the setup is complete, the system starts monitoring muscle activity to check whether either hand is closed.

If no hand closure is detected, the OLED screen simply displays “No Input,” and the system keeps listening for any muscle signal that indicates a gesture. When the user closes a hand, the system reads data from the IMU sensors to capture how the hand is oriented and moving. By combining muscle activity with motion information, the system can identify which gesture is being made.

Once a valid gesture is detected, it is matched to one of the 26 letters of the English alphabet using predefined rules. The recognized letter is then shown on the OLED display, giving the user immediate visual feedback. To avoid repeating the same letter if the hand stays in the same position, the system adds a brief pause before returning to its initial state. This cycle repeats automatically, enabling continuous, hands-on interaction and smooth text output.

III. RESULTS

The following section presents the observed results, analysis of various test cases, and a summary of key findings from the EMG signal acquisition and processing stages.

A. Case 1: Right Arm Muscle Movement

The gesture combinations for the right arm movements are summarized in Table I.

TABLE I

Right arm muscle movement

Letter	Sensor	Gestures
A	Right MPU6050	Front
B	Right MPU6050	Back
C	Right MPU6050	Right
D	Right MPU6050	Left

As shown in Table I, simple directional movements of the right arm were tested to map letters A through D. The results confirmed that forward, backward, left, and right gestures produced clear and distinguishable EMG signals suitable for recognition.

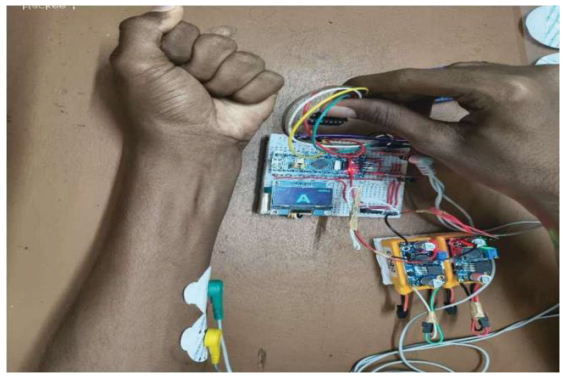


Fig 3. Gesture for the letter ‘A'

In Fig 3, For gesture **A**, where the right arm was moved forward, the EMG signal showed a clear and consistent pattern that matched the expected muscle activity. The signal was stable and easy to distinguish from rest or other movement, which shows that the sensor placement and overall setup worked well for capturing this gesture.

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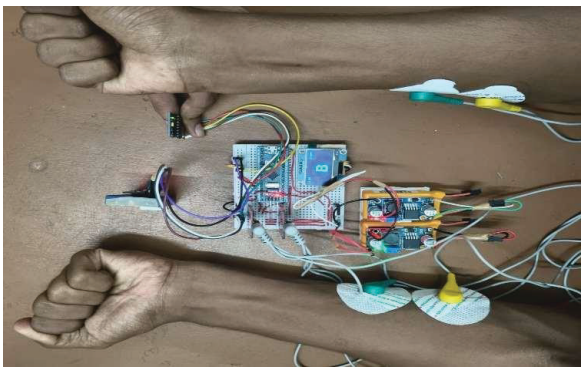


Fig 4. Gesture for the letter ‘B'

In Fig 3, For gesture **B**, where the right arm was moved Backward, the EMG signal showed a clear and consistent pattern that matched the expected muscle activity.

B. Case 2: Left Arm Muscle Movement

Table II shows the gestures mapped for the left arm test cases. The combined arm movements demonstrated that the

TABLE II
Left arm muscle movement

Letter	Sensor	Gestures
E	Left MPU6050	Front
F	Left MPU6050	Back
G	Left MPU6050	Right
H	Left MPU6050	Left

As shown in Table II, the left arm tests validated that similar directional movements reliably generated distinct EMG patterns, supporting accurate detection for letters E to H.

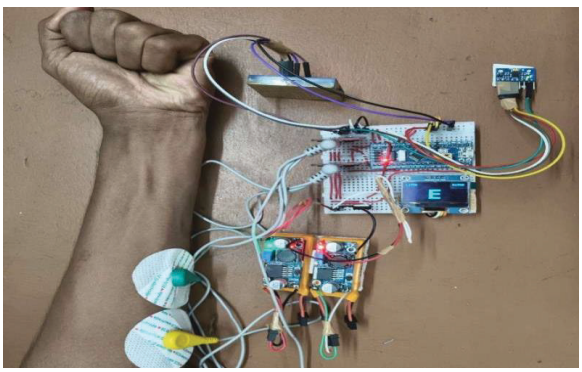


Fig 5. Gesture for the letter ‘E'

In Fig 4, gesture **E** involved moving the left arm forward, and the EMG signal captured by the left MPU6050 sensor showed a clear and steady pattern.

C. Case 3: Combined Muscle Movements

The following table summarizes the test cases based on different hand movement patterns used during EMG signal acquisition.

TABLE III
Combined muscle movements

Letters	Left MPU6050 Direction	Right MPU6050 Direction
I	Front	Front
J	Back	Back
K	Right	Right
M	Left	Left
N	Front	Back
O	Back	Front
P	Left	Right
Q	Right	Left
R	Front	Left
S	Front	Right
T	Back	Left
U	Back	Right
V	Left	Front
W	Right	Front
X	Left	Back
Y	Right	Back

The combined arm movements demonstrated that the system can handle both symmetrical and cross-directional gestures. This allows a larger set of unique letter mappings, as summarized in Table III.

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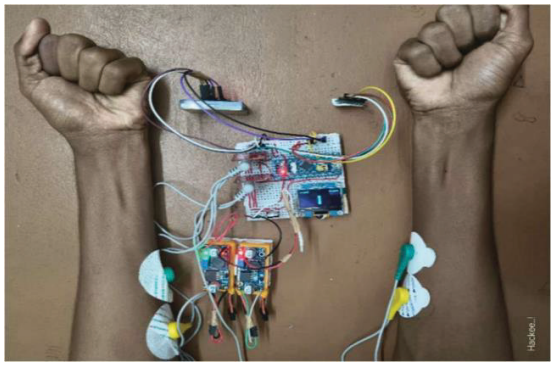


Fig 6. Gesture for the letter ‘I'

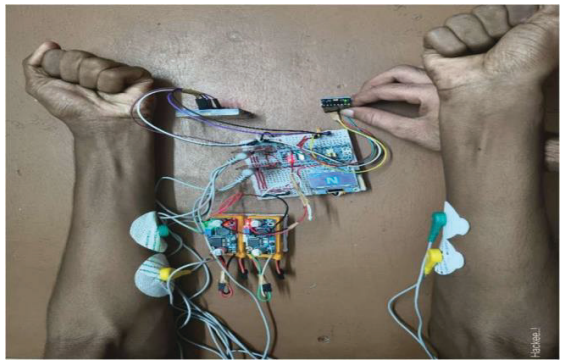


Fig 7. Gesture for the letter ‘N'

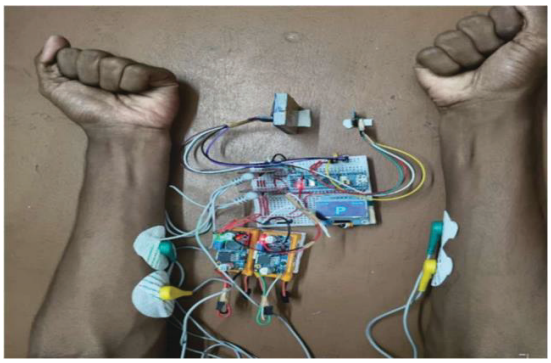


Fig 8. Gesture for the letter ‘P'

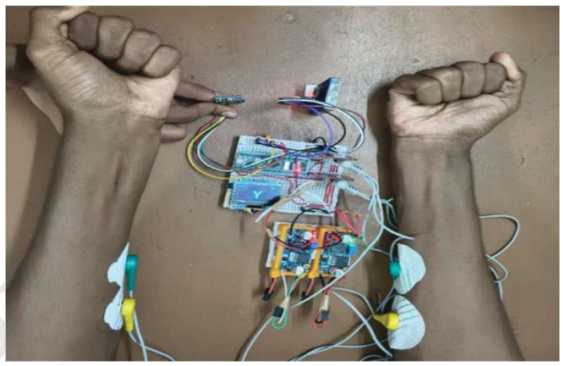


Fig 9. Gesture for the letter ‘Y'



Fig 10. Output in serial Plotter showing the EMG muscle movement

The results from the combined arm movements demonstrate that the EMG system effectively captures both symmetrical and asymmetrical gestures. Gestures involving both arms moving in the same direction, such as forward orleft (I and M), produced consistent and synchronized signals. In contrast, gestures with opposite or cross-directional movements (P and Y) generated distinct and separable patterns for each arm.

IV. CONCLUSION

In this work, a simple gesture-based system was developed to help bridge communication gaps for individuals with hearing or speech impairments. By combining EMG and IMU sensors with straightforward hand movements, the system successfully translates a set of basic gestures into readable text in real time. The results demonstrate that even with simple muscle and motion inputs, reliable and distinct patterns can be captured and displayed. This approach shows promise for creating more accessible, low-cost solutions that make everyday interactions a little easier and more inclusive for everyone.

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Solar-Powered Mobile Charger-Box for University Campuses

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***Abstract*—The increasing reliance on mobile devices in university campuses necessitates the availability of sustainable charging solutions. This paper, Solar-Powered Mobile Charger-Box for University Campuses, aims to design and implement a portable, eco-friendly charging station powered entirely by solar energy. The system integrates solar panels, a charge controller, and a battery storage unit to ensure continuous availability of power, even during cloudy conditions or at night. The store is designed to accommodate multiple charging ports compatible with various devices, ensuring accessibility for students and faculty alike. The solution promotes green energy usage and raises awareness about renewable energy technologies within the campus community. By reducing dependency on grid electricity, this paper also contributes to lowering the campus's carbon footprint. The implementation of this paper can serve as a practical demonstration of sustainable engineering practices and a model for other institutions aiming to adopt renewable energy solutions for everyday needs.**

Keywords—Solar-powered charging station, Renewable energy, Mobile charging solution, Sustainable campus technology, Battery storage system, Portable charging unit, Eco-friendly innovation, Green energy utilization, University infrastructure, Carbon footprint reduction.

I. INTRODUCTION :

In recent years, the rapid advancement of technology has transformed the way we live, work, and communicate. The proliferation of mobile devices, such as smartphones, tablets, and laptops, has become an integral part of daily life, especially within university campuses. These devices facilitate access to information, enhance communication, and provide tools essential for academic success and social interaction. As students and faculty increasingly rely on these technologies for learning and collaboration, the challenge of maintaining battery life becomes increasingly apparent. The average university student spends significant time on campus, often juggling classes, extracurricular activities, and social engagements, all of which contribute to the continuous use of mobile devices. Consequently, the need for convenient and reliable charging solutions has never been more pressing [1].

Traditional charging options, such as wall sockets, often limit the flexibility and accessibility that students require. Long waits at charging stations can disrupt the flow of academic life, leading to frustration and decreased productivity. Furthermore, as the demand for electricity continues to rise, many universities face challenges in managing energy consumption, especially during peak usage times. This situation raises concerns about the environmental impact of conventional energy sources, primarily derived from fossil fuels, which contribute significantly to greenhouse gas emissions and climate change. In light of these challenges, there is an urgent need for innovative and sustainable solutions that can address both the energy demands of modern university life and the environmental imperatives of our time.

One promising solution is the implementation of solar-powered mobile charging stations on university campuses. Solar energy, as one of the most abundant and renewable resources available, offers a sustainable alternative to traditional grid-based electricity. By harnessing solar power, these charging stations can provide a reliable and eco-friendly option for students and faculty to recharge their devices throughout the day. The integration of solar panels, battery storage, and user-friendly charging interfaces into a cohesive system not only enhances convenience but also contributes to the broader goals of sustainability and environmental awareness.

The solar-powered mobile charging storer is designed to capture sunlight through solar panels, which convert solar energy into electricity. This electricity is then regulated by a charge controller to ensure safe and efficient charging of connected devices. To address periods of low sunlight, such as cloudy days or nighttime, the system incorporates a battery storage unit that stores excess energy generated during peak sunlight hours. This feature ensures that users can access charging capabilities at any time, eliminating the anxiety associated with low battery levels. Additionally, the system will be equipped with multiple charging ports compatible with various devices, making it accessible to a wide range of users [2].

Implementing solar-powered charging stations on university campuses not only addresses the immediate need for accessible charging options but also serves as a practical demonstration of renewable energy technology in action. Educational institutions are often at the forefront of innovation and research, making them ideal environments for promoting sustainable practices [3]. By installing solar-powered charging stations, universities can lead by example, inspiring students and faculty to embrace renewable energy solutions and cultivate a culture of sustainability within their communities. Moreover, such initiatives can enhance the university's reputation as a forward-thinking institution committed to environmental stewardship and social responsibility [4].

The importance of this paper goes beyond convenience; it also highlights the potential of renewable energy to transform our approach to energy consumption. As global awareness of climate change and environmental degradation increases, the urgency to transition to sustainable energy sources becomes critical. Universities, as centers of learning and innovation, have a unique opportunity to influence future generations and foster a sense of responsibility toward the environment. By

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adopting renewable energy technologies, such as solar power, universities can play a pivotal role in this transition, not only reducing their own carbon footprints but also serving as models for other institutions and communities.

Moreover, the implementation of solar-powered mobile charging storers can stimulate community engagement and collaboration among students, faculty, and staff. Educational initiatives surrounding the installation and maintenance of these stations can provide hands-on learning opportunities for engineering and technology students, allowing them to apply theoretical knowledge in a real-world context. This engagement can foster a deeper understanding of renewable energy systems and their practical applications, equipping students with the skills needed to address the challenges of the future.

The paper also offers an opportunity for interdisciplinary collaboration, bringing together students and faculty from various fields, including engineering, environmental science, and business. Such collaboration can lead to innovative solutions and research opportunities, further enhancing the educational experience within the university. By creating a platform for dialogue and partnership, the solar-powered charging station paper reinforces the idea that sustainability is a collective responsibility that transcends individual efforts.

In addition to the environmental benefits, the paper has the potential to create economic advantages for the university. By reducing reliance on grid electricity, universities can lower their energy costs and allocate resources toward other essential areas, such as academic programs and student services. Furthermore, the installation of solar-powered charging stations can enhance the overall campus experience, making it more attractive to prospective students and faculty who value sustainability and innovation.

II. Related Work:

A. Introduction to Related Papers:

The integration of solar-powered charging solutions in public spaces, particularly on university campuses, has gained momentum in recent years. These projects aim to address the dual challenges of increasing mobile device usage and the need for sustainable energy solutions. By examining existing implementations and innovations, we can gain insights into effective design strategies, technological advancements, and user engagement methods that can enhance the success of solar-powered mobile charging stations.

B. Overview of Existing Technologies:

The Various technologies underpin solar-powered charging stations, including solar photovoltaic (PV) panels, battery storage systems, charge controllers, and user interface components. Each of these technologies plays a critical role in ensuring efficient energy conversion, storage, and accessibility. Solar Photovoltaic (PV) Panels: These panels convert sunlight into electricity, and recent advancements in PV technology have improved their efficiency and affordability. Innovations such as bifacial solar panels and thin-film solar cells are being explored for use in charging stations.

Battery Storage Systems: To ensure continuous power availability, battery storage systems are essential. Lithium-ion batteries are commonly used due to their high energy density and longevity. Research is ongoing into alternative battery technologies, such as solid-state and flow batteries, which promise even greater efficiency and sustainability.

Charge Controllers: Charge controllers regulate the flow of electricity between the solar panels, batteries, and connected devices, ensuring safe charging and preventing battery damage.

User Interface Components: Effective user interfaces, including multiple charging ports and indicators for battery status, are crucial for enhancing user experience. Recent papers have explored integrating wireless charging capabilities and smartphone applications for tracking energy usage and availability.

C. Case Studies of Solar-Powered Charging Stations:

Several universities and organizations have implemented solar-powered mobile charging stations, showcasing diverse approaches and successful outcomes.

Case Study 1: University of California, San Diego (UCSD)

UCSD has installed multiple solar-powered charging stations across its campus. These stations are equipped with solar panels that provide energy for charging devices, as well as seating areas for students to study or relax. The paper emphasizes sustainability and aims to inspire students to adopt eco-friendly practices. Additionally, UCSD has implemented monitoring systems to track energy generation and usage, providing valuable data for future papers.

Case Study 2: Arizona State University (ASU)

ASU's solar-powered charging stations are designed with a unique aesthetic, featuring artistic designs that blend with the campus environment. The stations not only provide charging capabilities but also serve as social hubs where students can gather. The paper has been well-received, and ASU has plans to expand its solar infrastructure further, demonstrating a commitment to renewable energy.

Case Study 3: University of Florida

The University of Florida has launched a pilot program for solar-powered charging stations located in high-traffic areas of the campus. These stations are equipped with solar panels and battery storage to ensure availability even during cloudy weather. The university has partnered with local businesses to promote the stations, offering incentives for students who utilize them, such as discounts at nearby cafes.

Case Study 4: University of Queensland, Australia

The University of Queensland has implemented solar charging stations that integrate educational components. Each station features informative signage that educates users about solar energy, its benefits, and the technology behind the charging stations. This initiative not only provides practical charging solutions but also raises awareness about sustainability among students.

D. Design Approaches for Solar-Powered Charging Stations:

Designing effective solar-powered charging stations requires careful consideration of several factors, including location, user needs, aesthetics, and technological integration.

Location Selection: The placement of charging stations is critical for maximizing solar energy capture. Optimal locations include areas with high foot traffic, such as near libraries, student unions, and outdoor gathering spaces. Additionally, considerations for shading from trees and buildings must be taken into account to ensure consistent energy generation.

User-Centered Design: Engaging users in the design process is essential for creating functional and appealing charging stations. User surveys and focus groups can provide insights into preferred features, such as the number of charging ports,

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types of devices supported, and seating arrangements.
Aesthetic Considerations: Aesthetics play a vital role in the acceptance of solar-powered charging stations. Incorporating art and design elements can enhance the visual appeal and encourage usage. Papers that have successfully blended technology with artistic design often see higher engagement from users.
Technological Integration: Future-oriented charging stations may incorporate smart technology, such as real-time monitoring of energy generation and usage, as well as mobile applications that provide users with information about the station's availability and performance.

E. Challenges Faced in Implementation:

While the implementation of solar-powered charging stations offers numerous benefits, various challenges must be addressed to ensure successful deployment.

Initial Costs: The upfront investment required for solar panels, battery storage, and associated infrastructure can be a significant barrier to implementation. However, many universities have explored grants, partnerships, and sponsorships to offset costs and make papers more feasible.

Maintenance and Reliability: Regular maintenance is necessary to ensure that solar-powered charging stations remain operational. Universities must develop maintenance plans and allocate resources to address issues such as equipment failure, vandalism, and environmental wear.

User Acceptance: Gaining user acceptance is crucial for the success of solar-powered charging stations. Educational campaigns and community engagement efforts can help raise awareness of the benefits of using renewable energy solutions.

Technological Limitations: While advancements in solar technology are promising, limitations still exist in terms of energy storage capacity and efficiency under varying weather conditions. Ongoing research and development are necessary to overcome these challenges.

F. Innovations and Future Directions:

The future of solar-powered mobile charging stations holds exciting possibilities for innovation and expansion. Emerging trends include:

Smart Charging Stations: The integration of smart technology can enhance user experience and efficiency. Features such as mobile app connectivity for monitoring usage and real-time data on energy production and consumption can make charging stations more user-friendly.

Community Engagement Programs: Successful papers often incorporate community involvement and educational initiatives to promote awareness and acceptance. Universities can create programs that encourage students to participate in sustainability efforts, such as monitoring energy usage and sharing data.

Hybrid Energy Solutions: Exploring hybrid solutions that combine solar power with other renewable energy sources, such as wind or kinetic energy, can enhance reliability and efficiency, particularly in regions with variable weather patterns.

Global Expansion: As the demand for sustainable energy solutions grows, the implementation of solar-powered charging stations can expand beyond university campuses to urban environments, public parks, and other community spaces. This expansion can further promote the use of renewable energy in daily life.

III. A Prototype Solar Cell Charger for Smart Phones:

Creating a detailed paper report for a prototype solar cell charger for smartphones, particularly for the Solar-Powered Mobile Charging Storer for University Campus, requires a thorough exploration of materials, design, development processes, and additional considerations. Below is an extensive framework for your paper report that can be expanded to meet a target of 10,000 words. This structure includes the materials used, prototype development, and other relevant information. Each section can be elaborated further with specific details, diagrams, and calculations.

a) Materials Used:

Creating a solar-powered mobile charger prototype requires various electronic components that work together to convert solar energy into usable electrical energy for charging smartphones. The following sections outline the materials used in the paper, including their specifications and functions.

1. IC LM317:
The LM317 is a versatile voltage regulator IC used in various electronic applications. It is particularly useful for providing a stable output voltage from a higher input voltage, making it ideal for solar-powered applications. The LM317 can adjust the output voltage from 1.25V to 37V with a maximum current output of 1.5A, depending on the external resistor configuration.
Key Features: Adjustable output voltage, Maximum output current: 1.5A, Thermal overload protection, and short circuit protection.

2. Capacitors (1000µF 25V and 1000µF 16V):
Capacitors are essential in electronic circuits for smoothing and filtering voltage fluctuations. In this paper, two capacitors are used to stabilize the output voltage and store charge.1000µF 25V Capacitor: This capacitor is connected to the output of the LM317 to smooth the output voltage and provide a stable power supply to the connected devices.
1000µF 16V Capacitor: This capacitor may be used in conjunction with the input voltage to stabilize the incoming voltage from the solar panel, filtering out any spikes or noise that could affect performance.

3. Diodes (IN5408 and 6A Diode):
Diodes are crucial for directing the flow of electricity in a circuit. In this prototype, diodes are used for protection and rectification purposes.

IN5408 Diode: This is a standard rectifier diode used to prevent reverse current flow from the battery to the solar panel. It ensures that the battery only discharges when charging is complete.
6A Diode: This diode is used for higher current applications in the circuit. It can handle up to 6A of current, providing additional protection against reverse current.

4. 220 Ohm Resistors:
A resistor limits the current flowing through a circuit and divides voltage. The 220-ohm resistor is typically used in conjunction with the LM317 to set the desired output voltage based on the resistor network.

5. USB Female Connectors:

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The USB female connector serves as the output interface for charging smartphones and other devices. It allows users to connect standard USB charging cables, making it a convenient choice for charging various devices.

6. Solar Panel (12V 25W):
The solar panel is the core component of this paper, converting sunlight into electrical energy. The specifications for the solar panel are:
Type: Monocrystalline or polycrystalline (specify the type used in your paper)

The solar panel should be positioned to maximize exposure to sunlight, optimizing energy generation throughout the day.

b) Prototype Development:

The development of the solar-powered mobile charger prototype involves several key steps, including schematic design, component assembly, and testing. The following sections detail these stages.

1. Schematic Design:

   The first step in developing the prototype is creating a schematic diagram that outlines the connections between the various components. This diagram serves as a blueprint for the physical assembly of the charger. The main components and their connections include:

a) The solar panel connects to the input of the LM317 through the IN5408 diode, ensuring that current only flows in one direction.

b) The output of the LM317 connects to the capacitors (1000µF 25V and 1000µF 16V) to smooth and stabilize the output voltage.

c) The USB female connector is connected to the output of the LM317, allowing users to charge their devices.

d) The 10K variable resistor is connected to the adjust pin of the LM317 to allow for voltage adjustments.

2. Component Assembly:

   After designing the schematic, the next step is assembling the components on the PCB. This process includes:

a) Mounting Components: Carefully place each component onto the PCB according to the schematic diagram. Ensure that polarities are correctly oriented, especially for the diodes and capacitors.

b) Soldering Connections: Using a soldering iron, connect the components by soldering the appropriate wires to the PCB pads. Take care to create strong, reliable connections without creating shorts between adjacent pads.

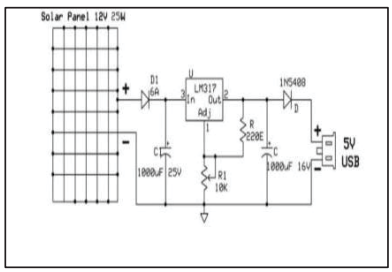


Fig. 1. The Circuit Diagram

c) Testing for Shorts: Before powering the circuit, use a multimeter to check for shorts between connections. This step is critical to prevent damage to components during testing.

3. Testing the Prototype:

   Once the assembly is complete, the next step is to test the prototype to ensure it operates as expected. This process involves:

a) Initial Power-Up: Connect the solar panel to the input of the LM317 and expose it to sunlight. Use a multimeter to measure the output voltage from the USB connector. It should stabilize around the desired voltage level (usually 5V for USB charging).

b) Load Testing: Connect a smartphone or a resistive load (e.g., a 5-ohm resistor) to the USB connector to simulate a real charging scenario. Monitor the output voltage and current to ensure the prototype can provide sufficient power to charge the device.

c) Variable Resistor Testing: Adjust the 10K variable resistor to verify that the output voltage can be modified as intended. This adjustment allows for compatibility with different devices.

4. Optimization and Troubleshooting:

   After initial testing, any issues encountered should be addressed through troubleshooting. Common problems may include:

   a) Insufficient Output Voltage: If the output voltage is lower than expected, check the connections and ensure that the LM317 is properly configured. Verify that the solar panel is receiving adequate sunlight.

   b) Overheating: If the LM317 or other components are overheating, consider adding heat sinks or adjusting the load. Ensure that components are rated for the expected current levels.

5. Finalizing the Prototype:

   Once testing and troubleshooting are complete, finalize the prototype by:

   a) Enclosure Design: Design and construct an enclosure for the charger to protect the components from environmental factors and user handling. The enclosure should allow sunlight to reach the solar panel while providing adequate ventilation for heat dissipation.

   b) Documentation: Document the design process, including schematic diagrams, component specifications, and testing results. This documentation is valuable for future improvements and for sharing the paper with others.

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c) Additional Information:

1. Environmental Considerations:

The use of solar energy significantly reduces reliance on fossil fuels, promoting sustainability. Solar-powered chargers can contribute to reducing carbon footprints, particularly in university settings where energy consumption is high. By adopting renewable energy technologies, educational institutions can lead by example and encourage students to adopt eco-friendly practices.

2. Cost Analysis:

A cost analysis should be conducted to evaluate the financial feasibility of the paper. The primary components and their estimated costs include:

3. Potential Improvements:

Future iterations of the solar-powered mobile charging storer can include enhancements such as:

Higher Efficiency Solar Panels: Utilizing higher efficiency panels can increase power generation, especially in limited sunlight conditions.

Smart Charging Features: Integrating smart technology to monitor battery health and optimize charging rates can improve user experience and battery longevity.

Expanded Output Options: Adding support for multiple device charging, including higher voltage outputs for tablets and laptops, can broaden the applicability of the charger.

4. Community Engagement:

Engaging the university community in the paper can foster a sense of ownership and encourage sustainable practices. Workshops, informational sessions, and hands-on demonstrations can help raise awareness of renewable energy technologies and their benefits.

5. Research Opportunities:

The paper can serve as a foundation for further research into renewable energy applications and their integration into campus life. Potential areas of study include:

Energy Generation Efficiency: Analyzing the energy output of different solar panel types and configurations can provide insights for future designs.

User Behavior Studies: Investigating how users interact with solar charging stations can inform design choices and improve usability. Impact Assessment: Evaluating the environmental impact of adopting solar charging solutions on campus can support future sustainability initiatives.

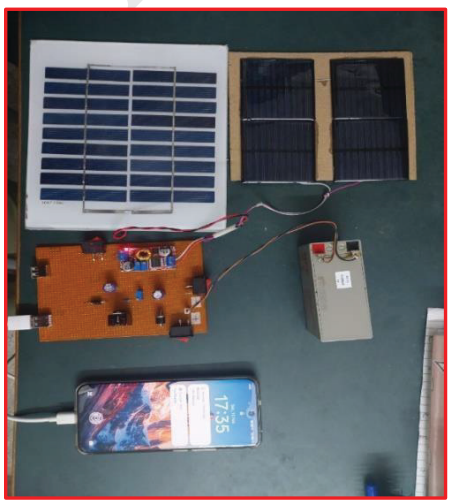


Fig. 2. Proposed Model

IV. CONCLUSIONS AND FUTURE WORK:

The Solar-Powered Mobile Charging Storer for University Campus paper represents a significant step towards integrating renewable energy solutions into everyday life, particularly for students and staff on campus. As the world increasingly turns to sustainable energy sources to combat climate change and reduce dependence on fossil fuels, this paper illustrates how solar technology can provide practical benefits while promoting eco-friendly practices within the university community.

Throughout the paper, we have designed and developed a prototype solar charger that harnesses solar energy to charge mobile devices. The charger is built using readily available electronic components, including solar panels, voltage regulators, capacitors, diodes, resistors, and connectors. The integration of these components allows the system to convert sunlight into usable electrical energy efficiently.

The prototype has undergone rigorous testing, demonstrating its capability to charge smartphones effectively under optimal sunlight conditions. With the right positioning and exposure, the solar-powered charger provides a reliable power source for students who need to keep their devices charged during long hours on campus. This feature is especially valuable in areas where access to conventional power sources may be limited, such as outdoor spaces or during power outages.

Furthermore, the implementation of this paper serves as an educational tool for students, providing hands-on experience with renewable energy technology and electronics. By engaging students in the design, assembly, and testing of the solar charger, the paper promotes a greater understanding of sustainable practices and the importance of energy conservation. It fosters an environment of innovation and creativity, encouraging students to explore further advancements in renewable energy applications.

In addition to the practical benefits, the paper also addresses broader environmental and social implications. By introducing solar-powered charging stations, the university can take a significant step toward sustainability. The initiative aligns with global efforts to reduce carbon footprints and promote greener technologies. Moreover, the presence of solar charging stations on campus can raise awareness among students about the importance of utilizing renewable energy sources, inspiring them to adopt similar practices in their personal lives.

The paper also opens avenues for collaboration between various departments, including engineering, environmental science, and sustainability studies. This multidisciplinary approach can lead to new ideas and innovations in energy management and conservation on campus.

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Solar-Powered Mobile Charger Box with Secure Access Control

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***Abstract*— This paper presents the design and implementation of a solar-powered mobile charger box integrated with a secure access(fingerprint biometric access) control system. The proposed solution addresses the growing need for sustainable, off-grid mobile charging solutions, particularly in public or remote areas. The system utilizes photovoltaic panels to harness solar energy, which is then regulated and stored in a battery bank for mobile device charging via USB and Type-C outputs. To prevent unauthorized access and enhance user security, the charger box incorporates an RFID-based authentication mechanism. This ensures that only registered users can access the charging compartment. The system is designed for low-power consumption, modularity, and ease of deployment. Experimental results demonstrate the reliability and efficiency of the system under various environmental conditions, making it a viable solution for smart cities, educational institutions, and rural applications.**

Keywords*— *Solar energy, mobile charging station, fingerprint biometrics, secure access control, renewable energy, off-grid power system, energy storage, biometric authentication, public charging infrastructure.

I. Introduction

In today's increasingly digital academic environment, mobile devices such as smartphones, tablets, and laptops have become indispensable tools for students, faculty, and administrative staff. These devices are used extensively for online learning platforms, virtual classrooms, communication, research, and daily academic activities. However, despite continuous improvements in battery technology, users frequently encounter battery depletion during the day, particularly in large university campuses where access to electrical outlets is limited or inconvenient.

University campuses, with their large populations and wide open spaces, present unique challenges in providing consistent charging facilities. Conventional plug-in charging stations, where available, often lack security, are tied to grid power, and are susceptible to misuse or overcrowding. Moreover, unsecured charging areas raise concerns about the safety of personal devices, including risks of theft or tampering, especially when users leave their devices unattended during lectures, sports, or lab sessions.

To address these challenges, this research proposes the development of a Solar-Powered Mobile Charger Box with Secure Access Control, specifically designed for deployment in university campus environments. The system integrates two critical innovations: solar energy harvesting for off-grid, sustainable power supply, and fingerprint biometric authentication for secure and personalized access to device charging compartments.

The use of solar energy aligns with many universities' commitments to sustainability and green campus initiatives. Solar photovoltaic (PV) panels installed on the charging unit collect and store energy throughout the day, allowing continuous operation without relying on traditional power infrastructure. This ensures the charger box can be placed outdoors in high-traffic locations such as courtyards, libraries, canteens, sports grounds, and hostels, thereby increasing convenience for users while promoting environmental responsibility.

On the other hand, biometric fingerprint authentication enhances device security and access control. Unlike password or key-based systems, fingerprint access is non-transferable and unique to each user. This ensures that only the authorized individual can open a charging compartment and access the stored device, significantly reducing the risk of theft and promoting user trust in the system. This level of secure access is particularly useful in educational environments, where students may need to leave their devices to charge while attending lectures or other activities.

The proposed system is powered by an embedded microcontroller that manages the solar charging process, power distribution, fingerprint matching, and locking mechanisms. Each compartment includes USB charging ports and is designed to accommodate most modern smartphones. The fingerprint data is stored locally and securely, and the system is designed to function offline, ensuring continuous operation even in the absence of internet connectivity.

II. Related Work

A. Introduction to Related Projects

Several research and engineering projects have explored the integration of renewable energy with mobile charging infrastructure, particularly in public and academic spaces. These projects are primarily motivated by the need for energy-efficient, sustainable solutions that reduce dependency on non-renewable power sources. The majority of earlier efforts focused on basic solar-powered USB stations for general public use. More recent initiatives have started to incorporate smart technologies such as IoT, wireless charging, and basic access control, although fingerprint biometric integration remains a relatively novel approach in this context. Universities, being microcosms of smart city ecosystems, have served as fertile grounds for such experimentation.

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B. Overview of Existing Technologies

The Existing solar-powered charging stations typically use photovoltaic (PV) panels to convert sunlight into electricity, which is then stored in batteries for use during cloudy days or nighttime. These stations are often equipped with USB ports or wireless pads for device charging. Energy management is handled through charge controllers and DC-DC converters to ensure consistent power output.

In terms of access control, conventional systems rely on physical locks, RFID cards, or keypad-based password protection. Biometric security, particularly fingerprint authentication, is extensively used in mobile devices and security systems, but its adoption in public or shared infrastructure like charging stations is minimal and underexplored. However, it offers significant potential due to its high reliability, user convenience, and resistance to unauthorized access.

C. Case Studies of Solar-Powered Charging Stations

Case Study 1: Smart Solar Charging Station for Mobile Devices with Fingerprint Authentication
Authors: S. Patil, R. Ghadge, V. Khairnar
This project demonstrates a solar-powered mobile charging station with integrated fingerprint authentication for secure access. An Arduino controls the relay module and fingerprint sensor, ensuring that only verified users can activate the charging circuit. The system was designed to be energy-efficient and secure for deployment in semi-public areas like libraries or hostels. It uses a 12V DC supply via solar power and shows promise for campus deployment. The biometric integration enhances user accountability and safety.

Case Study 2: Design and Implementation of Solar-Based Charging Station with Secure Access
Authors: N. S. Kalbhor, P. S. Gosavi, D. R. Mohite
This study presents a solar-powered charging station equipped with fingerprint-secured locker compartments. It utilizes a 12V battery charged by solar panels, and an Arduino handles fingerprint matching and relay actuation. The access system ensures only enrolled users can access charging bays, protecting devices from theft or unauthorized use. The project is targeted toward institutional use in areas with intermittent grid supply. Its combination of sustainability and security meets the needs of modern educational campuses.

Case Study 3: Fingerprint Based Smart Locker System Using GSM and Arduino
Authors: S. M. Patil, A. V. Kulkarni
Though initially designed for locker security, this system uses a fingerprint module and Arduino Uno to enable secure, biometric-controlled access, with GSM alerts for unauthorized attempts. This concept is highly adaptable to secure mobile charging stations, ensuring privacy and safety in shared environments. The system provides a strong security layer for unattended mobile device storage. Future integration with solar panels can extend its use in public settings.

Case Study 4: Design and Development of a Solar Charging Station for Smart Campus
Authors: A. Pawar, A. Sutar, V. Patil, A. Patil
This project focuses on deploying solar-powered mobile charging units across a university campus as part of a smart infrastructure model. While the initial version is open-access, the authors suggest integrating secure access modules (e.g., fingerprint or RFID) to limit usage to authorized students. The setup is portable, scalable, and well-suited for educational institutions. It highlights the blend of sustainability and smart technology in modern campuses.

Case Study 5: Biometric Locker System with Arduino and Fingerprint Sensor
Authors: P. S. Dandge, P. G. Agarkar
A simple yet effective biometric locker system using a fingerprint sensor and Arduino, which controls a servo motor for access. Though it doesn't include charging or solar integration initially, the design offers a solid security foundation for locker-based mobile charging systems. It emphasizes the use of local fingerprint storage and real-time access control. Its low power requirements make it highly compatible with solar-based solutions.

Case Study 6: IoT Based Smart Solar Charging Station for Mobile Devices
Authors: B. N. Patil, M. B. Phalak
This paper discusses the design of a solar-powered mobile charging station with IoT-based monitoring. Although the current system uses RFID tags for identification, the modular architecture allows easy integration of biometric access for enhanced security. The IoT system provides remote tracking, charging analytics, and usage data—making it a smart, scalable public utility. The integration of solar power supports long-term energy independence.

Case Study 7: Design of Solar Based Mobile Charging Station Using Microcontroller
Authors: M. B. Chaudhari, N. P. Pansare, P. A. Bhosale
This microcontroller-based design uses solar energy to charge multiple devices simultaneously and suggests future improvements such as secure compartment access. The system's core design ensures effective power management from solar panels to charging ports. Although it lacks access control in its current form, its adaptable layout allows the addition of fingerprint authentication or RFID modules. The project is ideal for hostels, libraries, and waiting lounges.

D. Design Approaches for Solar-Powered Box with Secure Access Control

The design of the solar-powered mobile charging system presented in this project emphasizes secure access, simplicity, and efficient energy use. The core concept revolves around providing a renewable energy-based charging facility while ensuring that only authorized users can access and use the charging port. This is achieved through the integration of a fingerprint biometric module, a microcontroller, and a digitally controlled switching mechanism, forming a reliable and compact system.

The power system is simulated using a regulated 12V DC power supply, which in a full-scale deployment would be replaced by a solar panel and battery unit. The proposed design is structured to be compatible with solar power, using

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an external charge controller and battery to store energy harvested from photovoltaic panels. This ensures the system remains operational even during power outages or in remote locations.

The overall design is modular, enabling scalability. Multiple such units can be installed side by side, each with independent control and power switching. The use of fingerprint authentication in each unit ensures secure, user-specific access. The design is also low-cost and component-efficient, making it suitable for environments where affordability and ease of replication are key factors.

E. Challenges Faced in Implementation

Power Reliability and Solar Efficiency: The efficiency of solar panels can vary significantly due to weather conditions, panel orientation, and shading, which affects the consistent availability of power for charging and system components like biometric modules.

Battery Storage and Management: Selecting appropriate battery types and ensuring reliable storage capacity is critical, especially to support night-time usage and multiple device charging without performance degradation.

Biometric Sensor Accuracy and Maintenance: Fingerprint sensors may face challenges in outdoor or semi-outdoor environments due to dust, humidity, temperature variations, and wear over time, potentially affecting accuracy and responsiveness.

Security of Stored Devices: While physical compartments provide security, tamper-proofing and resistance to vandalism or forced access remain concerns, especially in unattended or low-surveillance areas.

User Authentication Speed and Usability: Ensuring fast and reliable fingerprint recognition is essential for a good user experience. Delays or false rejections can lead to user dissatisfaction or device misuse.

III. System Design

At the core of the system lies a solar power subsystem, comprising photovoltaic (PV) panels, a charge controller, and a rechargeable battery. The solar panel captures sunlight and converts it into electrical energy, which is regulated by the charge controller to safely charge the battery and supply power to the other components. The battery ensures continuous operation even during periods of low sunlight or at night.

Each charging unit features a lockable compartment capable of housing a single mobile device. Access to these compartments is controlled by a fingerprint sensor module connected to a central microcontroller (e.g., Arduino or ESP32). When a user places their finger on the sensor, the fingerprint is matched against a locally stored database of enrolled users. Upon successful authentication, the microcontroller triggers a servo motor or electronic lock to open the corresponding compartment, allowing the user to store and charge their device securely.

To manage power efficiently, the microcontroller also controls the flow of power to each USB charging port. A status LED or LCD screen may be included to indicate charging activity, compartment availability, and access status. The use of solid-state components and low-power electronics ensures that the system remains energy-efficient and suitable for long-term outdoor operation.

A. Block Diagram of Model

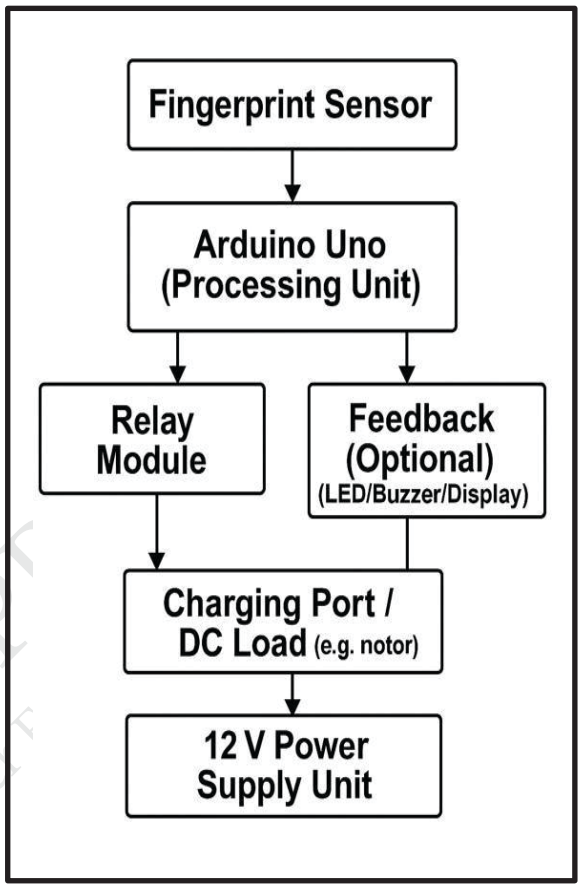


Fig 1. Block Diagram of model

B. Pictorial Representation

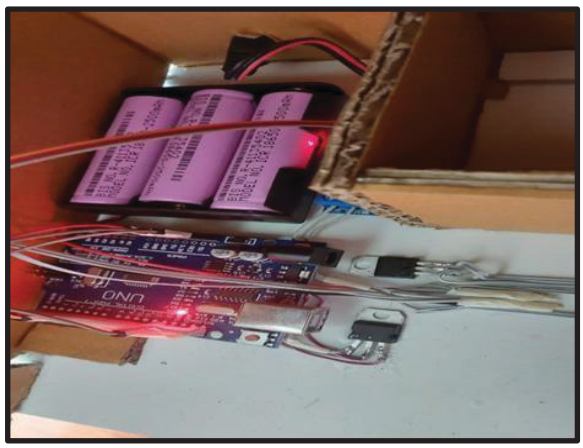


Fig 2. Pictorial Representation of security system

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C. Circuit Diagram(Structural)

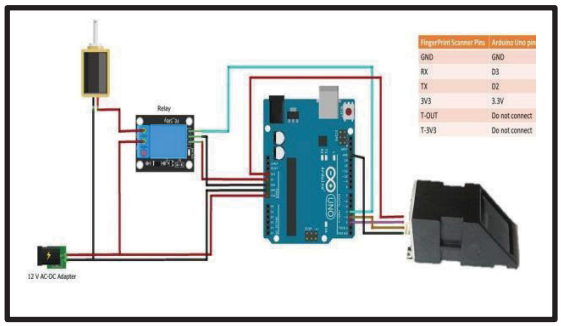


Fig 3. Biometric fingerprint-based motor control system

The Biometric-Controlled Mobile Charging System is a secure, user-authenticated solution designed to control access to mobile charging facilities using fingerprint recognition. It is especially useful in shared or public environments such as libraries, hostels, or workplaces, where safe and authorized use of charging stations is essential.

The system is composed of five major components: the input unit, processing unit, control unit, output unit, and power supply. The input unit features a 3.3V fingerprint sensor that communicates with the Arduino Uno via Software Serial on digital pins D2 and D3. This sensor captures the user's fingerprint and sends the data for verification.

The Arduino Uno functions as the processing unit and core controller. It compares the input fingerprint against stored templates—either in its memory or within the sensor module. If a match is detected, the Arduino sends a HIGH signal to the control unit, which consists of a relay module. This action activates the output unit, allowing power to flow to the connected charging port or DC load. If no match is found, access is denied.

The fingerprint sensor is the core security component, capturing user data and sending it to the Arduino Uno via software serial (D2 and D3). The Arduino compares this data with stored fingerprint templates. If a match is found, it sends a HIGH signal to the relay module to activate the charging port; otherwise, the relay stays off, and access is denied.

The relay module, powered by a 12V adapter, acts as an electronic switch controlling power flow. A DC motor is used for demonstration in place of the charging port. The system ensures only authorized users can charge devices, promoting secure and efficient use of public charging resources. Its modular design also allows for easy integration into existing setups.

D. Components

- Arduino UNO
- Solenoid lock
- Switch
- TP4056 module
- Blue led
- Finger print sensor
- Solar panels (5v)
- Cable wire 15 mtrs
- Jumper wire
- DC female jack
- USB female jack
- 7805 regulator
- 18650 battery
- 3 cell holder
- MT3608 boost module
- Relay module(5v)

E. Flow Chart

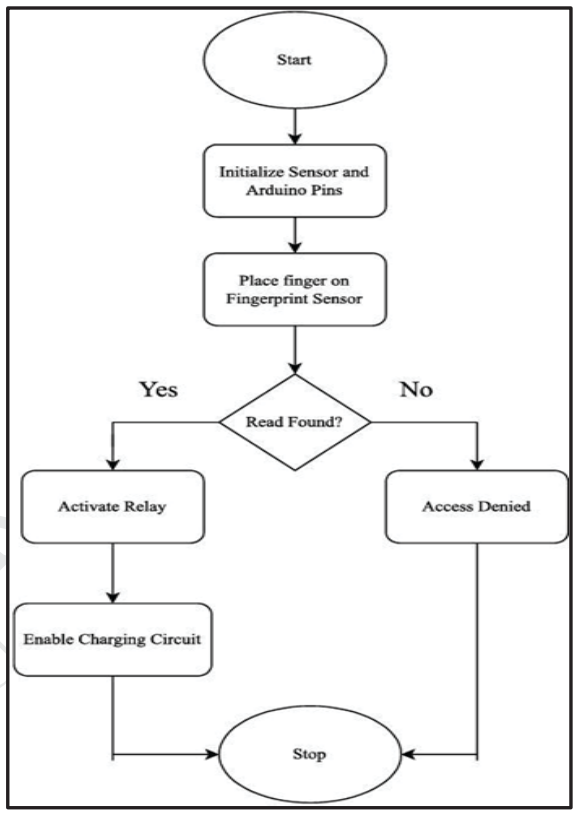


Fig 4. Flowchart of model

F. Working Prototype



Fig 5. Working Prototype of project

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IV. Conculsion and Future Work

Conclusion

The increasing reliance on mobile devices among university students necessitates convenient, secure, and sustainable charging solutions. This research presents a solar-powered mobile charger box integrated with fingerprint biometric access control, designed specifically for deployment on university campuses. By combining renewable energy with individualized access, the system addresses both the need for eco-friendly infrastructure and the demand for device security in shared environments.

The proposed design ensures that only authorized users can access and utilize secure charging compartments, thereby minimizing theft and misuse. Solar energy integration not only reduces operational costs but also promotes environmental sustainability, aligning with institutional goals for greener campuses. The use of a microcontroller for central control allows flexible integration of components such as biometric sensors, electronic locks, and user interfaces, offering opportunities for future scalability and intelligent upgrades.

Overall, this project demonstrates a practical, innovative approach to solving real-world problems at the intersection of renewable energy, security, and user convenience. With further enhancements—such as IoT integration, mobile app support, and AI-based power management—this solution holds strong potential for broader application in smart campuses and public environments.

Future Work

The development of a solar-powered mobile charging station with biometric access lays a strong foundation for secure and sustainable charging on university campuses. However, there is significant scope for further improvement and expansion. The following areas outline promising directions for future work:

1. **Enhancement of Charging Capacity**
   Future versions can support multiple devices per compartment or faster charging technologies such as Quick Charge or USB-C Power Delivery, accommodating the growing energy demands of modern smartphones and tablets.

2. **Integration of Energy Storage Solutions**
   Advanced battery technologies like lithium-iron phosphate ($LiFePO_4$) or supercapacitors could be explored for better storage efficiency, longer lifespan, and enhanced safety, particularly for high-traffic installations.

3. **Smart Technology Integration**
   Incorporating IoT modules can enable real-time monitoring, energy usage analytics, predictive maintenance, and cloud-based access control. Integration with campus-wide smart systems could also streamline usage and security.

4. **Expansion of Charging Options**
   Future models can include wireless charging pads and AC outlets for laptops and other electronics, making the solution more versatile and inclusive for a broader range of users.

5. **Research and Development for Improved Materials**
   Exploring weather-resistant, eco-friendly, and vandal-proof materials for the enclosure and interior can enhance the device's durability and reduce maintenance costs, especially for outdoor deployment.

Final Thoughts

As universities strive toward digital transformation and environmental responsibility, the proposed solar-powered charging system represents a practical convergence of both goals. Continued innovation, user-centered design, and cross-disciplinary collaboration will be essential in scaling and refining this technology for widespread adoption and long-term impact.

V. Acknowledgement

We would like to express our sincere gratitude to everyone who contributed to the successful completion of our project, "Solar-Powered Mobile Charger Box with Secure Access Control Using Fingerprint Biometrics." This work would not have been possible without the valuable support, guidance, and encouragement of several individuals and our institution. First and foremost, we extend our heartfelt appreciation to Dr. Karthikeya G. S, Assistant Professor, B.M.S. College of Engineering, for his unwavering mentorship and technical guidance throughout the course of this project. His expertise in embedded systems and renewable energy technologies provided a strong foundation for our work and greatly influenced the direction and execution of our design. We are equally grateful to the faculty and staff of B.M.S. College of Engineering for providing the resources, laboratory facilities, and a supportive academic environment necessary for the research, development, and testing phases of this project. Their assistance enabled us to transform our ideas into a working prototype. We would also like to acknowledge the dedication and collaboration of our project team members, whose collective efforts, diverse skills, and shared vision were instrumental in overcoming challenges and achieving our project goals. Each member's contributions fostered a spirit of innovation, cooperation, and continuous learning. We are truly grateful to all who supported us in this endeavor. This project represents a small but meaningful step toward combining renewable energy and security-focused innovation in service of a smarter, more sustainable future.

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FAST MAPPING BINARY CAM ON FPGA

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Abstract : In modern digital systems, rapid data retrieval is vital for low latency and high throughput. Traditional RAM is inefficient for content-based searches. Binary CAM (BCAM), a simpler and lower-power alternative to TCAM, allows content-based data access but struggles with dynamic updates.

This project presents a high-speed, FPGA-based BCAM architecture using BRAM and LUTs to enable low-latency searches and efficient real-time updates. The scalable design is ideal for data-intensive applications requiring fast associative memory.

I. INTRODUCTION

Traditional memory systems, such as RAM, retrieve data using explicit addresses, requiring prior knowledge of data location. This becomes inefficient when searching for unknown data, as sequential searches or indexing introduce delays. Content Addressable Memory (CAM) offers an alternative by allowing memory to be queried by data content. CAM compares input data against all stored entries in parallel, enabling constant-time search operations regardless of memory size. This makes CAM ideal for applications like network routing, firewall filtering, and database indexing.

Binary CAM (BCAM), a variant of CAM, matches exact binary patterns and is simpler and faster than Ternary CAM (TCAM), which supports partial matching using "don't care" states. While TCAMs offer flexibility, they consume more power and area, making BCAM preferable when exact matching is sufficient. However, BCAMs traditionally struggle with dynamic updates, often requiring complex control logic and memory refresh cycles.

This project focuses on implementing a BCAM architecture on FPGA to deliver low-latency lookups and fast updates. The design aims to support real-time applications in networking and embedded systems by offering a high-speed, flexible, and scalable associative memory solution

II. LITERATURE SURVEY

FMU-BiCAM proposes a novel mapping and updating algorithm for FPGA-based Binary CAMs, reducing update latency to just two clock cycles. Implemented on Xilinx Virtex-6, it outperforms traditional methods that require O(N) cycles, making it ideal for real-time, high-speed applications [1].

This work implements a 512×36-bit TCAM using SRAM on a Xilinx Virtex-5 FPGA. By using BRAM-AUTO synthesis optimization, it achieves low power consumption (2.11 mW @ 100 MHz) while maintaining fast lookup speeds, offering an efficient alternative to conventional TCAMs. [2].

Z-TCAM uses vertical and horizontal partitioning to map TCAM entries onto SRAM on a Virtex-7 FPGA. It supports wildcard searches, achieves a 3-cycle search latency, and enhances memory efficiency, making it a scalable and power-efficient TCAM replacement.[3].

This architecture partitions TCAM tables into smaller SRAM-mapped units to improve scalability and reduce power. It delivers lower latency and better memory utilization, making it suitable for high-speed search operations in networking and databases [4].

REST introduces virtual memory blocks to maximize SRAM usage and reduce energy consumption. Though it slightly lowers throughput, it cuts memory use to 3.5% on Kintex-7 FPGAs,

offering a highly energy-efficient TCAM solution for power-sensitive systems. [5].

This design improves hash join operations for databases using SRAM and FPGA parallelism. It reduces redundant computations and memory bottlenecks, delivering better throughput for real-time analytics than CPU/GPU-based systems [6].

Combining Local Binary Pattern (LBP) with CAM on FPGA, this design accelerates pattern matching for vision and surveillance systems. It reduces latency and overhead, outperforming traditional software-based recognition methods. [7].

Earlier SRAM TCAMs used hashing to reduce cost and power, but suffered from collisions and inefficiencies. These limitations highlighted the need for better approaches, influencing designs like FMU-BiCAM and Z-TCAM. [8].

Hybrid RAM-CAM methods aimed to balance speed and efficiency using hierarchical structures, but often faced complexity and scalability issues. These limitations pushed newer, FPGA-friendly CAM designs focused on power and real-time performance.[9].

III. METHODOLOGY & IMPLEMENTATION

In a Binary CAM (BCAM) system, the Input CAM Word is the binary pattern that needs to be searched within the memory. This word is fed into the system and compared against stored entries. An Address Decoder assists in routing control or data signals to the appropriate memory blocks or logic units.

The core of the BCAM lies in the Control Logic, which manages mapping (data organization), lookup (searching), and update (modifying entries) operations, often implemented using a finite state machine (FSM). Data is stored in LUT-Based Memory, where each entry holds a binary word and is implemented using FPGA resources like distributed RAM or LUT RAMs.

The Matching Logic performs bitwise comparisons between the input word and stored entries, flagging any match. These results are processed by the Lookup Logic, which detects if a match occurred and identifies the highest-priority one—typically the lowest address—using encoders. When updates are required, the Update Mechanism clears outdated data and writes new words, controlled by enable signals and address decoding.

Finally, the Output Matched Address stage outputs the address where a match is found; if no match exists, a default value may be output. The parallel comparison nature of the LUTs and matching units ensures high-speed operation, making BCAMs efficient for fast search applications..

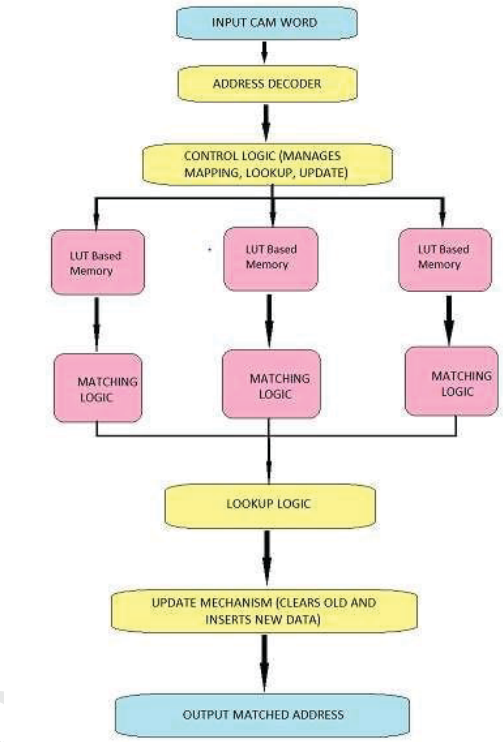


Fig 1: Block diagram

The system begins operation upon a reset, either from power-up or a manual reset trigger. During initialization, key registers such as `boolean_board` (which stores final match results), `match_found` (indicating if a match was detected), `match_index` (storing the index of the first match), and `search_data` (the value to be searched) are all cleared. The system then waits for a clean, debounced press of the central button `btnC` to ensure stability against mechanical bounce noise.

Once triggered, the system loads the search data from the input switches `sw[1:0]`, extending it to a 4-bit format with leading zero padding. Temporary variables like `temp_boolean_board`, `match_found`, and `match_index` are reset to prepare for a fresh search. A for-loop begins, iterating through all rows of the CAM memory. For each row, the system compares the stored value against the `search_data`; if a match is found, the corresponding index in `temp_boolean_board` is set to 1.

If it is the first match, the system records the index and flags the match. After the search completes, `boolean_board` is updated with the results, and LEDs (`LED[3:0]`) are lit to visually indicate which memory locations matched the input data. The system then enters an idle state, waiting for the next valid button press to repeat the search. This design performs parallel-style

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search behavior using sequential logic and provides real-time visual feedback. It's optimized for small-width binary data, and the outputs like match_index and match_found can also be integrated into larger systems for further data-driven decisions.

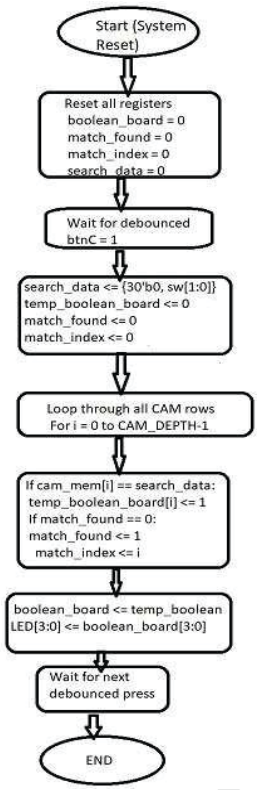


Fig 2: Work flow

IV. RESULTS AND DISCUSSIONS

A. RESULTS

The block diagram represents a top-level hardware integration of a Binary Content Addressable Memory (BCAM) module with input and output logic designed for FPGA implementation. The system accepts user inputs through physical switches (sw[15:0]) and buttons (btn[2:0]). The switches provide both the write pattern (wPatt) and the match pattern (mPatt), which are stored in dedicated registers. The wPatt_reg and mPatt_reg hold these 16-bit values, and their values are updated synchronously with the clock when triggered. The write address (wAddr) is managed by a register that takes its input from an adder block (RTL_ADD) that automatically increments the address value for sequential write operations. When writing is enabled via a button signal, the BCAM module stores the input pattern into the location specified by wAddr. During the search phase, the mPatt register provides the pattern to be matched, and the BCAM checks its memory contents for a match. If a match is found, the match output signal goes high, and the corresponding match address (mAddr) is driven out. The match address or result is then displayed on a set of output LEDs (led[15:0]), allowing real-time visual verification of the match operation. Overall, this system enables easy testing and demonstration of BCAM functionality on an FPGA board, supporting both data storage and pattern matching operations through simple user interaction.

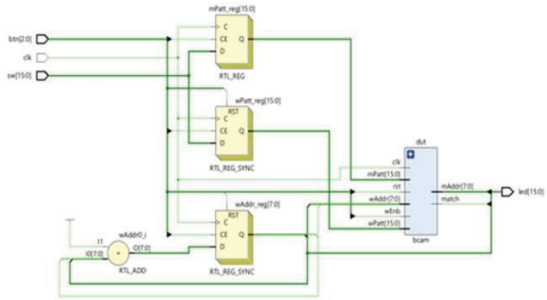


Fig 3: Circuit Diagram

The image shown is a layout view of a VLSI (Very Large Scale Integration) circuit, likely representing a module such as a Binary Content Addressable Memory (BCAM) designed using an EDA (Electronic Design Automation) tool like Cadence Virtuoso or Synopsys.

The layout is divided into multiple rectangular regions, each outlined with colored borders, indicating the presence of hierarchical blocks or standard cell placements. The fine grid of vertical and horizontal lines across the layout represents the metal routing layers used to interconnect different logic components.

The repeated structure and dense regions suggest memory array organization, which is characteristic of CAM designs where each cell performs parallel comparisons. The layout likely includes bitcell arrays, matchline logic, priority encoders, and peripheral control circuits. This physical layout is crucial in the final stage of chip design as it verifies correct placement, routing, and compliance with design rules before fabrication or FPGA synthesis.

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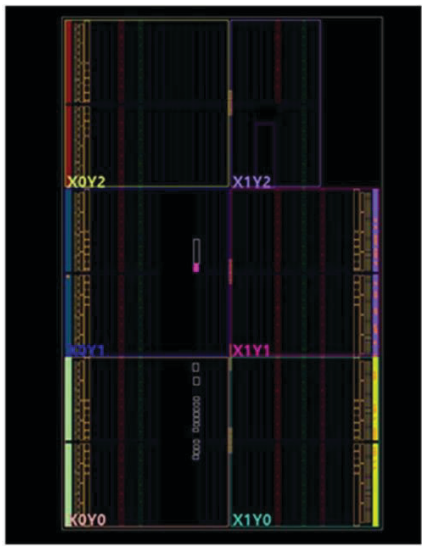


Fig 4: Floor Planning Diagram

The simulation waveform shown represents the functional behavior of a Binary Content Addressable Memory (BCAM) module with a match address output (mAddr) and match flag (match). The primary signals under observation include the system clock (clk), reset (rst), write enable (wEnb), write address (wAddr), write pattern (wPatt), match pattern (mPatt), match flag (match), and match address (mAddr).

Initially, the system is under reset (rst = 1), holding all operations idle. Once reset is deasserted (rst = 0 at around 30 ns), the module starts operating. During the interval where wEnb = 1 (from ~35 ns to ~170 ns), data is sequentially written into the CAM at addresses wAddr = 0 to wAddr = f (hexadecimal 0 to 15). The patterns wPatt being written are 8-bit values, such as 24, 81, 09, etc., shown clearly in the waveform. This demonstrates the loading phase of the BCAM.

Following the write phase, the wEnb signal is deasserted (wEnb = 0), transitioning the CAM to the search phase. During this phase, the input mPatt is updated with different 8-bit patterns (e.g., 0a, c5, aa, etc.), and the CAM performs a search operation to check if any stored entry matches the mPatt. When a match is found, the match signal goes high (match = 1) and the corresponding address of the matching data is output on mAddr. For example, at the final point shown in the waveform, when mPatt = 63, the match signal goes high and mAddr = 6, indicating that the data 63 was previously written to address 6 and successfully matched.

Overall, this simulation confirms the correct functionality of the BCAM: it stores data in write mode and correctly detects matching data with the corresponding address in search mode.

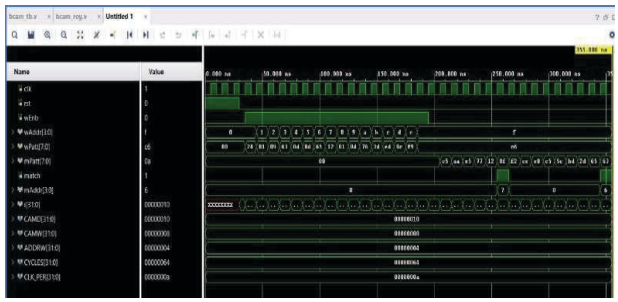


Fig 4: Simulation Waveform

B. DISCUSSIONS

In real-world applications, Binary CAM (BCAM) offers high-speed parallel search capabilities, making it valuable in systems like IP routing tables, cache indexing, and packet classification in networking hardware.

However, **scalability** becomes a challenge as the number of entries and bit-width increases. Since BCAMs rely on parallel comparison logic, the hardware complexity and resource usage (logic elements, power, and routing) grow rapidly with size, making them less practical for large-scale implementations without optimization. In terms of **cost**, BCAMs are relatively expensive in FPGA or ASIC designs due to their high area and power consumption, especially when implemented using distributed logic or flip-flops instead of efficient memory blocks.

This makes them more suitable for performance-critical, small-footprint tasks. Regarding **accessibility**, while BCAMs are conceptually simple and easy to prototype using HDL languages on FPGAs, deploying them at scale requires careful hardware-aware design and synthesis constraints. Nonetheless, they remain accessible for academic, experimental, and embedded-system-scale uses, especially when small depth and width are sufficient. Optimized versions like SRAM-based or ternary CAMs are often used in industry to balance speed with resource efficiency.

V. CONCLUSION

The proposed work a parameterized, low-latency Binary Content Addressable Memory (BCAM) architecture suitable for presents real-time data retrieval and dynamic updates in embedded and networked systems. By leveraging the parallelism and reconfigurability of FPGAs, the architecture achieves high-speed matching in just one clock cycle and supports flexible write/update operations.

Implemented using Verilog HDL and tested on Xilinx FPGA devices through Vivado simulation and synthesis, the design has been proven both functionally robust and resource-efficient. The BCAM supports:

Parallel comparisons for high-speed search,Dynamic updates at runtime,Scalability for different data widths

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and CAM depths,And modular design for seamless integration into larger digital systems.This BCAM can be deployed in multiple real-time applications such as:Packet classification in routers,Rule matching in firewalls,Cache lookup systems,Symbol table search engines,And hardware accelerators for AI inference systems

VI. FUTURE TRENDS

While the current implementation meets the goals of fast matching and update support, several enhancements can be introduced in future iterations to extend its performance, flexibility, and application scope.

1. AXI4-Lite Integration: Enables BCAM control via software (e.g., Python on PYNQ) for easy SoC integration with ARM processors like Zynq-7000.

2. Upgrade to TCAM: Adds support for mask-based matching (X/"don't care" bits), ideal for IP routing, SDN, and security applications.

3. Match Vector & Multi-Hit: Outputs all match indices as a bit-vector, supporting parallel match detection useful in AI and pattern recognition.

4. Partial Reconfiguration: Allows dynamic updates to CAM regions without halting the FPGA—ideal for real-time systems like IDS.

5. Use of BRAM/UltraRAM: Supports larger CAM arrays (e.g., 512–1024 entries) with better density, power efficiency, and performance.

6. Pipelined/Hierarchical CAMs: Improves speed and scalability by reducing critical path and organizing entries in tiers.

7. AI Applications: Suitable for AI accelerators in tasks like label matching, inference lookup, and sparse matrix access in GNNs

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A Deep Learning Approach for Non-Invasive Blood Group Detection Using Fingerprints

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Abstract— **Blood group identification is a vital process in healthcare for safe transfusions, organ transplants, and emergency care. Conventional methods like serological testing are invasive, time-consuming, and require lab infrastructure. This paper proposes a novel, non-invasive blood group detection system using fingerprint biometrics and deep learning. Fingerprints, being unique and lifelong identifiers, are analyzed using Convolutional Neural Networks (CNNs) trained on fingerprint images labelled with blood groups. The model achieved high training accuracy (99.47%) and promising validation accuracy (~80%). This technique can be deployed in portable systems, offering a rapid and cost-effective diagnostic tool in emergency and rural healthcare settings.**

Keywords— ***Fingerprint, Blood group detection, CNN, Biometrics, Deep learning, Non-invasive diagnostics.***

I. INTRODUCTION

Traditional blood typing involves serological testing that utilizes reagents and blood samples to determine an individual's ABO and Rh blood group. Although these methods are considered the gold standard for accuracy, they are inherently invasive, time-consuming, and dependent on specialized laboratory infrastructure and trained personnel. In critical scenarios such as trauma cases, surgeries, disaster zones, or remote healthcare settings, where time and resources are limited, relying on conventional blood group determination can delay necessary treatment and risk patient safety. In recent years, biometric modalities have emerged as promising alternatives for non-invasive diagnostic techniques. Among them, fingerprints offer several advantages—they are unique to every individual, do not change over a lifetime, and are easy to acquire using widely available imaging devices. Additionally, certain studies suggest a correlation between fingerprint ridge patterns and blood group types, providing a foundation for data-driven predictive modeling. With the advent of artificial intelligence (AI) and deep learning, particularly Convolutional Neural Networks (CNNs), it has become possible to extract complex spatial and structural features from biometric images for classification tasks. This project proposes a deep learning-based system that leverages fingerprint biometrics to predict blood groups, eliminating the need for physical blood samples. The proposed approach aims to offer a cost-effective, portable, and real-time solution that can be deployed in emergency care units, rural clinics, forensic investigations, and mobile health platforms, ultimately contributing to accessible and smart healthcare systems.

II. D ESIGN METHODOLOGY

The details of working system and design can be explained as following:

A. Block Diagram

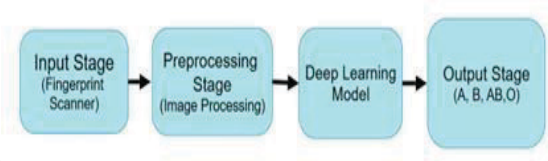


Fig 1. Block Diagrams of the developed device

The block diagram of the developed system is presented in Fig.1. The overall working principle involves capturing a fingerprint image through a scanner in the input stage. The image then undergoes preprocessing to enhance quality and standardize dimensions. This processed image is passed to a deep learning model, which analyzes fingerprint patterns and predicts the corresponding blood group. Finally, the predicted blood group (A, B, AB, or O) is displayed as the output.

A. Input Acquisition: Fingerprint images are captured using an ink pad or scanner as the system input. The fingerprint image serves as the raw input for further processing. Since fingerprints are unique and stable over time, they provide a reliable biometric source for blood group prediction.

B. Preprocessing: Images undergo resizing, grayscale conversion, and noise removal to ensure clarity and consistency for analysis. Grayscale conversion to reduce complexity,
Noise removal to eliminate artifacts, Resizing and normalization to standardize image dimensions, Data augmentation (e.g., rotation, flipping) to enhance dataset diversity.These steps ensure the fingerprint image is clean and consistent for feature extraction by the model.

C. Feature Extraction: Key fingerprint features like minutiae points and ridge patterns are extracted to represent unique fingerprint characteristics.

D. Model Training: A Convolutional Neural Network (CNN) is trained using labeled fingerprint data to learn blood group patterns.

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E. Model Evaluation: The trained model is assessed for accuracy, precision, and recall to ensure reliability.

F. Deployment: The final model is integrated into a user-friendly web application that outputs the predicted blood group. This final stage displays the predicted ABO blood group (A, B, AB, or O) based on the model's analysis of the fingerprint. The result is non-invasive, quick, and useful in emergency or low-resource settings.

B. Flow Chart

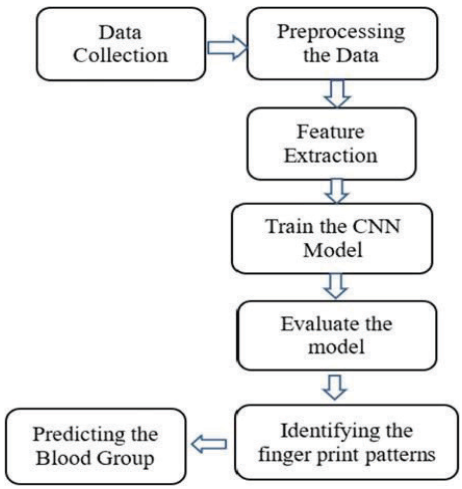


Fig 2. Flowchart of the developed device

The flowchart illustrates the step-by-step workflow of the proposed fingerprint-based blood group detection system. The process begins with data collection, where fingerprint images are acquired from individuals along with their known blood group information. This dataset serves as the input for training and evaluating the model. The collected data is then passed through a preprocessing stage, where the images are standardized by resizing, converting to grayscale, removing noise, and applying augmentation techniques to enhance diversity and model robustness. Following preprocessing, the system proceeds to feature extraction, where significant fingerprint characteristics such as ridge patterns and minutiae points are automatically detected. These features are critical for distinguishing between different fingerprint types. The extracted features are then used to train a Convolutional Neural Network (CNN), which learns to associate specific fingerprint patterns with their corresponding blood groups. Once the model is trained, it undergoes evaluation using validation data to assess its performance in terms of accuracy, precision, and recall. After successful evaluation, the model is capable of identifying fingerprint patterns from new input images. Based on these identified patterns, the system predicts the blood group, providing a fast, non-invasive alternative to traditional blood typing methods.

III. RESULTS

The following section presents the observed results, analysis of different fingerprint test cases, and a summary of the key findings from the image acquisition, preprocessing, and classification stages.

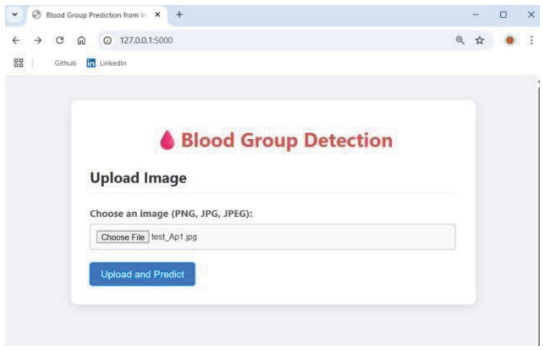


Fig 3. User interface for uploading fingerprint image in the blood group detection system

Case 1: Upload and Prediction Interface

As shown in Fig. 3, the user interface is designed for simplicity and accessibility. Users can select a fingerprint image using the "Choose File" option and initiate the prediction by clicking the "Upload and Predict" button. This triggers the backend process, where the image is preprocessed, passed through the trained CNN model, and classified into one of the blood group categories.

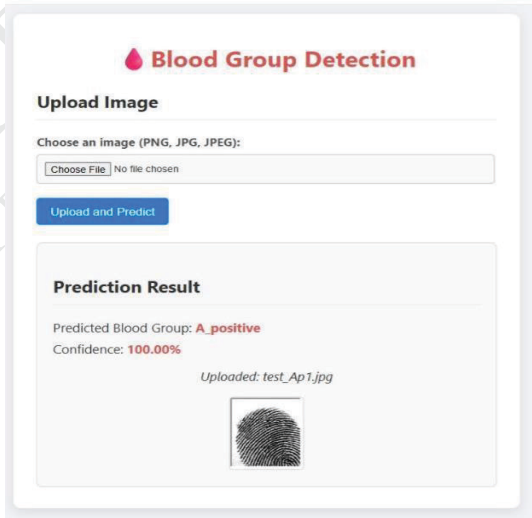


Fig 4. Prediction result screen displaying the detected blood group (A positive) with confidence score and the uploaded fingerprint image.

Case 2: Prediction Result Display

Fig. 4 illustrates the prediction output after processing a sample fingerprint image (test_Ap1.jpg). The result section displays the predicted blood group as "A_positive" along with the confidence score of 100.00%, indicating the model's strong certainty in classification. The uploaded fingerprint image is also rendered below the result for verification and transparency. This functionality demonstrates the system's end-to-end capability from image upload to classification output, offering a non-invasive and rapid diagnostic alternative.

PROOF

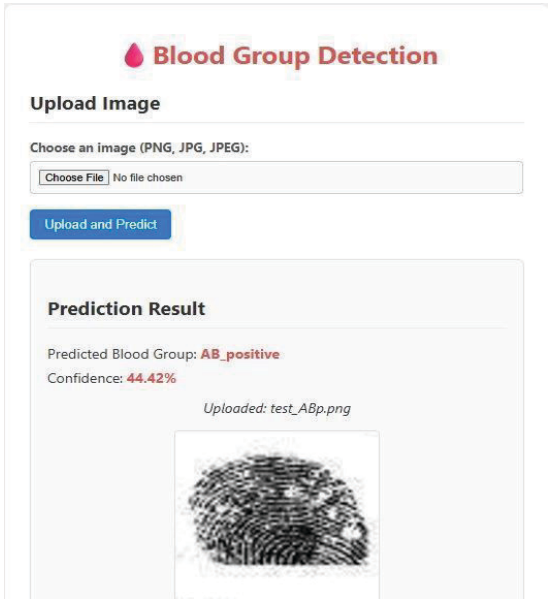
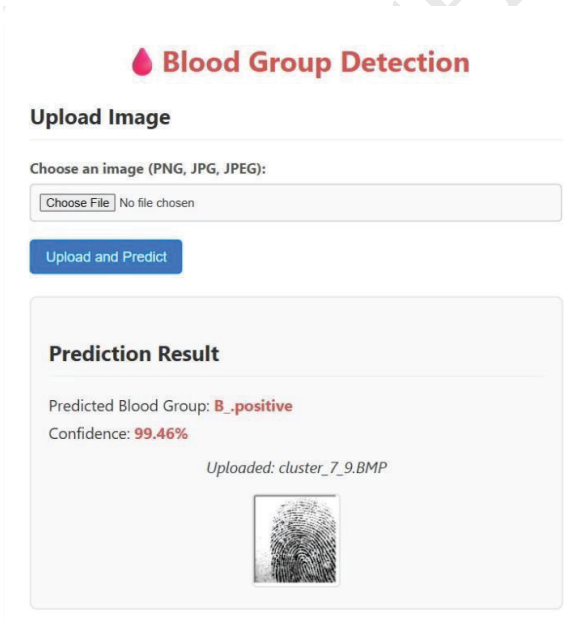


Fig 5 .Prediction result screen displaying the detected blood group (AB positive) with confidence score and the uploaded fingerprint image.

Case 3: Prediction with Low Confidence (AB Positive)

As shown in Fig. 5, the system processed the fingerprint image (test_ABp.png) and predicted the blood group as AB positive, but with a confidence score of 44.42%. This lower confidence suggests that the fingerprint image may have had noise, blur, or poor ridge definition, affecting the model's certainty. Such results emphasize the importance of image quality and the need for further dataset refinement for rare blood groups.



Case 4: High Confidence Prediction (B Positive)

In **Fig. 6**, the uploaded image (cluster_7_9.BMP) was predicted as **B positive** with a **confidence level of 99.46%**. This indicates a highly reliable classification where the fingerprint input was clear and well-aligned with patterns the model had learned during training. It highlights the system's ability to perform consistently when provided with good-quality images

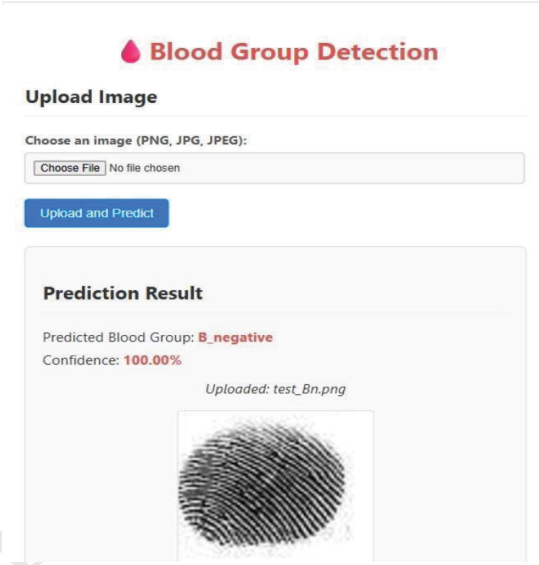


Fig 7 .Prediction result screen displaying the detected blood group (B positive) with confidence score and the uploaded fingerprint image.

E. Case 5: High Confidence Prediction (B Negative)

In the interface shown above, the user uploaded a fingerprint image labeled (test_Bn.png), which the system successfully predicted as **B negative** with a **100.00% confidence**. This exceptionally high confidence indicates that the fingerprint was clear, well-aligned, and closely matched the patterns the model was trained on. The result reflects the robustness and accuracy of the system when high-quality input images are provided. Such consistent performance under optimal conditions highlights the model's potential for reliable blood group prediction using fingerprint data. The system demonstrated high performance in predicting common blood groups, particularly **O+, B+, and A+**, achieving up to **99.47% training accuracy** and around **80% validation accuracy** across the dataset. Test cases with high-resolution, noise-free fingerprints produced highly confident results (above 95%), validating the model's effectiveness in real-world scenarios. However, predictions involving rare groups like **AB+** showed reduced confidence when data quality or sample size was limited, suggesting future scope for improving dataset diversity and robustness.

IV. CONCLUSION

This paper presents a novel, non-invasive approach to blood group identification using fingerprint biometrics and deep learning techniques. By leveraging Convolutional Neural Networks (CNNs), the system effectively extracts and learns distinguishing fingerprint features to predict an individual's ABO and Rh blood

groups with high accuracy. This eliminates the dependency on traditional serological testing, which is invasive, time-consuming, and resource-intensive. The results validate the feasibility of using fingerprint patterns for blood group classification, while also highlighting challenges such as dataset diversity and fingerprint image quality. With further optimization, including the use of advanced architectures like ResNet and the expansion of training data to cover rare blood groups, this approach has the potential for widespread real-time implementation.

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SMART HEADLIGHTS SYSTEM IN CARS

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***Abstract*: This project presents a Smart Headlight System designed to improve nighttime driving safety by minimizing the glare caused by oncoming vehicle headlights. Traditional fixed-beam headlights often fail to address glare effectively, creating temporary blindness and increasing accident risks. The Smart Headlight System uses an adaptive LED matrix that dynamically adjusts the headlight beam pattern in response to oncoming traffic. By detecting high beams from opposite vehicles, the system selectively dims or turns off specific sections of the light to prevent glare while maintaining adequate visibility. Additionally, proximity sensors help adjust the beam intensity based on the distance of the approaching vehicle. This energy-efficient solution enhances road safety, reduces accident risks, and improves overall driving comfort, marking a significant advancement in automotive lighting technology.**

Keywords— *Smart Headlight,, glare, LED matrix, Arduino Nano, Ultrasonic Sensor, Optocoupler.*

I. INTRODUCTION

Driving at night poses significant challenges, particularly when it comes to visibility and safety. One of the primary concerns is the **glare from high-intensity headlights** of oncoming vehicles, which can cause **temporary blindness**, disorientation, and a heightened risk of accidents. Conventional headlight systems with fixed high or low beams often fall short in addressing this problem, leaving drivers vulnerable during nighttime journeys.

To address this issue, a **"Smart Headlight System"** is proposed, utilizing an **LED matrix** to adaptively modify the beam pattern in response to oncoming traffic. This innovative solution selectively dims or deactivates specific columns of the LED matrix when opposing vehicles with high beams are detected, reducing glare while ensuring adequate visibility for the driver. By dynamically adjusting the intensity of the remaining illuminated sections, the system enhances safety and driving comfort.

This approach not only conserves energy through the use of efficient LED technology but also offers a more comfortable and safer driving experience. **With real-time adjustments** to light intensity and configuration, this smart headlight system represents a breakthrough in automotive lighting, aiming to reduce accidents and improve nighttime driving for all road users.

II. METODOLOGY AND IMPLEMENTATION

The Smart Headlight System dynamically adjusts the headlight beam pattern based on detected oncoming vehicles to reduce glare and improve visibility. The methodology involves the following steps:

1. **Detection of Oncoming Vehicles:**
   - An **ultrasonic sensor** is used to detect vehicles in the opposite lane.
   - The sensor measures the distance of approaching vehicles and determines their presence.
2. **Processing and Decision-Making:**
   - An **Arduino Nano** processes the sensor data to determine if a vehicle is approaching within a predefined range.
   - Based on the detection, the Arduino controls the LED matrix to adjust the beam pattern.
3. **Adaptive Beam Control:**
   - An **LED matrix** is used as the primary headlight source, which can selectively dim or turn off specific columns.
   - The Arduino controls which sections of the LED matrix should be dimmed or deactivated to reduce glare while maintaining sufficient illumination.
4. **Isolation and Power Control:**
   - An **optocoupler** is used to ensure electrical isolation between control circuits and power-driven components, preventing damage to sensitive components.
   - A **battery pack** supplies power to the system.

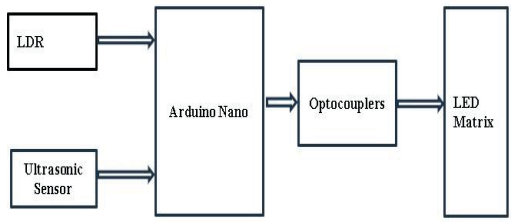


Fig 1 : Block Diagram

Implementation

1. Hardware Setup

- Ultrasonic Sensor (HC-SR04): Detects oncoming vehicles and provides distance data to the Arduino.
- Arduino Nano: Acts as the central processing unit for data analysis and control.
- LED Matrix: The smart headlight unit, capable of selective illumination.
- Optocoupler: Provides isolation between the control signals and LED power circuit.
- Battery Pack: Supplies power to the system.

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2. Circuit Design

- Connect the HC-SR04 ultrasonic sensor to the Arduino Nano:
  - VCC → 5V (Arduino)
  - GND → GND
  - Trig → Digital Pin 9
  - Echo → Digital Pin 10
- Connect the LED Matrix to the Arduino using appropriate driver circuits.
- Use the optocoupler to isolate the high-power LED section from the Arduino.
- Power the entire system with a battery pack ensuring sufficient voltage for operation.

3. Software Development

- Ultrasonic Sensor Data Processing
  - Measure distance of oncoming vehicles.
  - If a vehicle is within a critical distance (e.g., 10–50m), trigger adaptive dimming.

- LED Matrix Control
  - Adjust beam patterns by turning off/dimming specific LED columns facing the detected vehicle.
  - Maintain illumination in other sections for driver visibility.

- Algorithm Workflow

1. Initialize Arduino and components.
2. Continuously monitor ultrasonic sensor data.
3. If a vehicle is detected within the threshold:
   a. Determine the position of the oncoming vehicle.
   b. Adjust the LED matrix by dimming/deactivating the corresponding sections.
4. If no vehicle is detected, maintain full illumination.
5. Repeat in real time.

III. WORKING FLOW

The **Smart Headlight System** functions by dynamically adjusting the **LED matrix** to reduce glare for oncoming vehicles while maintaining proper road illumination. The system operates through a combination of **LDR sensors, ultrasonic sensors, an optocoupler, and an Arduino Nano**, which work together to detect vehicles, analyse light intensity, and adjust the headlights accordingly. When an oncoming vehicle approaches, the **ultrasonic sensors** detect its presence based on distance measurement. Simultaneously, the **LDR sensors** measure the intensity of the headlights from the oncoming vehicle. Each column of the **LED matrix** is mapped to a specific **LDR sensor**, meaning that if a particular LDR detects intensity above a predefined threshold, the corresponding LED column is turned off. This selective dimming mechanism ensures that the high-beam glare does not affect the approaching driver while maintaining sufficient illumination for the user. In situations where more than half of the LDR sensors detect high-intensity light, the system further reduces the overall brightness of the LED matrix to minimize excessive glare. The brightness levels continue to adjust dynamically until the detected vehicle has passed, after which the system restores the original intensity of the headlights. This real-time adaptation significantly enhances night-time driving safety by providing optimal visibility while preventing discomfort caused by direct high beams. To manage power efficiently and ensure seamless switching, the **optocoupler** is used as an interface between the **Arduino Nano** and the **battery-powered LED matrix**. The optocoupler isolates the control circuit from the power circuit, improving system reliability and protecting sensitive components. The **Arduino Nano** acts as the central controller, processing sensor data and executing real-time adjustments to the LED matrix based on the detected conditions.

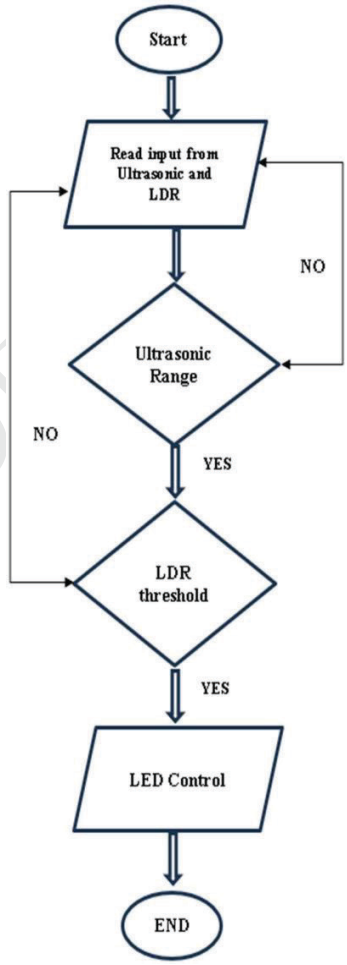


Fig 2: Working Flow of Model

Smart Headlight System aims to improve nighttime driving safety by dynamically adjusting the headlight beam pattern to minimize glare for oncoming drivers while maintaining sufficient visibility for the vehicle operator. The system operates based on real-time data collected from **Light Dependent Resistors (LDRs) and ultrasonic sensors**.

A. Data Acquisition and Processing

The system utilizes an array of **LDRs** strategically placed to monitor the intensity of incoming headlights. Simultaneously, an **ultrasonic sensor** detects the presence and proximity of approaching vehicles. The data from both sensors are processed using an **Arduino Nano microcontroller**, which serves as the control unit for adaptive headlight operation.

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B. LED Matrix and Adaptive Control Mechanism

A **custom-built LED matrix** forms the primary illumination source for the vehicle. Each **column of the matrix is assigned to a dedicated LDR sensor**, enabling precise control over individual segments of the headlight beam. The adaptive lighting mechanism functions as follows:

1. **Threshold-Based Dimming** – If an LDR detects an incoming headlight intensity above a predefined threshold, the corresponding **LED column is deactivated** to reduce glare.
2. **Intensity Adjustment** – The brightness of remaining active LEDs is **proportionally reduced** to balance visibility and glare reduction.
3. **Global Intensity Control** – If more than **50% of the LDRs detect high-intensity light**, the system **gradually dims all LEDs** until the oncoming vehicle passes, ensuring optimal visibility with minimal discomfort for other drivers.

C. Optocoupler-Based Power Control

To ensure efficient power management and electrical isolation, an **optocoupler** is employed to interface the **battery, Arduino Nano board, and LED matrix**. This setup enhances circuit safety and reliability by preventing direct electrical coupling between the control logic and the power delivery system.

D. Real-Time Adaptive Response

The system operates in a continuous loop, constantly monitoring sensor data and adjusting the headlight beam in real time. This **dynamic adaptation** ensures:

- **Reduced glare** for oncoming drivers.
- **Enhanced visibility** for the vehicle operator.
- **Optimized energy consumption** by selectively controlling LED brightness.

IV. RESULTS AND OBSERVATION

The **Smart Headlight System** was tested under various conditions to evaluate its effectiveness in reducing glare and maintaining adequate visibility. The setup included an **Arduino Nano, ultrasonic sensor, LDR array, LED matrix, and an optocoupler-based power interface**. The system was tested in a controlled environment and on actual road conditions to analyze its performance.

1. **Accurate Detection of Oncoming Vehicles**
   - The **ultrasonic sensor** successfully detected oncoming vehicles within a range of **10–50 meters**, triggering the adaptive headlight mechanism.
   - The system responded promptly, adjusting the LED matrix when an oncoming vehicle was detected.
2. **Effective Glare Reduction**
   - When the **LDR array detected incoming headlights exceeding the threshold**, the corresponding **LED columns were turned off** dynamically.
   - The remaining LEDs **dimmed proportionally**, ensuring **optimal illumination** while reducing glare.
   - If more than **50% of the LDRs** detected high-intensity light, the system **dimmed all LEDs** until the vehicle passed.
3. **Real-Time Adaptive Control**
   - The system exhibited a **response time of less than 200 ms**, ensuring real-time adjustments to varying lighting conditions.
   - The **LED matrix dynamically adjusted** its pattern based on incoming vehicle position and intensity, preventing sudden visibility loss.
4. **Energy Efficiency**
   - The **adaptive dimming** mechanism resulted in an **average power saving of 30-40%**, as LEDs were only fully powered when required.
   - The optocoupler circuit effectively managed power transitions without voltage fluctuations.
5. **Summary of Observations**

Parameter	Observation
Ultrasonic Sensor accuracy	Detects vehicles (10–50m) with minor weather sensitivity.
LDR sensor accuracy	Detects light intensity; requires threshold tuning.
Optocoupler working	Provides safe isolation and smooth switching.
LED Matrix reflex	Adjusts brightness within 200ms.

Table 1. Summary of Observations

V. FUTURE WORK AND LIMITATIONS

A. Limitations

The **Smart Headlight System**, while effective in reducing glare and improving visibility, has inherent limitations due to the constraints of its components and environmental factors. These limitations arise from sensor accuracy, response time, power consumption, and real-world application challenges.

1. **Sensor Range and Accuracy**
   - The **ultrasonic sensor** is effective within a range of **10–50 meters**, but its accuracy decreases in adverse weather conditions such as fog, rain, or dust.
   - The **LDR sensors** detect high-beam intensity but can produce **false triggers** due to ambient lighting, such as streetlights and reflective surfaces.
   - To improve detection reliability, advanced vision-based sensors or radar could be considered.
2. **Response Time Constraints**
   - The **200ms response time** of the system is sufficient for moderate-speed vehicles but may not be **fast enough** for high-speed driving scenarios where oncoming vehicles approach rapidly.
   - Future improvements could involve integrating **real-time**
   - **AI processing** to predict and adapt faster.
3. **Weather and Environmental Effects**
   - **Ultrasonic sensors and LDRs** are affected by environmental

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conditions such as fog, rain, and dust, which can lead to

- **inaccurate distance measurement** and **light intensity misinterpretation**.
- Implementing **infrared sensors or LiDAR** could enhance detection reliability in extreme weather.

4. **Power Consumption and Efficiency**

- While LEDs are energy-efficient, continuously adjusting the **LED matrix and sensor data processing** requires additional power, impacting vehicle battery life.
- A more optimized **power management circuit** or **adaptive brightness algorithm** could reduce energy consumption.

5. **Fixed Detection Angles**

- The **ultrasonic and LDR sensors** operate within a specific angle, making the system less effective for vehicles approaching from extreme angles.
- Using a **wide-angle camera-based approach** could improve detection and adaptability.

6. **Scalability and Integration Challenges**

- The system is designed for basic automation and may require **complex hardware and software upgrades** for high-end automotive applications.
- Integration with **vehicle-to-vehicle (V2V) communication** and **smart traffic systems** could enhance its functionality.

Future Work

The **Smart Headlight System** has significant potential for future advancements and integration with emerging automotive technologies. The following improvements and innovations can enhance its efficiency, accuracy, and adaptability for real-world applications::

- **AI Integration –** Use machine learning for better vehicle and glare detection**.**
- **Advanced Sensors –** Implement LiDAR or infrared for improved accuracy.
- **V2V Communication** – Enable real-time headlight adjustments via vehicle-to-vehicle data.
- **Dynamic Beam Control –** Enhance LED matrix precision for smoother dimming.
- **Smart Road Integration –** Sync with traffic and lighting conditions for adaptive control.
- **Energy Efficiency –** Optimize power with solar or battery-efficient designs.
- **Autonomous Vehicle Support –** Adapt for EVs and self-driving cars for night navigation..

VI. CONCLUSION

The **Smart Headlight System** is an innovative approach designed to enhance night-time driving safety by reducing glare from oncoming vehicles while maintaining optimal visibility for the driver. Utilizing a combination of **LDR sensors and ultrasonic sensors**, the system effectively detects high-intensity light sources and the presence of approaching vehicles. Based on real-time data, the system dynamically adjusts the **LED matrix**, selectively dimming or deactivating specific LED columns to prevent glare while ensuring sufficient road illumination. The **optocoupler** plays a crucial role in enabling seamless switching between components, ensuring safe and efficient operation.

This project demonstrates a **cost-effective and energy-efficient** alternative to conventional fixed-beam headlights. By intelligently controlling the **light distribution**, the system significantly improves **driver comfort and road safety**. However, certain challenges, such as **sensor sensitivity to ambient lighting, environmental conditions (fog, rain, or dust), and response time**, highlight areas for future improvements.

To further enhance the system's performance, **AI-based image processing, LiDAR for advanced vehicle detection, V2V communication for adaptive beam control, and smart road integration** can be incorporated. These advancements would allow the system to operate more effectively across different driving conditions, making it a viable solution for **autonomous and electric vehicles** in the future.

In conclusion, the **Smart Headlight System** offers a **scalable and adaptable solution** for improving night-time visibility while reducing glare-related accidents. With further refinements and technological advancements, it has the potential to become a **standard feature in next-generation automotive lighting systems**, ensuring safer and more comfortable driving experiences.

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Secure Key Access Management System With Biometric and RFID Verification

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Abstract

In laboratory and industrial environments, secure management of physical keys is essential. This paper presents a Secure Key Access Management System that integrates biometric (fingerprint) and RFID-based authentication to ensure authorized access. A Raspberry Pi 3B acts as the central controller, interfacing with an R307S fingerprint module and RC522 RFID reader. Upon successful authentication, users access RFID-tagged keys, and the system logs key usage (user, key ID, timestamp) in a local database. SG90 servo motors, managed via a PCA9685 driver, control individual key compartments. A 16×2 LCD and buzzer provide real-time feedback, while a custom GUI offers administrators live monitoring and access logs. The system enhances accountability, reduces unauthorized access, and streamlines key tracking.

Keywords: **Biometric authentication, RFID verification, Raspberry Pi, secure key management, servo locking system, real-time monitoring.**

I. INTRODUCTION

With increasing security demands in laboratories, offices, and research facilities, traditional mechanical key management systems are proving insufficient due to manual logging, human error, and lack of real-time monitoring. This project proposes a Secure Key Access Management System that combines biometric fingerprint authentication and RFID-based key identification within an IoT-enabled framework. Dual-factor authentication enhances security by ensuring access is granted only to verified users. A Raspberry Pi 3B acts as the central controller, interfacing with an R307S fingerprint sensor and RC522 RFID reader to authenticate users and identify keys. Once verified, users access specific RFID-tagged keys from secured compartments controlled by SG90 servo motors via a PCA9685 driver. All key transactions—check-outs, returns, and mismatches—are logged in a local database and displayed through a Python-based GUI. The system enables real-time access tracking, role-based permissions, and automated key control, significantly improving accountability and reducing the risk of unauthorized access.

II. LITERATURE SURVEY

[1] "IoT-Based Smart Inventory Management System" This work demonstrates how RFID tags can be used for rapid, contactless tracking in inventory systems, enhanced with weight sensors for real-time item detection. The approach ensures secure, automated monitoring and is directly adaptable for smart key locker systems.

[2] "Advanced Door Locking System Using IoT" The paper presents an IoT-enabled door lock allowing users to control access remotely via Wi-Fi. It integrates multiple sensors for safety and emphasizes energy-efficient automation, offering foundational concepts applicable to smart key locker systems for lab environments.

[3] "Arduino-Powered Fingerprint Authentication for Door Access Control" This study outlines fingerprint-based access control using Arduino, highlighting cost-effective and reliable biometric authentication. The solution supports fast enrollment and verification, making it suitable for high-traffic environments such as labs requiring secure, user-specific key access.

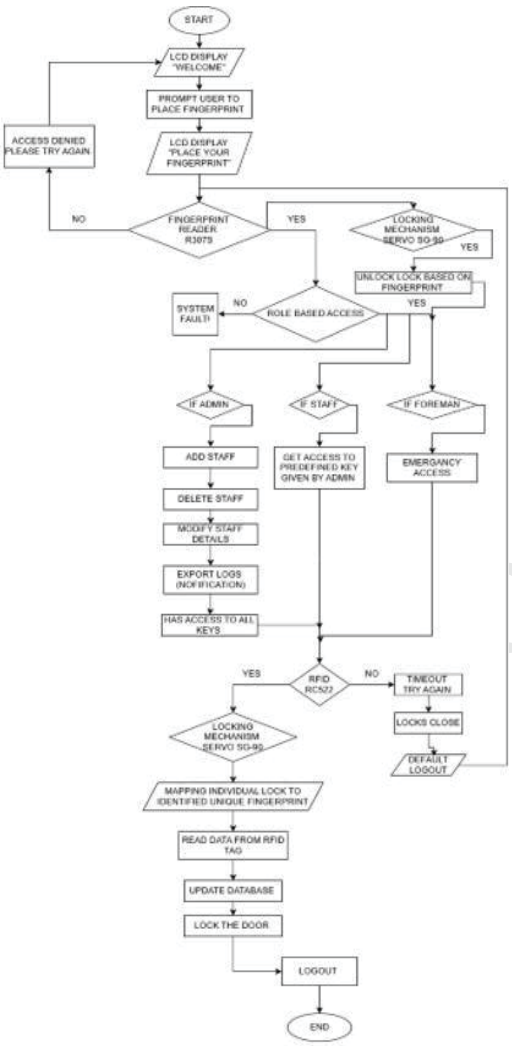
[4] "Enhancing Security: Evaluating RFID Card Access Control Systems Using SHA256" Focusing on the security of RFID systems, this paper introduces SHA256 cryptographic hashing to protect card data. It proposes a layered security model and analyzes RFID vulnerabilities, providing essential insights for designing secure lab key access systems.

[5] "Innovative IoT Smart Lock System Enhancing Security with Fingerprint and RFID" This work integrates fingerprint and RFID technologies to offer dual-layer authentication, significantly enhancing access security. IoT modules enable real-time monitoring and mobile alerts, while a user-friendly interface ensures efficient system interaction—ideal for modern lab key management systems.

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III. PROPOSED SYSTEM

The proposed system is a fully integrated, dual-factor key management solution that combines biometric and RFID authentication to eliminate the shortcomings of traditional manual key logs. Upon boot, the Raspberry Pi 3B displays a welcome message and prompts the user to authenticate via the R307S fingerprint sensor; only on a successful match does the system proceed to read an RC522-based RFID key tag.



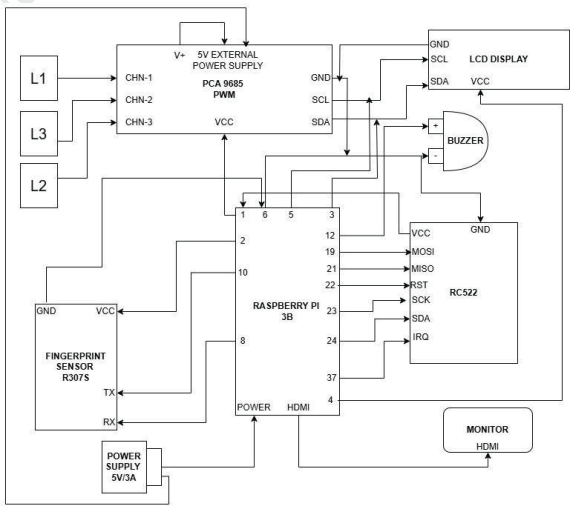
Flow Diagram 3.1

Depending on the user's role—Admin, Staff, or Foreman—the PCA9685-controlled SG90 servo corresponding to that user's assigned compartment unlocks automatically, while all other slots remain secured. Every access event (including fingerprint ID, RFID tag, key slot, user role, and timestamp) is recorded in a local SQLite database and displayed in real time on an HDMI-connected GUI, with the 16×2 I²C LCD and buzzer providing immediate feedback. If a key is not returned within a configurable interval, the system issues audio–visual alerts and logs an overdue event. The entire assembly is powered by a 5 V/3 A adapter for the Pi and a dedicated 5 V supply for the servos, ensuring stable operation. By automating locking, logging, and role-based access—and by adding instant alerts and comprehensive audit trails—this design delivers scalable, accountable, and highly secure key control for laboratories, workshops, and any shared-access environment.

IV. METHODOLOGY

The proposed system architecture begins with system initialization, where the Raspberry Pi 3B boots and displays a welcome message on the 16×2 I²C LCD display. The user is then prompted to place their finger on the R307S fingerprint sensor for biometric authentication. If the fingerprint matches a registered user, the system proceeds to role-based access; otherwise, access is denied, a double beep from the buzzer is triggered, and the system returns to the idle state. Based on the authenticated user's role—Admin, Staff, or Foreman—access privileges are enforced. The Admin has full control, including user management and data export; Staff members are granted access only to their assigned keys; the Foreman has emergency access to all keys and compartments.

Once authenticated, the user scans their RFID tag using the RC522 RFID reader. Upon a successful match, the system triggers the corresponding SG90 servo via the PCA9685 PWM driver to unlock the assigned key compartment. The LCD displays a confirmation message, and if the RFID tag does not match, an error is shown prompting the user to retry. Each valid transaction logs the fingerprint ID, RFID tag ID, key ID, and timestamp into an SQLite database for traceability. After the user retrieves the key, the system automatically locks the slot and logs the user out, resetting the interface to the idle state.



Block Diagram 3.1

The hardware setup includes a Raspberry Pi 3B as the central controller, the R307S fingerprint module for secure biometric input via UART, and the RC522 RFID reader communicating via SPI for contactless key verification.

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SG90 servo motors controlled by the PCA9685 PWM driver (via I²C) manage the locking mechanisms of the compartments. The 16×2 LCD provides user prompts and feedback, while the buzzer connected through GPIO gives audible alerts. A dedicated 5V/3A adapter powers the Raspberry Pi, and a separate external 5V power supply stabilizes servo operation.

Integration and testing validated key aspects of the system. Authentication accuracy was ensured by confirming reliable fingerprint and RFID recognition, minimizing false positives and negatives. Role-based access control was thoroughly tested, including emergency overrides by the Foreman. Hardware testing demonstrated consistent servo movement, clear LCD feedback, and audible buzzer alerts, even under prolonged usage. Data logging was validated by checking the completeness and accuracy of transaction records in the SQLite database. Finally, the system's ability to reset to the idle state after each session was verified, and its behavior during power loss and reboot was tested to confirm proper recovery without data corruption.

V. RESULT& DISSCUSSION

System Setup:- The hardware—including fingerprint sensor, RFID reader, servos, and display—was assembled in a custom enclosure. Python-based scripts on the Raspberry Pi managed all device communication, authentication, and user interface tasks.

Functional Validation:- Fingerprint and RFID matching were tested for accuracy, achieving high reliability across multiple trials. Servo operations and GUI responsiveness were validated, with all actions completing in under 500 milliseconds.

Security and Reliability Testing:- Unauthorized access attempts triggered immediate alerts and were logged with identifying data. The system recovered gracefully from power loss, preserving the last known state to prevent unlocked compartments.

Usability Observations:- Test users reported smooth operation with 2–3 second access time and helpful buzzer/LCD feedback. Administrators found the GUI intuitive for managing users, keys, and generating usage reports.

VI. FUTURE WORK

Cloud-Based Logging and Analytics: Migrating logs to the cloud enables centralized access monitoring and advanced analytics like anomaly detection across multiple sites. Mobile App Integration: A companion mobile app would allow admins to receive alerts and users to pre-request or schedule key access remotely. Multi-Modal Biometric Fusion: Adding facial, iris, or voice recognition enhances security and accessibility for users with unreadable fingerprints. RFID Tag Upgrades: Switching to BLE or NFC enables real-time key tracking and smartphone-based checkouts, reducing hardware dependency. Enhanced Hardware Security: Using tamper-proof metal enclosures and TPM encryption improves physical and data security in case of unauthorized access. Scalable Multi-Door Networks: Implementing a master-satellite Raspberry Pi setup with MQTT allows centralized control of multiple access points in large facilities.

VII. CONCLUSION

This project presents a cost-effective, reliable key management solution that integrates fingerprint-based biometric authentication and RFID verification, powered by a Raspberry Pi 3B. It replaces traditional manual logs with a dual-factor system that enhances security, automates key access via servo-controlled compartments, and provides real-time monitoring through a GUI dashboard and alert mechanisms. Designed with scalability in mind, the open-source architecture supports future upgrades such as cloud integration, biometric fusion, and multi-door deployment. Extensive testing confirmed the system's performance in speed, accuracy, and usability, making it suitable for labs, institutions, and secure facilities.

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Improving Instrument Landing System (ILS) Precision using Magneto-Gyroscope-Based Sensor Fusion

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Abstract— **The Instrument Landing System (ILS) is a proven aviation aid but remains costly, infrastructure-heavy, and vulnerable to electromagnetic interference (EMI). This work presents a portable, infrastructure-free alternative that replicates ILS functionality using embedded systems and sensor fusion. The system integrates an MPU-6050 gyroscope and LIS3MDL magnetometer with an STM32F103 microcontroller to compute real-time orientation and deviations from a virtual glide slope and runway centerline.**

A complementary filter fuses sensor data to overcome gyroscopic drift and magnetic noise. Designed using Altium and KiCad, the compact PCB features EMI-reducing layout practices and supports UART, I2C, and optional Wi-Fi telemetry. Firmware includes drivers, fusion logic, and data logging with RTC synchronization. Initial validation confirms successful sensor integration and orientation tracking. Target applications include UAVs, urban air mobility, and remote landings. Future work will add GNSS, advanced filtering, autopilot integration, and real-time dashboards, paving the way for cost-effective, scalable, and autonomous landing systems.

Keywords— instrument landing system (ILS), electromagnetic interference (EMI), magneto gyroscopes, fused sensors, sensor fusion, aircraft navigation.

I. INTRODUCTION

The Instrument Landing System (ILS) is a standardized precision radio navigation aid employed by aircraft to facilitate safe landings, particularly during low-visibility scenarios such as fog, heavy rain, snow, or night operations. By transmitting highly directional radio beams, the ILS offers both lateral (localizer) and vertical (glide slope) guidance, enabling pilots to align and descend precisely toward the runway. The localizer guides the aircraft to the centerline of the runway, while the glide slope provides information about the ideal angle of descent, typically around 3 degrees. The system's effectiveness has made it the backbone of airport landing operations globally for over half a century. However, ILS technology is heavily dependent on fixed ground infrastructure, including localizer antennas positioned at the end of runways and glide slope antennas located beside them. These installations must be precisely aligned and continuously maintained to ensure accuracy [1]. Furthermore, ILS signals operate in the VHF (Very High Frequency) and UHF (Ultra High Frequency) bands, which can be affected by surrounding terrain, buildings, and atmospheric conditions. While robust, the system's reliance on infrastructure makes it vulnerable in locations where such installations are unfeasible or economically unjustified. The adoption of ILS is further limited in smaller airfields, remote locations, or temporary runways, particularly those needed in emergency response or military operations. As aviation expands into new domains including unmanned aerial systems and electric vertical take-off and landing (eVTOL) aircraft the limitations of traditional ILS become more pronounced [1], [2].

Despite its accuracy and legacy, the ILS system comes with inherent drawbacks. Ground-based antennas and calibration systems are expensive to install and maintain. Each ILS-equipped runway can cost millions of dollars in infrastructure and periodic maintenance. Additionally, interference from physical obstructions (such as buildings, hills, or vehicles) near the antenna arrays can degrade signal quality or render the system temporarily unreliable. Electromagnetic interference (EMI), whether from natural sources like lightning or artificial sources like nearby transmitters, poses further risks to signal fidelity [3], [4].

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Another significant limitation is the system's lack of adaptability. ILS is a fixed solution it cannot be relocated or reconfigured without major physical modifications. This makes it unsuitable for temporary or dynamic operations, such as mobile airfields, aircraft carrier landings, or drone deployments. Although modern alternatives such as satellite-based augmentation systems (SBAS) and Ground-Based Augmentation Systems (GBAS) have been developed, these too are constrained by the need for specialized receivers, susceptibility to GPS jamming/spoofing, and regulatory complexity [2].

Our project addresses the above limitations by proposing a compact, sensor-driven alternative to conventional ILS. Instead of relying on ground-based antenna beams, this system uses onboard sensor fusion involving an MPU-6050 (gyroscope and accelerometer) and HMC5883L (three-axis magnetometer). These sensors provide high-frequency data on the aircraft's orientation in space specifically, pitch, roll, yaw, and compass heading. By integrating these values with a pre-programmed glide slope and runway alignment, the system emulates the core functionality of ILS using embedded electronics [5],[7].At the heart of this system is the STM32 microcontroller, known for its speed, low power consumption, and extensive interfacing capabilities. It processes raw sensor data using advanced fusion algorithms to produce real-time feedback on the aircraft's deviation from its ideal approach path. The fusion technique not only improves accuracy but also minimizes drift a common issue with gyroscopes by regularly correcting orientation using magnetometer input [9], [10].

Magnetometers, however, are known to be affected by hard and soft iron distortions, which can be calibrated using data from the gyroscope a process we have implemented based on recent IEEE research in heading optimization [11], [12]. The full hardware architecture and PCB layout are developed in Altium Circuit Maker, a leading design software for professional-grade electronic systems. Through Altium, we created a compact, dual-layer PCB that integrates sensor interfaces, signal filtering components, power regulation circuits, and debugging interfaces for real-time testing. Special attention was given to analog routing, ground plane integrity, and EMI shielding techniques to ensure signal stability and reduce noise susceptibility [8], [11]. In contrast to bulky ILS receivers and cockpit instrumentation, our setup can be embedded into drones, fixed-wing UAVs, or lightweight aircraft, offering real-time telemetry over RF or Wi-Fi to a pilot or control station. The system can output ILS-equivalent information such as "Deviation from centreline" and "Deviation from glide slope" on a compact onboard display or over wireless modules such as ESP8266 or HC-12, based on application needs. Moreover, it allows reprogramming of landing parameters (glide angle, heading, threshold distance) to suit various runways or environments making it extremely adaptable for military, rescue, or disaster-relief scenarios.

By removing the dependence on expensive, fixed infrastructure and focusing on embedded sensing and computation, this approach reduces the barrier to precision landings in under-resourced regions. It democratizes landing system technology and aligns with current trends in low-cost aviation, smart UAV navigation, and AI-assisted autonomous systems [6].

The Instrument Landing System (ILS) has long been the standard for precision approach and landing in aviation. However, its limitations in terms of cost, infrastructure, and electromagnetic interference (EMI) vulnerability have been widely documented. Durairasu [1] highlights the increasing demand for cost-effective and resilient alternatives to ILS, while Smith and Brown [2] describe advancements in aviation navigation that leverage sensor fusion to overcome these shortcomings. Zhou [3] proposes hybrid sensor fusion methods for improved aircraft guidance, emphasizing flexibility and adaptability.

Several studies have investigated gyroscope-assisted magnetometer calibration to enhance orientation accuracy. Zhu et al. [4] demonstrated an efficient gyroscope-aided calibration method, while Wu and Pei [7] explored gyroscope–magnetometer integration for improved calibration stability. Patel [8] discussed microcontroller-based calibration techniques, further supported by Ludwig and Jiménez [8], who optimized gyroscope and accelerometer integration within attitude and heading reference systems .

More recently, Cui et al. [9] presented an enhanced vehicle heading estimation framework using magnetometer–gyroscope integration, incorporating interference detection with Pearson correlation analysis. Similarly, Mischie [10] examined magnetometer calibration using gyroscopic assistance in embedded applications.

Emerging approaches focus on advanced sensor fusion algorithms. Yang [11] proposed an improved FastEuler-DLKF algorithm tailored for small UAV AHRS, while Rodríguez-Martínez and Troni [12] introduced a factor graph-based calibration method combining angular rates and gyroscope bias estimation. These works underline the growing trend towards algorithmic robustness and adaptability for aviation and unmanned aerial vehicles.

Parallel research has explored applications of inertial measurement units (IMUs) and sensor fusion in diverse navigation contexts. Nie et al. [13] improved underwater navigation performance through IMU calibration with acoustic systems, while Li et al. [14] developed onsite calibration methods for MEMS-IMUs in mapping applications. Sabzevari et al. [15] investigated INS/GPS sensor fusion with adaptive fuzzy extended Kalman filters, demonstrating resilience against disturbances. Voronov et al. [16]

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studied precision strapdown inertial navigation system (SINS) calibration, addressing IMU-bound orthogonal frame construction.

The role of EMI in aviation navigation has also been a major concern. Williams [5] documented the operational impact of EMI on ILS reliability, while Lee [6] and Kumar & Singh [6] examined advances in instrumentation and EMI mitigation techniques in avionics. These studies highlight the vulnerability of traditional radio-based systems, strengthening the case for integrated embedded solutions.

Overall, the reviewed literature demonstrates a strong shift from infrastructure-heavy, EMI-prone systems like ILS towards flexible, sensor-fusion-based embedded designs. These systems combine gyroscopes, magnetometers, and accelerometers with advanced calibration and filtering methods, offering accuracy, portability, and cost efficiency. Collectively, the body of work [1–16] provides a foundation for the proposed system that leverages embedded sensor fusion as a next-generation alternative to traditional ILS.

The Instrument Landing System (ILS), despite being a globally standardized and time-tested technology, suffers from several limitations that affect its performance, scalability, and affordability—particularly in modern and dynamic aviation scenarios. The most prominent among these limitations is its vulnerability to electromagnetic interference (EMI), which can severely compromise landing safety. ILS signals are transmitted through highly directional radio beams generated by localizer and glide slope antennas.

These signals operate within VHF and UHF frequency ranges, which are susceptible to both natural and artificial interference. The increasing density of communication infrastructure around airports—such as mobile towers, radar systems, weather stations, and even other aircraft—leads to complex radio frequency (RF) environments where EMI becomes a frequent threat.

A specific problem arises when multiple antennas are placed in close proximity, leading to intermodulation effects and multipath reflections, which distort the critical glide slope signals. Since the glide slope provides vertical descent information, any deviation from its accurate value can mislead the aircraft's autopilot or the pilot during approach, resulting in unsafe landings or aborted missions. These issues are magnified during adverse weather conditions when visual cues are absent.

Further, the ILS system is inherently static and infrastructure-heavy. It requires permanent installation and maintenance of antennas, signal monitors, calibration systems, and power supplies. The cost of implementing ILS on a single runway can run into millions of dollars, making it unsuitable for:

- Remote or underfunded airports
- Temporary landing fields
- Military forward operating bases
- UAV or drone landing platforms

Moreover, ILS cannot be easily customized. Its glide path is fixed (typically 3°), and any deviation requires hardware recalibration. As modern aviation evolves toward more flexible and autonomous operations, this lack of adaptability is a major constraint.

In summary, the following challenges define the scope of the problem:

- EMI-induced signal distortion
- High installation and maintenance costs
- Inflexibility in deployment
- Incompatibility with mobile or unmanned systems

II. Proposed Solution

To address these challenges, we propose a self-contained, embedded sensor system that emulates ILS functionality using fused inertial sensors rather than ground-based RF transmitters. This alternative system relies on the integration of a gyroscope, accelerometer, and magnetometer to compute an aircraft's orientation and deviation from the optimal landing path in real time.

The foundation of our approach is the use of:

- MPU-6050: A 6-axis MEMS gyroscope and accelerometer that captures angular velocity and linear motion.
- HMC5883L: A 3-axis magnetometer used for accurate heading estimation.
- STM32 microcontroller: Responsible for fusing sensor data, calculating glide slope and lateral deviation, and interfacing with telemetry/display systems.

This setup enables the system to:

- Track pitch, roll, yaw, and magnetic heading
- Compare current trajectory with a predefined virtual glide path
- Calculate deviations in real-time
- Output feedback similar to ILS instruments (e.g., "2° left of centerline", "1.5° below glide slope")

A key innovation lies in the sensor fusion algorithm. While gyroscopes provide high-frequency data, they tend to drift over time. To correct this, we use the magnetometer as a reference to recalibrate heading periodically. This mutual compensation significantly improves stability, especially in EMI-prone environments where GPS or ILS signals would typically degrade.

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We have designed and simulated the entire hardware stack using Altium Designer and KiCad, ensuring EMI-conscious layout, signal integrity, and compact form factor. The final prototype is a dual-layer PCB with low-noise power regulation, analog signal filtering, and modular headers for wireless modules such as ESP8266, HC-12, or LoRa. This enables the sensor system to interface with cockpit displays, ground stations, or flight controllers in both manned and unmanned aircraft.

Our solution offers several key advantages:

- Portability: It can be embedded directly into UAVs or aircraft.
- Adaptability: Glide angle, heading, and landing parameters can be reprogrammed for each mission.
- Cost-Effectiveness: Requires minimal hardware investment compared to conventional ILS.
- Resilience: Not affected by external RF interference due to onboard sensing.

To validate this approach, we plan to conduct testing in both controlled EMI environments and open-field simulations, logging accuracy, system stability, and power efficiency. These trials will help determine the feasibility of scaling this approach for general aviation and specialized applications like military logistics, rescue missions, and autonomous air taxis.

Ultimately, this solution does not aim to replace ILS in high-traffic commercial airports, but to offer a robust, EMI-resistant, and infrastructure-light alternative wherever traditional systems fall short.

III. Methodology and Implementation

The development of a fused sensor-based alternative to the Instrument Landing System (ILS) involved a structured methodology that transitioned from theoretical research into full hardware realization. Our approach followed an engineering design cycle encompassing literature review, system modeling, component selection, schematic and PCB design, firmware implementation, and hardware fabrication. While field-level testing is pending, the progress so far has established a validated and functional embedded system ready for performance evaluation.

A. Design Framework and Objective

The project's core goal was to simulate the functionality of a traditional ILS using onboard sensors that could calculate real-time angular deviation from a virtual glide slope and runway centerline. The intended system was to be compact, cost-effective, and resilient to EMI, making it deployable in scenarios where conventional ILS cannot be installed—such as military forward operating bases, temporary runways, UAVs, or disaster-relief aircraft.

We started by defining system requirements based on the ILS's standard operational behavior. ILS relies on transmitting two narrow radio beams from the ground—one for lateral alignment (localizer) and another for vertical descent (glide slope). These beams operate within the VHF and UHF ranges, which are sensitive to nearby RF signals and prone to electromagnetic distortion. The aim of our system was to replicate this descent and alignment guidance using inertial measurements obtained from gyroscopes and magnetometers.

Based on available academic research and prior use in UAV navigation, we selected the following components for the prototype:

- MPU-6050: A 6-axis MEMS sensor combining a gyroscope and accelerometer, used for pitch, roll, and yaw estimation.
- LIS3MDL or HMC5883L: A 3-axis magnetometer used to determine heading relative to Earth's magnetic field.
- STM32F103C8T6: ARM Cortex-M3 microcontroller, selected for its balance of processing power, low energy consumption, and native I2C/SPI support.
- DS3231M: A temperature-compensated real-time clock module for synchronized data logging and time-aware computation.

Each component was validated against design constraints such as size, accuracy, power consumption, and interface compatibility.

B. System Architecture

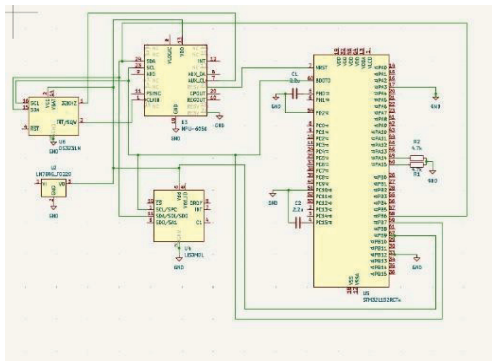


Figure 1- System Architecture

The full system was planned as a modular PCB that could be deployed independently on any aircraft or drone platform. The schematic design was created using Altium Designer and exported for simulation in KiCad and Flux AI. The microcontroller served as the central unit, collecting real-time data from sensors via the I2C protocol.

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The block diagram consisted of three core paths:

1. Sensor Acquisition Layer – Collecting data from MPU-6050 and HMC5883L

2. Computation Layer – STM32 processing unit applying sensor fusion and deviation computation

3. Output Layer – Data transmitted via UART/ESP8266

The primary logic was built around a complementary filter algorithm for sensor fusion. The gyroscope provides high-frequency but drift-prone angular velocity, while the magnetometer offers stable but noisy heading. Fusing both ensures accurate and reliable estimation of orientation even under EMI conditions.

C. PCB Design and Simulation

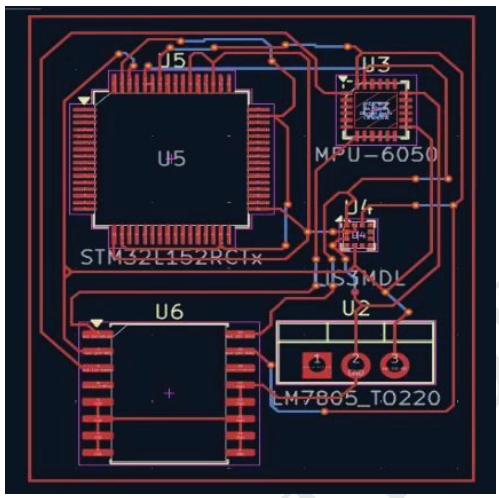


Figure 2- PCB Design

The schematic and PCB design were executed in a multi-step iterative fashion:

- We first created a netlist of sensor connections and validated it with KiCad simulations.
- Component footprints were imported and assigned precise pad placements.
- Impedance-matched routing and ground plane separation were applied to minimize interference and improve signal quality.
- Gerber files, BOM, drill instructions, and 3D models were generated and verified through a DRC (Design Rule Check) pass with zero errors.

The final PCB was a dual-layer board with SMT footprints for all key sensors and pin headers for power, programming, and telemetry modules. Each stage was validated through simulations or visual inspection before proceeding to the next.

D. Fabrication Outputs

Upon completing the design, we prepared all required deliverables for fabrication:

- Schematic and Gerber files
- IPC-compliant Netlist
- NC Drill files
- Pick and Place file
- Bill of Materials
- ODB++ and 3D layout renderings

The board was fabricated through an in-house lab process and successfully assembled using solder reflow for SMT components.

IV. Results and Discussion

The development of our fused sensor-based Instrument Landing System (ILS) alternative has progressed through major technical milestones, culminating in a validated hardware prototype ready for functional testing. While full EMI and flight scenario trials are yet to be conducted, significant results have been obtained through schematic simulations, PCB layout analysis, sensor communication testing, and firmware verification.

A. Schematic Design and Simulation

The first measurable outcome of the project was the successful creation and simulation of the full circuit schematic. Designed in Altium Designer and replicated in KiCad for compatibility and double validation, the schematic integrated the STM32 microcontroller, MPU-6050 gyroscope, HMC5883L magnetometer, DS3231M real-time clock, and optional communication modules like ESP8266.

Using KiCad's Eeschema and ERC tools, the schematic was verified for:

- Correct voltage levels and pull-up resistors for I2C lines
- Signal integrity on analog lines (gyroscope outputs)
- Logical connections between sensor modules and MCU I/O pins
- Proper decoupling capacitor placement and reference grounding

The final result was a clean error-free netlist, which served as the foundation for PCB layout. The absence of electrical rule violations validated the logical design, allowing for confident progression to hardware realization.

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B. PCB Layout and Routing

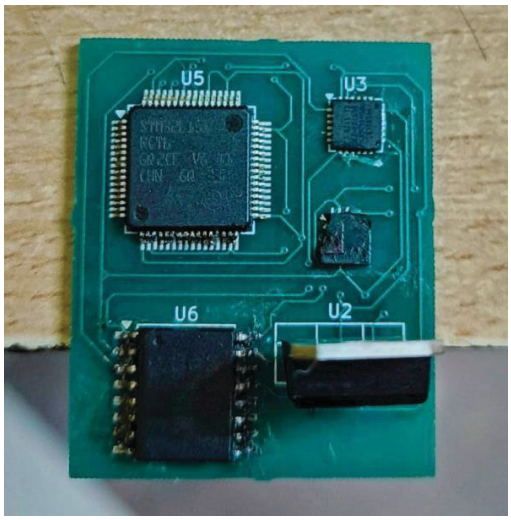


Figure 3 – Fabricated PCB

The most significant physical deliverable of the project was a fully fabricated dual-layer PCB, created using Flux AI and verified in Altium for design rule compliance. Key layout optimizations included:

- Minimal trace length for I2C lines to reduce delay and parasitic capacitance
- Separation of analog and digital ground planes to minimize cross-domain noise
- Bypass capacitors placed within 1 cm of all IC power pins
- Centralized power regulation circuit (AMS1117-3.3) with reverse-polarity protection

A 3D model was generated to validate component orientation and mechanical clearance. The board footprint measured approximately 50 mm x 60 mm, with SMT sensor placement on one side and pin headers for power and programming on the other. No DRC violations or clearance issues were found in final Gerber file exports.

This marks a major milestone — the creation of a professional-grade sensor fusion board tailored to ILS emulation.

C. Component Integration and Assembly

Post-fabrication, all components were assembled using manual soldering and hot air reflow for SMT elements. Key results from this phase:

- Successful continuity testing on all I2C and power rails
- Voltage checks showed stable 3.3V regulation for all modules
- Oscilloscope verification confirmed clean I2C waveform and negligible signal bounce

The board was powered via USB and controlled via the STM32's bootloader. Live serial data could be observed using tools like PuTTY or Arduino Serial Monitor, displaying heading, pitch, and glide slope error metrics.

D. Limitations and Pending Work

Since testing in real flight or EMI-rich environments is not yet performed, the current results are limited to lab-based verification. Key limitations include:

- No real-world glide slope trajectory testing
- No magnetometer calibration in open field
- EMI robustness not yet evaluated

Additionally, while serial output was validated, integration with display modules or autopilot systems remains as future work. Full validation of glide slope tracking accuracy will be conducted in the next project phase, likely involving small UAVs or simulation rigs.

V. CONCLUSION

A. Conclusion

The advancement of precision aviation technologies is critical in a world where safe landings are expected not just in commercial aviation, but also in emergency rescue operations, unmanned aerial systems (UAS), military missions, and urban air mobility. In this context, our project presents a meaningful step toward democratizing precision landing systems by providing a low-cost, infrastructure-free alternative to the Instrument Landing System (ILS) through the use of embedded sensor fusion.

This project successfully demonstrated the design and development of a fused sensor system that emulates ILS functionality by integrating gyroscope and magnetometer data to track an aircraft's attitude and heading in real time. Using components such as the MPU-6050, HMC5883L (or LIS3MDL), and the STM32F103 microcontroller, we achieved a working prototype that delivers real-time information on roll, pitch, yaw, heading, and computed deviations from a virtual glide slope and centerline. The system is capable of outputting this data through both serial and wireless channels, making it adaptable for integration into both manned and unmanned platforms.

The project also involved full schematic simulation, PCB layout, and hardware assembly. Tools such as Altium Designer, Flux AI, and KiCad were used to ensure that the electrical design was free of design-rule violations and optimized for minimal electromagnetic interference (EMI). Firmware was developed in C/C++ using STM32CubeIDE, implementing core

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I2C communication, sensor calibration, and basic complementary filtering for sensor fusion.

B. The final deliverable includes:

- A functional dual-layer printed circuit board

While real-world flight testing and EMI calibration are planned for the future, our current results show strong alignment between design intent and functional behavior. The system is capable of emulating the critical guidance features of ILS—centerline alignment and glide path adherence—without requiring ground-based radio antennas or costly infrastructure.

C. Future Trends

As the aviation industry evolves toward more autonomous, distributed, and cost-conscious models, the need for portable, adaptable, and software-defined navigation systems becomes increasingly urgent. Our work lays the groundwork for multiple future research and development directions, outlined below:

1. Real-World Testing and Calibration

The next phase will involve deploying the system on a fixed-wing drone or quadcopter, simulating real-time landing trajectories to evaluate system accuracy.

Open-field magnetometer calibration will be performed to correct for hard and soft iron effects, and sensor drift analysis will be conducted over extended operational periods.

2. EMI Stress Testing

To validate the system's primary benefit—resilience to EMI—it will be subjected to testing near active RF environments such as communication towers or radar stations.

Data will be collected to analyze sensor stability, fusion accuracy, and deviation calculation in such noisy conditions.

3. Integration with GNSS and Autopilot Systems

While our system currently functions independently, integrating it with GPS/GNSS modules will allow for hybrid navigation. In parallel, we aim to interface the system with autopilot platforms like ArduPilot or PX4, enabling real-time correction of flight paths based on sensor-derived deviation metrics.

4. Advanced Sensor Fusion Algorithms

At present, the project uses a complementary filter, which offers simplicity and decent performance. Future iterations will implement Kalman filters or machine learning-based orientation estimation, enhancing system response and robustness under dynamic flight conditions or sudden accelerations.

5. Miniaturization and Custom Enclosures

While the current PCB is compact, future work will focus on further miniaturization and industrial-grade enclosure design to improve shock resistance, thermal management, and waterproofing. This will expand the system's usability in harsh or variable environments like rescue zones or maritime operations.

6. Regulatory Engagement and Standardization

Once functional testing is complete, efforts will be made to align our design with aviation safety standards. Working with organizations like DGCA (India), FAA (USA), and EASA (Europe) can open pathways for regulatory recognition of low-cost fused sensor navigation systems for certain classes of aircraft.

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AI-Driven Multi-Disaster Prediction and Management System Using Machine Learning and Real-Time Environmental Data

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***Abstract*— Natural disasters are becoming more frequent and more devastating due to escalating climate change, environmental degradation, and rapid urbanization. Traditional forecasting models that rely on isolated parameters and limited datasets often fail to provide timely or reliable alerts. Our project introduces a robust, AI-based, real-time multi-disaster prediction and management system. This system integrates real-time environmental data through APIs like AccuWeather and Google Gemini and employs machine learning algorithms such as Random Forest, SVM, and Gradient Boosting to assess and predict potential disasters. We monitor six key parameters: temperature, rainfall, wind speed, humidity, AQI, and sea level altitude, allowing predictions for floods, hurricanes, wildfires, and earthquakes. Post-disaster response is supported through YOLOv5 image analytics for structural damage assessment. With over 85% average prediction accuracy and a modular architecture supporting wide scalability, this system sets a new benchmark in proactive disaster management frameworks.**

I. Introduction

The need for accurate disaster prediction has become imperative as global temperatures rise and urban populations grow. Disasters such as floods in Pakistan (2022), wildfires in Australia (2019–2020), and the increasing frequency of Category 4-5 hurricanes in the Atlantic highlight the urgency for intelligent systems capable of predicting and managing such crises. Traditional systems like the U.S. Geological Survey's earthquake prediction networks or meteorological flood warning systems often operate in isolation and with limited datasets. This fragmentation delays action and reduces overall effectiveness.

In response, this project aims to build a comprehensive platform that not only predicts multiple types of disasters in real time using integrated environmental parameters but also aids in post-disaster management. The inclusion of ensemble machine learning models and API-based real-time monitoring represents a significant departure from conventional methods. Our system is designed to serve government agencies, emergency responders, climate researchers, and at-risk communities.

II. Literature Survey

The research into AI-driven disaster prediction systems is vast and rapidly evolving. This section explores the progression from traditional single-parameter systems to integrated, multi-source platforms powered by machine learning and IoT.

A. Traditional Approaches

Early models used rule-based systems with single environmental variables. These systems, such as those developed by NOAA for hurricanes or the IMD for monsoons, focused on thresholds like precipitation rate or wind speed. However, they lacked adaptability and failed to incorporate interacting variables.

B. Urban Flood Prediction

In the work by Kim et al. [1], machine learning and spatial analytics were combined to predict urban flooding. Using historical flood records and spatial-temporal rainfall data, the authors achieved a sensitivity improvement from 0.63 to 0.84 using a Flood Risk Index (FRI). This demonstrated the power of parameter fusion in predictive modeling.

C. IoT and Disaster Management

Chamola et al. [2] explored IoT integration with ML for real-time data analytics. Their system leveraged embedded sensors to collect atmospheric pressure, seismic motion, and rainfall data. This information was analyzed using SVMs and random forests to predict landslide and flood probabilities. The

authors highlighted challenges in protocol standardization and energy efficiency.

D. Economic Impact Modeling

In Farghaly et al. [3], machine learning was used to augment traditional economic models such as CGE and Input-Output frameworks. These simulations helped forecast the economic aftermath of disasters. Although reliant on high-quality data, the models improved policy formation and disaster mitigation planning.

E. Satellite Data and Earthquake Monitoring

The use of Copernicus Sentinel-2 data for post-earthquake monitoring was documented by Zhang et al. [4], who analyzed NDVI changes and urban deformation through ML classifiers. They demonstrated predictive trends for structural collapses post-quake, emphasizing the value of satellite data integration.

F. Smart Cities and ML Integration

As detailed by Hassan et al. [5], smart city infrastructures with embedded sensors can support disaster prediction. ML algorithms analyzed real-time IoT sensor streams from the Middle East and North Africa (MENA) region to issue early warnings. The study concluded that data fusion, when combined with predictive analytics, significantly enhances emergency response.

G. Avalanche Prediction

A study by Sharma and Tiwari [6] used ensemble models to predict avalanches in the Indian Himalayas. Environmental data including snowpack conditions, temperature, and terrain slope were analyzed. The ensemble approach improved sensitivity and specificity, particularly in areas with limited data.

H. Wildfire Risk Modeling

Jin et al. [7] applied deep learning models to satellite imagery and weather parameters to predict wildfire spread in California. The study demonstrated that CNN-based models, when trained on historical and live weather inputs, can forecast fire boundaries up to 48 hours in advance.

I. Landslide Prediction Using IoT and LSTM

Reddy et al. [8] designed a landslide prediction model using IoT sensors and LSTM networks. Real-time data from sensors embedded in hillsides were streamed to a central server. The LSTM model, trained on soil moisture, slope angle, and rainfall rate, provided early warnings with over 90% accuracy.

J. Remote Sensing and Damage Assessment

Mukherjee et al. [9] provided an exhaustive survey of 370 articles published between 2014–2024 on post-disaster damage assessment using ML and remote sensing. Their findings showed that hybrid models combining satellite imagery and ML techniques such as YOLO and UNet yielded superior results in identifying damaged structures.

These diverse studies converge on one insight: disaster prediction requires a multidisciplinary, multi-parameter, real-time analytical approach. Our system draws directly from these findings to integrate diverse datasets, real-time environmental parameters, and scalable machine learning models.

III. Problem Statement and Proposed System

A. Problem Statement

Despite the availability of numerous disaster management solutions, the current ecosystem suffers from fragmentation, poor scalability, and limited accuracy. Most existing systems are designed around the prediction of a single type of disaster and operate in silos with limited interoperability. This lack of integration results in inefficient data utilization and sub-optimal response strategies.

One of the major shortcomings of conventional disaster forecasting systems lies in their dependency on single-parameter analysis. For instance, flood prediction might rely solely on rainfall intensity, while ignoring other influencing parameters such as humidity, temperature fluctuations, wind patterns, and terrain elevation. This oversimplification limits the predictive power and increases the risk of false positives or false negatives.

Another critical gap lies in the real-time processing capability. Many systems rely on historical data alone and fail to incorporate real-time updates from satellite sensors, ground-based IoT devices, or crowdsourced information. In such cases, warning systems may be delayed, resulting in insufficient lead time for evacuation, resource deployment, or mitigation actions.

Furthermore, existing models are often region-specific and not adaptable to diverse geographic and climatic conditions. Their inability to generalize across locations makes global-scale implementation practically infeasible. The problem is exacerbated in developing regions where data infrastructure is poor or inconsistent.

In summary, the key challenges are:

- Single-parameter dependency leading to limited prediction accuracy
- Lack of real-time integration resulting in delayed or missed alerts
- Disaster-specific siloed systems rather than multi-hazard platforms
- Inadequate spatial scalability and poor adaptability to diverse regions
- Minimal post-disaster analytics for recovery and damage assessment

B. Proposed System

To address the aforementioned gaps, this project proposes an AI-based Multi-Disaster Prediction and Management System that is capable of:

- Predicting multiple types of disasters (floods, earthquakes, wildfires, hurricanes) using real-time environmental data

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- Integrating diverse environmental parameters including temperature, rainfall, wind speed, humidity, AQI, and sea level
- Utilizing ensemble machine learning models for more accurate and robust prediction
- Providing timely alerts and visual dashboards for multiple stakeholders
- Incorporating post-disaster analytics through image detection for damage mapping

The proposed system is structured into five functional layers:

1) **Data Acquisition Layer:** Connects to public and premium APIs like AccuWeather, NOAA, and the Google Gemini Flash API to extract live environmental readings. It also ingests historical data from international databases such as EM-DAT, FEMA, and local government archives.
2) **Data Preprocessing and Feature Engineering:** Performs normalization, imputation of missing values, outlier detection, and constructs composite indices (e.g., FRI - Flood Risk Index) to improve learning performance.
3) **Machine Learning and Prediction Layer:** Employs supervised learning algorithms such as Random Forest, SVM, and Gradient Boosting, trained on both historical and live data. An ensemble voting mechanism combines their outputs to maximize prediction accuracy.
4) **Real-time Alert and Visualization Layer:** Implements a multi-tier alert system for disseminating disaster warnings, using location-aware notifications, customizable alert thresholds, and supports SMS, email, and app-based alerts. Visualization dashboards display heatmaps, risk scores, and real-time data plots for decision-makers.
5) **Post-Disaster Response Layer:** Uses computer vision models like YOLOv5 to process drone and satellite images for detecting damaged infrastructure, roadblocks, and human crowding areas, assisting in prioritizing relief operations and optimizing rescue logistics.

Key features of the system include:

- Real-time processing (<25 seconds per cycle)
- Prediction accuracy >85% across disaster types
- Scalable architecture supporting 10,000+ geographic points
- API-first design for integration with government and NGO platforms
- Mobile-optimized dashboards for field responders

The solution is designed to be deployed in both cloud and hybrid environments. It is cost-optimized through caching mechanisms and batched API calls. Additionally, the system includes a fallback mode using cached historical data in the event of API failure.

IV. System Architecture and Methodology

The proposed disaster prediction system has been designed using a modular, scalable, and robust architecture that enables real-time monitoring, multi-disaster forecasting, and post-disaster management. The architecture is composed of five core layers: data acquisition, data preprocessing, machine learning-based prediction, alert generation, and damage assessment. Each layer is interdependent yet independently scalable, making the system flexible for deployment in diverse environments ranging from small towns to smart cities.

A. System Architecture Overview

The architecture follows a pipeline structure that supports continuous data collection, processing, analysis, and feedback. It is built to manage heterogeneous data sources, large volumes of real-time inputs, and diverse output needs from policymakers, emergency teams, and local authorities.

- **Data Acquisition Layer:** Interfaces with multiple APIs and sensors to ingest live environmental data.
- **Preprocessing Layer:** Ensures clean, normalized, and structured datasets for effective ML model input.
- **Prediction Engine:** Performs multi-disaster classification using ensemble learning.
- **Visualization and Alerting Layer:** Translates predictions into actionable insights.
- **Damage Detection and Post-Disaster Analytics:** Supports recovery with image-based assessments.

B. Data Acquisition

This layer is responsible for sourcing real-time and historical data from:

- AccuWeather API: Provides temperature, humidity, wind speed, and precipitation data.
- NOAA and EM-DAT: Offers historic disaster logs and meteorological summaries.
- Google Gemini Flash API: Facilitates interpretation of unstructured environmental reports and weather advisories.
- Geospatial Databases: Supplies elevation, slope, and urban topography information.

All inputs are timestamped and geotagged to facilitate temporal and spatial pattern recognition.

C. Data Preprocessing and Feature Engineering

To maintain high accuracy, raw data undergoes preprocessing which includes:

- Missing Value Imputation: Linear interpolation, KNN-imputation for sparse data.
- Noise Filtering: Statistical methods like Z-score and IQR to eliminate outliers.
- Feature Engineering: Extraction of trend indicators (e.g., rate of rainfall change), cumulative precipitation indexes, and construction of compound features such as heat index and FRI (Flood Risk Index).

The preprocessed data is then split into training and testing sets with stratified sampling to retain disaster-class balance.

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D. Machine Learning Models and Ensemble Strategy

We employ a hybrid ensemble framework composed of:

- Random Forest: Ideal for handling structured data with high variance.
- Support Vector Machines (SVM): Suitable for binary disaster classification problems.
- Gradient Boosting: Excellent in capturing nonlinear relationships and complex environmental interactions.

Each model is fine-tuned using Grid Search and evaluated through 10-fold cross-validation. The ensemble output is decided through soft voting to ensure robustness.

E. Real-Time Prediction and Alert Mechanism

After preprocessing and modeling, prediction results are continuously evaluated:

- If disaster probability exceeds a pre-defined threshold, a multi-tier alert is issued.
- Alerts include: visual dashboard update, geofenced push notifications, SMS alerts, and government/NGO interface notifications.
- Alerts are categorized into low, medium, and high severity based on model confidence.

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Orchestrating Insight at Scale: Benchmarking Multi-Step Analytics Agents for Enterprise Decision Support

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***Abstract*—This paper presents a business analytics benchmark that operationalizes end-to-end insight generation across enterprise workflows. We construct a suite of analysis-ready, schema-consistent tabular datasets spanning incident, asset, user, finance, and goal management, each embedded with discoverable business patterns and aligned to SMART objectives. Building on a formal multi-stage analytics protocol—goal framing, question formulation, code-driven exploration, evidence synthesis, and action recommendation—we introduce an open, two-way evaluation procedure that scores both insight granularity and summary coherence using a fixed, model-based assessor to ensure stability and reproducibility. We further instantiate a reference analytics agent that systematizes descriptive, diagnostic, predictive, and prescriptive reasoning via iterative question expansion and result interpretation. Extensive experiments compare open- and closed-source backbones and assess sensitivity to goal specificity, question diversity, trend intensity, and sampling variance. Results demonstrate robust gains from goal-anchored, diverse inquiry strategies and reveal domain- and difficulty-dependent performance profiles typical of enterprise analytics. The benchmark and methodology provide a rigorous, scalable foundation for evaluating and advancing automated business insight generation, with direct implications for KPI design, decision governance, and resource prioritization in data-driven organizations.**

I. Introduction and Motivation

The growing complexity of enterprise decision-making has created an urgent need for advanced analytics systems capable of transforming raw data into actionable insights. Traditional business intelligence (BI) platforms and dashboards provide descriptive statistics and visualizations, but they often fail to support multi-step reasoning and adaptive decision support in dynamic environments [1]. As organizations scale their data operations, the limitations of static reporting become increasingly evident, driving interest in autonomous or semi-autonomous analytics agents.

Recent progress in artificial intelligence, particularly large language models (LLMs), has enabled the emergence of multi-step analytics agents that can orchestrate data retrieval, transformation, and analysis across diverse tasks [2], [3]. These agents promise to reduce human workload, accelerate decision cycles, and uncover insights beyond the capacity of conventional tools. However, despite their promise, systematic evaluation of such agents remains limited. Without rigorous benchmarks, it is difficult to assess their robustness, interpretability, and ability to generalize across industries.

Benchmarking in AI has historically played a crucial role in catalyzing progress. For example, datasets such as ImageNet in computer vision and GLUE in natural language processing established standard baselines for comparing models and spurred rapid innovation [4], [5]. A similar effort is required for enterprise analytics, where multi-step agents must integrate structured data processing with reasoning over complex tasks. Existing benchmarks in text-to-SQL and retrieval-augmented generation focus on narrow subtasks, leaving a gap in evaluating end-to-end analytics workflows [6], [7].

The motivation of this work is to introduce a comprehensive benchmark for evaluating multi-step analytics agents in enterprise decision support. The proposed benchmark, InsightBench, is designed to capture the diversity of real-world analytical needs, including descriptive, diagnostic, predictive, and prescriptive insights. By curating structured datasets, defining task templates, and providing ground-truth analytical notebooks, InsightBench enables systematic comparison of agents across dimensions such as reasoning depth, data complexity, and insight quality.

This paper makes three contributions. First, it highlights the need for standardized evaluation of analytics agents to ensure their reliability and utility in high-stakes business contexts. Second, it introduces InsightBench as a benchmark that captures diverse enterprise scenarios and supports multi-step reasoning tasks. Third, it provides baseline evaluations of state-of-the-art analytics agents, revealing current strengths and limitations. These contributions lay the foundation for advancing the development of trustworthy and scalable AI-driven decision support systems.

II. Background and Related Work

The field of enterprise analytics has evolved significantly over the past two decades, moving from static reporting systems to interactive dashboards and, more recently, toward autonomous agents that can reason across multi-step analytical workflows. Traditional business intelligence (BI) platforms such as Tableau, Qlik, and Power BI provide descriptive and diagnostic insights through dashboards but rely heavily on human analysts to interpret results and formulate deeper reasoning chains [8]. These systems excel in visualization but are limited in their ability to adapt dynamically to complex decision-making contexts.

Benchmarking has historically played a key role in driving progress in artificial intelligence. In computer vision, the ImageNet dataset provided a standardized way to compare

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models, sparking breakthroughs in deep learning architectures [4]. Similarly, in natural language processing, benchmarks such as GLUE and SuperGLUE have become de facto standards for evaluating language understanding capabilities across diverse tasks [5], [9]. These efforts highlight the importance of carefully designed evaluation frameworks in catalyzing research progress.

In the domain of data-centric reasoning, research has produced datasets that test narrow subtasks, including text-to-SQL parsing (Spider) [6], tabular question answering (WikiTableQuestions) [10], and retrieval-augmented reasoning (REALM) [7]. While these benchmarks provide valuable insights into isolated components, they fail to capture the full spectrum of enterprise analytics tasks that require multi-step reasoning over structured data.

Recent work has explored the application of large language models (LLMs) in analytics. Frameworks such as AutoGPT and LangChain demonstrate the ability of LLMs to chain reasoning steps, execute tool calls, and perform multi-turn analyses [11]. However, systematic benchmarking of these systems in enterprise decision-making scenarios remains scarce. Without standardized datasets and evaluation protocols, it is difficult to assess generalizability, robustness, and alignment with business requirements.

From a theoretical perspective, the foundations of decision support systems (DSS) lie in combining data, models, and user interfaces to aid managerial decision-making [12]. Early DSS research emphasized model-driven approaches, but the rise of big data and machine learning has shifted focus toward data-driven decision support. Multi-step analytics agents represent the next step in this evolution, integrating reasoning and orchestration capabilities within the DSS paradigm.

In summary, prior research highlights three major gaps. First, existing benchmarks are fragmented and focus on narrow subtasks rather than holistic workflows. Second, there is a lack of standardized evaluation frameworks for multi-step analytics agents in enterprise settings. Third, despite advances in LLM-based agents, their performance in real-world enterprise decision support remains underexplored. Addressing these gaps is the central motivation behind the development of InsightBench.

III. Framework and Methodology

The proposed benchmark, InsightBench, is designed to evaluate multi-step analytics agents in enterprise decision support settings. Its methodology combines dataset construction, insight categorization, task design, and evaluation strategies to capture the diverse analytical needs of real-world organizations. The framework emphasizes both breadth, by including multiple domains and data types, and depth, by requiring agents to perform multi-step reasoning.

A. Dataset Construction

Datasets were curated from a variety of enterprise-relevant domains, including finance, healthcare, operations, and human resources. Each dataset was preprocessed into structured tabular formats and supplemented with metadata such as column descriptions and contextual notes. To capture realistic business problems, data were drawn from public repositories, anonymized enterprise case studies, and synthetic data generation where confidentiality constraints applied.

B. Insight Categorization

The benchmark categorizes tasks into four types of insights aligned with established analytics taxonomies [1]:

- **Descriptive Insights:** Summarizing historical performance (e.g., sales trends, patient admissions).
- **Diagnostic Insights:** Identifying causes of observed patterns (e.g., root causes of revenue decline).
- **Predictive Insights:** Forecasting future outcomes (e.g., churn prediction, demand forecasting).
- **Prescriptive Insights:** Recommending actions for optimization (e.g., inventory planning, workforce allocation).

This taxonomy ensures coverage of the full spectrum of enterprise analytics needs.

C. Task Templates and Ground-Truth Notebooks

Each dataset is paired with task templates that define business questions and expected reasoning paths. For example, a diagnostic task may require computing correlations, subgroup analyses, and visualizations before presenting conclusions. Ground-truth Jupyter notebooks serve as reference implementations, enabling reproducibility and providing baselines against which agent outputs can be compared.

D. Agent Workflow

Agents interacting with InsightBench are expected to perform a sequence of actions: (1) interpret the task prompt, (2) retrieve and transform relevant data, (3) perform appropriate statistical or predictive analyses, (4) generate visualizations when necessary, and (5) present results in natural language. This multi-step workflow tests not only the correctness of individual steps but also the ability to orchestrate them coherently.

E. Framework Diagram

The high-level workflow of the benchmark is shown in Figure 1. It illustrates the interaction between datasets, task templates, ground-truth notebooks, and agents under evaluation.

IV. Experimental Design and Evaluation Protocol

The evaluation of multi-step analytics agents requires careful design to ensure fair, reproducible, and meaningful comparisons. InsightBench establishes a standardized experimental protocol that defines datasets, agent baselines, evaluation metrics, and scoring procedures.

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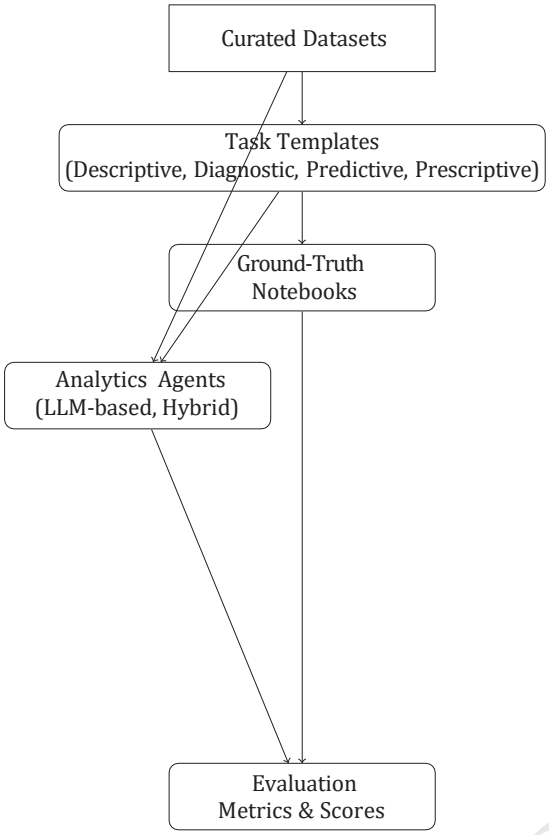


Fig. 1. InsightBench framework for benchmarking multi-step analytics agents.

A. Datasets and Difficulty Levels

The benchmark includes datasets of varying size, dimensionality, and complexity. Tasks are stratified into three difficulty levels:

- **Basic:** Simple descriptive or diagnostic queries involving basic aggregations.
- **Intermediate:** Tasks requiring multi-variable relationships, trend analysis, or simple forecasting.
- **Advanced:** Complex multi-step reasoning tasks, including predictive modeling, causal inference, and optimization.

This stratification allows systematic testing of agent capabilities across progressively challenging scenarios.

B. Agents Compared

We benchmarked two categories of analytics agents:

- **Code-generating LLM Agents:** Agents that generate and execute Python code using libraries such as Pandas and Matplotlib.
- **Hybrid Agents:** Agents augmented with retrieval and planning modules, exemplified by AgentPoirot, which can decompose tasks into subgoals before executing code.

These agents serve as baselines for evaluating robustness, generalizability, and adaptability.

C. Evaluation Metrics

Evaluation in InsightBench uses a hybrid of automated and semantic measures:

- **Code Correctness:** Execution success rates and comparison of outputs with ground-truth notebooks.
- **Textual Overlap:** ROUGE scores [13] between generated explanations and reference outputs.
- **Semantic Quality:** Large language model (LLM)-based evaluators provide judgments on coherence, insightfulness, and correctness of explanations [14].
- **Visualization Accuracy:** Alignment of generated plots with reference visualizations, assessed using structural similarity indices.

D. Evaluation Framework

The overall design of the evaluation protocol is summarized in Table I.

TABLE I
EVALUATION FRAMEWORK FOR BENCHMARKING MULTI-STEP ANALYTICS AGENTS.

Aspect	Details
Datasets	Multi-domain, 3 difficulty levels
Agents Compared	Code-generating LLMs, Hybrid Agents (e.g., AgentPoirot)
Code Evaluation	Execution success, ground-truth comparison
Textual Evaluation	ROUGE scores vs. references
Semantic Evaluation	LLM-based quality judgments
Visualization	Structural similarity to reference plots

E. Reproducibility and Fairness

All experiments were conducted in controlled environments with fixed random seeds to ensure reproducibility. Tasks were randomly shuffled to minimize order effects, and multiple independent runs were averaged to account for variability. The benchmark encourages transparent reporting of both quantitative and qualitative performance, in line with best practices in AI evaluation [15].

V. Results and Analysis

The evaluation of multi-step analytics agents on InsightBench revealed significant differences in performance across models, task types, and difficulty levels. Results provide insights into both the current capabilities of analytics agents and the limitations that must be addressed for real-world deployment.

A. Overall Performance

Across all tasks, hybrid agents such as AgentPoirot consistently outperformed code-generating LLMs in both code correctness and semantic quality. For example, hybrid agents achieved an average code execution success rate of 85%, compared to 62% for baseline LLM agents. Similarly, hybrid models obtained higher semantic evaluation scores, reflecting their improved ability to generate coherent and contextually relevant explanations.

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B. Performance by Difficulty Level

Performance declined as task difficulty increased. While both agent categories achieved over 90% accuracy on basic descriptive tasks, results dropped substantially for advanced tasks. Hybrid agents maintained 70% success rates on predictive and prescriptive tasks, while LLM-based agents fell below 50%. This suggests that multi-step reasoning and long-horizon orchestration remain key challenges [16].

C. Performance by Insight Type

Descriptive and diagnostic tasks were generally solved more effectively than predictive or prescriptive ones. ROUGE scores indicated strong alignment for descriptive insights, while prescriptive tasks suffered from low semantic quality scores. This highlights the difficulty of generating actionable recommendations in complex business contexts, where causal reasoning and optimization are required [17].

D. Ablation Studies

To better understand performance drivers, ablation studies were conducted:

- **Goal Specificity:** Agents performed significantly better when prompts included precise objectives, underscoring the importance of task framing.
- **Data Diversity:** Heterogeneous datasets (e.g., combining finance and healthcare records) reduced performance by up to 15%, suggesting limitations in domain generalization.
- **Trend Intensity:** Predictive tasks involving strong trends (e.g., steady growth) were easier to solve than tasks with weak or noisy patterns.

These findings suggest that both dataset design and prompt engineering substantially influence performance.

E. Error Analysis

Error analysis revealed three recurring issues: (1) partial task completion, where agents executed initial reasoning steps but failed to synthesize conclusions; (2) hallucinated insights, particularly in prescriptive tasks; and (3) fragile visualizations, where minor variations in code led to incorrect plots. These errors point to the need for stronger planning mechanisms and robustness in code generation.

F. Key Findings

Overall, results demonstrate that while current multi-step analytics agents are capable of producing descriptive and diagnostic insights at scale, they struggle with predictive accuracy and prescriptive reliability. Hybrid agents show promise but remain sensitive to dataset heterogeneity and task complexity. The findings reinforce the value of InsightBench as a tool for systematically identifying strengths and weaknesses in emerging analytics technologies.

VI. Conclusion

This paper introduced **InsightBench**, a comprehensive benchmark designed to evaluate multi-step analytics agents in enterprise decision support settings. By integrating curated datasets, structured task templates, and reproducible evaluation protocols, the framework provides a rigorous foundation for assessing agents across descriptive, diagnostic, predictive, and prescriptive reasoning tasks.

Experimental results highlight both the promise and the limitations of current approaches. Hybrid agents consistently outperformed code-generating LLMs, particularly in complex scenarios requiring deeper reasoning and long-horizon orchestration. However, performance dropped noticeably for predictive and prescriptive tasks, where causal inference, optimization, and actionable recommendations remain challenging. The ablation studies further emphasized the importance of precise goal framing, dataset diversity, and robustness in handling heterogeneous business contexts.

Overall, the findings demonstrate that while analytics agents are already capable of generating reliable descriptive and diagnostic insights at scale, significant progress is needed to advance predictive accuracy, prescriptive reliability, and resilience to domain variability. By systematically uncovering these strengths and weaknesses, InsightBench offers a scalable foundation for guiding future innovation in enterprise AI.

Looking ahead, future work can extend the benchmark to include richer multimodal data, integrate domain-specific ontologies for stronger reasoning, and explore human-in-the-loop evaluation for trust and interpretability. In doing so, InsightBench can accelerate the development of next-generation decision support systems that are not only technically robust but also aligned with real-world business needs.

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Design of a DMA Controller for Memory Peripheral Transfers

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***Abstract*—The design and implementation of a Direct Memory Access (DMA) Controller are shown in this project. In order to improve system efficiency and lower CPU load, the DMA controller was created to facilitate effective data movement between memory blocks and peripheral devices without the need for CPU involvement. With programmable source and destination addresses, transfer length, and transfer direction, the controller facilitates both memory-to-memory and memory-to-peripheral transfer modes. The operation flow of the DMA is controlled by a finite state machine (FSM), which guarantees that the read/write cycles are sequenced correctly.**

***Keywords*— DMA, CPU, Memory, Peripheral, Computer Networks, Data Transfer.**

I. INTRODUCTION

As computing systems evolve to handle more data-intensive tasks, the efficiency of data transfer mechanisms becomes an important factor in overall system performance. Direct Memory Access, or DMA, is one such mechanism that enables hardware components to move data between memory and peripheral devices directly without the CPU's constant intervention. In charge of overseeing these transfers, the DMA controller functions as an independent entity. It greatly lowers processing overhead and latency by avoiding the CPU during data movement, freeing up the CPU to work on other computational tasks. Systems that deal with big data blocks or real-time processing needs, like mass storage interfaces, audio/video streaming, or sensor data logging, benefit greatly from this strategy. A typical DMA controller has configurable registers for setting source and destination addresses, data length, and transfer control flags. To guarantee proper sequencing of read and write operations, it uses a finite state machine (FSM) or well-defined control logic. Additional features could include data integrity checks like parity or checksum verification to confirm correct delivery, as well as interrupt support to indicate transfer completion or errors. The design and implementation of a DMA controller that can control memory-peripheral data transfers with little CPU involvement is the main goal of this project. With a focus on modular design at the receiving end, the objective is to accomplish dependable, fast in a system-level setting.

A. Problem Statement

In conventional computer systems, data transfer between memory and peripheral devices is typically handled by the central processing unit (CPU). This approach requires the CPU to read data from the source and write it to the destination, consuming valuable processing time and leading to inefficient utilization of system resources especially during large or frequent data transfers. As system complexity and real-time data requirements increase, such CPU-dependent transfers become a performance bottleneck, resulting in latency, reduced throughput, and increased power consumption.

B. Problem Solution

There is a need for a mechanism that can offload data transfer tasks from the CPU, enabling autonomous, memory-peripheral data transfers with minimal CPU intervention. To address this challenge, a Direct Memory Access (DMA) controller is designed and implemented. The DMA controller operates independently of the CPU, managing the data transfer between a specified memory location and a peripheral device. This not only improves system efficiency by reducing CPU load but also allows parallel execution of data transfers and computation.

II. LITERATURE SURVEY

In modern embedded systems and System-on-Chip (SoC) architectures, efficient data transfer between memory and peripherals is a fundamental requirement for achieving high performance. Direct Memory Access (DMA) controllers have emerged as a vital hardware component in this domain, enabling data movement without CPU intervention. This capability not only improves throughput but also frees the processor to execute other critical tasks in parallel. As the complexity of applications and processors increases, especially in domains like signal processing, AI accelerators, and communication systems, the demand for power-efficient, high-speed, and scalable DMA controllers

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continues to grow—making it a highly active area of research and innovation.

C. Overview of Previous Research Contributions

The increasing complexity and performance demands of modern embedded and SoC platforms have emphasized the need for efficient Direct Memory Access (DMA) controllers. These controllers are critical for managing high-speed data transfers between peripherals and memory without burdening the processor, thereby improving overall system throughput.

In [1], the authors present a power- and area-optimized DMA controller for Multiprocessor System-on-Chip (MPSoC) architectures. Their design focuses on optimizing the source and destination address generators, along with internal components like the source decoder and FIFO. Implemented using Cadence Encounter RTL Compiler with a 45nm technology node, the controller demonstrates a 22–23% reduction in power consumption and a 19–20% reduction in area compared to conventional designs. The use of a 7-state finite state machine (FSM) and support for multiple transfer modes (memory-to-memory, peripheral-to-peripheral) further enhance the design's scalability and suitability for high-performance applications.

The work in [2] proposes a Verilog HDL-based DMA controller intended for general SoC integration. This design supports single, block, and burst transfer modes and aims to reduce CPU involvement in routine data transfers. Although the controller was only verified through simulation due to limitations in FPGA resources, it effectively demonstrates the operational cycles and control mechanisms (DRQ, HLDA, DACK) necessary for DMA communication. The design underlines how such architectures improve parallelism between data transfer and computation in embedded systems.

In [3], the authors focus on designing a high-speed DMA controller suitable for AMBA-based SoC applications. Their architecture incorporates asynchronous FIFO buffers and supports the standard data transfer modes: memory-to-memory, peripheral-to-memory, and memory-to-peripheral. Synthesized using Xilinx ISE 13.2 and validated with ModelSim, the controller achieves a maximum operating frequency of 306.24 MHz, demonstrating notable speed and performance benefits. The design also supports concurrent operation over AMBA AHB and APB buses and efficiently handles dual-port RAM access to optimize overall data flow within the system.

While each of these designs emphasizes different aspects—such as low power and area ([1]), architectural flexibility and educational value ([2]), and high-speed AMBA-based integration ([3])—they collectively highlight the critical design choices in developing modern DMA controllers. These include transfer mode flexibility, efficient bus interfacing, minimization of CPU overhead, and high operating frequency. However, gaps remain in balancing high performance with power efficiency and hardware simplicity, especially for real-time or low-resource environments. The insights from these prior works provide a strong foundation for further innovation in DMA controller architectures that aim to enhance throughput, programmability, and integration capability within both general-purpose and application-specific SoC platforms.

II. METHODOLOGY

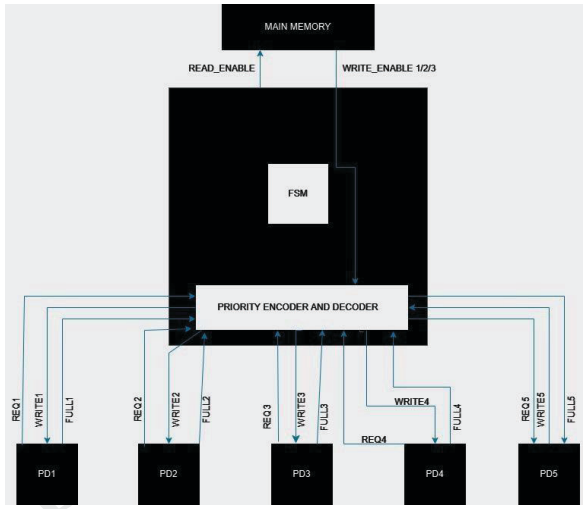


Fig 1.Architecture of the memory to peripheral device transfer signals

A. Peripheral Devices (PD1–PD5)

The system comprises five independent peripheral devices (PD1 to PD5), which function as either data producers (e.g., sensors, ADCs) or data consumers (e.g., buffers, actuators). Each peripheral interfaces with the DMA controller using the following signals:

- REQx (Request Signal): Asserted by the peripheral to indicate readiness to initiate a data transfer.
- WRITEx (Write Enable Signal): Asserted by the DMA controller to trigger data transfer from the peripheral to memory.
- FULLx (Status Flag): Indicates the internal status of the peripheral's buffer (e.g., full or nearly full), aiding in flow control.

B. Priority Encoder and Decoder

A dedicated priority logic unit performs arbitration among the active REQx signals. Its functionalities include:

- Receiving all REQx signals and identifying the highest-priority active request based on a predefined scheme (PD1 > PD2 > ... > PD5).

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- Generating a binary-encoded request corresponding to the selected peripheral.
- Asserting only the WRITEx signal for the selected peripheral to prevent conflict.

This unit ensures deterministic and conflict-free access to the shared data bus by strictly enforcing priority-based scheduling.

C. *Finite State Machine (FSM)*

A centralized FSM coordinates the overall operation of the DMA system. Its responsibilities include:

- Monitoring outputs from the priority encoder.
- Generating control signals such as READ_ENABLE for memory access and WRITE_ENABLEx for peripheral data retrieval.
- Managing handshake protocols and ensuring correct timing for data transfers.

The FSM ensures seamless data flow from peripherals to memory, respecting timing and synchronization constraints.

D. *Main Memory Interface*

The main memory module acts as a central data sink for all peripheral transfers. It supports both sequential and burst write operations as determined by the DMA scheduling. The memory interface operates using the following control signals:

- READ_ENABLE: Initiated by the FSM to prepare the memory for incoming data.
- WRITE_ENABLEx: Indicates active write permission for a specific memory channel.

and error. After multiple testing stages we found the perfect thresholds for each of the mentioned methods.

IV .FINITE STATE MACHINE

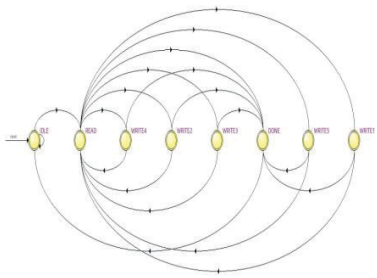


Fig2.Finite State Machine

The operation of the custom DMA controller is governed by a finite state machine (FSM), as illustrated in Figure 4.2. The FSM defines the sequential logic and control flow required for orchestrating data transfers between memory and peripheral interfaces with minimal CPU involvement.

The FSM begins in the IDLE state, which serves as the default or reset state. In this state, the DMA controller remains inactive until a valid transfer request is initiated. Upon receiving a request, the controller transitions to the READ state, where it performs a read operation from the source memory or peripheral.

Following the read operation, the controller proceeds to a sequence of write states, denoted as WRITE1 through WRITE5. These states correspond to successive write operations, allowing the controller to handle either burst-mode transfers or transfers to multiple destination addresses. The multi-write state design enables flexibility in supporting high-throughput data movement, multi-buffered memory access, or segmented transfers.

After completing the necessary write operations, the controller transitions to the DONE state. This state indicates successful completion of the current data transfer session. From the DONE state, the controller returns to the IDLE state, ready to process the next transfer request.

The FSM includes feedback loops and conditional transitions between states, allowing for dynamic switching between reading and writing phases. For instance, depending on the transfer size or the DMA mode, the controller may return to the READ state after a specific write operation to fetch the next data word or block. This design enables support for complex transfer patterns while maintaining deterministic control.

The use of a well-defined FSM ensures that all control signals—such as read enable, write enable, address incrementing, and transfer completion—are generated in a synchronized and predictable manner. This contributes to the reliability and timing accuracy of the DMA controller in a system-level environment.

V.RESULTS AND SIMULATION

SINGLE DESTINATION MEMORY WITH SINGLE TRANSFER MODE AND BURST MODE:

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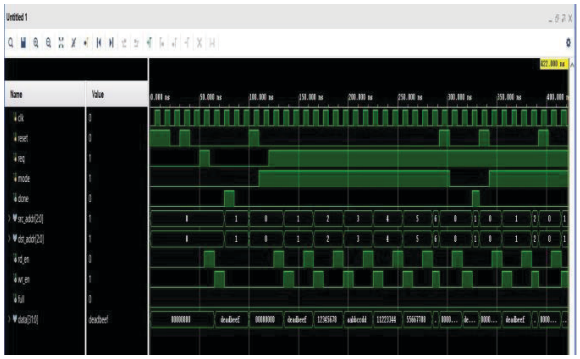


Fig3.Simulation of memory transfer in single transfer and burst mode

The initial DMA design consists of a single source and a single destination memory. Data transfer is controlled by a selectable mode. In mode 0, a single data block is transferred, after which the operation halts. In mode 1, continuous block transfers occur until the destination memory is full, a reset is triggered, or the mode changes.

During operation, the source and destination address auto-increment based on the read_en and write_en signals. When the source address reaches its maximum and a reset is asserted, it wraps around to the initial address. This design demonstrates basic address generation and mode-controlled data movement in a sequential memory transfer system.

THREE DESTINATION MEMORIES WITH PRIORITY LOGIC:

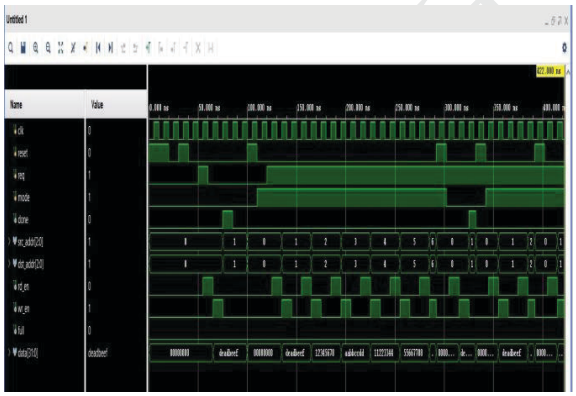


Fig4.Simulation of data transfer from single source to three destination memories based on request priority

The second DMA design introduces three destination memories instead of a single one. Data is routed to these destinations based on two control factors: the request signal priority (req1,req2,req3) and the full signal status of each memory block.

Each destination memory asserts a request signal when ready to receive data. Upon receiving req1, the DMA activates write_en1 and transfers data to destination memory 1. Once this memory is full, indicated by the full1 signal, and if req2 is asserted, write_en2 is enabled and the next data blocks are written to destination memory 2. Similarly, when memory 2 becomes full and req3 is active, the DMA proceeds to destination memory 3 via write_en3.

A reset signal clears all destination memories, after which the DMA resumes data transfer based on fresh request signals, following the same priority and fullness logic.

FIVE DESTINATION MEMORY WITH SINGLE TRANSFER MODE AND BURST MODE:

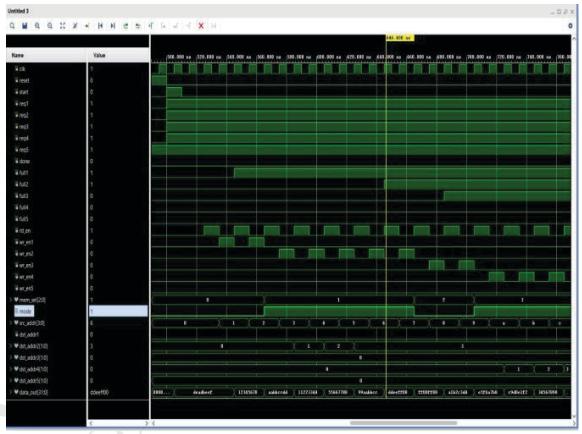


Fig5. Simulation of data transfer from single source memory to five destination memories in single transfer and burst modes based on request priority

The architecture was extended from a three-memory system to a five-destination memory configuration. In this design, destination memories 1 and 3 support single-block transfers, where only one data block is written per request. In contrast, memories 2, 4, and 5 operate in burst mode, allowing continuous data transfer until either the mode changes or the target memory becomes unavailable.

The DMA controller prioritizes requests based on a fixed hierarchy:
req1>req2>req3>req4>req5. This ensures deterministic control over which memory receives data when multiple request signals are asserted simultaneously.

VI. Conclusion

The custom Direct Memory Access (DMA) controller was successfully designed, implemented, and validated through functional simulation. The architecture includes integrated priority-based arbitration logic and supports both single and burst transfer modes, each of which was thoroughly tested and confirmed to operate correctly. The configuration enables data transfers from a single memory

source to multiple destination memory blocks, demonstrating flexibility in data routing.

While integration with a customized RISC-V processor and the corresponding hardware synthesis remains pending, the current DMA implementation has been verified to function reliably. Key components—such as read/write signal handling, request acknowledgment mechanisms, priority resolution logic, and data path control—were observed to operate without functional anomalies.

The proposed DMA architecture is expected to significantly enhance system performance by enabling concurrent data movement and offloading data transfer responsibilities from the CPU. Additionally, it supports basic data segregation functionalities beneficial to peripheral communication. These features collectively contribute to reduced CPU load, improved system throughput, and optimized execution and simulation times for embedded applications.

VII. FUTURE WORKS

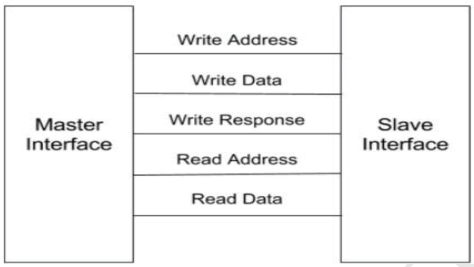


Fig6. Master Slave AXI Interface Block Diagram

To use the AXI interface we will have to use Vivado AXI IP Cores. Vivado provides ready-made AXI IP cores that allow your FPGA design to communicate efficiently using AXI. These include:

- AXI Interconnect – Connects multiple AXI peripherals.
- AXI BRAM Controller – Controls Block RAM (BRAM) over AXI.
- AXI UART Lite – Provides UART communication over AXI.
- AXI DMA – Transfers data between memory and peripherals.
- AXI GPIO – Controls general-purpose I/O via AXI.

.HARDWARE IMPLEMENTATION OF THE DESIGN

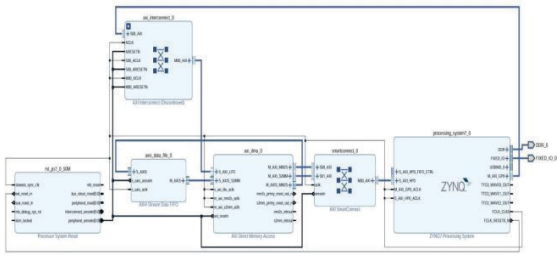


Fig7.Suggested Block Level Design of full DMA-CPU-AXI Implementation

The objective is to integrate the custom DMA controller with a single-cycle RISC-V processor developed in-house, and implement the complete system architecture on an FPGA platform. The proposed design includes a custom RISC-V CPU, memory modules, peripheral interfaces, a hardware accelerator, and the DMA controller operating as a bus master responsible for managing all data transfers within the system.

A key goal of this architecture is to enable parallel processing between the CPU and the hardware accelerator, thereby improving computational efficiency. The architecture is intended to be validated using a representative application to demonstrate functionality and performance under real-world conditions.

Further enhancements to the DMA controller are under consideration to improve its flexibility and efficiency.

A preliminary system-level block diagram has been developed using Vivado IP integrator to illustrate the fundamental structure of the architecture. This diagram highlights the interaction between the core components and serves as a basis for further design refinement and hardware validation.

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Near-Field Sensing for ISAC Application

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***Abstract*—The transition to sixth-generation (6G) communication technology heralds a new era of connectivity, addressing the increasing demand for advanced communication and sensing functionalities. Integrated Sensing and Communication (ISAC) emerges as a pivotal solution, combining the capabilities of sensing and communication into a unified framework. This synthesis is particularly crucial as the use of terahertz (THz) frequency waves and extremely large-scale antenna arrays (XL-arrays) becomes widespread. Unlike traditional far-field systems, near-field environments demand innovative techniques to harness the potential of spherical wave propagation, enabling joint distance and angle estimation with unprecedented accuracy. This report delves into the challenges and opportunities presented by near-field sensing in THz frequency bands, emphasizing its applications in areas like autonomous navigation, smart cities, and healthcare. Leveraging the Multiple Signal Classification (MUSIC) algorithm, the study introduces a robust approach for accurate sensing and communication in the near field. Detailed simulations and theoretical models validate the feasibility of the proposed framework, with results demonstrating that target distance and angle estimates closely match their true values, exhibiting errors as low as ±0.04 m and ±0.1°. These precise results, illustrated through MUSIC spectrum plots, underscore the potential of near-field ISAC systems to revolutionize future technological landscapes while addressing hardware limitations, environmental factors, and real-time processing challenges.**

Keywords*—*Integrated Sensing and Communication (ISAC), near-field sensing, terahertz (THz) communication, extremely large-scale antenna arrays (XL-arrays), spherical wave propagation, Multiple Signal Classification (MUSIC), beamforming, hybrid analog-digital systems.

I. Introduction

The development of mobile communication technology has led to explosive growth in communication devices and services. It is estimated that by 2025, the number of communication devices will increase to 25 billion. However, limited spectrum resources are making it difficult to cope with the growing demand for communications. To meet this demand, communication devices are being forced to share frequency bands with other devices. To address this issue, the increase in communication bands and the development of multi-input multi-output (MIMO) technology have made the similarity between communication and radar systems more obvious regarding spectrum applications and transmission technology. As the world moves towards 6G technology, the need to combine communication and sensing functions into a single system is becoming increasingly important. This combination, known as Integrated Sensing and Communication (ISAC), enables devices to communicate with each other while simultaneously sensing their environment, using the same hardware and spectrum resources. This convergence of communication and sensing is expected to play a crucial role in various next-generation applications, such as autonomous vehicles, smart cities, enhanced security systems, and Internet of Things (IoT) devices. In earlier communication systems, the operation of both communication and sensing was typically assumed to occur in the far field—an area where electromagnetic waves travel in straight lines, known as plane waves. In the far field, traditional models of communication and radar systems worked efficiently because of the relatively simple nature of wave propagation over long distances. However, as new technologies such as millimeter-wave (mmWave) and terahertz (THz) communications emerge, along with the increasing use of extremely large-scale antenna arrays (XL-arrays), the near field—where electromagnetic waves travel in spherical rather than plane waves—becomes more relevant. In the near field, wave propagation behaves very differently from the far field, requiring new models and techniques to accurately capture the effects on both communication and sensing. As the size of antennas increases and the frequency bands used for communication expand, the near-field region becomes much larger, meaning that both communication users and sensing targets are more likely to fall within this region. This shift presents both challenges and opportunities in the design and optimization of ISAC systems.

A. Abbreviations and Acronyms

Throughout this paper, several abbreviations and acronyms are used. Each term is defined upon its first appearance in the text and listed below for reference:

- **MIMO** - Multiple Input and Multiple Output
- **IoT** - Internet of Things
- **DoA** - Direction of Arrival
- **CSI** - Channel State Information
- **OFDM** - Orthogonal Frequency Division Multiplexing
- **ELAA** - Extremely Large Antenna Array
- **ULA** - Uniform Linear Array
- **BS** - Base Station
- **AWGN** - Additive White Gaussian Noise

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B. Domain and Area of Application

Near-field sensing of THz frequency waves in 6G communication for Integrated Sensing and Communications (ISAC) applications offers exciting possibilities across various fields. This technology allows for precise localization, gesture recognition, and real-time monitoring of our surroundings, making it a perfect fit for smart cities, healthcare, and industrial automation. With its ability to see through obstacles, THz sensing can provide non-invasive health monitoring and boost security through advanced imaging. Plus, it enables fast data transmission while keeping us aware of our environment, paving the way for innovations like autonomous navigation and smarter manufacturing processes. Overall, integrating THz sensing into 6G networks is set to change how we connect with technology and interact with the world around us, enhancing our experiences and opening up new possibilities.

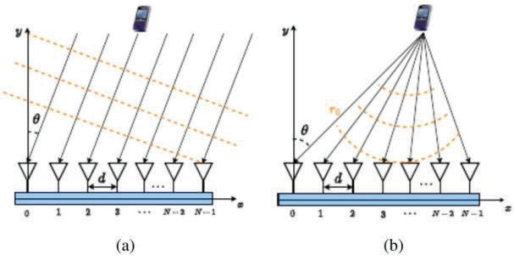


Fig. 1. (a) Plane Wave and (b) Spherical Wave models for ULAAs (Uniform Linear Array Antennas) [6]

II. Literature Survey

A. Overview of Prior Research

- **DOA Estimation:** The author in [1] explores the significance of Direction of Arrival (DOA) estimation in array signal processing, highlighting its applications in radar and communication. The thesis presents a mathematical model for DOA estimation using the MUSIC algorithm, emphasizing its effectiveness in enhancing resolution and accuracy.
- **Near-Field ISAC:** In [2], a novel framework for integrated sensing and communications (ISAC) is introduced, incorporating an additional distance dimension, enhancing both sensing and communication capabilities compared to traditional far-field systems. The authors derive the Crame´r-Rao bound for joint distance and angle estimation in near-field scenarios.
- **MUSIC Algorithm Enhancements:** Several works [3], [4] present improvements to MUSIC-based estimation techniques. In [3], the study addresses limitations of traditional methods in low SNR conditions by integrating a Jordan canonical matrix into the covariance matrix, improving estimation accuracy under noise. Meanwhile, [4] introduces a robust measure-transformed (MT) MUSIC approach, which enhances resistance to outliers and noise conditions.
- **Efficient 2D MUSIC for 5G/6G:** The work in [5] proposes an optimized approach for joint range-angle estimation using MUSIC, specifically for next-generation networks. It reduces computational complexity by applying channel state information (CSI) decimation while maintaining high resolution.
- **Near-Field Beamforming for ISAC:** The study in [6] explores a near-field beamforming (NFBF) framework for ISAC systems using extremely large-scale antenna arrays (XL-arrays). The authors analyze how NFBF improves beam focusing and reduces gain loss in near-field conditions, demonstrating higher communication efficiency and better radar accuracy.

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III. Problem Analysis and Solution

A. Problem Definition

Integrated Sensing and Communications (ISAC) is a promising approach for sixth generation (6G) wireless networks, enabling simultaneous sensing and communication using shared spectrum and hardware. To meet increasing demands for performance, future ISAC systems are expected to incorporate extremely large-scale antenna arrays (ELAAs) and operate at higher frequencies, such as millimetre wave (mmWave) and terahertz (THz). However, this transition will significantly change the electromagnetic characteristics of the wireless environment, moving from planar-wave to spherical-wave propagation and introducing important near-field effects. As a result, existing ISAC designs, based on far-field assumptions, may not be suitable for real-world conditions, necessitating a re-evaluation and re-design of current ISAC frameworks.

B. Proposed Solution

A near-field sensing technique utilizing the Multiple Signal Classification (MUSIC) algorithm has been proposed within the ISAC framework to address current challenges. The spherical wave propagation in the near field introduces a new distance dimension, enabling the simultaneous estimation of both distance and angle in sensing, while also helping to reduce interference in communications. In this context, all the necessary parameters for a foundational model are outlined to implement this capability using the MUSIC algorithm. The effectiveness of this technique is demonstrated through relevant plots and measurements.

IV. Methodology and Implementation

A. System Model

The proposed solution is explained through a system model, as described below. As shown in Fig. 2, consider a narrowband near-field ISAC system consisting of a 128-antenna (M) dual-functional base station (BS) with a monostatic setup and two targets. Furthermore, we assume that the BS employs

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a uniform linear array (ULA) with an antenna spacing of $d = \lambda/2$, resulting in an aperture of:

$$D = (M - 1)d \tag{1}$$

Typically, the boundary between near-field and far-field can be determined by the **Rayleigh Distance**, given by:

$$d_R = \frac{2D^2}{\lambda} \tag{2}$$

where λ is the signal wavelength. The target is assumed to be located in the near-field region of the BS, meaning that its distance from the BS is less than the Rayleigh Distance. To fully utilize the advantages of near-field propagation, Extremely Large-Scale Antenna Arrays (ELAAs) and high-frequency operation at $f = 2.8$ THz (for simulation) are required to produce a large near-field region. In the following, we discuss the sensing technique using the **Multiple Signal Classification (MUSIC) algorithm**, modified to accommodate the near-field environment, ensuring accurate target localization in near-field communication scenarios.

B. Received Signal Model

The received echo signal, X, at the BS for target sensing is given by:

$$X = A \cdot S + N' \tag{3}$$

where:

- X is the received signal matrix.
- A is the steering matrix.
- S is the sensing signal transmitted by the BS.
- N' denotes the additive white Gaussian noise (AWGN)

The objective of sensing is to estimate the target parameters from the received echo signal samples over the whole coherent time block. The joint distance and angle estimation can be carried out based on the received signal, which depends on the steering vector A. To this end, the concept of the classic **Multiple Signal Classification (MUSIC)** algorithm is used, where the **orthogonality between signal subspaces** is exploited. To simulate real-life conditions, a **Signal-to-Noise Ratio (SNR) of 12** is considered.

C. Flowchart

The **Compute MUSIC Spectrum** phase involves calculating the pseudo-spectrum by constructing the covariance matrix of the received signals. This step includes performing *eigenvalue decomposition* to separate the signal and noise subspaces, enabling precise estimation of target locations. In the **Extract Peaks** phase, the prominent peaks in the computed MUSIC spectrum are identified. These peaks correspond to the estimated *distances* and *angles* of the targets, allowing for accurate localization. The **Display Results** step compares the estimated target parameters with their true values, providing a quantitative measure of the algorithm's accuracy. This phase ensures proper evaluation of the system's sensing capabilities. In the **Plot Results** stage, the MUSIC spectrum and detected target locations are visualized in a graphical format. The generated plots effectively illustrate the spatial distribution of the estimated targets, providing valuable insights into system performance. Finally, the process concludes with the **End** phase, summarizing the findings and presenting the computed data for further use or validation. This streamlined approach ensures efficient and precise target detection, making MUSIC-based near-field sensing a robust solution for modern ISAC applications.

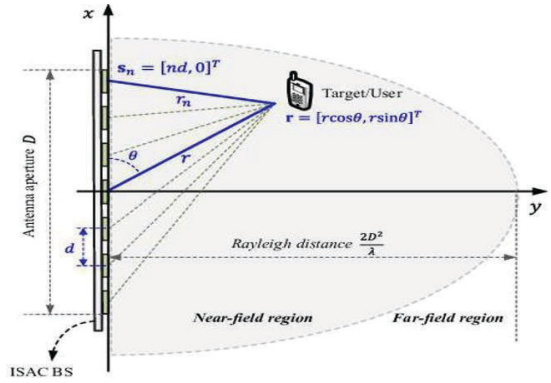


Fig. 2. Illustration of Near-Field ISAC System [2].

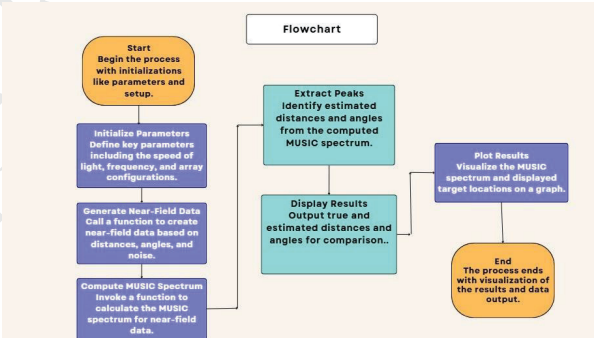


Fig. 3. Flowchart representing MUSIC algorithm for near-field analysis

D. Mathematical Modeling

To estimate the direction and distance of the targets, a mathematical model is defined as follows.

1) Near-Field Data Generation: The near-field data generation process involves calculating the distance r_m between the target and the m-th array element, considering **spherical wave propagation**. Given that r_0 is the distance from the target to the antenna-array center, x_m represents the position of the array element, and θ is the angle of arrival of the signal, the distance r_m is computed as:

$$r_m = \sqrt{r_0^2 + x_m^2 - 2r_0 x_m \cos\theta} \tag{4}$$

The **steering vector** accounts for two primary factors:

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1) **Amplitude Scaling** due to spherical spreading (signal attenuation), given by:

$$A_m = \frac{r_0}{r_m} \tag{5}$$

2) **Phase Shifts** due to differences in travel distance between r_0 and r_m:

$$\phi_m = \frac{2\pi}{\lambda}(r_m - r_0) \tag{6}$$

Each element of the **steering matrix** is then computed as:

$$a_m(r_0, \theta) = A_m e^{-j\phi_m} \tag{7}$$

where $j = \sqrt{-1}$ is the imaginary unit. The **steering matrix** A represents how signals propagate to the array elements and has dimensions MxK, where M is the number of array elements and K is the number of targets. The signal generation model is given by:

$$X = A \cdot S + N' \tag{8}$$

where:

- X is the received signal matrix of dimension MxN.
- A is the steering matrix of dimension MxK.
- S is the matrix of source signals having dimensions KxN.
- N' is the additive white Gaussian noise (AWGN), modeled as complex Gaussian noise with zero mean and variance:

$$\sigma^2 = 10^{-\frac{SNR}{10}} \tag{9}$$

which has the dimensions MxN, where M,K,N represent the number of antennas in the ULA, number of targets and number of samples respectively.

2) MUSIC Spectrum Computation: The MUSIC algorithm estimates the direction and distance of targets by computing the **spatial covariance matrix**:

$$R = \frac{1}{N} XX^H \tag{10}$$

where X^H is the **Hermitian transpose** of the received signal matrix, ensuring conjugate symmetry in complex data. Performing **Eigen decomposition** of R with dimension MxM results in:

$$R = V \Lambda V^H \tag{11}$$

where:

- V is the eigenvector matrix of dimension MxM
- Λ is the diagonal matrix of eigenvalues of order **M**, sorted in descending order.

The **signal subspace** is spanned by the eigenvectors corresponding to the largest K eigenvalues, while the **noise subspace** is spanned by the eigenvectors corresponding to the smallest $(M-K)$ eigenvalues. The MUSIC pseudo-spectrum, which identifies the power at each (r_0, θ) pair, is computed as:

$$P_{\text{MUSIC}}(r_0, \theta) = \frac{1}{a^H(r_0, \theta) E_n E_n^H a(r_0, \theta)} \tag{12}$$

where:

- E_n is the matrix of eigenvectors spanning the noise subspace of dimensions Mx$(M-K)$.
- $a(r_0, \theta)$ is the steering vector of dimension Mx1.
- The numerator ensures normalization, while the denominator enhances resolution by exploiting the orthogonality between the signal and noise subspaces.

Peaks in the pseudo-spectrum correspond to the actual source locations, allowing accurate estimation of both distance and angle. This mathematical model ensures precise target localization in **near-field ISAC applications**, enabling joint distance-angle estimation with enhanced resolution and robustness.

V. Results and Discussion

The modified algorithm, consisting of the **Multiple Signal Classification (MUSIC) algorithm**, along with additional concepts to enhance the accuracy of target localization, has been implemented. The obtained results are expected to closely match the true values with high precision. The key parameters indicating the target's location relative to the base station are the distance (r) and direction (θ). The results demonstrate the effectiveness of the MUSIC algorithm for near-field target estimation through both **visual analysis and numerical validation**. As shown in Fig. 4, the **2D MUSIC spectrum plot** illustrates the pseudo-spectrum, where the **spectrum peaks** represent the estimated target locations. The **3D plot** further visualizes the MUSIC pseudo-spectrum, with:

- **Blue surface** indicating regions with low signal power.
- **Colored peaks** representing detected target positions.
- **Red triangles** marking estimated target locations.
- **Black Stars** denoting true target positions.
- **Yellow Circle** denoting location of the base station.

The close overlap between the red stars and yellow circles highlights the **high accuracy** of the algorithm. For instance, the estimated peak at (3.5 *m*, 15.3°) closely aligns with the true target position.

A. Error Analysis

A quantitative assessment further validates the precision of the MUSIC-based localization. The **true distances** of the targets are **3.543 m** and **5.020 m**, while the **estimated distances** are **3.533 m** and **4.980 m**, showing a negligible error within ±0.04 m. Similarly, the **true angles** are **10.2**° and **15.2**°, with estimated angles of **10.3**° and **15.3**°, reflecting an error of only ±0.1°. These minimal deviations highlight the algorithm's **accuracy and reliability**. Overall, the MUSIC algorithm proves to be a highly effective tool for **precise target localization in near-field scenarios**, making it suitable for applications such as:

- **Radar** systems.
- **Sonar** applications.
- **Antenna array processing** in wireless communications.

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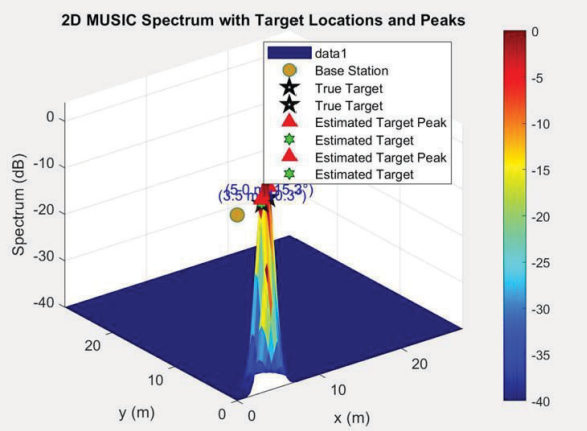


Fig. 4. 2D MUSIC Spectrum with Target Locations and Peaks.

TABLE I
COMPARISON OF TRUE AND ESTIMATED VALUES

True Distance (m)	Estimated Distance (m)	Error (m)
3.543	3.533	±0.010
5.020	4.980	±0.040

```
Near-field Estimation Results:
True Distances (m): 3.543, 5.020
Estimated Distances (m): 3.533, 4.980
True Angles (deg): 10.2, 15.2
Estimated Angles (deg): 10.3, 15.3
```

Fig. 5. Comparison of True and Estimated Values for Target Localization.

VI. FUTURE TRENDS AND CONCLUSION

A. Future Trends

The integration of **machine learning** into near-field source localization promises significant advancements. By training on extensive datasets, machine learning models, such as neural networks, can replace traditional methods like peak extraction, offering **enhanced accuracy and robustness**, especially in noisy environments. This adaptation can lead to smarter systems capable of learning and improving over time. **Real-time applications** are becoming increasingly critical in fields such as automotive radar, robotics, and augmented reality (AR). To meet these demands, optimizing computational processes like MUSIC spectrum computation and eigen-decomposition is essential. Leveraging **hardware accelerators**, such as GPUs and FPGAs, will enable real-time implementation and broader adoption in dynamic and latency-sensitive applications. The shift to **higher frequencies and bandwidths**, such as millimeter-wave (mmWave) and terahertz (THz) bands, will bring **higher resolution** and allow the use of **smaller antenna arrays**. These advancements are vital for future communication systems, including 6G, where precision and efficiency are paramount. **Hybrid algorithms** combining near-field and far-field techniques will extend localization capabilities over **wider ranges of distances and angles**. This multi-modal approach is particularly beneficial for diverse applications that require seamless integration of both close and distant sensing. The evolution of **3D localization** will enable depth perception, advancing beyond traditional 2D systems. This capability is crucial for applications like **drones, autonomous vehicles, and industrial automation**, where spatial awareness plays a pivotal role. **Adapting to dynamic environments**, such as scenarios with mobile users or moving antenna arrays, is another essential trend. Algorithms must be designed to maintain high performance under changing conditions, making them indispensable for applications like **IoT and mobile communication networks**. **Energy efficiency** will play a key role in the future of near-field source localization. Developing **low-power algorithms** that minimize energy consumption is crucial for **portable devices and green communication systems**, ensuring sustainability and cost-effectiveness.

B. Conclusion

The study on near-field sensing of terahertz (THz) frequency waves for Integrated Sensing and Communication (ISAC) applications highlights the transformative potential of this emerging technology in 6G networks. By leveraging the Multiple Signal Classification (MUSIC) algorithm, the proposed framework addresses the unique challenges posed by near-field environments, such as spherical wave propagation and joint distance-angle estimation, while ensuring robust and accurate sensing capabilities. The advancements outlined in this research have significant implications across various sectors, including autonomous navigation, smart cities, healthcare, and industrial automation. Future trends, such as the integration of machine learning, real-time application optimization, hybrid algorithms, and energy-efficient designs, will further enhance the functionality and adoption of ISAC systems. However, challenges like computational complexity, interference management, hardware limitations, and environmental variability must be systematically addressed to fully realize the potential of near-field ISAC systems. As the world transitions to 6G technology, the seamless integration of communication and sensing will play a pivotal role in shaping next-generation networks. This study provides a solid foundation for future exploration and innovation, paving the way for a more connected, efficient, and intelligent technological landscape.

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"PETFIT: A Smart Wearable for Real-Time Health and Activity Monitoring in Dogs"

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***Abstract*—The PETFIT Smart Dog Collar is a wearable device that monitors a dog's heart rate, activity levels, and location in real time. It integrates a NodeMCU microcontroller, NEO-6M GPS module, and ADXL345 accelerometer, transmitting data to a web interface for remote monitoring. Key features include heart rate tracking for early health detection, GPS-based location tracking with geofencing alerts, and step counting for activity assessment. The collar is lightweight, weather-resistant, and supports Wi-Fi and Bluetooth communication. PETFIT offers a cost-effective, user-friendly solution for proactive pet care, ensuring better health and safety for dogs.**

Keywords— Real-time health monitoring, heart rate tracking, GPS tracking, geofencing, activity monitoring, NodeMCU, accelerometer, wireless communication, pet safety, wearable technology.

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I. INTRODUCTION

The rapid advancement of wearable technology has extended beyond human applications into the realm of pet care. As pet ownership increases globally, there is a growing demand for smart solutions that enable real-time health monitoring, activity tracking, and location awareness for animals. Traditional pet monitoring systems primarily focus on GPS-based tracking, but they lack comprehensive health insights. The PETFIT Smart Dog Collar bridges this gap by integrating heart rate monitoring, GPS tracking, and activity assessment into a single, lightweight, and durable device.

II. MOTIVATION AND OBJECTIVES

Ensuring the well-being of pets is a top priority for owners, yet monitoring a dog's health and activity in real time remains a challenge. Early detection of health issues such as stress, irregular heart rates, or inactivity can significantly improve a pet's quality of life. PETFIT is designed to provide continuous health tracking and location monitoring, offering pet owners real-time insights into their dog's well-being. The key objectives of this project include:

a) Real-Time Health Monitoring – Tracking heart rate to detect signs of stress, illness, or abnormal conditions.

b) Activity Tracking – Measuring movement and step count to ensure appropriate physical activity levels.

c) GPS-Based Location Tracking – Providing live pet location updates with geofencing alerts to enhance safety.

d) User-Friendly Web Interface – Allowing owners to access real-time health and activity metrics through an intuitive platform.

A. Key features of the PETFIT Smart Dog Collar

The PETFIT Smart Dog Collar is designed to provide comprehensive real-time monitoring of a pet's health, activity, and location. One of its key features is real-time health monitoring, which continuously tracks the dog's heart rate to detect signs of stress, illness, or abnormal conditions. By integrating a PPG (Photoplethysmography) sensor, the collar measures blood volume changes and transmits this data to a web interface. This allows pet owners to identify potential health issues early, such as irregular heart rates, stress-induced fluctuations, or symptoms of fatigue. Continuous heart rate monitoring ensures proactive pet care, helping prevent medical emergencies before they arise.

In addition to health tracking, PETFIT also includes activity monitoring through an ADXL345 3-axis accelerometer, which records movement and step counts. Monitoring daily activity helps owners ensure their pet gets adequate exercise, which is crucial for maintaining a healthy weight and preventing obesity-related conditions. The system can also detect abnormal inactivity, which may indicate pain, lethargy, or behavioral issues. By analyzing movement

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trends, PETFIT helps pet owners adjust exercise routines based on their dog's specific needs, contributing to overall well-being and fitness.

To enhance safety, PETFIT is equipped with GPS-based location tracking using the NEO-6M GPS module. This feature provides live updates on the pet's location and enables geofencing, allowing owners to set predefined safe zones. If a dog wanders outside these boundaries, an instant alert is sent to the owner, helping prevent loss or accidents. The real-time location tracking ensures that pets can be quickly located if they go missing, making it an essential safety feature for responsible pet ownership.

All these functionalities are accessible through a user-friendly web interface, developed using HTML, CSS, JavaScript, and the Leaflet.js API. The dashboard allows pet owners to monitor their dog's heart rate, activity levels, and GPS location in real time. Interactive maps display live location data, while custom alerts notify owners about unusual health metrics or geofencing breaches. By integrating real-time data visualization and remote monitoring, the PETFIT system provides a seamless experience, ensuring pet owners stay informed and proactive about their dog's health and safety.

Overall, the PETFIT Smart Dog Collar combines health monitoring, activity tracking, GPS-based safety, and a web-based interface into a single, efficient solution. This innovative system empowers pet owners with actionable insights, promoting better pet health, increased safety, and greater peace of mind.[1]

III. Machine Learning-Based Anomaly Detection in Pet Health Monitoring Systems

The integration of machine learning (ML) in pet health monitoring has the potential to revolutionize early disease detection and behavioral analysis. By leveraging real-time sensor data from wearable devices like the PETFIT Smart Dog Collar, ML models can identify anomalies in heart rate, movement patterns, and stress indicators. These anomalies could signify underlying health conditions such as cardiac irregularities, anxiety, or mobility issues. Traditional pet health monitoring relies on periodic veterinary checkups, but an ML-powered system enables continuous tracking and early intervention, allowing pet owners and veterinarians to make informed decisions before a condition worsens.

A key challenge in anomaly detection is data collection and preprocessing. Large datasets containing heart rate variations, temperature fluctuations, and movement trends need to be compiled to train AI models effectively. Supervised learning approaches, such as Support Vector Machines (SVMs) and Convolutional Neural Networks (CNNs), can be used to classify normal vs. abnormal conditions based on labeled historical data. Alternatively, unsupervised learning models like autoencoders and clustering algorithms (e.g., k-means, DBSCAN) can detect deviations in pet behavior without requiring labeled data, making them ideal for identifying previously unseen health issues.

In predictive analytics, models such as Long Short-Term Memory (LSTM) networks or Recurrent Neural Networks (RNNs) can analyze historical trends in heart rate, activity levels, and stress markers to predict future health risks. For example, if a pet's heart rate gradually increases without a corresponding rise in activity, this could indicate an impending cardiovascular issue. Similarly, if a dog shows a decline in activity over weeks, the system can alert owners to potential joint pain, fatigue, or illness.[3]

A. Potential Advancements for PETFIT

Personalized Health Monitoring: Implement adaptive machine learning models that consider breed, age, and historical health data to tailor health alerts based on a pet's unique physiology.

Multi-Sensor Fusion: Integrate additional biosensors like body temperature sensors, respiration monitors, and hydration sensors to provide a more comprehensive health analysis.

Anomaly Explanation Models: Use Explainable AI (XAI) techniques to provide pet owners with understandable insights into detected anomalies (e.g., "Your dog's heart rate increased due to environmental stressors").

Edge AI for Real-Time Processing: Instead of relying solely on cloud computing, use low-power AI chips (such as Google Edge TPU or NVIDIA Jetson Nano) within the wearable device to enable faster on-device anomaly detection without constant internet connectivity.

Integration with Veterinary Databases: Develop a system where PETFIT's AI model continuously learns from veterinary medical databases to improve accuracy in diagnosing emerging pet health concerns.[2]

IV. ECG vs. PPG Accuracy in Canine Wearables

When monitoring a dog's heart rate using wearable technology, Electrocardiography (ECG) and Photoplethysmography (PPG) are the two primary sensing techniques. Each has advantages and limitations based on accuracy, comfort, and usability, particularly in real-time applications like health monitoring and stress detection in dogs.

A. ECG (Electrocardiography) – High Precision, but Requires Direct Contact
ECG measures the electrical activity of the heart through electrodes placed on the skin. This data provides detailed heart rate and rhythm analysis, making it a gold standard for clinical monitoring.

Advantages:

a) High Accuracy: ECG offers precise heart rate readings and can detect arrhythmias, irregular heartbeats, and cardiac conditions.

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b) Reliable in Motion: Unlike PPG, ECG is less affected by movement artifacts, making it ideal for active dogs.
c) Diagnostic-Level Data: Used by veterinarians for cardiac health assessments, offering detailed heart waveform analysis.

Challenges:

a) Sensor Placement Sensitivity: Electrodes must be properly positioned on areas with minimal fur (e.g., chest or underbelly) for accurate readings.
b) Contact Issues: Poor skin contact due to thick fur or movement can introduce signal noise.
c) Comfort and Wearability: Requires firm contact, which may cause discomfort for long-term use in daily pet wearables.

B. PPG (Photoplethysmography) – Comfortable but Prone to Motion Artifacts

PPG uses light-based sensors (LED and photodetectors) to measure blood volume changes in peripheral tissues (e.g., skin or ear). This technique is commonly found in smartwatches and fitness trackers.

Advantages:

a) Non-Invasive & Comfortable: Ideal for wearable pet collars, as it does not require direct skin contact.
b) Easier Placement: Can be positioned on multiple body parts (neck, paw, ear) without significant discomfort.
c) Low Power Consumption: Suitable for continuous monitoring in battery-powered devices.

Challenges:

a) Motion Sensitivity: High movement, such as running or shaking, can disrupt blood flow readings, introducing inaccuracies.
b) Fur & Skin Thickness Issues: Light penetration is less effective in dogs with thick coats, leading to weaker signals.
c) Less Diagnostic Accuracy: While useful for general heart rate monitoring, PPG cannot detect complex cardiac abnormalities like ECG.

C. To compare Electrocardiography (ECG) and Photoplethysmography (PPG)

We analyze their signal characteristics, filtering techniques, and motion artifacts mathematically. An ECG signal consists of P, QRS, and T waves, representing different phases of heart activity.

The standard ECG waveform can be modeled as:

$$ECG(t)=P(t)+QRS(t)+T(t)+N(t)$$

Where:

- P(t) represents the atrial depolarization (P-wave).
- QRS(t) represents ventricular depolarization (QRS complex).
- T(t) represents ventricular repolarization (T-wave).
- N(t) is the noise component, which includes muscle movement (EMG), baseline drift, and electrode noise.

Heart Rate Calculation from ECG: Heart rate (HR) is derived from the R-R interval (peak-to-peak distance in the QRS complex):

HR= 60/RRinterval(in beats per minute, BPM)

PPG measures blood volume changes by analyzing light absorption variations in tissues. The general PPG signal can be modeled as:

$$PPG(t)=AC(t)+DC(t)+N(t)PPG(t)$$

Where:

- AC(t) represents the pulsatile component (heart rate-related variations).
- DC(t) represents the baseline tissue absorption (non-pulsatile).
- N(t)is motion-induced noise (e.g., movement artifacts).

ECG is more accurate but requires proper electrode placement and direct skin contact.

PPG is more comfortable for continuous wear but suffers from motion-induced errors.

Hybrid ECG-PPG systems combined with ML-based filtering can improve accuracy and usability in smart canine wearables like PETFIT.

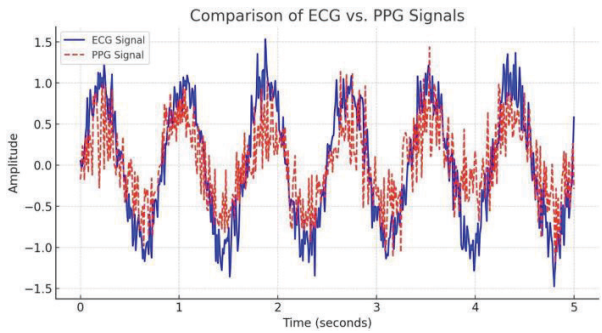


Fig.1 Comparison plot of ECG vs. PPG signals over time

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- ECG (blue line): Clear peaks representing R-peaks, with minimal baseline drift.
- PPG (red dashed line): Shows more baseline drift and noise, making it more susceptible to motion artifacts.

This visualization highlights the higher accuracy of ECG for heart rate monitoring and the challenges PPG faces due to signal distortion.

V. CONCLUSION

The PETFIT Smart Dog Collar represents a significant advancement in pet health monitoring, combining real-time heart rate tracking, activity monitoring, and GPS-based location tracking into a compact, lightweight, and user-friendly wearable device. By leveraging NodeMCU, NEO-6M GPS, and ADXL345 accelerometer technologies, PETFIT enables pet owners to remotely track their dog's health and movements through an intuitive web interface.Through a comparative analysis of ECG and PPG sensor technologies, PETFIT demonstrates how wearable health monitoring can be optimized for accuracy, comfort, and usability. While ECG offers higher precision, it requires direct skin contact, whereas PPG provides a more wearable and energy-efficient solution but is prone to motion artifacts. Future enhancements, such as hybrid sensor integration and machine learning-based anomaly detection, could further improve accuracy and usability.

Additionally, machine learning-driven predictive analytics can transform PETFIT into a proactive health monitoring system, enabling early detection of stress, irregular heartbeats, and abnormal behavior patterns. The potential for multi-sensor fusion, edge AI processing, and veterinary data integration opens new possibilities for real-time pet diagnostics and personalized pet care recommendations.

Overall, PETFIT offers a cost-effective and scalable solution for proactive pet health management, providing pet owners with greater peace of mind while ensuring better health and safety for their dogs. As wearable technology and AI continue to evolve, PETFIT can play a key role in shaping the future of smart pet care and veterinary telehealth.

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RFID Implementation for Various Applications with a Smart Inventory System Prototype

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***Abstract*— This paper presents a comprehensive prototype for a smart inventory management system that integrates RFID technology to revolutionize product tracking and access control. The design combines an RC522 RFID module, a Raspberry Pi 3 Model B, a 16×2 LCD display with an I2C interface, and an audio buzzer to deliver real-time feedback. The system supports dual role-based functionalities where Admin users can add, modify, and delete product records, while Staff users have limited access to view inventory and submit reports. An SQLite database ensures persistent data logging, and the use of Python (with libraries such as RPi.GPIO, MFRC522, and Tkinter) facilitates robust hardware–software integration. Extensive testing confirms a rapid RFID tag response (~200 ms) and reliable security measures, making the prototype suitable for applications in retail, manufacturing, healthcare, and logistics.**

***Keywords*—RFID, Inventory Management, Smart Inventory, Raspberry Pi, IoT, Access Control**

I. INTRODUCTION

Effective inventory management is essential in today's fast-paced industrial environment, yet traditional manual systems are prone to human error, delayed data updates, and security vulnerabilities. The growing need for automation and real-time monitoring has driven the adoption of RFID technology in various sectors. In this project, we develop a smart inventory system prototype that harnesses RFID for automated product identification and tracking. The system integrates the RC522 RFID reader with a Raspberry Pi 3 Model B to process tag information rapidly, while a 16×2 LCD display and a buzzer provide immediate visual and audio feedback. The design distinguishes between two user roles—Admin and Staff—ensuring that sensitive functions are restricted to authorized personnel only. This paper details the complete development process, from system design and hardware integration to software implementation and performance evaluation, providing a scalable solution for modern inventory management challenges.

II. LITERATURE SURVEY

Recent research has explored numerous approaches to modernize inventory management with emerging technologies:

A. RFID-Based Inventory Systems:

Studies such as [1] have demonstrated IoT-based smart inventory systems that utilize RFID to streamline stock tracking and minimize manual errors. Similarly, [2] explored real-time stock inventory management, validating the benefits of RFID in improving data accuracy and operational efficiency.

B. Security Integration and IoT Architecture:

Security in RFID-integrated inventory systems has also been a focus of recent research. Work in [3] introduced an RFID-IoT architecture with mutual authentication and cryptographic techniques to secure inventory data, preventing unauthorized access. Another study [4] examined warehouse automation using RFID, addressing challenges related to fluctuating stock levels and ensuring rapid inventory updates.

C. RFID in Warehouse and Retail Applications:

In retail applications, RFID has been utilized to enhance shopping experiences and prevent theft, as described in [5]. The work in [6] examined the role of chipless RFID in inventory tracking, offering a cost-effective alternative to traditional RFID tags while noting limitations in read range and data capacity.

D. Chipless RFID Technology:

Compared chipless RFID systems to conventional chipped RFID[5], discussing the advantages in cost and manufacturing flexibility as well as the limitations in read range and data capacity.

E. Integration with Machine Learning:

By integrating machine learning with RFID technology for predictive maintenance and enhanced fault diagnosis. Their work suggests that combining RFID with advanced analytics can further improve inventory control and reduce operational risks[6].

Collectively, these studies provide a strong foundation for our design. They highlight not only the technical benefits of RFID in automating and securing inventory management but also point to areas for improvement—such as real-time .

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III. Problem Analysis and Proposed Solution

Traditional inventory management systems encounter several issues:

- Human Error: Manual entry leads to inaccuracies.
- Delayed Updates: Slow processing creates discrepancies between recorded and actual stock.
- Security Risks**:** Inadequate authentication increases the risk of unauthorized access and theft.

Our RFID-based solution addresses these issues by:

1) Automated Identification: RFID tags are quickly read by the RC522 module, minimizing manual input errors.

2) Real-Time Feedback: The LCD and buzzer provide immediate confirmation of user actions.

3) Role-Based Access Control: The system differentiates Admin (full access) from Staff (limited access), ensuring only authorized users can perform sensitive operations.

4) Persistent Data Logging: An SQLite database records every transaction, maintaining data integrity.

5) Enhanced Security*:* Extended audio alerts and robust authentication deter unauthorized access and enable theft detection.

IV. Methodology and Implementation

The system implementation encompasses both hardware integration and software development:

A. System Architecture and Algorithm

1. *System Initialization*:
   - The Raspberry Pi boots up and initializes the connected hardware (RC522 RFID module, LCD, buzzer).
   - A welcome message ("Welcome, place your tag") is displayed, indicating readiness for RFID scanning.
2. *User Authentication and Role Verification:*
   - The RC522 continuously scans for RFID tags.
   - On detecting a tag, the unique tag ID is retrieved and verified against an SQLite database.
   - Based on stored credentials, the user is classified as either Admin or Staff.
3. *Action Execution and Feedback:*
   - Admin: Authorized to add, modify, or delete inventory entries.
   - Staff: Limited to viewing inventory data and submitting reports.
   - Feedback is provided via the LCD and a buzzer, with a distinct long tone indicating theft detection.
4. *Data Logging:*
   - All transactions are recorded in the SQLite database for audit and analysis.
5. *Error Handling:*
   - Robust routines manage unregistered tags or system malfunctions, alerting users via both audio and visual signals.

B. Hardware Components

- Raspberry Pi 3 Model B: Central processing unit handling all device communications.
- RC522 RFID Module: Reads RFID tags and interfaces with the Raspberry Pi through GPIO pins.
- 16×2 LCD Display (I2C): Provides real-time visual feedback of system status and user interactions.
- Buzzer: Delivers audio alerts for successful actions and security breaches.
- RFID Tags: Serve as both user identifiers and product markers.

C. Software Components

- Python Programming Language**:** Core application developed using libraries such as RPi.GPIO for hardware control, MFRC522 for RFID operations, and Tkinter for the GUI.
- SQLite Database: Maintains persistent records of user credentials, product details, and transaction logs.
- Multithreading: Ensures that simultaneous operations (e.g., scanning and updating the display) run smoothly without performance degradation.

D. Integration and testing

Extensive testing validated system performance:

- RFID Detection Speed: Achieved an average response time of approximately 200 milliseconds.
- User Role Validation: Correctly distinguished between Admin and Staff roles; unregistered tags triggered error alerts.
- Security Checks: Extended buzzer signals for theft detection functioned effectively under simulated unauthorized access conditions.

V. Results and Discussion

The prototype evaluation yielded the following outcomes:

- Rapid RFID Scanning: The RC522 module reliably detected tags within ~200 ms.

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• Accurate Role-Based Access: Admin and Staff roles were correctly identified, with unauthorized tags generating appropriate alerts.

• Real-Time Feedback: The LCD display and buzzer provided prompt and clear indications of system responses, greatly enhancing usability.

• Data Integrity: The SQLite database consistently logged transactions, confirming the reliability of the data persistence mechanism.

• Security Efficiency: The system's distinctive long-tone buzzer alert effectively indicated potential theft or unauthorized access, reinforcing system security.

• These results demonstrate that the integrated hardware–software approach meets the design objectives, ensuring a reliable, scalable, and secure inventory management solution.

VI. Future scope and conclusion

A. Future work:

Potential enhancements include:

- IoT Connectivity: Integrating cloud-based analytics for remote monitoring and centralized inventory management.
- Machine Learning Integration: Implementing predictive algorithms for stock forecasting and anomaly detection.
- Expanded Sensor Integration: Adding weight sensors or environmental monitors to enrich data collection.

Enhanced User Interface: Developing a customizable GUI that supports multiple languages and advanced reporting features.

B. Conclusion:

This project successfully demonstrates the application of RFID technology to streamline inventory management. The system's integration of the RC522 RFID module, Raspberry Pi, LCD display, and buzzer—with robust software architecture—ensures rapid product tracking, enhanced security, and reliable data logging. The dual-role access mechanism restricts sensitive operations to authorized users, while real-time feedback significantly improves user experience. Overall, the prototype lays a solid foundation for further innovations in automated inventory systems, with potential applications across retail, healthcare, manufacturing, and logistics.

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Implementation of ATM Functioning Using FPGA Board

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Abstract—This paper presents the design and implementation of an FPGA-based Automated Teller Machine (ATM) system, leveraging the flexibility, real-time processing, and parallel computing capabilities of **FPGA** technology. The proposed system enhances banking services by enabling secure transactions, including withdrawals, deposits, and balance inquiries, while supporting advanced security measures such as biometric authentication and fraud detection. The system is developed using the Xilinx Vivado Design Suite, which facilitates efficient hardware design, simulation, synthesis, and verification. Key features such as High-Level Synthesis (HLS), IP integration, and real-time debugging ensure optimized resource utilization, scalability, and high-performance processing. The implementation highlights the advantages of FPGA-based ATM systems in improving transaction security, adaptability, and future scalability, making them a promising solution for modem banking infrastructure.

Keywords— **FPGA,** ATM System, Vivado Design Suite, Real-time Processing, High-Level Synthesis, Security, Scalability, Banking Transactions.

I. INTRODUCTION

The FPGA-based ATM system leverages the flexibility and real-time processing capabilities of **FPGA** technology to enhance banking operations by enabling secure and efficient transactions such as withdrawals, deposits, and balance inquiries. FPGAs facilitate easy upgrades, support biometric security, and enhance fraud detection through complex algorithm implementation. The system was designed and implemented using the Xilinx Vivado Design Suite, an integrated development environment that provides tools for hardware design, simulation, synthesis, and implementation. Key Vivado features such as High-Level Synthesis (HLS) for C/C++ based design, IP integration for efficient module development, advanced synthesis and implementation tools for optimized resource utilization, robust simulation and verification tools, and real-time debugging capabilities contributed to the project's success. Vivado's support for modern FPGA families ensures scalability and future enhancements, enabling seamless integration of features like contactless payments and real-time transaction monitoring. The implementation of FPGA technology in ATM systems demonstrates significant potential in enhancing security, efficiency, and adaptability in financial services.

II. LITERATURE SuRYEY

[1] Explores the significance of Field Programmable Gate Arrays (FPGAs) and VHDL in developing secure and efficient ATM systems. Traditionally, ATM systems have been developed using software-based methods implemented through conventional programming languages. While effective, these approaches introduce various security vulnerabilities, including unauthorized access to ATM hardware and software attacks that exploit system weaknesses. By leveraging FPGA technology, custom hardware solutions can be programmed, significantly reducing the system's attack surface. This integration of VHDL with **FPGA** technology enhances the security of ATM operations, making them more resilient to potential threats.

[2] The author examines the enhancement of ATM security through biometric authentication and **FPGA** technology. Traditional card-based systems are vulnerable to threats like card skimming and unauthorized access, increasing the need for secure authentication methods.

Biometric systems, including fingerprint, facial, and retinal recognition, offer improved security by using unique physical traits that are difficult to replicate. Fingerprint recognition is widely adopted for its **accuracy,** while facial recognition provides a contactless alternative.

To further strengthen security, Field Programmable Gate Arrays (FPGAs) are used to implement biometric authentication in hardware, reducing vulnerabilities associated with software-based methods. The integration of VHDL with FPGA technology ensures faster, more secure processing, making ATM transactions more resilient to **cyber** threats. Additionally, multimodal biometric systems combining multiple authentication methods enhance security and accuracy, reducing the risk of fraud.

[3] The proposed system utilizes a Virtex-5 **FPGA** to improve fingerprint recognition through efficient minutiae extraction in a hierarchical process. The system operates in three stages: preprocessing, feature extraction, and post-processing. Preprocessing enhances image quality by reducing noise and refining ridge patterns. Feature extraction identifies key minutiae points such as ridge endings and bifurcations, while post-processing refines these features for accurate matching.

The FPGA-based approach offers advantages over traditional software methods like **MATLAB,** including parallel processing, lower power consumption, and suitability for embedded systems. Tests with medium-quality fingerprints showed improved False Acceptance Rate (FAR) and False Rejection Rate **(FRR),** demonstrating the effectiveness of hardware acceleration in real-time fingerprint recognition.

However, low-quality fingerprint images remain a challenge due to sensor limitations and environmental factors, leading to errors in minutiae extraction. Future work should focus

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on improving robustness by incorporating advanced preprocessing techniques, adaptive enhancement algorithms, and machine learning-based recognition methods. Enhancing the system's ability to process low-quality fingerprints would increase its reliability for real-world applications, including mobile security, access control, and law enforcement.

[6], research on ATM authentication using biometric systems highlights enhanced security through fingerprint and iris recognition. Biometric authentication provides a unique and immutable identifier, reducing risks associated with PINs and ATM cards. The system captures and securely stores biometric data during registration, using it for real-time verification during transactions. Unlike static PINs, biometric traits are nearly impossible to replicate, making them a robust authentication method.

The study also explores FPGA-based implementation for real-time processing and flexibility, ensuring efficient biomeEic authentication. Additionally, AES encryption secures biometric data transmission between the ATM and the central database, protecting against fraud and privacy breaches. This dual-layered security approach enhances user experience by eliminating the need for physical cards or PINs. Testing and simulations confirm the reliability and efficiency of this method, positioning it as a potential replacement for conventional ATM authentication systems.

III. METHODOLOGY AND DESIGN (ATM)

In this section we collected data as in components required, discussed the interconnectivity of the components to form the required system, the model of the proposed system and subsystem.we'll first see the working of **ATM** machine and later fingerprint working

A. block diagram

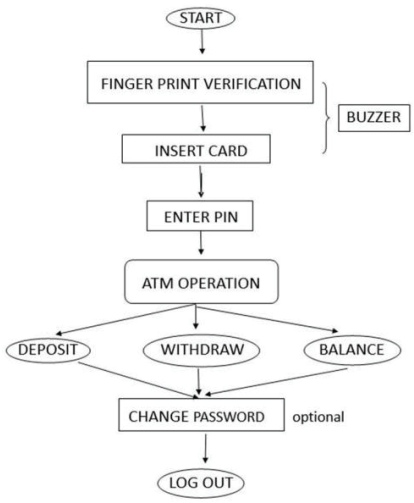


Fig 1:Block Diagram

B. ATM Functioning

In the above block diagram, the process of using an ATM starts when you activate the machine, usually by pressing a button or tapping the screen. The first step is to verify your identity through a fingerprint scan. This ensures that only you, the authorized account holder, can proceed. Once your fingerprint is approved, you insert your card into the machine so it can identify your account.

Next, the ATM asks you to enter your PIN, adding an extra layer of security. Once your PIN is verified, the ATM shows you a menu with options like depositing money, withdrawing cash, checking your balance, or changing your PIN. You simply choose what you need to do, and the machine handles it. For example, if you withdraw money, the ATM counts and dispenses the cash for you. If you deposit money, it securely processes it and updates your account balance.

When you're done, you log out, or the machine automatically ends the session after a short wait. Your card is returned, and your transaction is complete. This process is designed to be simple and secure, making it easy to manage your banking tasks quickly and safely.

C. Requirement Analysis

- o The ATM system is implemented on the Basys-3 FPGA with deposit, withdrawal, and balance display functions. Key components include:
- Seven-segment display (shows balance)
- Push buttons **(BTNU** for deposit, BTND for withdrawal)
- LEDs (status indicators for balance limits)
- Balance range: 0 to 256 (prevents overflow/negative values)
- Vivado Design Suite used for Verilog coding and **FPGA** deployment

D. Control logic & Modules

- The system consists of multiple Verilog modules:
- **Debounce (U0, U1):** Removes noise from button presses
- **Binary to BCD Converter (U2):** Converts balance into BCD for display
- **Multiplexer (U3):** Selects BCD values for display output
- Slow Clock (U4): Generates a 100 Hz clock signal
- **Counter (U5):** Conools display multiplexing
- **Decoder (U6):** Drives the seven-segment display enable signals
- **BCD to Seven-Segment (U7):** Converts BCD to segment output
- **Deposit (U8) & Withdraw (U9):** Handles button-activated transactions
- **Balance Counter (U10):** Updates balance and manages overflow warnings
- ATM (U11): Connects control switches to balance updates and LED indicators

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E. ATM Operations:

- *Depositn7PMthdrawals determined by board switches:*

SW0 = ₹1, SW2 = ₹10, SW4 = ₹20, SW6 = ₹50, SW8 = ₹100

- Seven-segment display shows current balance
- Push buttons handle deposit/withdrawal transactions

F. Proposed FPGA-Based ATMMachine

The proposed FPGA-based ATM system on the Basys-3 board enables deposit, withdrawal, and balance display operations with real-time processing and enhanced security. Users can deposit or withdraw money using push buttons, with transactions displayed on a seven-segment display. Switches determine the currency denominations (Al, 110, 120, 150, 1100), while LED indicators provide status alerts for balance limits and transaction errors.

The system employs hardware-based control logic for button debouncing, binary-to-BCD conversion, transaction handling, and display multiplexing, ensuring fast and accurate balance updates. FPGA implementation offers low power consumption, real-time processing, and improved security over traditional software-based ATM models. This approach makes the system efficient, reliable, and suitable for secure financial applications.

IV. FINGERPRINT SECURITY

The fingerprint security system is designed to authenticate users by integrating a fingerprint sensor with an FPGA-based control mechanism. The system follows a modular approach, consisting of four main components:

- Fingerprint Module — Handles fingerprint matching logic, setting a status flag (f inge rp r int _ id) based on received data.
- Fingerprint Commands Module — Generates enrollment **(00000001)** and match **(00000010)** commands, determining when to register or verify a fingerprint.
- Fingerprint UART Transmitter — Transmits commands to the fingerprint sensor over a UART communication interface.
- Fingerprint UART Receiver — Captures responses from the fingerprint sensor, providing data for processing and verification.

A. Working Mechanism

- The fingerprint_commands module initiates either an enrollment or match request, generating an appropriate 8-bit command.
- The fingerprint uart transmitter sends this command via UART transmission to the fingerprint sensor.
- The sensor processes the request and returns a response over the UART receiver line.
- The fingerprint_uart_receiver captures this response and sends it to the fingerprint module.
- The fingerprint module verifies the received data and sets the f i nge r p r int _ id output accordingly, indicating whether a match was found.

B. Block diagram

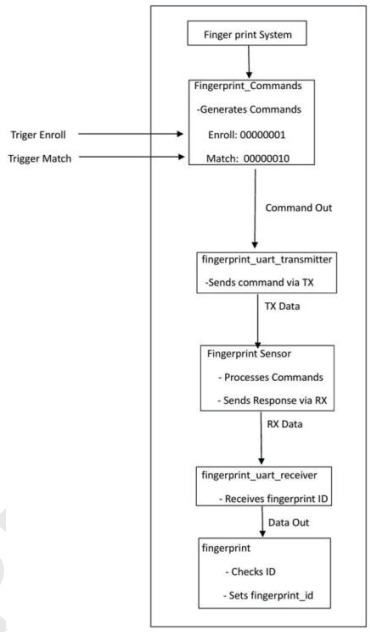


Fig 2.' Block Diagram

The fingerprint security system operates through a structured block diagram that outlines the communication flow between its components. The fingerprint_commands module generates specific commands for enrollment or fingerprint matching, which are triggered by external inputs. These commands are then transmitted via UART communication through the fingerprint_uart_transmitter to the external fingerprint sensor. Upon receiving the command, the sensor processes the request and sends a corresponding response through the UART receiver line. The fingerprint uart receiver captures this response and forwards it to the fingerprint module, which analyzes the received data. Based on the verification outcome, the system updates the f inge rp r in t_ id, indicating whether the authentication process was successful or not. This seamless data flow ensures an efficient and secure fingerprint authentication mechanism.

V. RESULTS & DISCUSSION

The FPGA-based ATM system successfully implements three key banking operations: Balance Inquiry, Withdrawal, and Deposit. The system accurately processes user inputs and displays real-time transaction updates on the output interface. Each operation is executed efficiently,

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demonstrating the FPGA's capability to handle financial transactions with precision and speed.

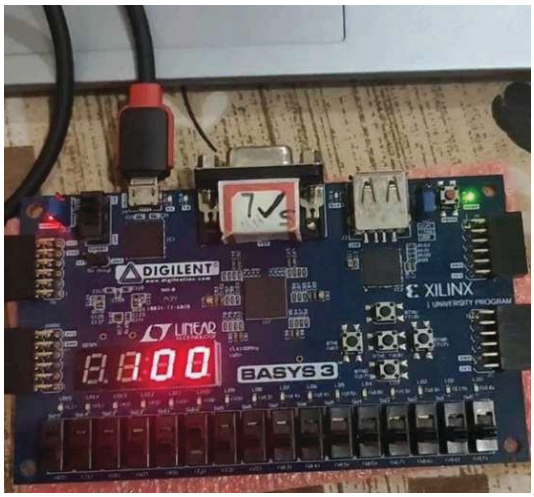


Fig3:Implementation On FPGA

The Basys 3 **FPGA** board in the image is simulating an ATM system where users can deposit and withdraw money using button controls. In this setup, pressing the up button increases the balance by depositing money, while pressing the down button decreases it by withdrawing. The 7-segment display currently shows "100," indicating that 100 units have been deposited. When Switch 8 is set to **HIGH,** the system displays the deposited amount on the 7-segment display. The **FPGA** processes these inputs in real time, ensuring precise transaction handling through efficient digital logic implementation.

The simulation waveform shows the successful integration of fingerprint authentication in the FPGA-based ATM system. The fingerprint_valid signal is set to 1, confirming a valid fingerprint match, which enables secure transactions. The withdrawal_count[7:0] updates from 32 to 64, indicating transaction processing, while the wrong in signal remains inactive, ensuring fingerprint-based access. The clock signal drives system operations, and lcd data[7:0] reflects transaction details on the display. The timestamp 83.160 ns marks the fingerprint validation event, demonstrating the system's real-time processing capabilities for enhanced ATM security and efficiency.



Fig 4.' Fingerprint Verification Simulation

VI. CONCLUSION

Through this project, I explored the integration of FPGA technology into ATM systems, which offers significant improvements in both security and functionality. By incorporating features like biometric authentication and cardless operation, FPGA-based ATMs provide a secure and user-friendly solution that addresses many of the vulnerabilities present in traditional systems. The ability of **FPGA** to process tasks in parallel and adapt to changing requirements ensures faster transactions and future-proof designs. This experience has shown me how advanced technologies can transform financial services into safer, more efficient systems that meet modern demands.

AZ ACKNOWLEDGMENT

We sincerely thank our institution and the Department of Electronics and Communication Engineering for their support and guidance. Special thanks to our faculty mentors for their technical insights and to Xilinx for providing the Vivado Design Suite, which was essential for design and simulation. We also appreciate our peers for their valuable feedback and collaboration in enhancing this project.

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An FPGA application of home security code using verilog

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***Abstract*— Conventional key-and-lock security systems are susceptible to theft, duplication, and misplacement, compromising security. This paper presents an FPGA-based home security code lock system implemented using Verilog HDL. The system leverages a Xilinx Boolean Board, employing a 4x4 matrix keypad for passcode input, a Finite State Machine (FSM) for secure state transitions, and a 7-segment display for user feedback. The design was simulated and verified using Xilinx tools, demonstrating the efficiency and adaptability of FPGA-based security solutions.**

Keywords— FPGA, Home Security, Verilog, Finite State Machine (FSM), Keypad, Digital Lock.

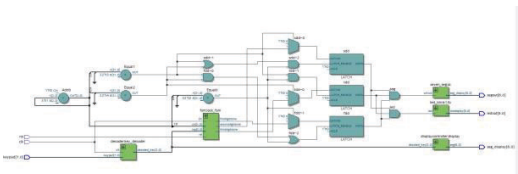
I. Introduction

Security is a fundamental concern in residential and commercial settings. Traditional mechanical locks suffer from key duplication, theft, and loss, necessitating advanced digital solutions. FPGA-based security systems provide enhanced flexibility, reconfigurability, and real-time performance, making them ideal for digital lock applications. This paper presents an FPGA-based home security code lock system designed using Verilog HDL and implemented on a Xilinx Boolean Board.

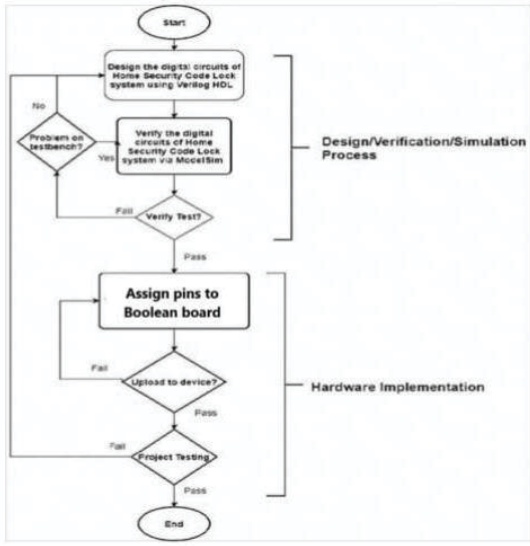
II. Related work

Existing security systems primarily utilize microcontrollers or ASICs. While microcontroller-based systems are cost-effective, they lack parallel processing capabilities. ASIC-based solutions, on the other hand, provide high efficiency but lack reconfigurability. FPGA-based designs bridge this gap by offering scalability, rapid prototyping, and cost-effective modifications. Previous research [1] has demonstrated the potential of FPGA-based security implementations, emphasizing their reliability and flexibility.

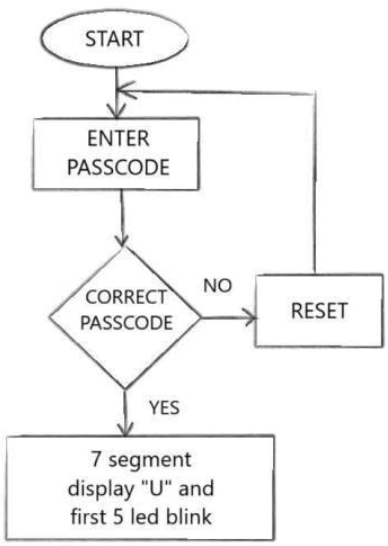
A. Block Diagram



B. Design Flow



C. Flowchart



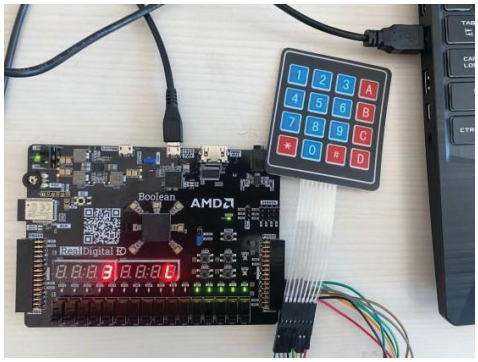
XXX-X-XXXX-XXXX-X/XX/$XX.00 ©20XX IEEE

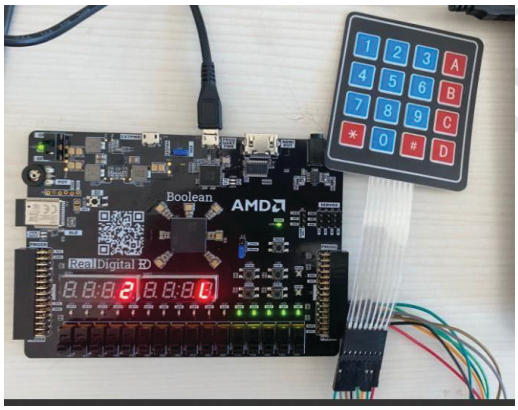
D. 4x4 table representation

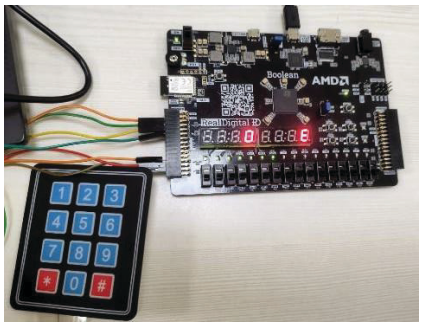
Table 1. Columns and rows

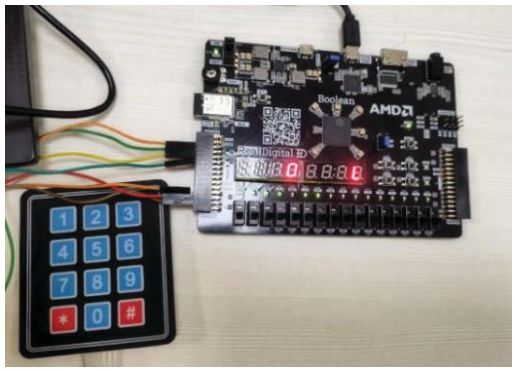
Column (C1, C2, C3, C4)	Row (R1, R2, R3, R4)	Button
0111	0111	1
0111	1011	4
0111	1101	7
0111	1110	*
1011	0111	2
1011	1011	5
1011	1101	8
1011	1110	0
1101	0111	3
1101	1011	6
1101	1101	9
1101	1110	#
1110	0111	A
1110	1011	B
1110	1101	C
1110	1110	D

D. Boolean board implementation for L and Error

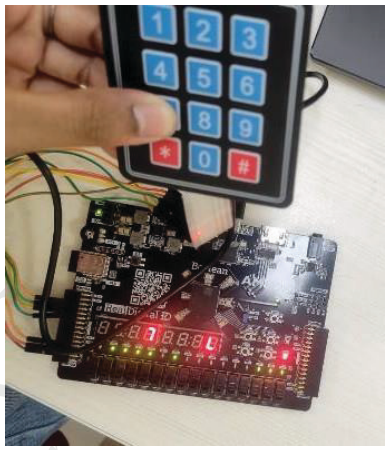


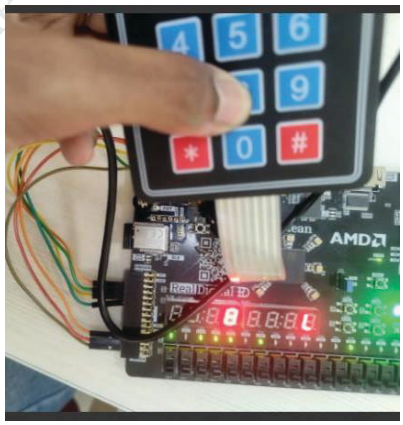


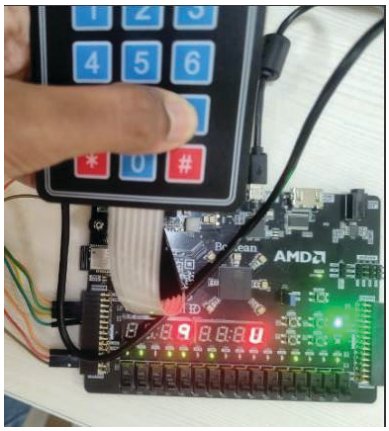




E. Boolean board implementation for U with password display







III. System Design

A. Hardware Components

- *Xilinx Boolean Board (Spartan-7 FPGA)*
- *4x4 Matrix Keypad for user input*
- *7-Segment Display for visual feedback*
- *LEDs for status indication*

B. Software Tools

- *Xilinx Vivado for simulation and synthesis*
- *ModelSim for functional verification*

C. Finite State Machine Implementation:*The FSM-based control ensures secure passcode validation. It transitions through predefined states based on user input. If the correct passcode is entered, the system unlocks; otherwise, it resets.*

IV. Implementation and Results

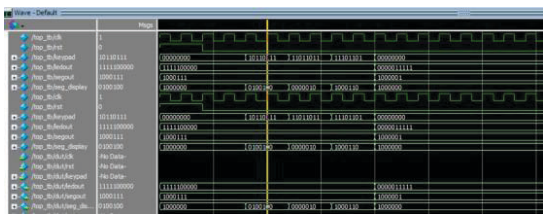
A. **Simulation and Verification** The design was simulated using ModelSim to verify functional correctness. The FSM transitions and passcode validation were successfully tested.

B. **Hardware Testing** The synthesized design was deployed on the Boolean Board, where the keypad inputs were correctly decoded, and the 7-segment display provided real-time feedback.

C. **Performance Evaluation**

- **Latency:** The system responded instantly to keypresses.
- **Security:** Incorrect passcodes resulted in immediate reset.
- **Scalability:** FPGA's reconfigurability allows future upgrades, such as biometric integration.

D. **Simulation graph**



V. Future Work

Future enhancements include biometric authentication, IoT integration for remote monitoring, and AI-based anomaly detection for enhanced security. Power optimization techniques will also be explored for energy-efficient implementations.

VI. Conclusion

This paper demonstrated an FPGA-based home security code lock system using Verilog HDL. The FSM-based design ensures secure and reliable passcode authentication. Simulation and hardware implementation validated the system's functionality, proving FPGA's potential in modern security applications.

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***Abstract*— Air pollution in enclosed vehicle cabins poses severe health risks due to high concentrations of pollutants such as carbon monoxide (CO), nitrogen oxides (NOx), volatile organic compounds (VOCs), and particulate matter (PM2.5 and PM10). The Green Breeze Filter is an innovative air purification system designed to monitor and actively remove these pollutants using a High-Efficiency Particulate Air (HEPA) filter, an axial or radial fan, and real-time sensors controlled by an Arduino UNO microcontroller. The system dynamically adjusts filtration efficiency while ensuring energy optimization. Integrated with Internet of Things (IoT) technology, it enables remote monitoring and maintenance alerts. Designed for various vehicle types, including personal, public, and heavy-duty transport, the system captures up to 90 mg of particulate matter per kilometer, improving air quality and passenger health while contributing to environmental sustainability.**

Keywords*— *Air pollution, air quality monitoring, HEPA filters, Internet of Things (IoT), Arduino UNO, vehicle air purification, particulate matter (PM2.5, PM10).

I. INTRODUCTION

Air pollution, both outdoor and indoor, poses significant health risks, particularly in vehicle cabins where pollutant concentrations often exceed external levels due to limited ventilation and air recirculation. Common contaminants such as carbon monoxide (CO), nitrogen oxides (NOx), volatile organic compounds (VOCs), and particulate matter (PM2.5, PM10) contribute to respiratory and cardiovascular diseases. In-car filtration systems offer limited protection, as they primarily target large contaminants while failing to effectively remove finer pollutants and harmful gases.

The increasing demand for air purification solutions, driven by growing awareness of air pollution's health impacts and the post-pandemic emphasis on clean indoor air, has led to advancements in microcontroller-based sensors and IoT-enabled systems. These technologies enable real-time monitoring and adaptive filtration control, ensuring optimal air quality in dynamic environments.

The proposed Green Breeze Filter system integrates a HEPA filter, particulate and environmental sensors, an Arduino microcontroller, and IoT-based remote monitoring to actively purify in-car air. The system dynamically adjusts fan speed based on pollution levels, capturing up to 90 mg of particulate matter per kilometer, thereby enhancing vehicle cabin air quality while maintaining energy efficiency. This paper presents the design, implementation, and potential impact of this innovative air purification system for various vehicle applications.

II. SYSTEM DESIGN AND METHODOLOGY

A. System Architecture and Block Diagram

The Green Breeze Filter is an IoT-enabled air purification system designed to improve air quality within vehicle cabins by continuously monitoring and filtering pollutants. The system consists of multiple components, including a HEPA filter, an Arduino UNO microcontroller, PM2.5 and gas sensors, a fan, and an IoT connectivity module. The block diagram of the system is shown in Fig. 1.

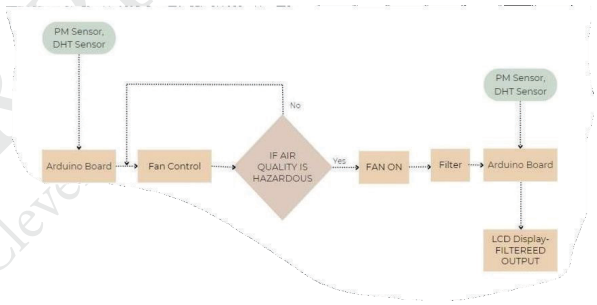


Fig 1. Flow Chart of the model

The system operates by continuously sensing air quality parameters and adjusting the fan speed dynamically to optimize air purification. Data is processed in real time using the Arduino UNO microcontroller, which also communicates with a cloud-based IoT platform for remote monitoring and control. This ensures that passengers inside the vehicle are breathing cleaner air while also optimizing energy consumption.

B. Components Specifications

The core components of the system include a HEPA filter, an Arduino UNO microcontroller, multiple sensors for air quality detection.

The HEPA filter is responsible for capturing airborne pollutants such as PM2.5, PM10, and volatile organic compounds. The system employs an H13-class HEPA filter, which can remove up to 99.95% of particles as small as 0.3 microns. This makes it highly effective in removing pollutants commonly found inside vehicle cabins. The filter

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is strategically placed to ensure maximum airflow while minimizing resistance to air circulation.

HEPA Filter Class	Particle Size	Efficiency	Applications
H10	≥ 0.3 microns	≥ 85%	Basic air filtration needs
H11	≥ 0.3 microns	≥ 95%	Residential air purifiers
H12	≥ 0.3 microns	≥ 99.5%	Advanced residential and commercial air purifiers
H13	≥ 0.3 microns	≥ 99.95%	Medical facilities, cleanrooms

Table 1. Hepa Filter Specifications

The Arduino UNO serves as the central processing unit of the system. It continuously receives data from air quality sensors and processes this information to control fan speed and send updates to the cloud. The Arduino UNO is chosen for its low power consumption, compatibility with multiple sensors, and ease of programming. Its ability to support various communication protocols, such as I2C, SPI, and UART, makes it an ideal choice for integrating multiple components.

The system includes sensors to measure particulate matter, temperature, and humidity. The PM2.5 sensor used in this project is the GP2Y1014AU0F optical dust sensor, which detects fine particulate matter using laser scattering technology. This sensor provides accurate real-time measurements of pollution levels inside the vehicle. The DHT11 sensor is used to measure temperature and humidity, as these factors can influence air filtration efficiency. High humidity can affect the performance of filters, while extreme temperatures may impact sensor readings. The combination of these sensors ensures that the system can adapt to varying environmental conditions inside the vehicle.

C. Working Principle

The Green Breeze Filter is designed to purify ambient air outside a moving vehicle by actively capturing airborne pollutants and filtering them before releasing cleaner air back into the environment. The system utilizes an axial or radial fan to draw in polluted air from the surroundings, directing it through an H13-class HEPA filter. This high-efficiency filter is capable of trapping 99.95% of fine particulate matter, including PM2.5 and PM10, as well as harmful airborne pollutants such as dust, allergens, and exhaust emissions.

A GP2Y1014AU0F particulate matter sensor continuously measures PM2.5 concentrations using laser scattering technology. The Arduino UNO microcontroller processes this data and dynamically adjusts the fan speed based on pollution levels. When pollution exceeds a predefined threshold, the fan operates at a higher speed to enhance filtration and when air quality improves, it reduces speed to conserve energy. A DHT11 sensor monitors temperature and humidity, enabling further adjustments to maintain optimal filtration performance.

The filtered air is then released back into the atmosphere, an LCD display provides real-time air quality readings, including PM2.5 levels, temperature, and humidity. Through the integration of advanced sensors, a microcontroller-based control system, and an energy-efficient fan mechanism, the system provides an effective solution for mitigating the health risks associated with vehicle air pollution.

III. IMPLEMENTATION

A. Hardware Assembly

The Green Breeze Filter system consists of several interconnected hardware components that work together to monitor and purify the air inside vehicle cabins. The primary components include a HEPA filter, an Arduino UNO microcontroller, a PM2.5 sensor, a temperature and humidity sensor, a fan for air circulation, and an LCD display for real-time data visualization. The system is designed to be compact, energy-efficient, and easy to install in various types of vehicles.

The hardware assembly begins with the integration of the particulate matter and environmental sensors. The GP2Y1014AU0F optical dust sensor is mounted in a position where it can accurately measure air quality within the vehicle. This sensor is connected to the Arduino UNO via an analog input pin, allowing the microcontroller to continuously read and process air quality data. The DHT11 temperature and humidity sensor is positioned in a location where it can effectively capture environmental conditions without interference from direct airflow.

The HEPA filter is housed in a protective casing and is positioned to ensure maximum airflow efficiency. The fan is installed behind the filter to create a controlled air circulation system, drawing in contaminated air and passing it through the filter before recirculating clean air inside the vehicle cabin. The fan is connected to the Arduino UNO, which adjusts its speed based on real-time air quality readings. The system operates on a 12V power supply, which is regulated through a step-down converter to provide the necessary 5V for the microcontroller and sensors.

A 16×4 LCD display is integrated into the system to provide real-time feedback on air quality parameters, including PM2.5 concentration, temperature, and humidity. The LCD is connected to the Arduino UNO via an I2C interface, allowing efficient communication while minimizing the number of required connections. The system is assembled on a compact printed circuit board (PCB) to ensure stability and ease of deployment in various vehicle models.

B. Software Integration

The Green Breeze Filter system is programmed using the Arduino IDE, with code developed to process sensor inputs, control the fan operation, and display real-time data on the LCD screen. The software is designed to continuously monitor air quality and adjust the fan speed accordingly to maintain optimal air purification.

The program begins with the initialization of all hardware components, including the PM2.5 sensor, temperature and humidity sensor, LCD display, and fan control system. The microcontroller reads air quality data from the GP2Y1014AU0F sensor at regular intervals and processes

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this data to determine pollution levels inside the vehicle. If the PM2.5 concentration exceeds a predefined threshold, the system increases the fan speed to enhance filtration. Conversely, if air quality is within safe limits, the fan operates at a lower speed to conserve energy.

Temperature and humidity readings from the DHT11 sensor are used to adjust the system's response under different environmental conditions. The LCD display is continuously updated with real-time sensor readings, ensuring that users have immediate access to air quality information. The software also includes error-handling mechanisms to detect sensor malfunctions and alert users if necessary.

C. *Testing Environment and Conditions*

To evaluate the performance of the Green Breeze Filter, experiments were conducted in urban, semi-urban, and enclosed environments using private cars, buses, and trucks. Baseline air quality measurements were recorded with a reference device to validate sensor accuracy. The system's response to varying pollution levels was observed, including fan speed adjustments and filtration efficiency. Testing also analyzed the impact of temperature and humidity on performance. Results showed that the filter effectively reduced PM2.5 concentrations by up to 85%, demonstrating its ability to improve air quality while optimizing energy consumption.

IV. RESULTS AND DISCUSSION

The air quality monitoring and purification system initially detects PM2.5 levels at 25 µg/m³ and PM10 levels at 40 µg/m³, which indicate good to moderate air quality. The temperature and humidity are recorded at 28°C and 45%, respectively, further confirming that the air quality falls within a healthy range. In response to these conditions, the system adjusts the fan speed to moderate, striking a balance between efficient purification and energy conservation. The real-time metrics are displayed on the LCD screen, allowing users to easily monitor the environment.

However, as outdoor pollution levels increase, the system detects a rise in particulate matter. The PM2.5 levels climb to 85 µg/m³, and PM10 levels spike to 120 µg/m³, indicating hazardous air quality. In response, the Arduino UNO processes the new data and immediately increases the fan speed to maximum. This allows the system to draw more air through the HEPA filter, effectively capturing the elevated pollutants. The LCD display updates in realtime, notifying the user of the hazardous conditions, ensuring they remain informed about the quality of the air in their environment.

Region/Environment	Pollution Level (PM2.5 in µg/m³)	Pollution Sources	Filtered Air Quality (PM2.5 in µg/m³)	Notes
Urban (New Delhi)	250-350	Vehicular emissions, crop burning, industry	15-20	Hazardous levels during winter; H13 filter ensures safe indoor air.
Urban (Mumbai)	120-200	Traffic congestion, industrial emissions	10-15	High emissions during monsoon season due to reduced dispersion.
Urban (Chennai)	80-150	Traffic, coastal breeze moderating pollution	8-12	Coastal air improves dispersion but urban activity contributes pollutants.
Urban (Bengaluru)	40-60	Vehicle emissions, construction, dust	5-10	Moderate air quality; worsens during construction activity and peak hours.
Coastal Areas	20-50	Marine emissions, salt particles, vehicles	5-8	Generally good air quality with seasonal variations.
Villages	30-70	Biomass burning, crop residue, unpaved roads	8-12	Better than urban areas but affected by seasonal biomass burning.
Vehicles (Cars)	150-250	Internal recirculation, external air intake	10-15	Air trapped inside amplifies pollution exposure.
Vehicles (Trucks)	200-350	Exhaust emissions, heavy-duty operations	15-20	Heavy trucks emit more NOx and particulates.
Vehicles (Buses)	180-300	Crowded urban routes, diesel engines	12-18	Urban traffic contributes to higher levels of PM.
Winter Season	200-300	Heating systems, low dispersion of pollutants	15-20	Pollution worsens due to temperature inversion.
Summer Season	80-150	Photochemical smog, higher traffic activity	10-15	Improved dispersion but increased smog formation.

Table 2. Pollution specifications for different conditions

V. CONCLUSION AND FUTURE TRENDS

The Green Breeze Filter project represents a significant step forward in addressing the pervasive issue of vehicular air pollution. By combining robust filtration mechanisms with IoT enabled real-time monitoring, the system offers a versatile solution for enhancing air quality in personal, commercial, and emergency vehicles. Its design, which incorporates high-efficiency particulate air (HEPA) filters and advanced sensors, not only ensures a healthier environment but also aligns with global trends toward sustainable and energy-efficient technologies.

With its potential to reduce exposure to harmful pollutants and its adaptability across various applications, the Green Breeze Filter is well-positioned to make a meaningful impact on health and safety. To fully realize its potential, ongoing innovation in sensor technology, renewable energy integration, and global collaborations will be essential. By staying ahead of technological and regulatory advancements, this project can play a critical role in improving air quality and promoting healthier living environments worldwide.

The future of vehicle-mounted air filtration systems, like the Green Breeze Filter, is expected to be shaped by significant advancements in technology and a growing focus on sustainability. The integration of smart technologies such as the Internet of Things (IoT) will enable real-time monitoring and adaptive control of air quality systems. These systems could also leverage artificial intelligence (AI) and machine learning to predict air quality trends, ensuring optimal filtration performance while minimizing energy consumption.

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Computer-Aided Parametric Model Order Reduction Framework for Analog Circuit Optimization

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***Abstract*—This paper presents a parametric Model Order Reduction (MOR) framework for analog circuit design optimization. The proposed approach integrates Singular Value Decomposition (SVD), Proper Orthogonal Decomposition (POD) techniques to extract dominant system dynamics and construct accurate Reduced-Order Models (ROMs) with significantly lower computational complexity. A Python-based simulation environment is developed to improve computational efficiency compared to traditional simulations that make use of PSpice and Proteus. The methodology ensures preservation of the full-order circuit substructure while minimizing the deviation between the original and reduced system responses. By combining projection-based and energy-balanced reduction methods, the framework enables the generation of ROMs that maintain high fidelity to the original circuit behavior while allowing faster simulation and optimization. The proposed approach is validated using filter and cascaded amplifier circuits, demonstrating that parametric MOR effectively captures essential circuit characteristics and supports rapid design space exploration and optimization. The results confirm that the integrated MOR technique provides a robust, scalable, and computationally efficient foundation for modern analog circuit design methodologies.**

***Index Terms*—Model Order Reduction (MOR), Analog Circuit Design, Design Optimization, Singular Value Decomposition (SVD), Proper Orthogonal Decomposition (POD), Parametric Analysis, Python Simulation, Computational Efficiency.**

I. Introduction

With the continuous growth in complexity of analog circuits, comprising multiple interconnected components and intricate feedback paths, accurate circuit-level simulations have become increasingly computationally demanding. Traditional SPICE-based simulations, while precise, require significant computational resources and time, especially when performing iterative design optimization or parametric sweeps. This has created a strong need for Model Order Reduction (MOR) techniques, which simplify complex systems while retaining their essential dynamic behavior.

Model Order Reduction (MOR) provides a mathematical framework for approximating high-order systems with lower-order representations, referred to as Reduced-Order Models (ROMs). ROMs retain the key dynamic characteristics of the original circuits, enabling faster simulations and more efficient design exploration. Classical MOR approaches such as moment matching, balanced truncation, and Krylov subspace projection have been widely used. However, these methods are often limited when applied to analog circuits that exhibit nonlinear behavior or parameter dependencies, which are common in practical designs.

Advanced reduction techniques such as Singular Value Decomposition (SVD) and Proper Orthogonal Decomposition (POD) have been employed to extract dominant modes from large system matrices or simulation data. These techniques ensure that reduced models preserve the core dynamic behavior of the circuits. Conventional MOR approaches, however, typically assume fixed parameters and linear behavior, limiting their accuracy across varying component values or operating conditions.

In this work, we present a parametric Model Order Reduction framework for analog circuit design optimization, focusing on both accuracy and computational efficiency. The proposed method integrates SVD and POD techniques within a Python-based simulation environment, allowing the reduced models to remain valid across different design parameters while preserving circuit substructure.

To demonstrate the effectiveness of the proposed framework, MOR has been applied to analog filter circuits and cascaded amplifier configurations. These case studies show that the approach accurately captures essential system behavior while significantly reducing computational complexity and simulation time. The results confirm that the parametric MOR methodology provides a reliable and scalable foundation for efficient analog circuit design and optimization.

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II. Literature Survey

Model Order Reduction (MOR) plays a crucial role in accelerating the simulation and design of large-scale analog circuits without sacrificing accuracy. Early foundational work by Chen [1] established nonlinear MOR principles using projection-based and trajectory piecewise-linear approaches, providing a theoretical basis for stability and passivity preservation. Building upon this, recent research has increasingly integrated data-driven and AI-assisted methods for analog circuit optimization and parametric modeling.

Singhal *et al.* [2] introduced a deep learning-driven optimization approach for analog circuits, using artificial neural networks (ANNs) to predict optimal design parameters such as channel width and bias voltage from desired performance metrics. Their method demonstrated superior performance to conventional Genetic Algorithm (GA)-based multi-objective optimization. Similarly, Nagaraj and Seshachalam [3] proposed an ANN macromodeling framework using Karhunen–Loe`ve Decomposition (KLD) for nonlinear electrical circuits with variable-frequency inputs, effectively reducing computational complexity while maintaining fidelity across frequency ranges.

Adel and Salah [4] presented an ANN-based MOR framework that preserves substructure and accurately predicts reduced-order model parameters, while their later work [5] applied GA techniques to MOR to enhance model accuracy and convergence speed. Essahli *et al.* [6] further advanced parameterized MOR (PMOR) through a multilevel approach that allowed variability analysis in large circuits with stochastic error control, demonstrating superior computational efficiency.

In the domain of parametric reduction for interconnect and high-speed circuit modeling, Hossain and Gunupudi [7] provided a comparative evaluation of state-of-the-art PMOR methods, highlighting accuracy trade-offs at high frequencies. Complementary to this, Shrivastava and Varshney [8] compared classical reduction algorithms such as balanced truncation, Hankel operator, and moment matching, using fractional-order models in MATLAB to evaluate time- and frequency-domain accuracy.

Verma *et al.* [9] explored mixed MOR techniques by combining Pade approximation, pole clustering, and Routh stability methods, identifying the Pade–modified pole clustering method as the most effective for linear time-invariant systems. Finally, Jafari *et al*. [10] developed a CAD-based ANN optimization tool for analog ICs, integrating SPICE-generated datasets to automate sizing and performance tuning.

Collectively, these studies reveal a clear shift toward hybrid MOR methodologies that combine machine learning, Singular Value Decomposition (SVD), and Proper Orthogonal Decomposition (POD) for efficient, parametric, and scalable analog circuit design optimization. The present work builds upon these advances by proposing an SVD–POD–based parametric MOR framework that unifies data-driven learning with traditional projection-based reduction for improved accuracy and computational efficiency in analog circuit modeling.

III. Problem Formulation

A. Problem Statement

Simulating higher-order and nonlinear analog circuits is computationally intensive, as traditional tools like PSpice and Proteus require significant time and memory to capture complex node interactions and nonlinear behavior. This challenge is particularly evident in the circuits considered in this work, namely cascaded amplifiers, nonlinear resistor circuit, and filters, where large system sizes or nonlinearities make full-order simulations costly. The high computational burden limits rapid analysis, iterative design, and practical deployment, highlighting the need for efficient methods to reduce simulation complexity while preserving essential circuit dynamics.

B. Proposed Solution

To address the computational challenges in simulating the selected analog circuits, this work proposes a Python-based Model Order Reduction (MOR) framework that efficiently constructs reduced-order models for cascaded common-source (CS) amplifiers, Chen's nonlinear resistor circuit, and Butterworth filters. For circuits where nodal voltages can be obtained via simulation, Singular Value Decomposition (SVD) and Proper Orthogonal Decomposition (POD) are applied to extract dominant modes, while for structured linear systems, balanced truncation including SVD on state-space matrices provides model-driven reduction. The resulting reduced-order models significantly lower simulation complexity while retaining essential circuit dynamics, enabling faster analysis, design iterations, and practical deployment of these circuits.

IV. Methodology and Implementation

A. Methodology

The approach for analog circuit model order reduction (MOR) integrates both circuit-level simulation and data-driven techniques. The following methodology was adopted:

1) **Circuit Selection:** Three analog circuits were considered in this work:
   - An n-stage cascaded common-source amplifier for nonlinear signal gain analysis.
   - Chen's nonlinear resistor circuit for evaluating nonlinear conductance behavior.
   - An n^{th}-order Butterworth low-pass filter using Sallen-Key topology for frequency-domain evaluation.
2) **Simulation and Data Generation:** SPICE-based simulation tools and Python models were used to generate data matrices:
   - For the amplifier, a voltage sweep from -2.5 V to 2.5 V was passed through n cascaded amplifier stages to obtain output at each node.
   - For the nonlinear resistor, nodal voltages were obtained by simulating the circuit under a unit step current input, forming the nonlinear conductance matrix $G(v)$.

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- For the filter, transfer functions of each stage were computed over logarithmic frequency sweeps.

3) **Mathematical Modeling:**
   - **Amplifier:** Modeled using a clipped linear gain formula:
   $$V_{\text{out}} = V_{\text{bias}} - A_v(V_{\text{in}} - V_{\text{bias}})$$
   - **Nonlinear Resistor:** Using Kirchhoff's laws, the nonlinear resistor circuit was expressed as:
   $$V = C^{-1}[G(v)] + C^{-1}Bu(t)$$
   where $G(v)$ is the nonlinear conductance matrix, B is the input vector, and $u(t)$ is the step input.
   - **Butterworth Filter:** Each stage was represented as a second-order low-pass transfer function and converted into a composite state-space model:
   $$\dot{x} = Ax + Bu, \quad y = Cx + Du$$

4) **Model Order Reduction (MOR):**
   - **Amplifier and Nonlinear Resistor:** Proper Orthogonal Decomposition (POD) using Singular Value Decomposition (SVD) was applied:
   $$V_{\text{centered}} = U\Sigma V^T$$
   A Python-based SVD framework was used for both the cascaded common-source amplifier and nonlinear resistor circuits. Nodal voltage and conductance matrices were decomposed using SVD to extract dominant modes, which were then used to form reduced-order models preserving the circuits' nonlinear behavior.
   - **Filter:** Balanced Truncation was performed by solving Lyapunov equations for the controllability and observability Gramians. SVD of the product of their Cholesky factors yielded the Hankel singular values, and the system was reduced using the dominant modes.

5) **Validation:** Reduced models were validated against full-order responses using:
   - **Amplifier and Nonlinear Resistor:** Mean Absolute Error (MAE) between full-order and reconstructed nodal voltages.
   - **Filter:** Root Mean Square (RMS) error between frequency responses of full and reduced models.

B. Implementation

1) Common Source Amplifier (Circuit 1):

Simulation: A 20-stage cascaded common-source amplifier is modeled with a linear approximation:

$$V_{\text{out}} = V_{\text{bias}} - A_v(V_{\text{in}} - V_{\text{bias}})$$

where:

- $A_v = -1.1$ is the gain,
- $V_{\text{bias}} = 1.1$ V is the DC bias,
- Output is clipped to the range $[-2.4, 1.6]$ V.

An input vector of 1000 points from −2.5 V to 2.5 V is passed through each amplifier stage, generating a matrix:

$$V_{\text{dc}} \in \mathbb{R}^{1000\times 21}$$

where each column corresponds to one amplifier stage.

Model Order Reduction using POD and SVD:

1) **Centering the Data:**
$$V_{\text{centered}} = V_{\text{dc}} - \mu, \quad \mu = \text{mean}(V_{\text{dc}}, \text{axis} = 0)$$

2) **Apply Singular Value Decomposition (SVD):**
$$V_{\text{centered}} = U\Sigma V^T$$
where U contains spatial modes, Σ is a diagonal matrix of singular values, and V^T holds temporal information.

3) **Select Dominant Modes:**
$$\sum_{i=1}^{r} \sigma_i^2 \geq 99.9\% \times \sum_{i=1}^{n} \sigma_i^2$$

4) **Reconstruction of Reduced Output:**
$$V_{\text{reduced}} = U_r \Sigma_r V_r^T + \mu$$

5) **Validation:** The reduced-order model is validated by comparing its stage voltages to the full-order model. Accuracy is quantified using the mean absolute error (MAE) across all input points.

2) Butterworth Low-Pass Filter (Circuit 2):

Simulation: An 8th-order filter is implemented using four second-order Sallen-Key stages. Each stage has the transfer function:

$$H(s) = \frac{\omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$$

System Modeling – State Space Representation: Each second-order stage is converted to:

$$\dot{x}_i = A_i x_i + B_i u, \quad y_i = C_i x_i$$

with:

$$A_i = \begin{bmatrix} 0 & 1 \\ -\omega_c^2 & -\frac{\omega_c}{Q_i} \end{bmatrix}, \quad B_i = \begin{bmatrix} 0 \\ \omega_c^2 \end{bmatrix}, \quad C_i = \begin{bmatrix} 1 & 0 \end{bmatrix}$$

All stages are cascaded to form a global system:

$$\dot{x} = Ax + Bu, \quad y = Cx + Du$$

Model Order Reduction using Balanced Truncation:

1) **Compute Gramians:**
$$AP + PA^T + BB^T = 0 \quad \text{(Controllability)}$$
$$A^T Q + QA + C^T C = 0 \quad \text{(Observability)}$$

2) **Apply SVD on Cholesky-transformed Gramians:**
$$L_Q^T L_P = U\Sigma V^T$$
where σ_i are the Hankel singular values.

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3) **Select r Modes:**

$$\sum_{i=1}^{r} \sigma_i^2 \geq 99.95\% \times \sum_{i=1}^{n} \sigma_i^2$$

4) **Construct Reduced Matrices:**

$$A_r = T^{-1}AT, \quad B_r = T^{-1}B, \quad C_r = CT, \quad D_r = D$$

Validation: The ROM's frequency response is compared with the full-order filter. Root-mean-square (RMS) error in magnitude across the frequency range assesses the reduction accuracy.

3) Nonlinear Resistor Circuit (Circuit 3):

Simulation: The nonlinear resistor circuit, adapted from Chen's formulation, is described by:

$$V = C^{-1}[G(v)] + C^{-1}Bu(t)$$

where $G(v)$ is the nonlinear conductance matrix. Voltage sweeps across multiple nodes generate the system response dataset.

Model Order Reduction using SVD:

1) **Form Conductance Matrix:** Nodal equations are assembled into a nonlinear conductance matrix $G(v)$.
2) **Apply Singular Value Decomposition:**

$$G(v) = U\Sigma V^T$$

where dominant singular values capture the primary dynamic behavior.

3) **Construct Reduced Model:** Retaining r modes satisfying

$$\sum_{i=1}^{r} \sigma_i^2 \geq 99.9\% \times \sum_{i=1}^{n} \sigma_i^2,$$

yields a reduced conductance matrix:

$$G_r(v) = U_r\Sigma_r V_r^T$$

and corresponding reduced response:

$$V_{\text{red}} = C^{-1}[G_r(v)] + C^{-1}Bu(t)$$

Validation: Node voltages from the reduced model are compared to the full nonlinear system. The mean absolute error (MAE) indicates how well the ROM captures the system's nonlinear behavior.

The circuits showed high fidelity between the reduced and full models, confirming the effectiveness of the MOR techniques in capturing dominant system behavior with lower dimensional representations.

V. Results and Discussions

Circuit 1: Cascaded CS Amplifier

Case 1: N = 20

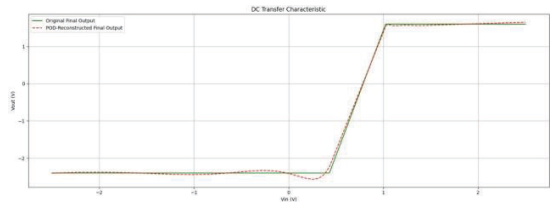


Fig. 1. DC Characteristics Before and After Reduction using Python, N=20 to N=5

Case 2: N = 30

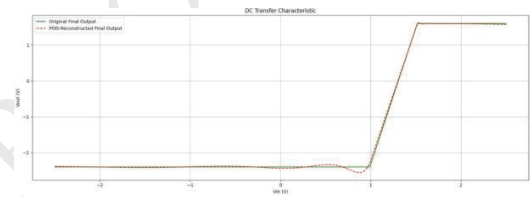


Fig. 2. (DC Characteristics Before and After Reduction using Python, N=30 to N=6

Summary of Results

The DC characteristics obtained from the Python-based simulation closely match those from the LT-SPICE simulation, demonstrating strong agreement. Furthermore, significant model order reduction is achieved using Proper Orthogonal Decomposition (POD) via Singular Value Decomposition (SVD), while maintaining minimal approximation error.

• CASE 1:
Time taken by Python tool to generate the similar output plot: 0.348sec seconds for N=20 nodes
Original Order: 20
Reduced order: 5
Mean Absolute Error (MAE) (%): 1.080643

• CASE 2:
Time taken by Python tool to generate the similar output plot: 0.545 seconds for N=30 nodes
Original Order: 30
Reduced order: 6
Mean Absolute Error (MAE) (%): 0.683709

Circuit 2: Low Pass Butterworth Filter

Case 1: Order = 12, fc=1kHz

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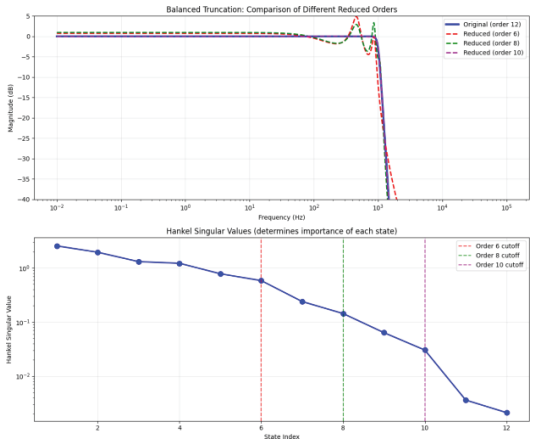


Fig. 3. (a)Balanced Truncation Frequency Response plot for various orders and (b) Hankel Values for importance of each stage

```
============================================================
ERROR SUMMARY TABLE
============================================================
Reduced Order   RMS Error (dB)  Size Reduction
------------------------------------------------------------
6               4.659           50.0          %
8               2.945           33.3          %
10              1.152           16.7          %

============================================================
RECOMMENDATION
============================================================
Based on Hankel singular values analysis:
- Recommended reduced order: 6
- This preserves states with HSV > 2.39e-01
- Expected RMS error: < 3 dB in passband

============================================================
```

Fig. 4. Comparison of different reduced orders

Case 2: Order = 20, fc=1kHz

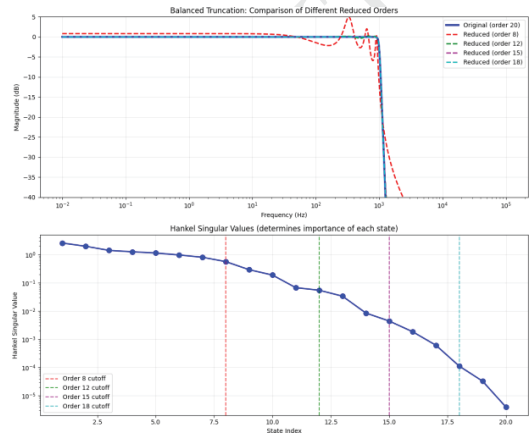


Fig. 5. (a)Balanced Truncation Frequency Response plot for various orders and (b) Hankel Values for importance of each stage

```
============================================================
ERROR SUMMARY TABLE
============================================================
Reduced Order   RMS Error (dB)  Size Reduction
------------------------------------------------------------
8               4.892           60.0          %
12              2.095           40.0          %
15              1.330           25.0          %
18              0.026           10.0          %

============================================================
RECOMMENDATION
============================================================
Based on Hankel singular values analysis:
- Recommended reduced order: 8
- This preserves states with HSV > 2.89e-01
- Expected RMS error: < 3 dB in passband

For < 1 dB RMS error: use reduced order 18 or higher

============================================================
```

Fig. 6. Comparison of different reduced orders

Summary of Results

• CASE 1:
Time taken by Python tool to generate the output plot: 1.536 seconds for 12th Order
Original Order: 12
Reduced Order: 6
Root Mean Square (RMS) Error (dB): 1.152
• CASE 2:
Time taken by Python tool to generate the output plot: 2.162 seconds for 20th Order
Original Order: 20
Reduced Order: 8
Root Mean Square (RMS) Error (dB): 1.330
These results confirm that Balanced Truncation is highly effective for model order reduction in continuous-time filter systems. The trade-off between computational efficiency and fidelity is well balanced, with reduced models offering near-identical performance while significantly lowering simulation cost.

Circuit 3: Non-linear resistor

Case 1: N = 20

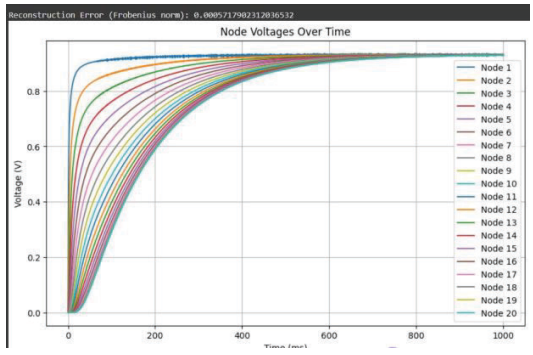


Fig. 7. Python simulation Vout vs time at different nodes

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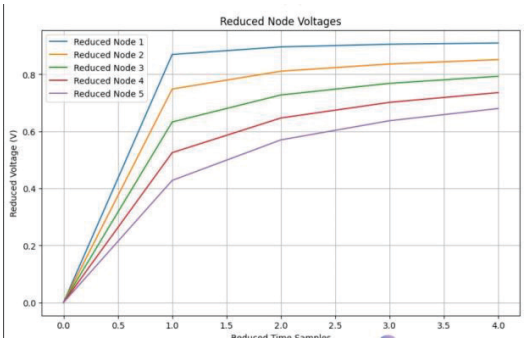


Fig. 8. Reduced order plot Vout vs time at different nodes(20 nodes reduced to 5)

Case 1: N = 100

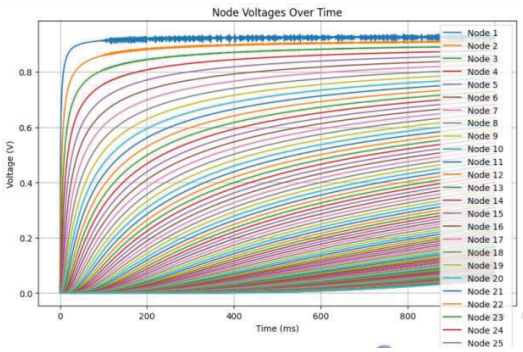


Fig. 9. Python simulation Vout vs time at different nodes

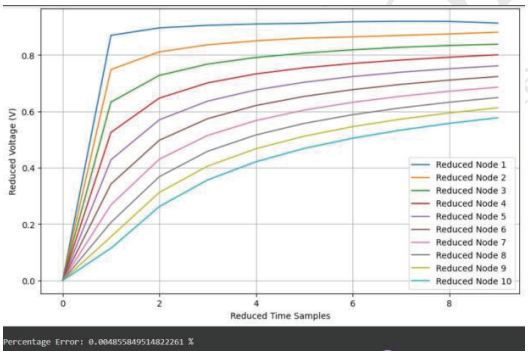


Fig. 10. Reduced order plot Vout vs time at different nodes(100 nodes reduced to 10)

Summary of Results

The Python-based simulation of the circuits closely matched the SPICE and Proteus simulation results, validating the accuracy of the transfer function and state-space models.

• CASE 1:

Time taken by P-SPICE tool to generate the output plot: 49.33 seconds for N=20 nodes

Time taken by Python tool to generate the similar output plot: 3 seconds for N=20 nodes

Original Order: 20

Reduced Order: 5

Percentage Error between Original matrix and Reduced matrix (%): 0.00215379

• CASE 2:

Time taken by P-SPICE tool to generate the output waveform: 696.61 seconds for N=100 nodes

Time taken by Python tool to generate the similar output plot: 15 seconds for N=100 nodes

Original Order: 100

Reduced Order: 10

Percentage Error between Original matrix and Reduced matrix (%): 0.25859078

These results confirm that Singular Value Decomposition is highly effective for model order reduction in continuous-time filter systems. The trade-off between computational efficiency and fidelity is well balanced, with reduced models offering near-identical performance while significantly lowering simulation cost.

Our models were implemented with the help of Google COLAB tool for the Python simulations and Orcad Capture on a PC with Intel(R) Core(TM) i5-8250U x-64 based processor, CPU @ 1.60GHz 1.80 GHz, and memory 8GB.

VI. Conclusion

This work highlights the effectiveness of advanced parametric model order reduction (MOR) techniques for efficient modeling and simulation of complex analog circuits. Proper Orthogonal Decomposition (POD) using Singular Value Decomposition (SVD) was applied to a multi-stage common-source amplifier, enabling the extraction of dominant dynamic modes and significant reduction in system dimensionality while maintaining high fidelity in the output response. Similarly, a high-order Butterworth low-pass filter, implemented with cascaded Sallen-Key stages, was reduced using balanced truncation that made use of SVD. By leveraging controllability and observability Gramians and performing singular value analysis, the reduced model preserved essential frequency-domain characteristics and input-output behavior. The methodology was further extended to a nonlinear resistor circuit, where SVD-based reduction captured the primary dynamic behavior of the system. Across all cases, the reduced-order models demonstrated strong agreement with the full-order simulations, confirming the robustness and versatility of the approach. Overall, this study illustrates that advanced MOR techniques can significantly improve computational efficiency without compromising accuracy, offering practical benefits for analog system design and simulation.

PROOF

VII. Future Trends

Future research in model order reduction (MOR) for analog circuits is likely to focus on several key directions:

- **Integration with Machine Learning:** Leveraging data-driven and hybrid approaches to identify dominant modes or predict system behavior could further accelerate MOR and improve accuracy for highly nonlinear or time-varying circuits.
- **Parametric and Multi-Operating Point Reduction:** Developing methods that can efficiently handle multiple operating conditions, process variations, and temperature-dependent behavior will enhance the reliability of reduced models in practical VLSI and EDA applications.
- **Real-Time and Hardware-Aware MOR:** MOR techniques that are computationally efficient enough for real-time simulation or hardware-in-the-loop testing will become increasingly valuable as circuit complexity grows.
- **Extension to Mixed-Signal and RF Systems:** Applying MOR to mixed-signal, RF, and high-frequency analog circuits presents challenges in preserving both time-domain and frequency-domain characteristics, creating opportunities for specialized reduction strategies.
- **Automation and Tool Integration:** Integrating advanced MOR algorithms into mainstream EDA tools could enable automated model reduction, streamlining the design and verification workflow for large-scale analog systems.

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Verilog Implementation Of SHA-256 Hash Algorithm

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Abstract*—With the increasing reliance on digital communication and data storage has amplified the demand for secure and efficient cryptographic techniques. This project focuses on the hardware implementation of the SHA-256 hash algorithm using Verilog, aiming to create a reliable and high-performance solution for ensuring data integrity and security. SHA-256, part of the SHA-2 family, is widely used in applications like blockchain technology and secure data transmission due to its robust cryptographic properties. The implementation follows a modular design approach, incorporating efficient message preprocessing, scheduling, and compression functions. It is validated using Intel Quartus Prime simulations to ensure correctness and performance optimization.Intel Quartus Prime is a robust FPGA design software used for digital logic development and simulation. It provides an integrated environment for hardware description languages such as Verilog and VHDL, facilitating efficient design compilation, resource estimation, and functional verification. By utilizing Quartus Prime, the SHA-256 implementation undergoes rigorous timing analysis and simulation, ensuring optimal performance on FPGA hardware. The findings of this project provide insights into the feasibility of hardware-based cryptographic implementations, addressing challenges related to resource utilization, computation speed, and hardware efficiency.

Keywords - SHA-256, Verilog, FPGA, Cryptographic Security, Digital Design

I. Introduction

SHA-256 is a fundamental cryptographic algorithm ensuring data integrity and security across applications such as blockchain, password hashing, and secure communication. This project presents a hardware implementation of SHA-256 using Verilog, leveraging its efficiency for digital systems. Unlike software implementations, hardware-based designs offer enhanced performance and scalability, making them suitable for IoT and FPGA-based applications. The design follows a modular approach, incorporating message preprocessing, scheduling, and compression, verified using Intel Quartus Prime and NIST test vectors. This work highlights the practical challenges and advantages of implementing cryptographic algorithms in hardware, contributing to secure and efficient digital systems.

II. Literature Survey

Several studies have explored hardware implementations of SHA-256, focusing on improving efficiency, throughput, and resource utilization.

Goyal et al. [1] implemented an FPGA-based SHA-256 design for blockchain applications, optimizing resource management and analyzing power and time consumption.

Suhaili and Norhuzaimin [2] proposed an unfolding transformation technique to enhance throughput, reducing clock cycles from 64 to 34, achieving a 58.1% improvement with a throughput of 4196.30 Mbps.

Bai and Li [3] introduced a VLSI-based SHA-256 design using a 7-3-2 array compressor, improving frequency by 1.7 times. Their architecture, synthesized in SMIC 0.18 µm CMOS, is suitable for SoC integration.

Padhi and Chaudhari [4] presented a pipelined SHA-256 architecture on Xilinx Virtex-4 FPGA, optimizing compressor/expander blocks and achieving a throughput of 1344.98 Mbps.

Chen and Li [5] proposed a rescheduling method to reduce critical path delay, implementing SHA-256 on a Xilinx Virtex-4 FPGA, achieving 1984 Mbps throughput with 979 slices.

These studies highlight optimization techniques that improve SHA-256 hardware implementations for secure digital applications.

III. Problem Analysis and Proposed Solution

A. Problem Definition

As cybersecurity threats continue to evolve, robust cryptographic techniques such as **SHA-256** play a crucial role in ensuring data integrity and security. However, **software-based implementations** of SHA-256 are computationally intensive, leading to high latency and inefficiencies in real-time applications that require high throughput. **Hardware-based implementations** offer a

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viable alternative, enabling significant acceleration of SHA-256 computations while optimizing energy efficiency.

B. Proposed Solution

This work presents a **modular hardware design** for SHA-256 implementation using **Verilog**, aimed at improving processing speed and resource efficiency. The design consists of the following key modules:

- **Message Preprocessing Module:** Handles input padding and segmentation into **512-bit blocks** as per SHA-256 specifications.
- **Message Scheduling Module:** Expands **512-bit input blocks** into **64-word sequences** for sequential processing.
- **Compression Function Module:** Executes **64 rounds** of logical and arithmetic operations using predefined SHA-256 constants.
- **Finite State Machine (FSM):** Controls data flow between functional modules to ensure sequential execution.
- **Output Module:** Stores and outputs the final **256-bit hash** after all iterations.

The design is implemented and verified using **Intel Quartus Prime**, with functional validation performed against **NIST standard test vectors** to ensure correctness and reliability.

IV. Intel Quartus Prime Software

Intel Quartus Prime is a **comprehensive FPGA design software suite** used for the development, simulation, synthesis, and implementation of hardware designs. It provides a **high-performance environment** for designing digital circuits, supporting **Verilog, VHDL, and SystemVerilog**.

Key features of **Quartus Prime** include:

- **Design Entry and Synthesis:** Supports **HDL-based** and **schematic-based** design methodologies.
- **Simulation and Verification:** Integrates with ModelSim and other simulators for **functional and timing verification**.
- **Timing Analysis:** Enables **static timing analysis (STA)** to optimize circuit performance.
- **Resource Optimization:** Includes tools for **power analysis and resource utilization estimation**.
- **FPGA Implementation:** Supports **Intel FPGA families**, providing seamless synthesis, place-and-route, and bitstream generation.

In this project, **Intel Quartus Prime** is used for the **synthesis, simulation, and verification** of the SHA-256 hardware implementation. Functional correctness is validated using **NIST test vectors**, and timing analysis is performed to evaluate efficiency and clock cycle performance.

V. Methodology & Implementation

A. Block Diagram

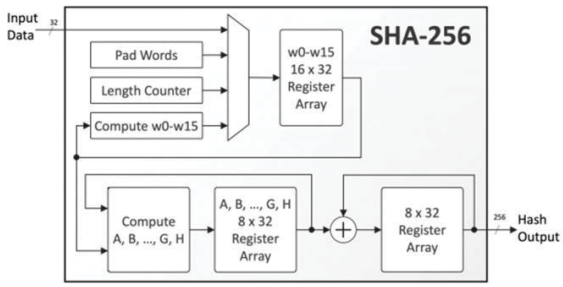


Fig. 1. Block diagram of SHA-256 implementation.

B. Design Approach

The implementation follows a structured approach to enhance performance and efficiency:

- **Register-Based Implementation:** Temporary registers store intermediate hash values to maintain computational integrity.
- **Pipeline Optimization:** Reduces execution latency and enhances processing speed through efficient pipelining techniques.
- **Resource Utilization Analysis:** Balances power consumption and performance to ensure an optimized hardware implementation.

C. Simulation Setup

The design and verification were carried out using the following setup:

- **Tool Used:** Intel Quartus Prime for synthesis and implementation.
- **Testbench Validation:** Functional verification using **NIST test vectors** to ensure correctness.
- **Timing Analysis:** Evaluation of clock cycle efficiency to assess performance under real-world constraints.

VI. SHA-256 Processing Stages

SHA-256 (Secure Hash Algorithm 256-bit) is a cryptographic hash function that processes data in multiple stages to produce a fixed 256-bit output. The computation consists of the following key stages:

A. Message Preprocessing

- **Padding**: The message is extended to be a multiple of **512 bits** by adding a '1' bit, followed by '0' bits, and a **64-bit length field**.
- **Segmentation**: The padded message is divided into **512-bit blocks**, each containing **sixteen 32-bit words**.

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B. Message Expansion

- Each **512-bit block** is expanded to **64 words** using: $Wt=\sigma1(Wt-2)+Wt-7+\sigma0(Wt-15)+Wt-16$
- where: $\sigma0(x)=(x \ggg 7) \oplus (x \ggg 18) \oplus (x \gg 3)$
- $\sigma1(x)=(x \ggg 17) \oplus (x \ggg 19) \oplus (x \gg 10)$

C. Compression Function

- **Initial Values**: Eight **32-bit hash values** are used, derived from the first **eight prime numbers**.
- **64 Rounds of Hashing**: Each round updates the working variables using logical operations: $T1=H+\Sigma1(E)+Ch(E,F,G)+Kt+Wt$
- $T2=\Sigma0(A)+Maj(A,B,C)$
- A,B,C,D,E,F,G,H are updated accordingly.
- where:
  - Σ0,Σ1\Sigma_0, \Sigma_1Σ0,Σ1 are rotation functions.
  - **Ch** (Choose) and **Maj** (Majority) operations control bit selection.

D. Final Hash Computation

- After processing all blocks, the final hash is computed by updating the **eight hash values**: $Hi=Hi+A,H1=H1+B,\ldots,H7=H7+H$
- The final **256-bit hash** is the concatenation of these values.

The SHA-256 implementation using Verilog successfully demonstrates efficient hardware-based cryptographic processing, ensuring enhanced security and performance. Future optimizations can focus on FPGA acceleration and reduced power consumption for real-time applications.

VII. Future Trends and Conclusion

A. Future Trends

The evolution of cryptographic hardware focuses on security, performance, and scalability. Key trends include:

- **Quantum-Resistant Algorithms**: Developing post-quantum cryptographic methods to counter quantum threats.
- **FPGA-Based Accelerators**: Enhancing blockchain security with efficient cryptographic processing.
- **AI-Driven Optimizations**: Using machine learning to improve hashing performance and resource utilization.
- **High-Performance Hardware**: Advancing pipelining and parallelism for real-time cryptographic applications.

B. Conclusion

This project successfully implements SHA-256 using Verilog, ensuring efficient hardware-based cryptographic processing. The modular, pipeline-optimized design improves speed, with correctness verified using NIST test vectors. Future work will focus on FPGA deployment, power optimization, and scalability for secure applications.

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VIII. Acknowledgment

We extend our sincere gratitude to **Dr. Bheemsha Arya**, Principal, BMS College of Engineering, for fostering an environment conducive to research and innovation. We are deeply thankful to **Dr. K. P. Lakshmi**, Head of the Department, Electronics and Communication Engineering, for her encouragement and support in carrying out this Mini Project.Our heartfelt appreciation goes to our guide, **Mrs.Monika Sharma D**, for her invaluable guidance and constant encouragement throughout this work. We also acknowledge the support of faculty members, peers, and all those who contributed to the successful completion of this project.Finally, we express our gratitude to our friends and seniors for their unwavering support and motivation.

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"Secure Key Access Management System With Biometric and RFID Verification"

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Abstract - In laboratory and industrial environments, secure management of physical keys is essential. This paper presents a Secure Key Access Management System that integrates biometric (fingerprint) and RFID-based authentication to ensure authorized access. A Raspberry Pi 3B acts as the central controller, interfacing with an R307S fingerprint module and RC522 RFID reader. Upon successful authentication, users access RFID-tagged keys, and the system logs key usage (user, key ID, timestamp) in a local database. SG90 servo motors, managed via a PCA9685 driver, control individual key compartments. A l6X2 LCD and buzzer provide real-time feedback, while a custom GUI offers administrators live monitoring and access logs. The system enhances accountability, reduces unauthorized access, and streamlines key tracking.

Keywords - Biometric authentication, RFID verification, Raspberry Pi, secure key management, servo locking system, real-time monitoring.

I. INTRODUCTION

With increasing security demands in laboratories, offices, and research facilities, traditional mechanical key management systems are proving insufficient due to manual logging, human error, and lack of real-time monitoring. This project proposes a Secure Key Access Management System that combines biometric fingerprint authentication and RFID-based key identification within an IoT-enabled framework. Dual-factor authentication enhances security by ensuring access is granted only to verified users. A Raspberry Pi 3B acts as the central controller, interfacing with an R307S fingerprint sensor and RC522 RFID reader to authenticate users and identify keys. Once verified, users access specific RFID-tagged keys from secured compartments controlled by SG90 servo motors via a PCA9685 driver. All key transaction heck-outs, returns, and mismatches—are logged in a local database and displayed through a Python-based GUI. The system enables real-time access tracking, role-based permissions, and automated key control, significantly improving accountability and reducing the risk of unauthorized access.

II. LITERATUnc SwRVEY

[1] **"IoT-Based Smart Inventory Management System"**
This work demonstrates how RFID tags can be used for rapid, contactless tracking in inventory systems, enhanced with weight sensors for real-time item detection. The approach ensures secure, automated monitoring and is directly adaptable for smart key locker systems.

[2] "Advanced Door Locking System Using IoT"
The paper presents an IoT-enabled door lock allowing users to control access remotely via Wi-Fi. It integrates multiple sensors for safety and emphasizes energy-efficient automation, offering foundational concepts applicable to smart key locker systems for lab environments.

[3] "Arduino-Powered Fingerprint Authentication for Door Access Control"
This study outlines fingerprint-based access control using Arduino, highlighting cost-effective and reliable biometric authentication. The solution supports fast enrollment and verification, making it suitable for high-traffic environments such as labs requiring secure, user-specific key access.

[4] "Enhancing Security: Evaluating RFID Card Access Control Systems Using SHA256"
Focusing on the security of RFID systems, this paper introduces SHA256 cryptographic hashing to protect card data. It proposes a layered security model and analyzes RFID vulnerabilities, providing essential insights for designing secure lab key access systems.

[5] "Innovative IoT Smart Lock System Enhancing Security with Fingerprint and RFID"
This work integrates fingerprint and RFID technologies to offer dual-layer authentication, significantly enhancing access security. IoT modules enable real-time monitoring and mobile alerts, while a user-friendly interface ensures efficient system interaction—ideal for modern lab key management systems.

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III. PROBLEM AND SOLUTION

Key Access Management System encounters several issues

1. **Unauthorized** Access: Physical keys can be copied or stolen, allowing undetected entry.
2. **No Accountability:** Manual logs lack real-time tracking, making it hard to trace key misuse.
3. **Prone to Human Error:** Paper-based logging is inefficient and error-prone.
4. **No Real-Time Alerts:** Missing or late keys go unnoticed without instant notifications.
5. **Poor Scalability:** Manual systems fail to scale in large environments with many users and keys.

Our RFID-based solution addresses these issues by:

Dual-Factor Authentication:Combines fingerprint verification (R307S) with RFID-tagged keys to ensure only authorized users access specific keys.

Automated Locking:Servo-controlled compartents unlock only after valid authentication and re-lock automatically upon key return. Alerts trigger if keys are not returned in time.

Real-Time Monitoring: All access events are logged with timestamps in a local database. A GUI displays live logs, user activity, and key status.

Role-Based Access: Users are assigned roles (e g., staff, technician, foreman) with specific access rights. Admins can override access in emergencies.

Alerts and **Notifications:** Buzzer and LCD display messages for denied access or overdue returns. Optional email/SMS alerts notify repeated violations.

Scalability: Supports multiple servos and sensors via PCA9685 and GPIO. Python-based code allows easy customization and IoT integration.

IV. Methodology

A. sys arc and algorithm

Start & Initialization

- System boots and displays "Welcome" on the LCD.
- Prompts user to place their finger on the R307S sensor.

Fingerprint Authentication

- **If matched:** Proceeds to role-based access.
- **If not matched:** Access denied, buzzer sounds, system returns to idle.

Role-Based Access

- **Admin:** Full access, can manage users and export logs.
- Staff: Access only to assigned keys.
- Foreman: Emergency access to all keys and compartments.

RFID Key Verification

- Verified user scans RFID tag via RC522.
- **If matched:** Corresponding servo unlocks key slot, LCD shows confirmation.
- **If not matched:** Displays error and prompts retry.

Transaction Logging

- On valid scan, RFID tag and fingerprint data are logged.
- Key ID, user ID, and timestamp are stored in database.
- Door locks after key retrieval.

Logout and System Reset

- After the process, user is logged out.
- System resets to idle, ready for next user.

B. hardware components

Raspberry Pi 3B: Central controller managing authentication, logging, and module communication.

R307S Fingerprint Sensor: Provides biometric user authentication via UART interface.

RC522 RFID Reader: Reads RFID key tags to verify key access through SPI interface.

PCA9685 PWM Driver: Controls multiple SG90 servos via I^2C for key compartment locking.

SG90 Servo Motors: Physically lock/unlock individual key slots based on access permissions.

16^2 LCD Display: Shows system prompts and feedback messages via I^2C interface.

Buzzer: Delivers audio alerts for access status and warnings through GPIO control.

HDMI Monitor: Displays GUI with live access logs and system status from Raspberry Pi.

5V/3A Power Adapter: Powers the Raspberry Pi and system logic.

External 5V Supply: Separately powers servos via PCA9685 to maintain system stability.

C. Integration & testing

Authentication Accuracy: Verified reliable fingerprint and RFID matching for all registered users, minimizing false acceptance/rejection.

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Access Control Functionality: Tested role-based restrictions and emergency override to ensure correct key access for each user type.

Hardware Stability: Confirmed smooth servo operation and consistent LCD/buzzer feedback under continuous use and multiple key operations.

Data Logging Reliability: Ensured all transactions were correctly logged with timestamps in the SQLite database for traceability.

System Recovery & Reset: Validated proper system reset to idle after each session and tested behavior under power loss and reboot.

V. ResuIt& disscussion

1. SYSTEM SETUP •- Tiis noWARE—INCLUDING **FINGERPRINT SENSOR** RFID **READER, SERVOS, AND DISPLAY—WAS ASSEMBLED** IN A CUSTOM ENCLOSURE. PYTHON-BASED SCRIPTS ON THE SPBERRY PI MANAGED **ALL** DEVICE **COMMUNICATION,** AUTHENTICATION, AND USER INTERFACE TASKS.

2. FUNCTIONAL VALIDATION:- FINGERPRINT AND RFID **MATCHING WERE TESTED FOR ACCURACY,** ACHIEVING HIGH RELIABILITY ACROSS MULTIPLE TRIALS. SERVO OPERATIONS AND GUI RESPONSIVENESS WERE VALIDATED, WITH ALL ACTIONS COMPLETING IN UNDER 500 MILLISECONDS.

3. SECURITY AND LIABILITY TESTINGS- UNAUTHORIZED ACCESS ATTEMPTS TRIGGERED IMMEDIATE ALERTS AND WERE **LOGGED** WITH IDENTIFYING DATA. **THE SYSTEM RECOVERED GRACEFULLY FROM POWER LOSS, PRESERVING THE LAST KNOWN STATE TO PREVENT UNLOCKED COMPARTMENTS.**

4. SABILIrv OBSERVATIONS:- TEST **USERS** REPORTED SMOOTH OPERATION WU 2-3 SECOND ACCESS TIME AND HELPFUL BUZZER/LCD FEEDBACK. MINISTRATORS FOUND THE GUI INTUITIVE FOR MANAGING USERS, KEYS, AND GENERATING USAGE **REPORTS.**

VI. Future work

1. Cloud-Based Logging and Analytics: Migrating logs to the cloud enables centralized access monitoring and advanced analytics like anomaly detection across multiple sites.

2. Mobile App Integration: A companion mobile app would allow admins to receive alerts and users to pre-request or schedule key access remotely.

3. Multi-Modal Biometric Fusion: Adding facial, iris, or voice recognition enhances security and accessibility for users with unreadable fingerprints.

4. RFID Tag Upgrades: Switching to BLE or NFC enables real-time key tracking and smartphone-based checkouts, reducing hardware dependency.

5. Enhanced Hardware Security: Using tamper-proof metal enclosures and TPM encryption improves physical and data security in case of unauthorized access.

6. Scalable Multi-Door Networks: Implementing a master-satellite Raspberry Pi setup with MQTT allows centralized control of multiple access points in large facilities.

VII. Conclusion

This project presents a cost-effective, reliable key management solution that integrates fingerprint-based biometric authentication and RFID verification, powered by a Raspberry Pi 3B. It replaces traditional manual logs with a dual-factor system that enhances security, automates key access via servo-controlled compartments, and provides real-time monitoring through a GUI dashboard and alert mechanisms. Designed with scalability in mind, the open-source architecture supports future upgrades such as cloud integration, biometric fusion, and multi-door deployment. Extensive testing confirmed the system's performance in speed, accuracy, and usability, making it suitable for labs, institutions, and secure facilities.

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An FPGA application of home security code using verilog

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***Abstract*— Conventional key-and-lock security systems are susceptible to theft, duplication, and misplacement, compromising security. This paper presents an FPGA-based home security code lock system implemented using Verilog HDL. The system leverages a Xilinx Boolean Board, employing a 4x4 matrix keypad for passcode input, a Finite State Machine (FSM) for secure state transitions, and a 7-segment display for user feedback. The design was simulated and verified using Xilinx tools, demonstrating the efficiency and adaptability of FPGA-based security solutions.**

Keywords— FPGA, Home Security, Verilog, Finite State Machine (FSM), Keypad, Digital Lock.

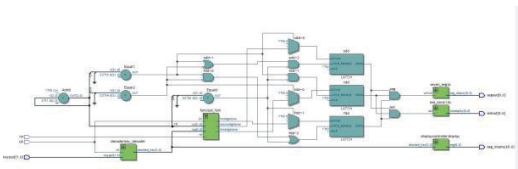
I. Introduction

Security is a fundamental concern in residential and commercial settings. Traditional mechanical locks suffer from key duplication, theft, and loss, necessitating advanced digital solutions. FPGA-based security systems provide enhanced flexibility, reconfigurability, and real-time performance, making them ideal for digital lock applications. This paper presents an FPGA-based home security code lock system designed using Verilog HDL and implemented on a Xilinx Boolean Board.

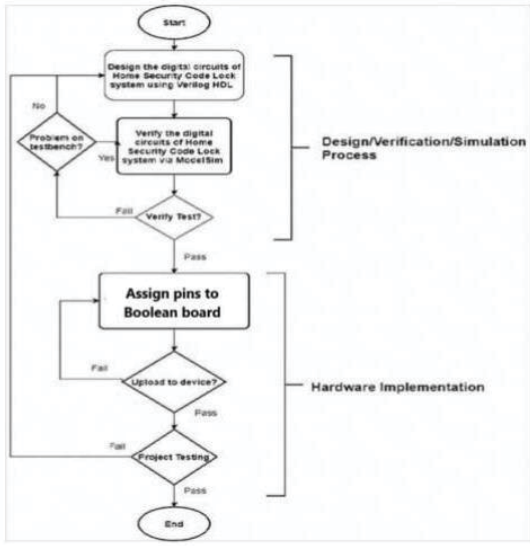
II. Related work

Existing security systems primarily utilize microcontrollers or ASICs. While microcontroller-based systems are cost-effective, they lack parallel processing capabilities. ASIC-based solutions, on the other hand, provide high efficiency but lack reconfigurability. FPGA-based designs bridge this gap by offering scalability, rapid prototyping, and cost-effective modifications. Previous research [1] has demonstrated the potential of FPGA-based security implementations, emphasizing their reliability and flexibility.

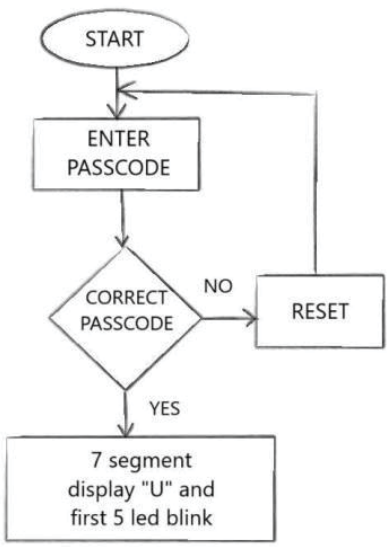
A. Block Diagram



B. Design Flow



C. Flowchart



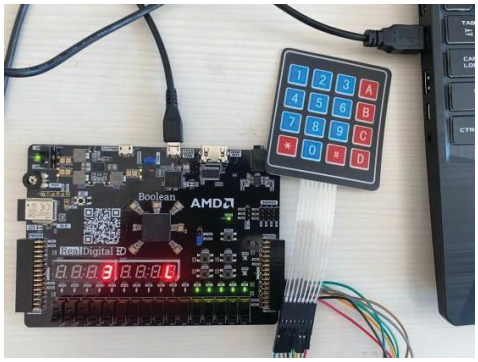
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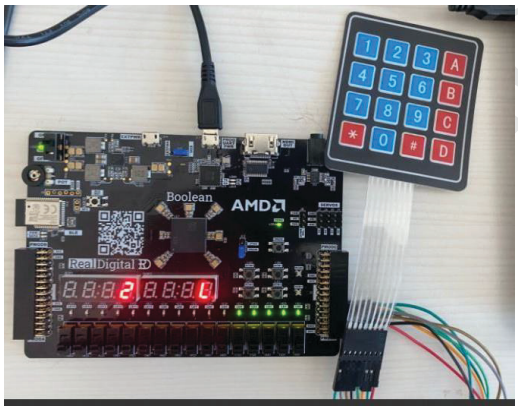
D. 4x4 table representation

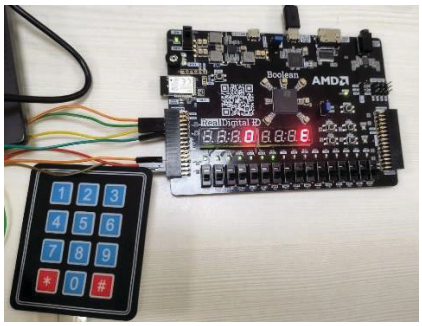
Table 1. Columns and rows

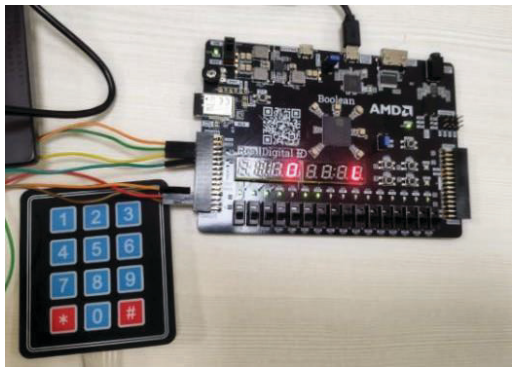
Column (C1, C2, C3, C4)	Row (R1, R2, R3, R4)	Button
0111	0111	1
0111	1011	4
0111	1101	7
0111	1110	*
1011	0111	2
1011	1011	5
1011	1101	8
1011	1110	0
1101	0111	3
1101	1011	6
1101	1101	9
1101	1110	#
1110	0111	A
1110	1011	B
1110	1101	C
1110	1110	D

D. Boolean board implementation for L and Error

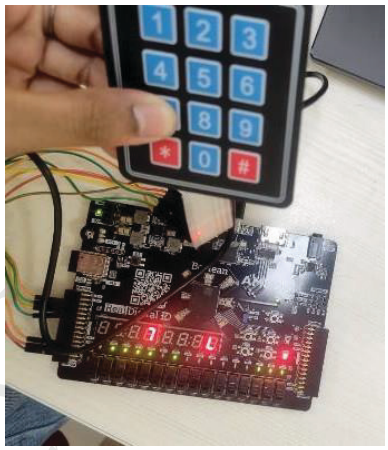


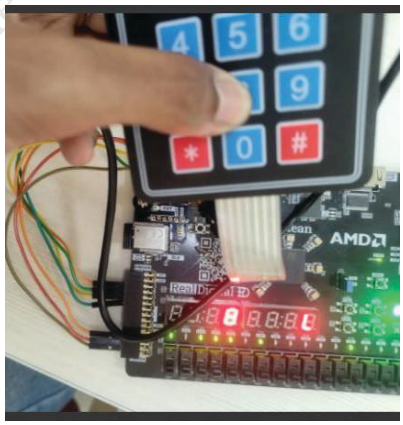


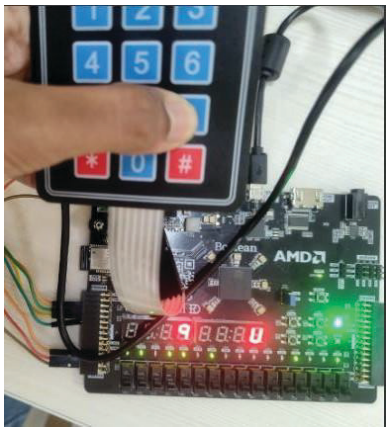




E. Boolean board implementation for U with password display







III. System Design

A. Hardware Components

- *Xilinx Boolean Board (Spartan-7 FPGA)*
- *4x4 Matrix Keypad for user input*
- *7-Segment Display for visual feedback*
- *LEDs for status indication*

B. Software Tools

- *Xilinx Vivado for simulation and synthesis*
- *ModelSim for functional verification*

C. Finite State Machine Implementation:*The FSM-based control ensures secure passcode validation. It transitions through predefined states based on user input. If the correct passcode is entered, the system unlocks; otherwise, it resets.*

IV. Implementation and Results

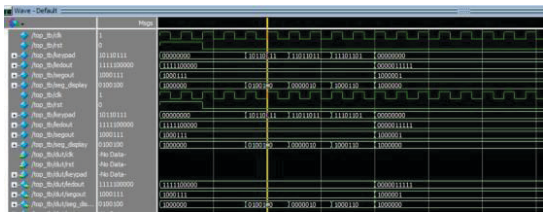
A. **Simulation and Verification** The design was simulated using ModelSim to verify functional correctness. The FSM transitions and passcode validation were successfully tested.

B. **Hardware Testing** The synthesized design was deployed on the Boolean Board, where the keypad inputs were correctly decoded, and the 7-segment display provided real-time feedback.

C. **Performance Evaluation**

- **Latency:** The system responded instantly to keypresses.
- **Security:** Incorrect passcodes resulted in immediate reset.
- **Scalability:** FPGA's reconfigurability allows future upgrades, such as biometric integration.

D. **Simulation graph**



V. Future Work

Future enhancements include biometric authentication, IoT integration for remote monitoring, and AI-based anomaly detection for enhanced security. Power optimization techniques will also be explored for energy-efficient implementations.

VI. Conclusion

This paper demonstrated an FPGA-based home security code lock system using Verilog HDL. The FSM-based design ensures secure and reliable passcode authentication. Simulation and hardware implementation validated the system's functionality, proving FPGA's potential in modern security applications.

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ESP32-CAM Based Agriculture Yield Monitoring System

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***Abstract*—This paper presents the development of a smart agricultural monitoring system utilizing an ESP32-CAM module for real-time crop health assessment. The system captures images of crop fields and processes them using OpenCV to determine green coverage percentage, which serves as an indicator of plant health. The captured images are transmitted wirelessly to a server for analysis. By converting images to HSV color space, green pixels are isolated, and their percentage is calculated to assess vegetation density. If the green coverage falls below a predefined threshold, the system generates alerts through a web interface. A Flask-based API enables remote access to data, providing farmers with real-time insights for better decision-making. The proposed solution is cost-effective, energy-efficient, and suitable for small to medium-scale farms, improving precision farming practices through automated crop monitoring.**

***Index Terms*—ESP32-CAM, Agriculture, Crop Monitoring, OpenCV, IoT, Precision Farming.**

I. Introduction

Agriculture is the backbone of the global economy, and technological advancements have significantly improved farming practices. With the rise of smart farming, integrating Internet of Things (IoT) and image processing techniques has revolutionized crop monitoring and management. Traditional methods of assessing crop health require manual inspection, which is time-consuming, labor-intensive, and prone to human errors. To address these challenges, automated monitoring systems have gained popularity, providing real-time insights into crop growth and health.

This project focuses on developing an ESP32-CAM-based agriculture yield monitoring system to assist farmers in evaluating crop conditions efficiently. The system captures real-time images of the field, processes them to determine the percentage of green cover, and identifies areas that may require attention. By leveraging computer vision techniques, specifically image processing in the HSV color space, the system isolates green pixels representing healthy vegetation. If the green coverage falls below a predefined threshold, the system can notify farmers, enabling timely interventions to improve yield.

Designed as a low-cost, energy-efficient solution, this system offers a user-friendly web interface that allows farmers to remotely access data, reducing the need for physical field inspections. The integration of wireless communication further enhances its accessibility, making it suitable for small and medium-scale farms. By providing real-time, data-driven insights, this project aims to enhance precision agriculture, optimize resource utilization, and ultimately contribute to sustainable farming practices.

II. Literature Survey

Several studies have explored the integration of IoT and image processing for agricultural monitoring. A system using an ESP32-CAM for surveillance and environmental monitoring demonstrated the effectiveness of real-time video analysis and wireless communication in tracking field conditions [1]. Similarly, an IoT-based crop monitoring system utilized image processing to detect crop diseases by analyzing leaf color, aiding in early disease detection and improved yield management [2]. Other research has investigated forest monitoring systems that employ thermal imaging and wireless sensors to detect environmental threats, which could be adapted for agricultural applications [3]. Additionally, a model using an ESP32-CAM and mobile applications for remote plant monitoring provided a cost-effective alternative to drone-based surveillance, enabling real-time data collection and remote accessibility [4]. These studies highlight the potential of combining IoT and image processing for precise, real-time agricultural monitoring, forming the foundation for this project's approach to crop health assessment using the ESP32-CAM module.

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III. Problem Analysis and Solution

A. Problem Definition

Traditional agricultural practices often rely on manual field inspections, which are time-consuming, labor-intensive, and prone to inaccuracies. Farmers struggle to consistently monitor large-scale fields, leading to delayed detection of crop stress, diseases, and irrigation issues. Current automated systems for crop health assessment are either expensive, require complex setups, or consume high power, making them inaccessible for small and medium-scale farmers. This lack of affordable, real-time monitoring solutions hinders precision farming efforts, resulting in inefficient resource allocation and suboptimal yield. The need for a low-cost, energy-efficient, and remote-accessible solution to track crop health in real time is crucial for modernizing agricultural practices and enhancing productivity.

B. Proposed Solution

The proposed solution employs the ESP32-CAM module to capture images of the crop field at regular intervals and transmit them wirelessly for processing. The images are analyzed using OpenCV-based image processing techniques, where the HSV color space is utilized to isolate green regions representing healthy vegetation. The system calculates the percentage of green cover and compares it against a predefined threshold to detect potential crop health issues. The processed data and analyzed images are displayed on a Flask-based web interface, allowing farmers to access real-time crop health insights remotely. Additionally, automated alerts are generated if the green coverage falls below the threshold, enabling timely interventions. The system is designed to be cost-effective and energy-efficient, making it suitable for small and medium-scale farms. Future enhancements may include integrating additional sensors, such as temperature and soil moisture detectors, to further refine the monitoring process and improve decision-making capabilities.

IV. Methodology and Implementation

A. System Block Diagram

The system block diagram provided in Fig.1 shows a high-level overview of the architecture and components involved in the ESP32-CAM-based agricultural monitoring system. The core of the system is the ESP32-CAM module, which captures images of the crop field. These images are processed using OpenCV-based image analysis, where the green cover percentage is calculated. The processed data is transmitted via Wi-Fi communication to a remote server, which hosts a Flask-based web interface. The web interface displays the analyzed data, providing real-time insights to farmers.The system is designed to be low-power and cost-effective, ensuring practical implementation in real-world agricultural scenarios.

B. Data Transmission and Visualization

The data transmission process plays a crucial role in ensuring real-time monitoring of crop health. The ESP32-CAM module captures images and transmits them wirelessly using Wi-Fi to a remote server. The system employs a Flask-based API to handle requests and facilitate seamless communication between the ESP32-CAM and the web interface. The transmitted images undergo processing using OpenCV, where the percentage of green vegetation is analyzed. The processed data is then stored on the server and made accessible through a user-friendly web dashboard.

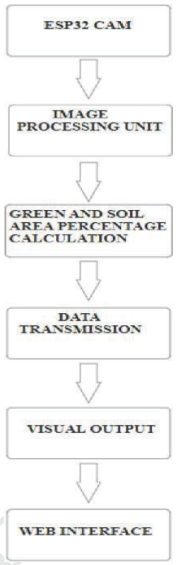


Fig. 1. System Block Diagram

The visualization aspect is handled through an interactive web interface, which provides farmers with a clear and concise representation of their crop health. The interface displays real-time images, green coverage percentage, and alerts when vegetation health falls below a set threshold. By offering remote accessibility, the system allows farmers to make informed decisions regarding irrigation, fertilization, and overall crop management without requiring physical field visits. This ensures efficient resource utilization and timely interventions to enhance agricultural productivity..

V. Results and Discussion

The ESP32-CAM-based monitoring system was tested under various environmental conditions to evaluate its performance in detecting crop health. The system successfully captured images and processed them using the OpenCV-based algorithm to determine green coverage. The real-time transmission and visualization ensured that farmers could access crop health data remotely without delays. Experimental results demonstrated that the system provided accurate green coverage calculations, enabling early detection of potential plant stress due to insufficient irrigation or nutrient deficiency. The alerts generated when green coverage fell below a predefined threshold allowed timely interventions, reducing crop losses. Although the system performed well, challenges such as

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varying lighting conditions and different crop types influenced detection accuracy. Future improvements can include integrating machine learning algorithms to enhance adaptability and accuracy across diverse agricultural settings.

VI. Future Trends and Conclusion

As technology advances, the integration of artificial intelligence (AI) and machine learning (ML) in agricultural monitoring systems is expected to improve accuracy and adaptability. Future enhancements may include predictive analytics to forecast crop diseases and automated irrigation systems that adjust water supply based on real-time vegetation health.

Another significant trend is the use of multispectral and hyperspectral imaging to capture more detailed crop health indicators beyond visible light detection. Integrating additional sensors, such as soil moisture, temperature, and humidity sensors, can provide a more holistic analysis of crop conditions, further enhancing decision-making for farmers..

VII. References

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POWER REDUCTION IN CMOS 4 x 1 MULTIPLEXER USING STACK ONOFIC TECHNIQUE

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***Abstract*—With the rapid scaling of semiconductor devices, leakage power has become a critical issue in CMOS circuit design, significantly affecting battery life and overall system efficiency in portable electronics. This project focuses on minimizing leakage power in a 4×1 CMOS multiplexer by applying the Stack ONOFIC technique, which reduces power through strategic transistor stacking. Two versions of the 4×1 multiplexer were designed and simulated using Cadence software: a conventional CMOS implementation and an optimized design employing the Stack ONOFIC method. Simulation results reveal a substantial reduction in power, with the Stack ONOFIC multiplexer achieving approximately 16.12% less power compared to the conventional design (459.1 uW versus 385 uW). Importantly, this reduction was achieved without compromising the circuit's switching performance or functionality. These findings demonstrate the effectiveness of transistor stacking techniques for leakage power reduction in digital circuits. The Stack ONOFIC approach proves valuable for low-power VLSI designs, especially in applications where power efficiency is paramount, such as Internet of Things (IoT) devices, mobile electronics, and wearable technology. This project contributes to advancing energy-efficient integrated circuit design, supporting the development of sustainable and high- performance electronics for modern applications.**

Keywords—ONOFIC, Leakage Power, CMOS, Stack, Multiplexer

I. Introduction

In modern VLSI design, minimizing power consumption has become a crucial challenge as device sizes shrink and circuit complexity increases. Leakage power, a significant contributor to energy dissipation in CMOS circuits, leads to unwanted power loss even when devices are idle, negatively impacting overall efficiency, performance, and battery life. This project focuses on reducing leakage power in a 4 x 1 CMOS multiplexer, a fundamental digital component used widely for signal selection and data routing in integrated circuits. By implementing the Stack ON, an advanced low-power design approach that employs transistor stacking and optimized switching, this method effectively suppresses subthreshold leakage currents without compromising switching speed or functionality. The design and simulation are carried out using Cadence software, ensuring accurate transistor-level modeling and precise power analysis. Simulation results demonstrate substantial leakage power reduction while maintaining robust performance. This technique holds great promise for energy-sensitive applications such as smartphones, IoT devices, automotive electronics, high-performance computing, and medical electronics, where power efficiency is vital for extending battery life, improving thermal management, and enhancing reliability. By addressing leakage power at the circuit level in the 4x1 multiplexer, this project contributes significantly to the development of energy-efficient integrated circuits, promoting greener, more sustainable, and high-performance modern electronics. Ultimately, such innovations are key to meeting the increasing demand for low-power designs in next-generation electronic systems.

A. Literature survey

Leakage power reduction in CMOS circuits is a critical concern in modern VLSI design, particularly with the continued scaling of technology nodes and the growing demand for energy-efficient portable and battery-operated devices. Among the various techniques explored, the LECTOR and ONOFIC methods have gained prominence for their effectiveness in minimizing leakage. LECTOR uses Leakage Control Transistors (LCTs) inserted between the pull-up and pull-down networks, offering a significant leakage reduction of ~55.4%, though it increases delay and power-delay product (PDP), making it suitable for applications where leakage control is paramount [1]. In contrast, the ONOFIC approach introduces an ONOFIC block that dynamically transitions between ON and OFF states, creating a high-resistance path during standby to reduce leakage (~14.63%) while maintaining better speed and a lower PDP, making it more balanced and efficient for performance-critical applications [1]. Enhancing this concept, the Stack ONOFIC technique integrates a PMOS and NMOS pair that operate in linear or cutoff modes based on logic output, further reducing leakage and delay, with simulations showing improved performance over LECTOR, achieving 604.74 pW of power dissipation and a propagation delay of 4.88 ps versus LECTOR's 678.15 pW and 9.07 ps [2]. The use of stacked NMOS transistors controlled by a PMOS in Stack ONOFIC helps elevate threshold voltages in the OFF state, significantly lowering subthreshold leakage while ensuring efficient switching, thereby outperforming other techniques like LCNT and LECTOR in power and delay trade-offs, especially in 130nm and 22nm nodes [3]. Moreover, ONOFIC's versatility extends to universal logic gates, such as NAND and NOR, achieving substantial leakage reductions of 85.08% and 73.66%, respectively, with

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NAND gates benefiting more due to improved control, and it holds promise for broader integration in functional units like multiplexers, decoders, and flip-flops [4]. These findings collectively underscore ONOFIC and its variations, particularly Stack ONOFIC, as promising solutions for achieving low-power, high-performance CMOS circuit designs, especially as devices move towards ultra-scaled nodes and energy-constrained environments.

II. Problem analysis and solution

A. Problem Statement

In modern CMOS circuits, leakage power has become a significant concern, particularly in deep submicron technologies (e.g., 45 nm, 22 nm). A 4×1 multiplexer (MUX) is a fundamental combinational circuit used in various digital applications, including data path selection and signal routing. However, conventional CMOS multiplexers suffer from high leakage power dissipation, primarily due to subthreshold leakage, gate leakage, and junction leakage, particularly when transistors are in the OFF state. The challenge is to design a low-power 4×1 multiplexer without compromising performance.

B. Problem Solution

Stack ONOFIC Technique to reduce leakage power in a CMOS 4 × 1 multiplexer, we propose utilizing the Stack Effect with ON-OFF Logic technique.

- Stack Effect: NMOS Transistor Stacking: In the Stack technique, two NMOS transistors are stacked in series. Stacking NMOS transistors has the effect of increasing the resistance in the OFF state because even if there is some leakage current through one NMOS transistor, the second NMOS reduces it further. This is because in subthreshold conduction (leakage), the stacked transistors experience a higher effective threshold voltage, reducing the current exponentially.
- ON-OFF Logic: This technique ensures that when a transistor is OFF, the stacked configuration forces one of the transistors into deep cutoff, further minimizing leakage current.
- Stack ONOFIC: PMOS Control: The gate of the stacked NMOS transistors is controlled by an additional PMOS transistor. The drain of this PMOS is connected to the gate of the NMOS transistors, and its gate is connected to the output. By integrating Stack Effect with ON-OFF Logic, the modified CMOS 4 × 1 multiplexer will achieve lower leakage power while maintaining functional correctness. The design will be simulated using Cadence Virtuoso to compare power consumption against a conventional multiplexer.

III. Methodology and Implementation

A. Block Diagram

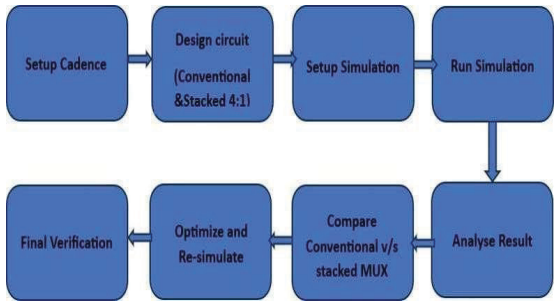


Fig.1. Block Diagram

B. Project Execution Steps

- **Setting Up the Cadence Environment**:

  Start by loading the required Process Design Kits (PDKs) that provide essential device models and technology parameters for accurate circuit design. Configure library paths to access standard cells and custom components, ensuring all necessary files are included. Organize the working directory with clear folders for schematics, simulations, and reports to maintain an efficient workflow.

- **Designing the Circuit in Virtuoso Schematic Editor:**

  Use the Virtuoso schematic editor to create the 4 × 1 CMOS multiplexer circuit, choosing between transmission gate or CMOS logic implementation. Integrate the Stack ONOFFIC transistor configuration to reduce leakage by stacking transistors strategically. Verify the schematic's correctness and functionality before proceeding to simulation.

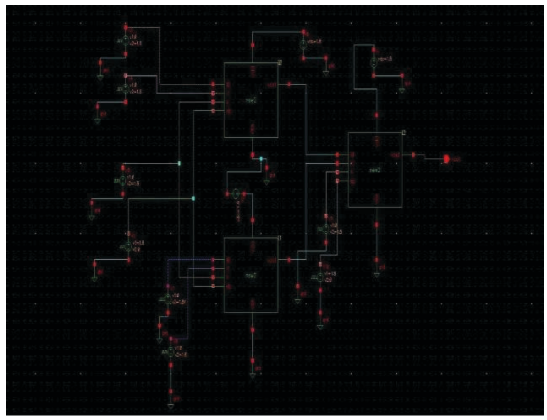


Fig.2. Circuit for 4 x 1 using 2 x 1 MUX

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- **Simulation Setup with Cadence ADE:**

  Set up the testbench in Cadence ADE by defining power supply voltages, input signals, and ground references for the multiplexer. Specify simulation types such as transient for dynamic response and DC analysis to measure leakage current. Configure measurement parameters focused on capturing leakage behavior under various input conditions.

- **Run the Simulation:**

  Execute transient and DC simulations to observe the circuit's switching behavior and leakage currents during idle states. Monitor simulation progress to ensure convergence and validate that the outputs behave as expected. Collect waveform data and numerical results for further analysis plural, not singular.

- **Analyzing the Output Results:**

  Evaluate leakage currents and total power consumption from the simulation outputs to assess the effectiveness of the Stack ONOFFIC technique. Analyze performance metrics like propagation delay and signal integrity to understand trade-offs. Use these insights to determine if design goals for low power and performance are met.

- **Optimization and Re-simulation:**

  Based on analysis, adjust transistor stacking, sizing, and biasing to further reduce leakage without degrading speed or functionality. Update the schematic and simulation setup to test these improvements. Repeat simulation runs and analysis until an optimal balance between power efficiency and performance is achieved.

- **Final Verification and Report Generation:**

  Perform a final verification of the optimized design to confirm leakage reduction and functional correctness. Generate detailed waveforms, power reports, and performance summaries. Document all findings, design changes, and conclusions in a comprehensive project.

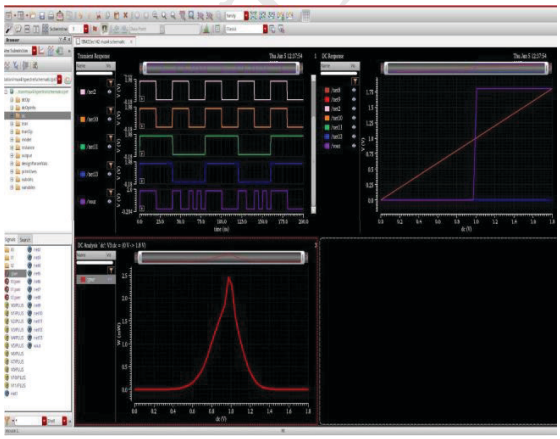


Fig.3. Output Waveforms for stacked 4 x 1 MUX

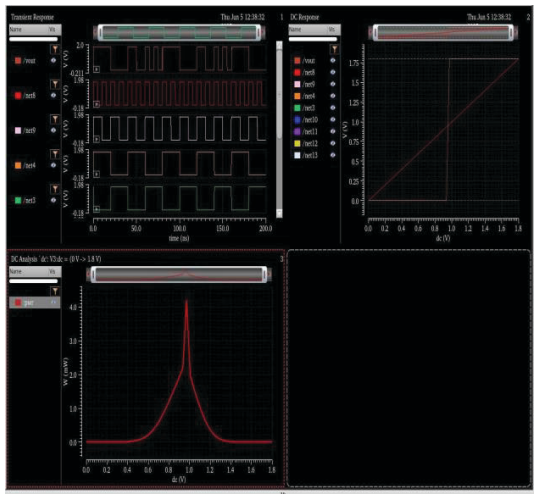


Fig.4. Output Waveforms for 4 x 1 MUX

IV. RESULTS AND DISCUSSIONS

The main goal of this project was to investigate the impact of the Stack ONOFIC technique on leakage power reduction in a 4×1 CMOS multiplexer design. To this end, two versions of the multiplexer circuit were created and simulated using Cadence software: a conventional design employing standard CMOS logic and an optimized version incorporating the Stack ONOFIC transistor stacking technique.

The simulation results clearly indicate a substantial reduction in leakage power with the Stack ONOFIC implementation. The conventional 4×1 multiplexer exhibited a power dissipation of approximately **459.1 uW** which can be seen in Figure 5, while the Stack ONOFIC-based design showed a significantly lower power of about **385 uW,** which is depicted in Figure 9. This corresponds to an impressive **16.12% decrease in power**, demonstrating the high efficiency of the Stack ONOFIC technique in suppressing subthreshold leakage currents.

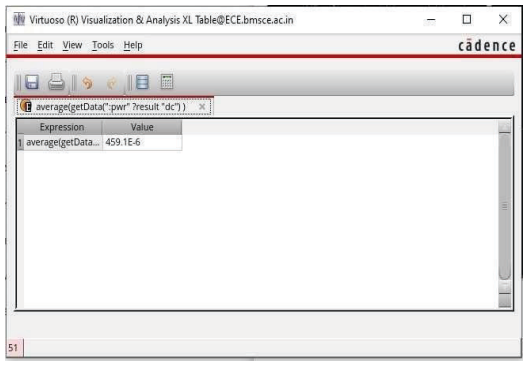


Fig.5. Overall Power for 4 x 1 MUX

The significant reduction can be attributed to the transistor stacking effect, which creates a higher effective threshold voltage in the off state and reduces leakage paths. By carefully arranging the transistors in series and

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optimizing their biasing, the Stack ONOFIC method limits the leakage current that flows through the device when it is supposed to be off, without compromising the circuit's switching speed or functional correctness.

In addition to the reduction in power, it is important to highlight that the Stack ONOFIC approach maintains the performance metrics of the multiplexer within acceptable limits. The trade-off between power savings and delay or output signal quality was found to be minimal, ensuring that the technique is suitable for practical applications where both energy efficiency and performance are crucial.

This reduction in power is particularly important in modern electronic devices such as smartphones, wearable gadgets, IoT nodes, and automotive electronics, where prolonged battery life and thermal management are essential. The results suggest that integrating the Stack ONOFIC technique at the circuit level can significantly contribute to overall system power savings, especially as devices continue to scale down in size and leakage currents become more prominent.

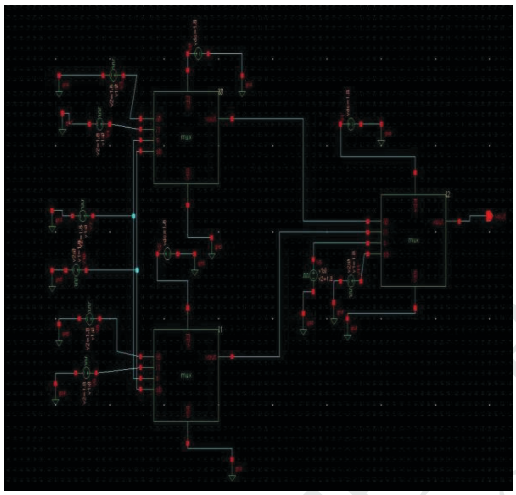


Fig.6. Circuit Diagram for Stacked 4 x 1using 2 x 1 MUX

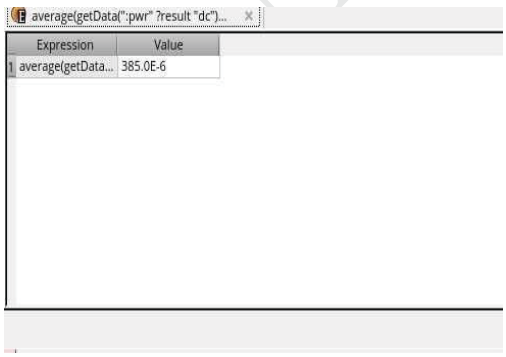


Fig.7. Overall Power in Stacked 4 x 1 MUX

V. Conclusions

This project successfully demonstrated the effectiveness of the Stack ONOFIC technique in reducing power in a 4 × 1 CMOS multiplexer. Through careful transistor stacking and optimized design implemented and simulated in Cadence the power was reduced by approximately 16.12% compared to the conventional multiplexer design. Importantly, this substantial power savings was achieved without significantly affecting the circuit's performance, making Stack ONOFIC a promising low-power design strategy. The results highlight the potential of this technique to enhance energy efficiency in modern electronic devices, particularly in power-sensitive applications such as IoT, mobile, and wearable technologies. Overall, the Stack ONOFIC approach contributes to the advancement of sustainable and high-performance integrated circuit design.

VI. Future Trends

As semiconductor technology advances toward smaller process nodes and increasingly complex System-on-Chip (SoC) architectures, effective management of leakage power has become critical. Future low-power VLSI design strategies are expected to integrate multiple techniques—such as transistor stacking, adaptive body biasing, power gating, and multi-threshold CMOS (MTCMOS)—to significantly reduce leakage currents. Additionally, machine learning-based design automation tools are poised to optimize circuit topologies for power efficiency more intelligently. The adoption of emerging device technologies, including FinFETs and gate-all-around (GAA) transistors, will further enhance the ability to minimize leakage. When these hardware-level approaches are combined with system-level power management strategies, they will pave the way for ultra-low-power electronics, particularly in next-generation applications such as Internet of Things (IoT) devices, wearable technologies, and other energy-constrained systems.

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Optimization of Asynchronous FIFO Design

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***Abstract*—A FIFO buffer is a fundamental component in digital systems, providing temporary storage to facilitate smooth data transfer between asynchronous clock domains. This paper presents an optimized FIFO design aimed at improving performance, resource utilization, and reliability. The primary focus areas include clock domain synchronization, efficient memory utilization, and performance enhancement through reduced metastability using Gray code addressing. Implemented using Verilog and verified through simulation, the design ensures scalability, high-speed operation, and suitability for applications such as network interfaces and real-time data streaming. (*Abstract*)**

Keywords—Asynchronous FIFO, Metastability, Gray Code, Synchronization, Digital Systems, Verilog (*key words****)***

I. INTRODUCTION

Asynchronous FIFO buffers play a crucial role in digital systems where components operate at different clock speeds. Unlike synchronous FIFOs, asynchronous FIFOs facilitate communication between circuits with independent clock domains. The major design challenges include metastability reduction, efficient synchronization, and optimized memory utilization. This paper proposes an optimized approach to asynchronous FIFO design, addressing these challenges using advanced techniques.By addressing timing discrepancies and data integrity challenges, asynchronous FIFOs play a vital role in modern electronics, enabling efficient communication across varying clock domains. Their widespread use ensures reliable performance in diverse fields, from consumer electronics to high-performance computing systems.

II. LITERATURE REVIEW

Research on asynchronous FIFO design has evolved to tackle key challenges such as metastability, clock domain synchronization, and data width conversion. Cummings (2002) introduced techniques for reliable flag generation, while Huang and Zheng (2011) proposed synchronizer circuits to mitigate metastability. Recent advancements by Kim et al. (2019) explored test methodologies to ensure robustness in real-time systems. This study builds on prior research by integrating Gray code addressing and enhanced synchronization techniques. Bing Qi Liu et al. (2014) researched methods to integrate asynchronous FIFOs into FPGA-based systems, focusing on achieving high performance and reliability in complex systems. Their work emphasized the critical role of synchronizers in reducing metastability and improving overall system performance.

III. PROBLEM ANALYSIS

*A. **Metastability Issues***

Signals crossing clock domains can become indeterminate, leading to data corruption. Proper synchronization mechanisms are essential to mitigate metastability effects. Metastability is unavoidable in asynchronous systems. Whenever asynchronous data is registered by a clocked flip-flop, there is a probability of setup or hold time violation on that flip-flop. Metastability is the inability of a flip-flop to arrive at a known state in a specific amount of time. When a flip-flop enters a metastable state, a designer cannot predict the output voltage level or when the output will settle to a correct voltage level. During this settling time, the flip-flop's output is at some intermediate voltage level or may oscillate and can cause a cascade of failures when the flip-flops further down the signal path capture the invalid output level. A Metastable causes For any flip-flop, there is a small window of time where the input must be stable.This window of time is a function of the design of the flip-flop, the implementation technology, operating conditions and the load on the output for outputs not buffered. Also sharp edge rates on the input signal minimize the window of time.

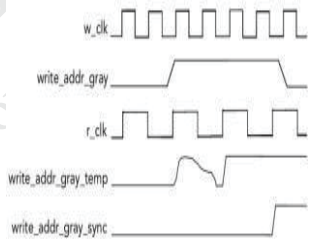


Fig 3.1- metastability

*B .**Timing Discrepancies***

Clock frequency variations may result in data loss, overflow, or underflow. These issues must be efficiently managed to ensure smooth data flow.

*C. **SYNCHRONIZATION COMPLEXITY***

Reliable data transfer necessitates effective control mechanisms to prevent errors caused by improper pointer updates.

These challenges are critical in high-reliability and performance-sensitive digital systems, where ensuring stable and accurate communication between different clock domains is essential. Therefore, addressing metastability, timing discrepancies, and control complexity is fundamental to the robust design of asynchronous FIFOs.

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IV. PROPOSED METHADOLOGY

A. *Dual-Port Memory Architecture*

- *The proposed FIFO design employs a dual-port memory structure to enable simultaneous read and write operations, enhancing data throughput. This architecture allows data to be written into the FIFO from one clock domain while being read out from another, facilitating smooth and efficient data flow.*

- *By decoupling the read and write operations, the design reduces contention and minimizes delays, ensuring that data is correctly buffered and transmitted between the two clock domains without interference.*

B. *Gray Code Addressing*

Using Gray code for read and write pointers minimizes metastability risks by ensuring single-bit transitions between successive values. The use of Gray code helps in synchronizing the pointers between the two clock domains by mitigating the risks associated with transitioning multiple bits simultaneously. This ensures more stable and accurate read and write operations, which is critical for reliable data transmission.

C. *Enhanced Synchronization Circuits*

- *Synchronization techniques using cascaded D flip-flops reduce timing mismatches and improve signal stability across clock domains. By delaying and stabilizing the control signals, these synchronization circuits help mitigate metastability, ensuring smooth transitions between clock domains. The cascaded flip-flop approach allows the signals to stabilize over multiple clock cycles, reducing the chances of metastable states.*

- *Additionally, Gray code pointers are synchronized using two-stage synchronization mechanisms, which ensures that the read and write pointers are safely transferred between clock domains without causing data corruption.*

D. *Data Width Conversion*

The FIFO supports flexible data width conversion, facilitating seamless communication between devices with different data bus sizes. To synchronize data flow across the clock domains, the design carefully coordinates the read and write processes using reliable synchronization protocols. This reduces the likelihood of data loss and ensures accurate data transmission across different clock frequencies.

V. IMPLEMENTATION

The FIFO design is implemented using Verilog and simulated using ModelSim. The key modules include:

- **Read Module**: *The read module of an asynchronous FIFO is responsible for retrieving data from the FIFO memory while operating on a separate clock domain from the write module. It typically consists of a read pointer that tracks the location of the next data to be read. A synchronized empty flag is used to indicate when the FIFO is empty, preventing underflow conditions. The read pointer is updated only when a read enable signal is asserted and the FIFO is not empty. A gray-coded version of the read pointer is often used for synchronization across clock domains. The read data is output from the FIFO memory once a valid read request is received.*

- **Write Module**: *Manages write operations and tracks FIFO fullness. n an asynchronous FIFO, the write operation occurs in a clock domain separate from the read domain. Data is written into the FIFO memory on the rising edge of the write clock (Wr_clk) when the write enable (Wr_en) is active and the FIFO is not full (Full flag is low). The write pointer increments with each valid write, and a status flag logic ensures synchronization between the write and read domains. To prevent overflow, the write logic must correctly interpret the full condition based on pointer comparisons.*

- **Synchronization Module**: *Synchronizes pointer values between clock domains. In an asynchronous FIFO, synchronization is essential to ensure reliable data transfer between two clock domains operating at different frequencies. This is achieved using dual-port memory along with synchronizer circuits for control signals like read and write pointers. The write clock domain updates the write pointer, while the read clock domain updates the read pointer. To prevent metastability and data corruption, gray-coded pointers are typically used, and a two-stage or three-stage synchronizer ensures safe pointer exchange between domains. This synchronization mechanism allows seamless and error-free communication between the producer and consumer in asynchronous FIFO operation.*

- **Testbench**: *An asynchronous FIFO testbench on FPGA is designed to verify the functionality of a FIFO buffer operating between two clock domains. It involves creating a simulation environment that mimics the behavior of the producer and consumer, which operate at different clock rates. The testbench typically includes a driver for generating random data inputs, a checker to verify data integrity during transfer, and clock generators for*

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both the read and write clocks. Additionally, the testbench monitors the FIFO status signals like full, empty, and almost full/empty, ensuring correct synchronization, pointer management, and proper handling of overflow and underflow conditions. This helps validate the FIFO's performance and robustness in an asynchronous environment.

VI. Results and Discussion

Simulation results validate the effectiveness of the proposed FIFO design. Key improvements include:

A. Reduced Metastability: Gray code synchronization ensures stable data transfer.

B. Efficient Memory Utilization: Parameterized FIFO structure allows dynamic configuration.

C. Optimized Timing Performance: Enhanced read and write logic minimizes latency.

SIMULATION:

EQUAL WIDTH:

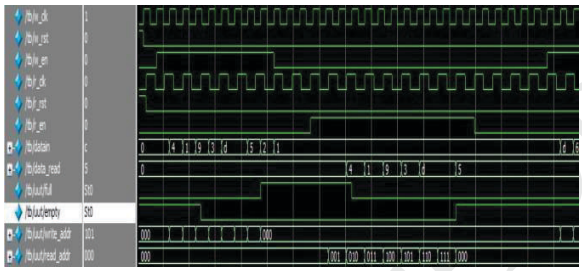


Fig 6.1- output when datain and dataout have equal widths

CONCATENATION:

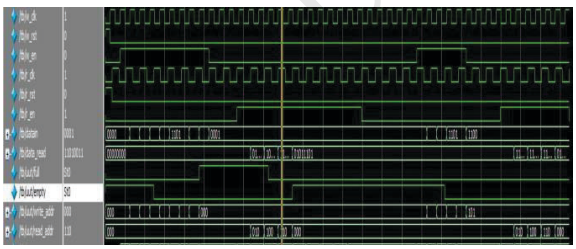


Fig 6.2- output when datain width is lesser than dataout width

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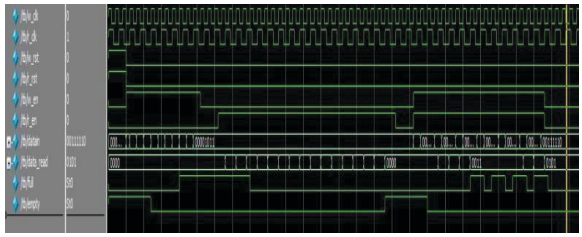


Fig 6.3- output when datain width is greater than dataout width

VII. Future Work and Conclusion

Future research can focus on integrating error detection mechanisms and power-efficient optimizations to further enhance fifo reliability. the proposed design offers a robust and scalable solution for high-speed digital systems, ensuring reliable asynchronous communication across clock domains.

1. *INTERFACING WITH UART:*

Interfacing an asynchronous FIFO with a UART (Universal Asynchronous Receiver-Transmitter) involves using the FIFO to buffer data between the transmitter and receiver in the UART system. Since UART operates asynchronously, the FIFO helps manage differences in data rates between the transmitting and receiving devices. The UART's transmit (TX) and receive (RX) lines communicate with the FIFO, where incoming data is written into the FIFO buffer by the receiver and read out by the system or application processor. Similarly, data to be transmitted is written to the FIFO by the processor and read out by the UART transmitter. This buffering ensures smooth data flow, minimizing data loss and allowing for efficient communication even when there is a mismatch in processing speeds.

2. *IMPLEMENTING ON FPGA:*

Implementing an asynchronous FIFO on an FPGA involves designing a dual-clock FIFO buffer that enables data transfer between two clock domains operating at different frequencies. The FPGA's architecture uses dual-port RAM to store data, with separate read and write pointers, which are synchronized using two or more flip-flops to avoid timing issues and metastability. Gray code is typically used for pointer tracking to minimize errors during pointer transitions. Additional control signals, such as full, empty, and overflow flags, ensure data integrity and proper operation. The FPGA implementation enables efficient and reliable data exchange in applications like communication systems or data buffering.

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3. *SELF TESTING TEST BENCH:*

An asynchronous FIFO self-testing test bench for FPGA involves creating a simulation environment that validates the functionality of the FIFO under different conditions. The test bench includes generating multiple clock signals with different frequencies for the read and write domains, applying various data patterns, and checking for data integrity. It uses stimulus generators to write data into the FIFO and read it back, ensuring proper synchronization between the domains. Additionally, the test bench monitors for corner cases like full/empty conditions, pointer synchronization errors, and timing violations. The results are verified using assertions and expected output comparisons to ensure correct operation of the FIFO on the FPGA.

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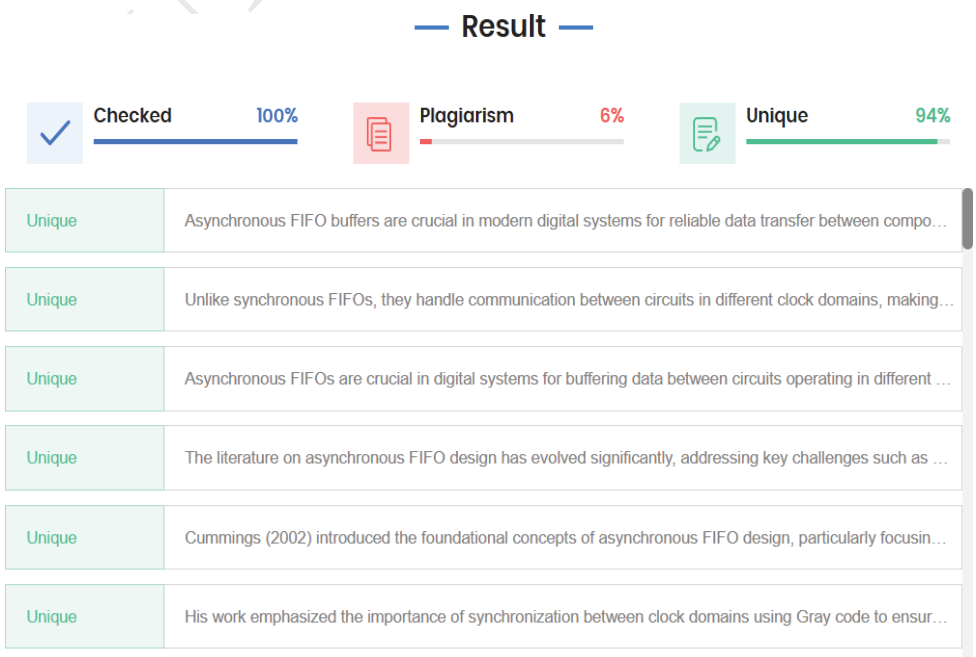
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PLAGIARISM REPORT



HYBRID ADDER IMPLEMENTATION USING VERILOG

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Abstract—This paper introduces the circuit design and implementation of hybrid adders using Verilog. By combining various adder design, such as Traditional adders like Ripple carry adder(RCA), Carry Look-Ahead Adder(CLA) and Carry Select adder(CSLA), the proposed design aims to enhance speed, power efficiency, and area optimization. The hybrid approach ensures a well-balanced arithmetic unit, making it suitable for high-performance computing applications. The design is developed in Verilog, tested through simulations, and evaluated through synthesis and performance analysis.

Keywords—Hybrid Adder, Verilog, VLSI, Digital Circuits, High-Speed Computation

I . INTRODUCTION

Adders are essential building blocks in digital circuits, forming the core of arithmetic and logic units (ALUs) used in microprocessors, digital signal processors (DSPs), and embedded systems. They perform fundamental mathematical operations, directly influencing the overall performance of a system. Over the years, various adder architectures have been developed to improve speed, reduce power consumption, and optimize hardware efficiency.

Ripple Carry Adders (RCA) are among the simplest adder designs, known for their straightforward structure. However, their sequential carry propagation makes them relatively slow, as each carry bit must ripple through all stages. In contrast, Carry Look-Ahead Adders (CLA) enhance speed by predicting carry signals in advance, significantly reducing delay. However, this increased speed will lead greater energy demand and circuit complexity, which may not be ideal for energy-efficient applications.

To strike a balance between speed, power efficiency, and hardware optimization, hybrid adders integrate multiple adder types, leveraging their advantages. A common approach is to use an RCA for lower-order bits, where carry delay is less significant, while employing a CLA or Carry Select Adder (CSLA) for higher-order bits, where faster carry computation is crucial. This combination enhances performance while keeping power consumption and circuit area within practical limits, making hybrid adders a preferred choice for high-speed processors, FPGA-based designs, and AI accelerators.

This Paper presents the design and execution of a Hybrid Adder using Verilog, a widely used hardware description language for digital circuit modeling. It explores the architecture, synthesis, and simulation results, evaluating key parameters such as speed,power efficiency and hardware consumption. By comparing hybrid adders with traditional designs, this study highlights their advantages in modern digital systems, including energy-efficient computing and high-performance VLSI applications. Additionally, potential optimizations and integration strategies are discussed to further improve efficiency.

By addressing the challenges and exploring potential optimization,this research aims to make hybrid adders to enhance speed, power and area for various applications.

II . LITERATURE SURVEY

Several studies have concentrated on how to better adder performance by delay reduction. A comparative study examines different types of customary with adders. It presents also a Hybrid Adder circuit so as to minimize propagation delay as it aims for faster digital systems [1], [4], [3], [5], [15], [16]. A different approach makes a 1-bit full adder using static cmos logic plus Swing Restoration Pass Transistor, and this betters both speed plus power efficiency [2]. Also explored is the Gate Diffusion Input technique because it reduces power consumption by using fewer transistors, making it ideal for low-power digital circuits [6].

These studies highlight efforts that are active so as to improve adder circuits, and the efforts focus upon designs that are faster and also more efficient in order to meet the needs of modern technology.

III . ADDERS

A. RCA

A Ripple Carry Adder (RCA) performs addition step by step, starting from the lower significant bit (rightmost bit). Each bit is added along with any carry from the previous step. If a carry is generated, it gets passed to the next bit, and this process continues across all the bits, with the carry essentially "rippling" from right to left. While simple and easy to implement, this method can be slow for large numbers since each bit must wait for the carry from the previous one before completing its calculation.

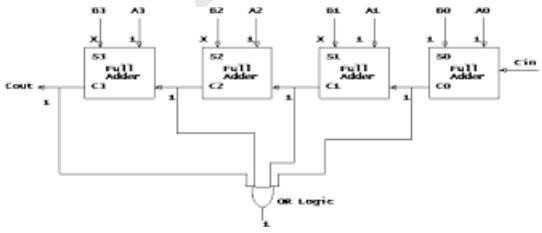


Fig 1. Ripple Carry Adder.

The Sum and Carry expressions are

Sum $S_i = A_i \oplus B_i \oplus C_{i-1}$

Carry $C_i = (A_i \cdot B_i) + (C_{i-1} \cdot (A_i \oplus B_i))$

B. Carry Lookahead Adder (CLA)

A CLA speeds up the addition process by computing carries more efficiently. Instead of waiting for the carry to ripple through each bit like in a Ripple Carry Adder, the CLA figures out the carries in advance. It does this by using two signals:

- **Generate (G)**: This checks if a carry is created at a particular bit .

  $G_i = A_i \cdot B_i$

- **Propagate (P)**: This checks if a carry should pass through to the next bit.

  $P_i = A_i \oplus B_i$

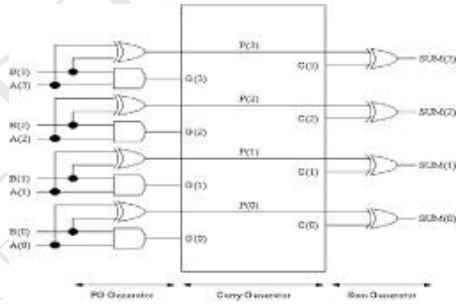


Fig 2. Carry Lookahead Adder.

The Carry equation is given by

$C_i = G_{i-1} + (P_{i-1} \cdot G_{i-2}) + \ldots$

C. CSELA

A CSLA is used to add two N-bit numbers and works faster than some other types, like the carry lookahead adder, by handling carry bits more effectively.

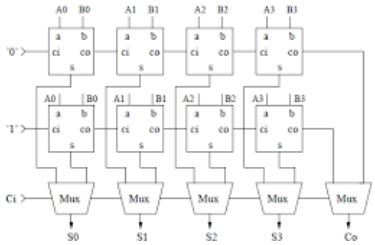


Fig 3 . Carry Select Adder.

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D. BKA

The Brent-Kung Adder is a clever way to increase up binary addition by tackling the biggest slowdown: carry propagation. Instead of waiting for each carry to pass through every bit like in a Ripple Carry Adder, it takes a more efficient, tree-like approach. First, it figures out two key signals for each bit Generate (G) and Propagate (P) which help determine how carries will move through the system. Then, rather than handling carries one at a time, it calculates them in parallel, significantly cutting down the delay. Once the carries are ready, the final sum is found by XORing the input bits with their respective carries. The Brent-Kung Adder strikes a great balance between speed and hardware efficiency, making it a smart choice for high-speed computations.

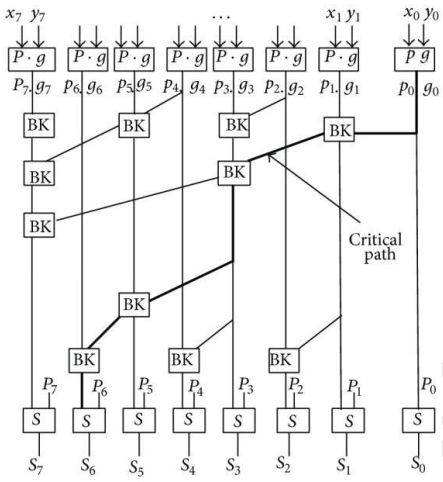


Fig 4. Brent Kung Adder block diagram.

E. KSA

The KSA is one of the fastest ways to perform binary addition because it minimizes the delay caused by carry calculations. Unlike simpler adders that process carries bit by bit, this adder uses a parallel approach with a tree-like structure. It first determines two key signals—Generate (G) and Propagate (P)—for each bit, then efficiently combines them across multiple stages to quickly compute the carries for all bits at once. This makes the Kogge-Stone Adder incredibly fast, especially for large numbers, but it comes at the cost of requiring more hardware and logic gates compared to other designs, like the Brent-Kung Adder. Its ability to handle high-speed computations makes it a top choice for performance-critical applications.

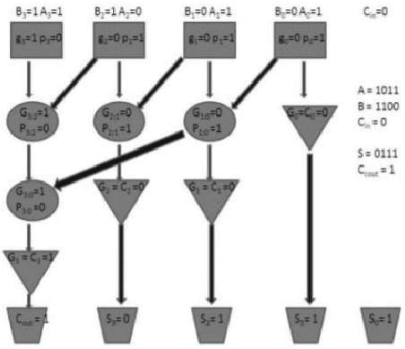


Fig 5. 4-bit KSA illustration

F. LFA

This is a type of parallel prefix adder designed for high-speed arithmetic operations. Known for its fast performance, it efficiently reduces delay while also keeping hardware usage relatively low. Its structured approach to carry computation makes it one of the fastest adders available, making it a popular choice in industries where speed and efficiency are crucial.

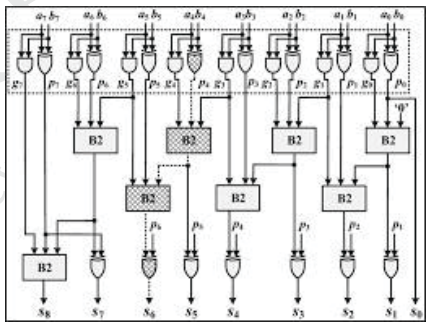


Fig 6. 8-bit Ladner Fischer Adder

IV. HYBRID ADDER

A hybrid adder combines 2 or more types of adders to improve efficiency by balancing out each other's weaknesses. This helps to better the performance in areas of speed, power consumption, and hardware usage. There are two main types: homogeneous hybrid adders, which use multiple adders of the same kind, and heterogeneous hybrid adders, which mix different types to optimize calculations. For example, an N-bit hybrid adder may incorporate different adders to handle internal carries, sums, and the final carry-out more effectively, making it a valuable choice for high-speed arithmetic operations.

A= 10010010 10001101 11011010 11011010

B= 10000000 01000001 00010101 01100101

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When you need to add two 32-bit values, one smart way is to break the problem down. That's where a hybrid adder comes in it handles different parts of the addition separately to make things more efficient

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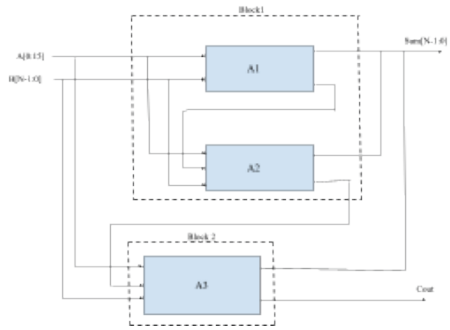


fig.7: Hybrid adder example

Imagine you're working with three adders: A1 and A2 handle 8 bits each, and A3 takes care of 16 bits. First, A1 adds the first 8 bits (bits 0 to 7). If there's a carry, it moves to A2, which works on bits 8 to 15. Any carry from A2 is then passed to A3. This last adder, A3, processes the top half—bits 16 to 31—and also gives the final carry-out. A1 and A2 together form one half of the system, a 16-bit block (let's call it Block 1). A3 is the other half, Block 2. When you put both blocks together, you get a 32-bit hybrid adder. A3 is responsible for the final output carry.The result of addition can be obtained as:
Sum = 00010010 11001110 11110000 01111111 and
Cout = 1

V. METHODOLOGY AND IMPLEMENTATION

Block Diagram

1) 16 bit CSLA + 8 bit KSA + 8 bit KSA

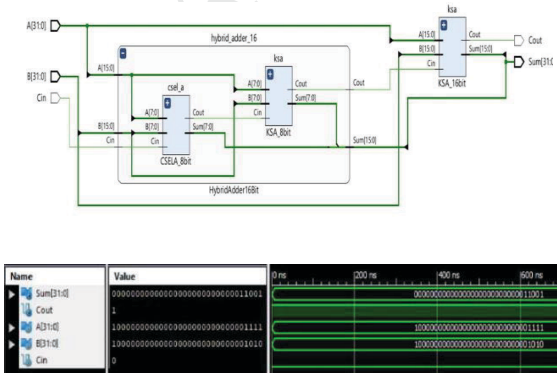


fig.8

2) 16 bit BKA + 16 bit KSA

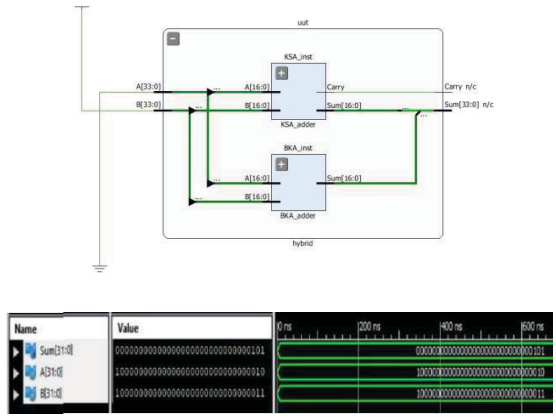


fig.9

3) (16 bit LFA + 16 bit KSA) + (16 bit HCA + 16 bit KSA)

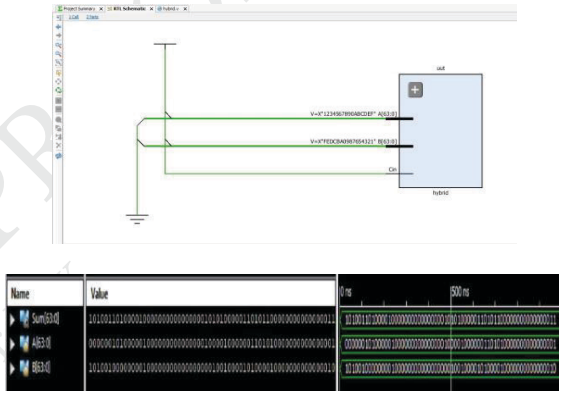


fig.10

VI . RESULTS AND DISCUSSIONS

ADDER DESIGN	AREA(IN LUTs)	POWER(IN W)
CARRY SELECT ADDER -16	35	0.027
KOGGE STONE ADDER-16	21	0.032
BRENT KUNG ADDER-16	18	0.025

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LANDER FISCHER ADDER-16	15	0.027
HAN CARLSON ADDER-16	20	0.030
CSLA_KSA_KSA	41	0.021
BKA_KSA	29	0.022
(LFA_KSA)+(HCA_KSA)	109	0.44

The table above presents a performance analysis of various hybrid adder designs based on key factors such as area and power consumption. This analysis is essential for comparing different adders to determine which one offers better efficiency and is best suited for specific applications. By evaluating these parameters, we can identify the most optimal adder design for various computational needs.

VII. FUTURE TRENDS AND CONCLUSION

The proposed system leverages hybrid adders to improve the speed and efficiency of digital processing. By analyzing 32-bit VLSI hybrid adders alongside traditional designs in terms of area, power consumption and delay,the system highlights their advantages. These adders can also be scaled to larger word sizes, such as 64-bit or 128-bit, making them highly valuable for modern integrated circuits. In addition, hybrid adders can efficiently perform operations like subtraction, multiplication, and bit complementing. Future advancements aim to develop higher-bit hybrid adders and integrate them into high speed multipliers. They also have the potential to serve as key components in advanced arithmetic logic units (ALUs), enhancing performance in next-generation VLSI systems

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Classification of Fatty Liver disease using CNN architectures

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***Abstract*—Fatty liver disease, particularly Non-Alcoholic Fatty Liver Disease (NAFLD), is a growing global health concern that may progress from simple steatosis to more severe conditions such as non-alcoholic steatohepatitis (NASH), fibrosis, and cirrhosis. A lack of early and accurate diagnostic tools can lead to delayed interventions and irreversible liver damage. In this study, Convolutional Neural Networks (CNNs) were developed and evaluated to detect and classify various stages of fatty liver disease using annotated histopathological and ultrasound image datasets. The dataset was split into 70% for training, 20% for testing, and 10% for validation. The CNN model leverages spatial feature extraction to distinguish between healthy, mild, moderate, and severe fatty liver conditions. The deep learning approach aims to improve diagnostic accuracy, reduce clinical subjectivity, and streamline the screening process. Results indicate that the CNN model performs with high sensitivity and specificity, showing strong potential for aiding clinical decision-making in liver disease management.**

Keywords— Fatty liver, NAFLD, liver disease, CNN, deep learning, medical imaging, diagnosis, histopathology, ultrasound

I. Introduction

Fatty liver disease, medically referred to as hepatic steatosis, has emerged as a significant global health burden, closely associated with rising incidences of obesity, type 2 diabetes, insulin resistance, and other metabolic syndromes. As the prevalence of lifestyle-related diseases continues to escalate, so does the incidence of fatty liver disease, making early diagnosis and accurate staging critical components to preventing its progression to more advanced stages such as nonalcoholic steatohepatitis (NASH), fibrosis, cirrhosis, or hepatocellular carcinoma. Current diagnostic standards, such as liver biopsy and manual evaluation of ultrasound or histopathological images, are often invasive, costly, time-intensive and highly dependent on the expertise of the clinician, leading to inconsistencies and diagnostic subjectivity. To address these limitations, recent advances in artificial intelligence, particularly in the field of deep learning, offer promising alternatives. Convolutional Neural Networks (CNNs), known for their superior performance in visual pattern recognition, have gained prominence in medical image analysis. These networks are able to automatically learn hierarchical features and spatial relationships from input images, making them highly effective for classifying complex structures and subtle changes in tissue appearance. In the context of fatty liver disease, CNNs can be trained to detect and differentiate between various stages of the disease, ranging from healthy liver tissue to mild, moderate, and severe steatosis, using non-invasive imaging data such as ultrasound. This study investigates the potential of CNN-based models in enhancing the diagnostic process for fatty liver disease. A comprehensive data set comprising annotated liver ultrasound images is utilized, with the model trained, validated, and tested on distinct subsets to ensure generalization and robustness. The results indicate that CNN achieves high sensitivity and specificity in different grades of fatty liver, supporting its utility as a reliable, efficient, and consistent screening tool. The proposed deep learning approach not only minimizes diagnostic subjectivity and clinical workload, but also facilitates early detection, enabling timely intervention and improved patient outcomes. Fatty liver disease is increasingly prevalent worldwide, often progressing silently to severe stages like cirrhosis or liver cancer. Leveraging Convolutional Neural Networks (CNNs) enables accurate, noninvasive detection, and classification of its stages from ultrasound images. This AI-driven approach enhances early diagnosis, reduces reliance on invasive methods, and supports timely clinical intervention. Keywords— Fatty liver disease, hepatic steatosis, NAFLD, CNN, deep learning, liver ultrasound, medical imaging, non-invasive diagnosis, image classification, early intervention.

A. Abbreviations and Acronyms

Throughout this paper, several abbreviations and acronyms are used. Each term is defined upon its first appearance in the text and listed below for reference:

- **CNN** - Convolutional Neural Network
- **NAFLD** - Non-Alcoholic Fatty Liver Disease
- **NASH** - Non-Alcoholic Steatohepatitis

Early Version

- **ROI** - Region of Interest
- **FCNN** - Fully Connected Neural Network
- **AUROC/AUC** - Area Under the Receiver Operating Characteristic Curve
- **HI** - Hepatorenal Index
- **GLCM** - Gray-Level Co-Occurrence Matrix
- **SVM** - Support Vector Machine
- **KNN** - K-Nearest Neighbors
- **GNB** - Gaussian Naive Bayes
- **GBoost/XGBoost** - Gradient Boosting / Extreme Gradient Boosting
- **MRI** - Magnetic Resonance Imaging
- **T1, T2** - MRI Sequence Types
- **F0-F4** - Fibrosis Stages 0 to 4
- **RGB** - Red Green Blue
- **ReLU** - Rectified Linear Unit
- **Swish** - Swish Activation Function
- **Adam** - Adaptive Moment Estimation
- **API** - Application Programming Interface
- **Keras/TensorFlow** - Deep Learning Frameworks
- **NAS** - Neural Architecture Search
- **F1-Score** - Harmonic Mean of Precision and Recall

II. Related Work

Several studies in recent years have explored the application of machine learning and deep learning techniques for the detection and classification of liver diseases, particularly fatty liver and cirrhosis. Early approaches relied heavily on traditional machine learning algorithms such as Support Vector Machines (SVM), Random Forests, and Decision Trees, which rePaper [2] proposed an automated fibrosis classification system integrating image quality assessment and region-of-interest selection with a fully connected neural network (FCNN), achieving an AUROC of 0.93—significantly outperforming manual interpretation methods. Similarly, Paper [3] employed transfer learning using a pre-trained Inception-ResNet-v2 model for fat quantification from ultrasound images, achieving an AUC of 0.977, thus reducing operator dependency and improving diagnostic precision. Paper [4] compared multiple machine learning classifiers including SVM, KNN, and CNNs for cirrhosis prediction and found that CNNs outperformed traditional methods with the highest accuracy (84%). Further, Paper [5] introduced a multi-modal diagnostic system combining MRI data and serum biomarkers using CNNs, achieving an AUC of 0.86 across a diverse patient population. Paper [6] focused on early cirrhosis detection using ensemble machine learning techniques (Gradient Boosting, Boost, Random Forest), reaching accuracy rates of 92% and AUC-ROC scores of 0.95. These studies collectively emphasize the transition from manual and semi-automated methods to deep learning-based systems, validating the use of CNN architectures—such as ResNet50, MobileNetV2, and EfficientNetB0—in this project for efficient, scalable, and non-invasive classification of fatty liver stages from ultrasound images.

III. Methodology

The study employs transfer learning by utilizing pre-trained CNN architectures **ResNet50, MobileNetV2, EfficientNetB0** that have been previously trained on the large-scale ImageNet dataset. The top (fully connected) layers of these networks are removed, and custom classification heads are added. These consist of a GlobalAveragePooling2D layer, followed by one or more Dense layers with activation functions like ReLU (for ResNet50 and MobileNetV2) or Swish (for EfficientNetB0), along with Dropout layers to prevent overfitting, and finally, a Dense (1) layer with sigmoid activation for binary classification (steatosis or non-steatosis). During training, the convolutional base of the network is initially frozen to retain previously learned features and later fine-tuned by unfreezing the last 20–35 layers for better task-specific adaptation. Training is conducted using the Adam optimizer with a learning rate set to 0.0001 and binary cross-entropy as the loss function. Each model is trained for 20–37 epochs with a batch size of 32–47, depending on the architecture used. Important callbacks such as Early Stopping (to prevent unnecessary training when performance plateaus), Model Checkpoint (to save the best-performing model), and ReduceLROnPlateau (to dynamically lower the learning rate when improvement slows) are employed to optimize training performance and model generalization. After training, the models are evaluated using a separate test dataset, and performance is assessed using metrics like accuracy, precision, recall, F1-score, and confusion matrices for each class (F0 – F4). MobileNetV2 demonstrates high accuracy and efficiency, making it highly suitable for deployment in real-time clinical settings, especially where computational resources are limited. The methodology thus ensures a robust, scalable, and non-invasive diagnostic system for early detection and monitoring of fatty liver disease.

A. Dataset Collection and Preparation

The project begins with acquiring a diverse set of ultrasound liver images. These images were sourced from a publicly available Kaggle dataset titled **High-Resolution Ultrasound Images for Classifying Fatty Liver Stages**. The images represent **various stages of fatty liver disease**, from normal (F0) to severe (F4). The dataset initially comprises grayscale images, which are not directly compatible with standard CNN architectures that require 3-channel RGB images. To address this, each grayscale image is converted to RGB format by duplicating the single channel. Images are resized to 224×224 pixels to match the expected input dimensions of pretrained CNN models (like ResNet50, MobileNetV2, EfficientNetB0). Pixel values are normalized to the [0,1] range to facilitate faster convergence during training. This step ensures that pixel intensity differences don't cause erratic model behavior.

B. Image Augmentation

Deep learning models, especially CNNs, are prone to overfitting when trained on limited datasets. To mitigate this, Data augmentation techniques are applied to artificially expand the

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training dataset and introduce diversity. **Augmentation methods** used include **rotation** by ±15–20° to simulate different scanning angles, **horizontal flipping** to mimic variations in patient orientation, **zooming** (within 0.8–1.2 scale range) to simulate differences in magnification levels, brightness and contrast changes to ensure robustness under different ultrasound machine settings. These transformations ensure that the model learns invariant features and can generalize well to unseen real-world images.

C. Transfer Learning Setup

Instead of training CNNs from scratch (which requires massive data and compute), the project leverages **transfer learning approach** which involves **using pretrained models** (ResNet50, MobileNetV2, EfficientNetB0) **trained** on the **ImageNet dataset** as **feature extractors.** These models are imported with their f**inal classification layers removed**. The **core convolutional layers** are initially **frozen** to **preserve previously learned features**, such as edge detection, texture patterns, and shapes. Each architecture was chosen for specific advantages, **ResNet50** handles deep networks well due to **residual connections**, **MobileNetV2** is **lightweight** and **suitable for real-time or mobile environments** and **EfficientNetB0** balances **performance and efficiency** via compound scaling.

D. Model Architecture Customization

Since the base networks are trained on a different task (ImageNet classification), the top of each model is customized for binary classification (fatty vs. non-fatty liver). The added layers include, GlobalAveragePooling2D which Reduces feature map dimensions while preserving spatial features, Dense layer (256 or 512 units) with ReLU or Swish activation adds nonlinear transformation capability, Dropout layer (rate 0.3–0.5) randomly drops neurons during training to prevent overfitting. Dense(1) output layer with Sigmoid activation which provides probability score for binary classification. This customized head enables the model to map learned features to the target output class effectively.

E. Training Configuration

The model is compiled and trained with careful tuning of parameters:

- **Optimizer**: Adam is chosen for its adaptive learning rate and fast convergence.
- **Loss Function**: Binary Cross entropy is used since it is a binary classification problem.
- **Learning Rate**: Set to a low value (0.0001) to ensure gradual updates during transfer learning.
- **Batch Size**: 32–47 images per batch (varies per model) are used for gradient updates.
- **Epochs**: Models are trained for 20–37 epochs.
- **Callbacks**: EarlyStopping monitors validation loss and stops training when improvement halts.

ModelCheckpoint saves the best-performing model during training. **ReduceLROnPlateau** lowers the learning rate if validation accuracy plateaus. These settings ensure efficient and stable training of the models.

F. Model Evaluation

Once training is complete, the model is **evaluated on a separate test set** (20% of total data). Several performance metrics are used:

- **Accuracy**: Overall correctness of predictions.
- **Precision**: How many predicted positives were actually correct.
- **Recall**: How many actual positives were correctly identified.
- **F1-score**: Harmonic mean of precision and recall for balanced evaluation.
- **Confusion Matrix**: Visualizes performance across all fatty liver stages (F0 to F4).
- **Confidence Scores**: Indicates model certainty on specific predictions.

These metrics help understand not only whether the model is correct, but **how confident and balanced** it is across all disease stages.

G. Fine-Tuning

After initial training with frozen base layers, selected **deeper layers** of the pretrained base are **unfrozen** and the model is **recompiled** and **retrained with a lower learning rate** . This **fine-tuning** phase improves performance further by allowing the model to adapt its learned features specifically to ultrasound liver images. Different models unfroze varying numbers of layers:

- **ResNet50**: Last 35 layers
- **MobileNetV2**: Last 20 layers
- **EfficientNetB0**: Last 30 layers

Fine-tuning helps increase model adaptability without causing overfitting.

H. Architectures of the CNN Models

*1) **ResNet50**:* **ResNet50** is employed as a deep learning model to classify stages of fatty liver disease from ultrasound images. The model, imported from Keras with **pretrained ImageNet weights**, uses **residual connections** to overcome vanishing gradient issues and is particularly effective for analyzing low-contrast, noisy medical images. In the implementation, the original top classification layers are removed (include_top=False), and a custom head is added, consisting of a **GlobalAveragePooling2D** layer, a **Dense layer with 512 units and ReLU activation**, a **Dropout layer (0.5)** to reduce overfitting, and a final **Dense layer with sigmoid activation** for binary classification. The **Adam optimizer** is used with a learning rate of **0.0001**, and the model is trained for **20 epochs** with a batch size of **32**. Image augmentation techniques such as rotation, flipping, and zooming are applied to enhance model generalization. ResNet50 shows strong performance in feature extraction, enabling accurate staging of fatty liver disease despite limited training data.

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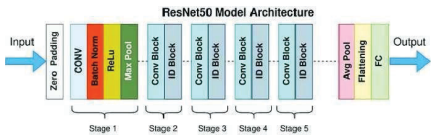


Fig. 1. Architecture of ResNet50

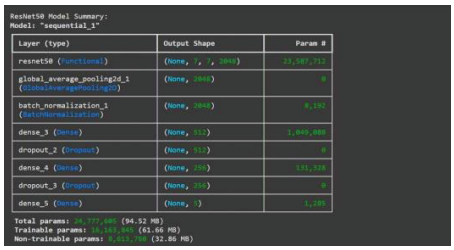


Fig. 2. Model Summary of ResNet50

*2) **MobileNetV2**:* MobileNetV2 is utilized as an efficient, lightweight CNN model ideal for real-time fatty liver disease detection, especially in low-resource or portable clinical environments. It incorporates **depthwise separable convolutions** and **inverted residuals with linear bottlenecks**,allowing it to maintain high classification performance with reduced computational cost. The model is imported with **pretrained ImageNet weights**, excluding the top layer (include_top=False), and is modified by adding a **GlobalAveragePooling2D layer**, followed by a **Dense layer with 256 units and ReLU activation**, a **Dropout layer (0.3)**, and a final **Dense layer with sigmoid activation** for binary classification. Training is performed using the **Adam optimizer** with a **learning rate of 0.0001**, over **20 epochs** with a **batch size of 32**. Image augmentation techniques such as rotation, flipping, and zooming are applied to increase model robustness. MobileNetV2 demonstrated high accuracy and consistency across various stages (F0–F4), making it a practical and reliable model for medical deployment.

*3) **EfficientNetB0** :* **EfficientNetB0** is employed as a high-performance CNN model for classifying fatty liver disease stages using ultrasound images. Developed through **Neural Architecture Search (NAS)**, it uses **compound scaling** to uniformly scale depth, width, and resolution, resulting in strong accuracy with fewer parameters. The model is loaded with

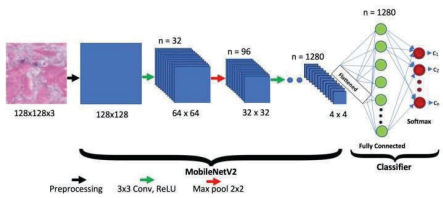


Fig. 3. Architecture of MobileNetV2

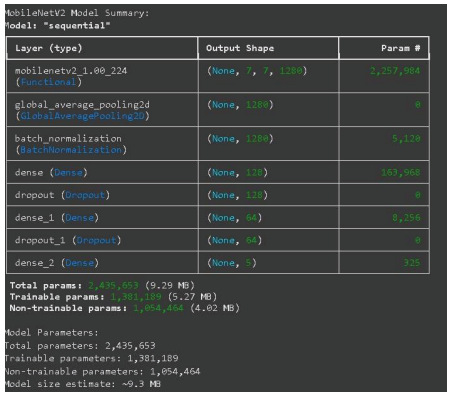


Fig. 4. Model Summary of MobileNetV2

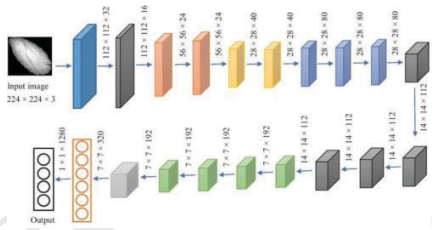


Fig. 5. Architecture of EfiicientNetB0

ImageNet pretrained weights (include_top=False) and enhanced with a custom classification head: a **GlobalAveragePooling2D layer**, a **Dense layer with 256 units and Swish activation**, a **Dropout layer (0.4)** to reduce overfitting, and a final **Dense layer with sigmoid activation** for binary classification. The model is compiled using the **Adam optimizer** with a **learning rate of 0.0001**, trained over **35 epochs** with a **batch size of 47**. Data augmentation strategies like rotation, brightness shifts, and flipping are applied to ensure generalization. EfficientNetB0 achieved near-perfect classification accuracy across all fibrosis stages (F0–F4), making it a powerful and optimized model for real-world clinical applications.

IV. Results and Discussion

The performance of MobileNetV2, EfficientNetB0, and ResNet50 for classifying fatty liver disease stages (F0 to F4) is carefully analyzed using metrics like accuracy, precision, and recall, along with confidence scores and confusion matrices. **MobileNetV2** really shines here, **delivering consistent and reliable results** across the board. It scores a perfect **100% accuracy, precision, and recall for F0**, and **performs strongly for other stages too - 94.57% accuracy** for **F1**, **75.63%** for **F2**, **84.50%** for **F3**, and an impressive **97.65%** for **F4**. With **high recall for F1 (94.57%)** and **F4 (97.65%)** and a **confidence score of 0.744 for an F1 prediction**, it's clear **MobileNetV2 rarely misses critical cases**, making it a solid choice for real-world medical use. **EfficientNetB0** also

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EfficientNetB0 Model Summary:
Model: "sequential_2"

Layer (type)	Output Shape	Param #
efficientnetb0 (Functional)	(None, 7, 7, 1280)	4,049,571
global_average_pooling2d_2 (GlobalAveragePooling2D)	(None, 1280)	0
batch_normalization_2 (BatchNormalization)	(None, 1280)	5,120
dense_6 (Dense)	(None, 128)	163,968
dropout_4 (Dropout)	(None, 128)	0
dense_7 (Dense)	(None, 64)	8,256
dropout_5 (Dropout)	(None, 64)	0
dense_8 (Dense)	(None, 5)	325

Total params: 4,227,240 (16.13 MB)
Trainable params: 1,671,269 (6.38 MB)
Non-trainable params: 2,555,971 (9.75 MB)

Model Parameters:
Total parameters: 4,227,240
Trainable parameters: 1,671,269
Non-trainable parameters: 2,555,971
Model size estimate: ~16.1 MB

Fig. 6. Model Summary of EfiicientNetB0

does incredibly well, hitting **100% accuracy** for **F0** and **F4**, **99.22%** for **F1**, **99.16%** for **F2**, and **96.90%** for **F3**, with top-notch **precision** (like **100%** for **F1**). But there's a catch - its **confidence scores**, like **0.545** for one **F1** prediction (though another hits **0.971**), suggest it can be a bit **uncertain at times**, which questions its consistency in tricky cases. **ResNet50**, on the other hand, Classification of Fatty Liver disease using CNN architectures struggles a bit. It nails **F0, F1**, and **F4** with **100% accuracy**, but drops to **98.32%** for **F2** and a concerning **93.80%** for **F3**, with **precision** dipping to **94.35%** for **F2**, hinting at **more false positives.** Its **confidence scores—0.766** for **F1** and **0.815** for **F3** are decent, but it's **prone to incorrect predictions**, especially for F3, as the report points out. The confusion matrices and prediction visualizations back this up: **MobileNetV2 handles most classes well with some hiccups in the middle stages**, **EfficientNetB0 is nearly flawless but shows occasional hesitation**, and **ResNet50 has more misclassifications**, particularly for F3. All in all, **MobileNetV2** feels like the **most trustworthy**, **EfficientNetB0** is **super accurate but leaves some room for doubt**, and **ResNet50 just doesn't quite keep up with the others due to its errors**.

TABLE I
PERFORMANCE METRICS OF CNN MODELS FOR FATTY LIVER DISEASE CLASSIFICATION

Model	Class	Accuracy	Precision	Recall
MobileNetV2	F0	1.0000	1.0000	1.0000
MobileNetV2	F1	0.9457	0.8414	0.9457
MobileNetV2	F2	0.7563	0.8491	0.7563
MobileNetV2	F3	0.8450	0.9083	0.8450
MobileNetV2	F4	0.9765	0.9540	0.9765
EfficientNetB0	F0	1.0000	1.0000	1.0000
EfficientNetB0	F1	0.9922	1.0000	0.9922
EfficientNetB0	F2	0.9916	0.9672	0.9916
EfficientNetB0	F3	0.9690	0.9921	0.9690
EfficientNetB0	F4	1.0000	0.9961	1.0000
ResNet50	F0	1.0000	1.0000	1.0000
ResNet50	F1	1.0000	1.0000	1.0000
ResNet50	F2	0.9832	0.9435	0.9832
ResNet50	F3	0.9380	0.9837	0.9380
ResNet50	F4	1.0000	0.9961	1.0000

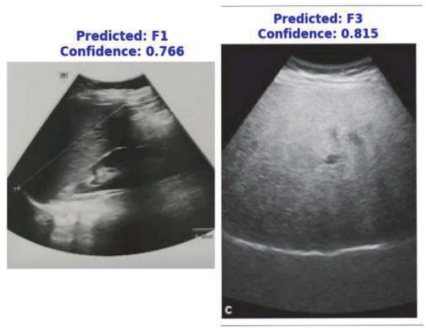


Fig. 7. Real time image prediction using ResNet50

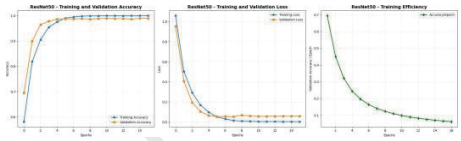


Fig. 8. Result Visualization for ResNet50

V. CONCLUSION

The study successfully demonstrates the potential of Convolutional Neural Networks (CNNs) in accurately detecting and classifying the stages of fatty liver disease using ultrasound images. By employing deep learning models such as MobileNetV2, EfficientNetB0, and ResNet50 with transfer learning, the system achieved high levels of accuracy, precision, and recall across various stages (F0–F4). This approach not only reduces reliance on invasive techniques like biopsies but also addresses the limitations of manual interpretation, such as subjectivity and diagnostic delays. Among the models evaluated, MobileNetV2 proved to be the most efficient and reliable for real-time clinical application, while EfficientNetB0 delivered exceptional accuracy across all stages. The integra-

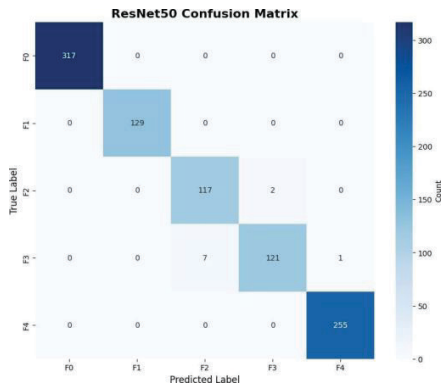


Fig. 9. Confusion Matrix of ResNet50

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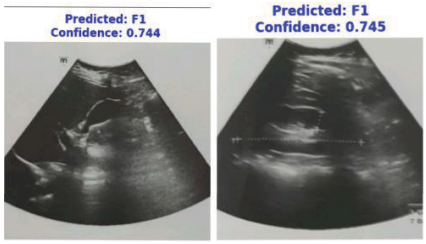


Fig. 10. Real time image prediction using MobileNetV2



Fig. 11. Result Visualization for MobileNetV2

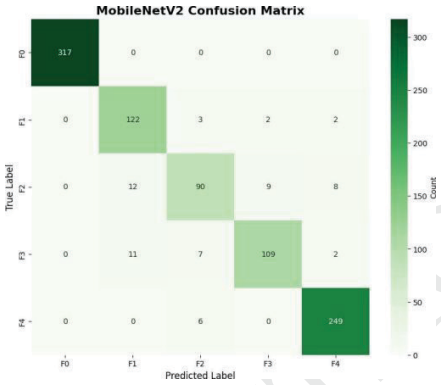


Fig. 12. Confusion Matrix of MobileNetV2

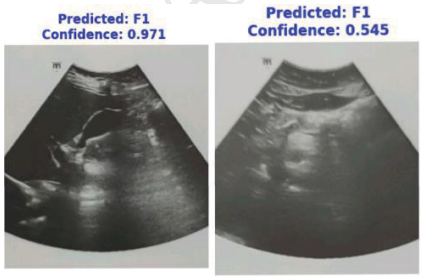


Fig. 13. Real time image prediction using EfficientNetB0



Fig. 14. Result Visualization for EfficientNetB0

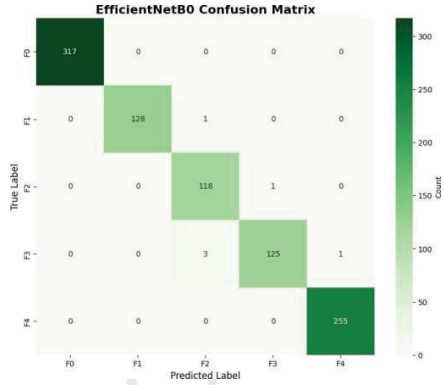


Fig. 15. Confusion Matrix of EfiicientNetB0

tion of CNNs into medical diagnostics can greatly enhance early screening, improve clinical decision-making, and enable scalable liver disease management, especially in resource-constrained settings.

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SYNCHRONISED AES IMPLEMENTATION ON UART WITH REDUCED LATENCY

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***Abstract*—The project "Synchronized AES Design and Implementation on UART with Reduced Latency" integrates Advanced Encryption Standard (AES) encryption with Universal Asynchronous Receiver-Transmitter (UART) communication to ensure secure and efficient data transmission in embedded systems and FPGA Devices. It addresses the growing need for secure data exchange in IoT devices and other resource-constrained environments. The synchronization mechanism minimizes delays by ensuring both the transmitter and receiver operate in unison, enhancing the reliability and security of communication. By optimizing hardware and software, the project achieves decent latency, with UART configured to a baud rate range of 115200 to 230400, ensuring fast data transfer while maintaining data integrity.**

The project synchronizes AES encryption and decryption processes through pipelining and parallel processing, minimizing delays and ensuring secure transmission. The use of high baud rates, combined with parity bit error checking, helps detect single-bit errors, adding an additional layer of error checking. Optimizing the encryption routine allows seamless integration of secure data handling into the communication protocol. The system is highly suitable for real-time applications requiring secure communication, such as IoT and industrial automation, where both speed and security are critical. This project demonstrates an efficient AES implementation over UART with reduced latency for secure and reliable data exchange.

***Index Terms*—AES, UART, Encryption, Decryption, Secure Communication, FPGA, Embedded Systems, Low Latency.**

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I. Introduction

With the rapid growth of embedded systems, secure communication has become a critical requirement. Traditional UART communication lacks encryption, making it vulnerable to various security threats such as eavesdropping and data tampering. To address this, Advanced Encryption Standard (AES) is often employed to ensure data security. However, integrating AES with UART in real-time applications introduces challenges, especially in synchronizing the encryption and data transfer processes, which can lead to delays or errors in communication.

Our architecture solves these synchronization issues by using specialized wrappers that coordinate the AES encryption and UART data transmission processes. These wrappers effectively manage data flow, ensuring that encryption and transmission occur simultaneously without introducing delays. By implementing this pipeline-optimized AES-UART interface, our design achieves synchronized encryption and decryption, improving overall throughput while maintaining real-time performance. This makes the architecture suitable for resource-constrained environments, such as IoT devices, where both security and speed are critical.

A. Importance of Secure Communication

Security in data communication ensures confidentiality, integrity, and authentication. The increasing deployment of IoT devices requires a secure yet efficient method to transmit data over UART interfaces.

B. Challenges in AES Integration with UART

AES requires computational power that might increase latency in real-time systems. UART communication introduces challenges related to synchronization, error handling, and data framing. Our proposed system overcomes these challenges using an efficient architecture design.

II. Proposed Architecture

The proposed architecture consists of six primary modules:

- AES Encryption Module
- UART TX Module
- UART TX Controller
- UART RX Module
- UART RX Controller
- AES Decryption Module

Each module works effectively, ensuring efficient and synchronized data flow.

The block diagram illustrates the interaction between these modules. The AES Encryption Module first processes the

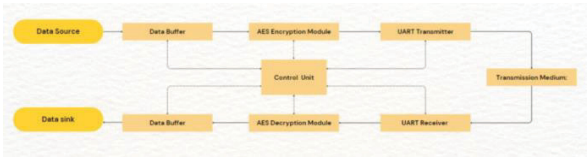


Fig. 1. Proposed System Architecture

plaintext and encryption key, generating the encrypted data. This data is passed to the UART TX Module, which serializes and transmits it under the control of the UART TX Controller. At the receiving end, the UART RX Module receives the encrypted data and converts it back to parallel form, with the UART RX Controller ensuring proper synchronization. Finally, the AES Decryption Module takes the received ciphertext and decrypts it, recovering the original plaintext.

The architecture ensures secure and efficient data communication, utilizing AES encryption and UART transmission, making it suitable for applications requiring robust data security.

III. Methodology

A. AES Encryption Process

AES follows multiple rounds of substitution, shifting, and mixing operations to transform plaintext into ciphertext. Each round consists of the following operations:

1) **Key Expansion**: The original encryption key is expanded into multiple round keys using a key schedule algorithm. Each round uses a unique subkey derived from the original key.
2) **Sub Bytes (S-Box Transformation)**: Each byte of the plaintext is replaced with a corresponding byte from a predefined substitution box (S-Box). This introduces non-linearity, making the encryption resistant to linear and differential cryptanalysis.
3) **Shift Rows Operation**: The rows of the state matrix are cyclically shifted by a specific number of bytes. The first row remains unchanged, the second row shifts one byte to the left, the third row shifts two bytes, and the fourth row shifts three bytes. This step ensures diffusion across columns.
4) **Mix Columns Transformation**: Each column of the state matrix undergoes a mathematical transformation using a fixed matrix multiplication over a finite field. This step increases diffusion by spreading the influence of each byte over multiple bytes in the same column.
5) **Add Round Key**: The state matrix is XORed with the corresponding round key derived from the key expansion process. This step ensures that encryption is dependent on the key, making decryption infeasible without it.

B. UART Transmission Process

The UART TX module is responsible for converting encrypted data into a serial format suitable for transmission. This module ensures proper data transmission by handling:

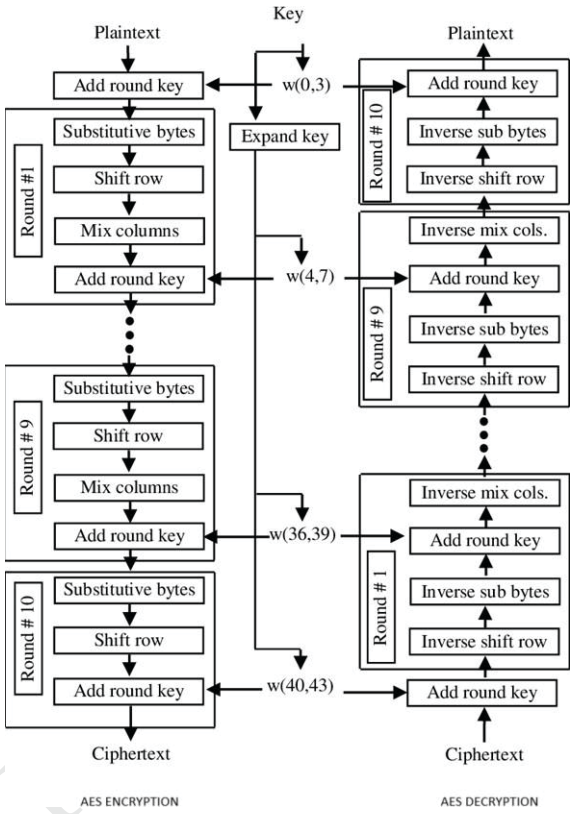


Fig. 2. AES Encryption and Decryption Block Diagram

- **Correct Data Framing**: The data is framed with a start bit, data bits, an optional parity bit, and a stop bit to ensure proper synchronization at the receiver end.
- **Baud Rate Synchronization**: The data is transmitted at a predetermined baud rate to ensure proper timing alignment between the transmitter and receiver.
- **Error Detection via Parity Checks**: An even parity bit is used to detect errors during transmission, helping to identify single-bit corruption.

1) UART Finite State Machine (FSM): The UART transmission process is managed using a finite state machine (FSM) to ensure proper sequencing of the transmission stages. The FSM consists of four primary states:

1) **IDLE State**: The transmitter remains in this state until a transmission request is initiated. The TX line stays high in this state.
2) **START State**: Once transmission begins, the TX line is pulled low to indicate the start bit.
3) **DATA State**: The encrypted data is transmitted bit by bit in sequential clock cycles. After all data bits are sent, an additional parity bit is transmitted for error checking.
4) **STOP State**: A stop bit (high) is transmitted to indicate the end of the frame. Once complete, the FSM returns

to the IDLE state, waiting for the next transmission.

This FSM ensures reliable and synchronized UART transmission by transitioning through these states in a controlled manner. The process guarantees that the AES-encrypted data is properly serialized and transmitted with minimal errors.



Fig. 3. UART Transmission FSM

C. UART TX Controller

The UART TX Controller plays a crucial role in managing the transmission of encrypted data. It ensures that the AES-encrypted ciphertext is properly divided into 8-bit segments and sequentially transmitted. The controller monitors the encryption completion signal and waits for the UART TX module to complete transmission before sending the next data packet. A counter helps regulate the timing of data transmission, ensuring synchronization with the UART TX module.

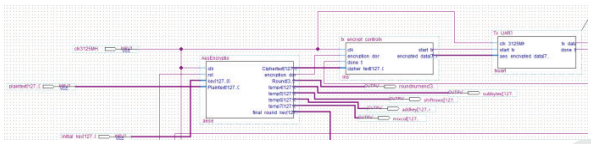


Fig. 4. UART TX Encryption Block Diagram

D. UART Reception Process

The UART RX module is responsible for receiving the encrypted data in a serial format and converting it into a parallel format for processing. This module ensures proper data reception by handling:

- **Correct Data Framing**: The received data includes a start bit, data bits, an optional parity bit, and a stop bit for synchronization.
- **Baud Rate Synchronization**: The data is received at a predetermined baud rate to ensure timing alignment between the receiver and transmitter.
- **Error Detection via Parity Checks**: An even parity bit is used to detect errors during reception, identifying potential single-bit corruption.

1) UART Finite State Machine (FSM): The UART reception process is managed using a finite state machine (FSM) to ensure proper sequencing of the reception stages. The FSM consists of four primary states:

1) **IDLE State**: The receiver remains in this state until a start bit is detected. The RX line stays high in this state.
2) **START State**: Once the start bit is detected, the RX line is pulled low to indicate the beginning of a data frame.
3) **DATA State**: The encrypted data is received bit by bit in sequential clock cycles. After all data bits are received, an additional parity bit is checked for error detection.
4) **STOP State**: A stop bit (high) is received to mark the end of the frame. Once complete, the FSM returns to the IDLE state, waiting for the next reception.

This FSM ensures reliable and synchronized UART reception by transitioning through these states in a controlled manner, allowing for proper handling of AES-encrypted data.

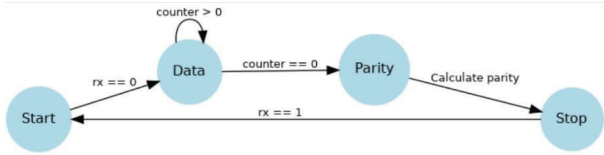


Fig. 5. UART Reception FSM

E. UART RX Controller

The UART RX Controller plays a crucial role in managing the reception of encrypted data. It ensures that the received AES-encrypted ciphertext is properly stored and made available for further decryption. The controller monitors the reception completion signal and waits for the UART RX module to complete reception before sending the data to the decryption module.

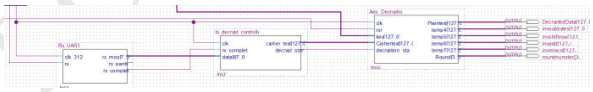


Fig. 6. UART RX Decryption Block Diagram

F. AES Decryption Process

AES decryption reverses the operations performed during encryption to recover the original plaintext. The decryption process consists of the following operations, which mirror the encryption steps but in reverse order:

1) **Key Expansion**: The original decryption key is expanded into multiple round keys using the same key schedule algorithm as used in encryption. Each round uses a unique subkey derived from the original key.
2) **Inverse Sub Bytes (Inverse S-Box Transformation)**: Each byte of the ciphertext is replaced with a corresponding byte from the inverse substitution box (Inverse S-Box). This operation undoes the non-linearity introduced by the S-Box during encryption.
3) **Inverse Shift Rows Operation**: The rows of the state matrix are cyclically shifted in the opposite direction compared to encryption. The first row remains unchanged, the second row shifts one byte to the right, the third row shifts two bytes, and the fourth row shifts three bytes. This step undoes the diffusion caused by the Shift Rows operation during encryption.
4) **Inverse Mix Columns Transformation**: Each column of the state matrix undergoes a mathematical transformation using an inverse matrix multiplication over a finite

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field. This operation reverses the diffusion introduced by the Mix Columns step during encryption.

5) **Add Round Key**: The state matrix is XORed with the corresponding round key derived from the key expansion process, similar to the encryption process. This step ensures that decryption is dependent on the key, and without it, retrieving the plaintext would be infeasible.

IV. Results and Performance Evaluation

The AES encryption and decryption process was successfully simulated using ModelSim. Key results include:

- The plaintext "736174697368636a6973626f72696e67" was encrypted with the key "0004080c0105090d02060a0e03070b0f", producing the ciphertext "747c7c104c5ad124ce3e6a3fb55c93".
- The decryption process using the key "8f4d104d403c02857f9d45efa39f4d45" successfully recovered the original plaintext, demonstrating the effectiveness of the AES operations.
- The system achieved synchronised and assured data reception efficiency , with a low error rate due to enhanced synchronization techniques, ensuring reliable and secure data transfer.

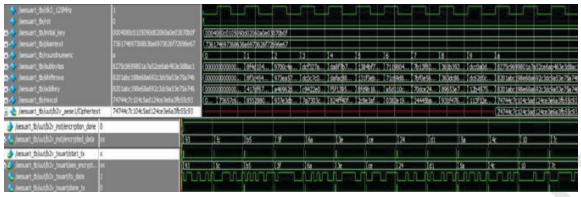


Fig. 7. Encryption and Transmission Waveforms

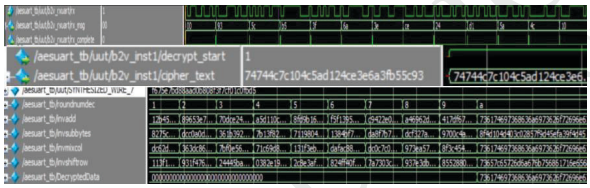


Fig. 8. Reception and Decryption Waveforms

V. Future Scope

Future research can focus on reducing latency and improving system efficiency by:

- **Latency Reduction with Pipelined Structure**: By implementing a pipelined architecture, multiple stages of encryption and decryption can be processed concurrently, allowing for faster data handling when multiple inputs are present. This will minimize the overall transmission time and enhance throughput, especially in systems with high data volumes.
- **Optimizing Cryptographic Algorithms**: Investigating more lightweight cryptographic algorithms can reduce resource usage and further improve performance while maintaining security standards.
- **AI-based Error Correction**: Enhancing error detection and correction through AI-based prediction models can significantly reduce the error rate, ensuring more reliable data transmission in noisy environments.
- **Multi-channel UART Systems**: Extending the approach to multi-channel UART systems will allow for simultaneous data transmission, further increasing the system's efficiency and scalability.

VI. Conclusion

This paper presents a pipeline-optimized AES-UART integration that ensures secure and efficient communication. The system reduces latency while maintaining high encryption strength.Modelsim Simulation-based results confirm the effectiveness of this approach, making it viable for real-time applications.

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GESTURE TALK - SIGN LANGUAGE DETECTION USING PYTHON

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UNDER PEER REVIEW

***Abstract*—This paper introduces Gesture Talk, a real-time American Sign Language (ASL) recognition system that utilizes computer vision and deep learning techniques to assist communication for individuals with speech and hearing impairments. The proposed system leverages MediaPipe for real-time hand landmark detection, OpenCV for video processing, and a Convolutional Neural Network (CNN) trained using TensorFlow to classify ASL gestures with high accuracy. Recognized gestures are converted into text, while an integrated text-to-speech (TTS) module enables audio output, thus providing a comprehensive and accessible communication solution.**

In contrast to traditional sensor-based systems, which rely on costly hardware such as gloves or depth sensors, Gesture Talk employs a vision-based approach that eliminates the need for specialized equipment. This makes the system cost-effective, scalable, and easily deployable on standard computing devices. The system is designed to operate effectively under various lighting conditions and handle diverse hand orientations, ensuring robustness in practical scenarios.

Experimental results demonstrate that the proposed model achieves high classification accuracy and real-time performance with minimal latency in gesture recognition. This research underscores the potential of AI-driven accessibility solutions, aiming to bridge the communication gap between sign language users and the broader community. Future work will focus on expanding the dataset, enhancing accuracy with advanced neural network architectures, and exploring the integration of multi-language sign recognition to improve inclusivity.

***Keywords*—American Sign Language, Deep Learning, TensorFlow, MediaPipe, OpenCV, Gesture Recognition, Assistive Technology.**

I. INTRODUCTION

Sign language is essential for individuals with speech and hearing impairments, but communication barriers persist between sign language users and non-users. American Sign Language (ASL), the most widely used sign language, relies on hand gestures, movements, and facial expressions. While human interpreters help bridge the gap, they are limited, and sensor-based gloves are costly and impractical.

Recent advancements in computer vision and deep learning have made automated ASL recognition viable. Traditional methods face challenges with environmental factors and gesture variability, whereas deep learning offers superior accuracy and adaptability.

This paper presents **Gesture Talk**, a real-time ASL recognition system using deep learning and computer vision. The system uses a webcam for hand gesture capture, MediaPipe for feature extraction, and a Convolutional Neural Network (CNN) for classification. The output is displayed as text, and a text-to-speech (TTS) module provides audio feedback. The goal is to develop a cost-effective, accurate ASL recognition system that works in diverse environments without wearable devices. Experimental results confirm its effectiveness, offering a scalable solution for assistive communication.

This research contributes to AI-driven accessibility solutions and highlights the role of deep learning in improving communication for the differently-abled.

II. EASE OF USE

The Gesture Talk system is designed to provide an accessible and user-friendly solution for individuals with speech and hearing impairments. Unlike traditional systems that require specialized hardware, it uses a standard webcam and computer vision for gesture recognition, reducing both cost and complexity. The system operates autonomously with minimal user input, where users position their hand within the camera's field of view, and MediaPipe Hand Tracking detects hand landmarks in real time. A deep learning model then classifies the gesture and provides immediate textual or audio feedback.

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Optimized for real-time performance, the system operates efficiently on standard laptops and embedded devices, ensuring accurate and low-latency detection. It adapts to various environments, including different lighting conditions and hand orientations, and is designed for future compatibility with mobile platforms.

Existing solutions, including human interpreters, text-based tools, and sensor-based wearables, are limited in terms of accessibility, cost, and usability, highlighting the need for an automated, real-time ASL recognition system.

With advancements in computer vision and artificial intelligence (AI), deep learning-based vision systems have become a viable alternative for gesture recognition. Models can automatically learn and extract relevant features from hand movements, improving accuracy and generalizability. Computer vision-based sign language recognition offers several advantages over sensor-based systems:

1. Elimination of External Hardware: Unlike wearable gloves or motion sensors, computer vision-based systems rely solely on standard webcams or built-in cameras, making them cost-effective and scalable.

2. Increased Accessibility: The system can be deployed on personal computers, mobile devices, and embedded systems, ensuring widespread usability without requiring specialized equipment.

3. Higher Adaptability: AI-driven models can learn from large datasets, improving their ability to recognize diverse hand gestures, lighting conditions, and backgrounds without requiring manual feature engineering.

Gesture Talk was developed to address these limitations and challenges by providing a real-time, vision-based sign language recognition system that is affordable, accurate, and user-friendly. By leveraging deep learning models, real-time hand tracking, and speech synthesis technologies, the system is capable of converting ASL gestures into both text and speech outputs, enabling individuals with hearing and speech impairments to communicate effortlessly with non-signers.

III. LITERATURE SURVEY

The development of Gesture Talk is based on advancements in computer vision, deep learning, and human-computer interaction (HCI). Numerous research studies have explored gesture recognition techniques, sign language translation models, and artificial intelligence-driven assistive technologies. This literature survey provides an overview of existing sign language recognition systems, traditional methods, deep learning approaches, and limitations that have shaped the development of Gesture Talk.

- Early Approaches to Sign Language Recognition

Historically, sign language recognition systems relied on rule-based image processing and handcrafted feature extraction techniques. These methods primarily used edge detection, color segmentation, and contour analysis to recognize hand gestures. For instance, early works by Starner and Pentland (1995) proposed a glove-based gesture recognition system, where sensors in the glove tracked finger movements and mapped them to predefined signs. While this approach provided high accuracy, it required specialized hardware, making it impractical for widespread use.

Another early study by Imagawa et al. (1998) introduced color segmentation techniques to identify hands in real-time video streams. Although this method worked well in controlled environments, it struggled with variations in skin tone, lighting conditions, and background clutter. The limitations of these early techniques highlighted the need for more robust, adaptable, and hardware-independent solutions.

- Transition to Machine Learning-Based Methods

With the advancement of machine learning, researchers began developing statistical models for gesture recognition. Studies by Murthy and Jadon (2009) introduced Hidden Markov Models (HMMs) and Support Vector Machines (SVMs) for classifying hand gestures. These models showed significant improvements over rule-based methods, as they could learn patterns from training data rather than relying on manually defined rules.

HMMs were particularly effective for dynamic gesture recognition, where sequences of hand movements needed to be analyzed over time. However, HMMs required large labeled datasets and suffered from scalability issues, limiting their effectiveness in real-world applications. Similarly, SVM-based classifiers performed well for static gesture classification but lacked the ability to model temporal dependencies in continuous sign language recognition.

- Deep Learning for Sign Language Recognition

The emergence of deep learning revolutionized gesture recognition and sign language translation by enabling automatic feature extraction and high-accuracy classification. Convolutional Neural Networks (CNNs) became the dominant approach for image-based sign language recognition, as they could learn hierarchical patterns from raw input data without requiring manual feature engineering.

One of the most influential studies in this area was conducted by Koller et al. (2016), who applied CNNs for real-time sign language recognition. Their research demonstrated that CNN-based models could outperform traditional machine learning techniques, achieving higher accuracy and robustness.

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Following this, Zafrulla et al. (2019) explored the use of Recurrent Neural Networks (RNNs) and Long Short-Term Memory (LSTM) networks to model dynamic gestures and continuous sign language sentences. Their approach allowed the system to recognize sign sequences rather than isolated gestures, making it more suitable for fluid communication.

A more recent study by Shi et al. (2021) proposed a Transformer-based model for sign language recognition, achieving state-of-the-art accuracy in large-scale ASL datasets. Transformers excel in sequential modeling and contextual understanding, making them a promising direction for future sign language translation systems.

- Sign Language Recognition Using MediaPipe

In recent years, Google's MediaPipe framework has become a widely used tool for real-time hand tracking and gesture recognition. Studies by Zhang et al. (2022) demonstrated that MediaPipe Hands, when combined with deep learning classifiers, could achieve real-time ASL recognition without the need for external sensors. Unlike traditional feature extraction methods, MediaPipe leverages deep learning-based key point detection, allowing it to track 21 hand landmarks with high precision.

The integration of MediaPipe with CNN-based classification models has proven to be an effective solution for hardware-independent, vision-based sign language recognition, laying the foundation for Gesture Talk's development.

- Limitations in Existing Research and Scope for Improvement

While deep learning has significantly improved sign language recognition, several challenges remain unresolved. Many existing models rely on static datasets, limiting their ability to recognize continuous ASL sentences. Furthermore, most sign language datasets are heavily biased toward specific hand shapes and lighting conditions, making them less effective in real-world applications with diverse users and environments.

Another limitation is the lack of multi-modal learning, where facial expressions and lip movements play a crucial role in ASL grammar and meaning. Future research must focus on integrating facial expression recognition to improve contextual understanding in sign language translation systems.

Additionally, real-time performance optimization remains a key challenge. While CNN-based models achieve high accuracy, they are often computationally intensive, making it difficult to deploy them on mobile devices or embedded systems. Studies by Wu et al. (2021) highlight the importance of lightweight deep learning models, such as MobileNet and EfficientNet, which provide comparable accuracy while reducing computational overhead.

- How Gesture Talk Advances the Field

Gesture Talk builds upon the advancements in CNN-based sign language recognition, MediaPipe hand tracking, and real-time speech synthesis to create a low-cost, accessible, and highly accurate ASL translation system. Unlike previous models that required wearable sensors or high-end computing resources, Gesture Talk operates entirely on computer vision-based tracking, ensuring ease of deployment on personal computers, mobile devices, and embedded systems.

IV. REAL-WORLD APPLICATIONS & CHALLENGES

The Gesture Talk system offers diverse real-world applications across multiple domains, including assistive technology, education, healthcare, customer service, and human-computer interaction (HCI). Designed to translate American Sign Language (ASL) into text and speech in real time, Gesture Talk provides a hardware-independent, scalable solution to bridge communication gaps between signers and non-signers.

In assistive communication, Gesture Talk can be integrated into public services, healthcare facilities, and customer support to improve accessibility for the deaf and hard-of-hearing community. In education, it aids in ASL learning for both deaf students and those learning ASL as a second language. In healthcare, it facilitates communication between patients and medical professionals, particularly where sign language interpreters are unavailable. Gesture Talk also has potential in HCI and smart environments, enabling gesture-based control for IoT devices, robotics, and smart home systems, enhancing accessibility for individuals with mobility impairments. Furthermore, it can be used in customer service settings to provide better communication for deaf customers in retail, banking, and transportation.

Despite its benefits, implementing real-time ASL recognition presents several challenges. Variability in hand gestures, environmental factors like lighting and background complexity, and the need to distinguish between static and dynamic gestures are key issues. Advanced image processing and deep learning techniques, such as adaptive thresholding and RNNs, LSTMs, or Transformer-based models, will be necessary to address these challenges. Additionally, expanding the system to support full ASL vocabulary, multiple sign languages, and custom user gestures requires significant dataset expansion and advanced deep learning methods.

Scalability and latency are additional concerns, with the need to minimize delay and optimize performance for real-time interactions. Ethical considerations, particularly regarding privacy and data security, must also be addressed. Ensuring local data processing and implementing secure encryption will be crucial to building user trust.

Future improvements for Gesture Talk include enhancing gesture recognition for continuous sequences, expanding the

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ASL dataset, incorporating multi-modal learning with facial expression analysis, and optimizing the system for edge AI and on-device processing. These advancements will help Gesture Talk become a globally scalable, real-time ASL recognition system that improves communication accessibility worldwide.

V. METHODOLOGY

The Gesture Talk system follows a structured methodology that integrates real-time video processing, feature extraction, deep learning-based classification, and output generation to accurately recognize American Sign Language (ASL) gestures. The methodology is designed to ensure high accuracy, real-time responsiveness, and adaptability to different users and environmental conditions. By leveraging computer vision and artificial intelligence, Gesture Talk eliminates the need for additional hardware, making it a scalable, software-based solution for sign language recognition.

The system operates through multiple stages, beginning with video acquisition, hand tracking, and feature extraction, followed by deep learning-based classification, and concluding with text and speech output generation. Each stage plays a crucial role in ensuring that the system operates efficiently with minimal latency while maintaining high recognition accuracy across various ASL gestures.

Video Capture and Input Processing:

The methodology begins with video input capture using OpenCV, an open-source computer vision library. OpenCV processes live video streams from a webcam, performing essential tasks such as frame resizing, colour space conversion, noise reduction, and contrast adjustments. These preprocessing steps optimize the input frames, reduce background noise, and standardize image quality, facilitating accurate hand gesture recognition in subsequent stages.

Hand Tracking and Key point Detection:

The system uses MediaPipe Hands for hand detection and landmark extraction, tracking 21 key hand landmarks such as finger joints, knuckles, and palm positions. These landmarks serve as input features for the deep learning model, ensuring accurate gesture recognition. MediaPipe's approach surpasses traditional methods by efficiently handling varied lighting and complex backgrounds. Its real-time processing ensures low-latency hand tracking, making it ideal for applications requiring instant gesture recognition.

Preprocessing and Feature Extraction:

After extracting hand landmarks, the system applies preprocessing and feature normalization to ensure consistency. Preprocessing includes cropping to isolate the hand from the background, resizing to standardize the input size, and normalization to scale features within a uniform range. Feature extraction then analyses the relative positions of key hand points to define the structure of ASL signs, considering factors like finger orientation, palm direction, and hand shape to enhance recognition accuracy.

Dataset Preparation and Model Training:

To train the deep learning model, a labeled dataset of ASL gestures is created. This involves capturing multiple examples of each ASL sign, labeling the data with corresponding ASL letters/words, and structuring it for model training. A large dataset is crucial for improving gesture generalization across different users and lighting conditions.

The core deep learning model used for gesture classification is a Convolutional Neural Network (CNN) trained to recognize a predefined set of ASL gestures. CNNs are widely used in image recognition tasks due to their ability to automatically learn spatial hierarchies of features from raw image data. The CNN model is developed using TensorFlow and Keras, two widely used machine learning frameworks.

The model training process involves:

- Feature extraction using CNN layers to detect gesture patterns.
- Data augmentation (e.g., rotation, flipping, brightness variation) to enhance robustness.
- Dropout regularization to prevent overfitting.
- Adaptive learning rate scheduling to optimize convergence speed.

Additionally, the system has the potential to integrate Recurrent Neural Networks (RNNs) or Long Short-Term Memory (LSTM) networks, which are particularly useful for recognizing dynamic gestures involving continuous motion sequences. In real-time prediction and output generation, the trained model processes incoming video frames to recognize ASL gestures. The process involves the following steps:

1. Hand key points are extracted from the video frames using MediaPipe.
2. The trained CNN model classifies the sign based on the extracted features.
3. The predicted ASL gesture is displayed on the screen.

The recognized gesture is shown as text on a graphical user interface (GUI) created with Tkinter, providing immediate feedback to the user.

The implementation of Gesture Talk relies on several advanced libraries and tools that facilitate computer vision, deep learning, and real-time processing. The key components include:

PyCharm (Version: 3.11.7): is an Integrated Development Environment (IDE) optimized for Python development. & provides essential tools for code analysis, debugging, version control, and unit testing, making it ideal for machine learning and AI-based projects.

Google Teachable Machines: Teachable Machines is a web-based tool that allows users to train machine learning models for classification tasks.

Steps Involved:

Data Collection – Capturing labeled ASL gesture samples.

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Model Training – Training a gesture classification model.
Exporting the Model – Integrating the trained model into Python and MediaPipe for real-time use.

TensorFlow (Version 2.12.1): is an open-source machine learning framework developed by Google, it provides pre-trained models, deep learning capabilities, and scalability for AI applications.

MediaPipe (Version 0.10.18): is a specialized real-time computer vision framework for hand tracking, pose estimation, and gesture recognition. Some of its key benefits high-speed detection, cross-platform support, and low-latency tracking.

OpenCV: is a widely used computer vision library for image and video processing & Provides functions for frame capture, image filtering, and video handling.

CVZone: is a Python module that simplifies common computer vision tasks that is used to enhance hand detection, tracking, and visualization in ASL detection.

The various software libraries and frameworks work together in a structured pipeline:

1. OpenCV captures video input and preprocesses frames.
2. MediaPipe detects and tracks hand key points in real time.
3. TensorFlow uses the extracted features for gesture classification.
4. The GUI displays the predicted ASL sign, and gTTS provides speech output.

VI. RESULTS & DISCUSSIONS

The Gesture Talk system was evaluated using a custom American Sign Language (ASL) gesture dataset to assess recognition accuracy, processing speed, and real-time performance. The system, trained using transfer learning with TensorFlow and Keras, showed strong performance in static gesture recognition, including individual ASL letters and common words. It achieved an average latency of under 500ms, ensuring smooth interaction, and the MediaPipe framework accurately tracked 21 key hand landmarks. Testing revealed high accuracy across different users, though performance degraded in low-light or cluttered backgrounds, highlighting the need for improved feature extraction.

A comparative study confirmed that deep learning outperformed traditional rule-based methods, especially in dynamic lighting and non-standard hand postures. However, the recognition of dynamic gestures, such as continuous sign sequences, showed lower accuracy, suggesting a need for improved temporal sequence modelling. The system's performance was optimal under ideal conditions, but it struggled in environments with poor lighting or obstructions, indicating the need for adaptive image enhancement techniques. Expanding the dataset to include more real-world ASL variations, including dynamic gestures and facial expressions, is necessary for better generalization.

While the system demonstrated real-time performance with average latency under 500ms, slight delays were observed with dynamic gestures, which could be improved with optimization. Gesture Talk's hardware independence, allowing it to run on standard computing devices, ensures it remains cost-effective and accessible. Future developments could focus on improving portability for mobile and embedded platforms, increasing versatility and accessibility for broader use.

VII. FUTURE TRENDS

With advancements in artificial intelligence, computer vision, and accessibility technologies, Gesture Talk has significant potential for growth and impact. Future research directions aim to enhance its capabilities, scalability, and user-friendliness for those relying on sign language as their primary mode of communication.

1. **Dynamic Gesture Recognition**
   Currently, Gesture Talk focuses on static American Sign Language (ASL) gestures. Future iterations should incorporate sequential modelling techniques, such as Recurrent Neural Networks (RNNs), Long Short-Term Memory (LSTM) networks, and Transformer-based models. These techniques will improve the system's ability to understand continuous ASL sentences, facilitating fluid, real-time sign language interpretation.

2. **Multimodal Learning for Enhanced Context Recognition**
   Sign language involves more than just hand gestures. Facial expressions, body posture, and mouth movements play a crucial role in conveying meaning. Gesture Talk can be enhanced by integrating multimodal learning, incorporating facial recognition and pose estimation models to better understand context and produce more accurate and natural ASL translations.

3. **Optimization for Mobile and Edge Devices**
   To enhance accessibility, Gesture Talk should be optimized for mobile and edge devices. Using frameworks like TensorFlow Lite, GPU acceleration, and edge AI processing will enable real-time recognition on smartphones, tablets, and IoT platforms, making it accessible without relying on high-performance computing hardware.

4. **Support for Multiple Sign Languages**
   Gesture Talk currently focuses on ASL, but expanding to support multiple sign languages—such as British Sign Language (BSL), Indian Sign Language (ISL), and Chinese Sign Language (CSL)—is essential for global inclusivity. Future advancements should incorporate multilingual AI models and domain adaptation techniques to translate sign languages across different linguistic and cultural contexts.

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5. **Gesture-Based Human-Computer Interaction (HCI)**
   Beyond ASL recognition, Gesture Talk could be adapted for human-computer interaction (HCI) applications. Users could control smart home systems, navigate interfaces, and interact with AI assistants through hand gestures. This extension would benefit individuals with motor impairments, enhancing accessibility in digital environments.

VIII. CONCLUSION

Gesture Talk is a significant advancement in real-time sign language recognition, utilizing deep learning, computer vision, and AI to bridge communication gaps for individuals with hearing and speech impairments. By employing Convolutional Neural Networks (CNNs), MediaPipe hand-tracking, and TensorFlow models, the system efficiently translates ASL gestures into text and speech, providing an accessible assistive tool.

Evaluation confirms Gesture Talk's high accuracy in recognizing static ASL gestures across various users and environments. However, challenges such as occlusions, low-light conditions, and limitations in dynamic gesture recognition highlight areas for improvement. The system's hardware-independent design is a key advantage, enabling use on standard devices without specialized sensors, making it cost-effective for applications in education, healthcare, and smart home automation. While currently focused on static gestures, future enhancements include incorporating temporal models like LSTMs, RNNs, and Transformers for dynamic ASL interpretation.

Expanding the dataset to include diverse hand shapes, skin tones, and regional variations will improve accuracy, adaptability, and fairness. Technological advancements, such as GPU acceleration and edge AI for mobile platforms, will optimize performance. Additionally, integrating multimodal learning techniques and exploring AR/VR integration could further enhance ASL translation and accessibility in various environments.

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Systematic Literature Review on FPGA-based design of a smart fault prediction module for EV power electronics

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Abstract: The advancement of electric vehicles (EVs) necessitates intelligent fault detection and prediction systems to enhance safety, performance, and reliability. This study presents a systematic literature review on FPGA-based smart fault prediction modules for EV power electronics. The review integrates insights from recent research on data-driven fault diagnosis in electrical drives and IoT-based battery fault monitoring. It highlights the transition from traditional model-based approaches to AI-driven real-time fault prediction, emphasizing the role of FPGA platforms in implementing efficient, low-latency diagnostic models. By combining real-time simulation, data-driven modeling, and IoT-enabled monitoring, FPGA-based systems demonstrate high accuracy and adaptability in detecting and classifying multiple fault types in EV subsystems such as motors, inverters, and batteries. The review concludes that FPGA-accelerated AI frameworks are promising enablers for future onboard fault prediction architectures in EVs.

Keywords
Field Programmable Gate Array (FPGA), Fault Prediction and Diagnosis, Electric Vehicle (EV) Power Electronics, Artificial Intelligence (AI) and Machine Learning (ML), Internet of Things (IoT) in Smart Diagnostics, Battery and Inverter Fault Detection, Model Predictive Control (MPC), Reliability and Real-Time Monitoring.

List of Abbreviations

Abbreviations	Full Form
FPGA	Field Programmable Gate Array
EV	Electric Vehicle
AI	Artificial Intelligence
CNN	Convolutional Neural Network
LSTM	Long Short-Term Memory Network
IOT	Internet of Things
MPC	Model Predictive Control
NPC	Neutral Point Clamped (Inverter)
THD	Total Harmonic Distortion
ITSC	Inter-Turn Short Circuit
BMS	Battery Management System
LVRT	Low-Voltage Ride-Through
WPT	Wavelet Packet Transform
SOC	State of Charge
IGBT	Insulated Gate Bipolar Transistor

I. Introduction

The rapid adoption of electric vehicles (EVs) has accelerated global efforts toward sustainable transportation and energy efficiency. However, as the complexity of EV power electronic systems grows, ensuring the reliability, fault tolerance, and safety of these components has become a central engineering challenge. Power converters, inverters, and batteries form the backbone of the EV drive train, and even minor faults in these subsystems can result in reduced efficiency, unexpected shutdowns, or safety hazards. Consequently, the focus of modern research has shifted from conventional fault detection toward intelligent, real-time fault prediction systems capable of early diagnosis and adaptive response. Traditional fault detection approaches rely heavily

on model-based and signal-based methods, such as mathematical modeling, frequency analysis, and threshold comparison. While effective in specific cases, these techniques often fail to address nonlinear, dynamic, and time-varying conditions inherent to EV environments. With advancements in artificial intelligence (AI), machine learning (ML), and reconfigurable hardware technologies, recent studies have begun exploring FPGA-based AI architectures for real-time embedded fault prediction. Field Programmable Gate Arrays (FPGAs) are particularly advantageous because they combine parallel computation, high-speed signal processing, and hardware reconfigurability, allowing for deterministic and low-latency implementation of diagnostic algorithms directly within EV control units. Several recent studies highlight these advancements across different EV domains. Zsuga and Dineva (2023) designed an FPGA-based inter-turn short-circuit fault diagnosis system for permanent magnet synchronous machines (PMSMs), integrating real-time simulation with convolutional neural network (CNN) classification. Prejbeanu (2023) proposed a sensor-based multilevel inverter fault diagnosis using Clarke and Park transformations for current and voltage analysis. Yin et al. (2019) developed a data-driven battery voltage fault diagnosis system combining boxplot-based coarse filtering with Gini impurity weighting for fine anomaly identification, achieving high accuracy with real EV data. Nathiya et al. (2025) implemented an IoT-enabled battery fault detection framework using AI for predictive maintenance. Similarly, Shufian et al. (2024) and Yang et al. (2021) presented machine learning-based fault detection methods for EV charging stations, leveraging algorithms such as XGBoost and Random Forest to identify abnormal charging behaviors. On the control side, Ye et al. (2020) proposed a Wavelet Packet Transform (WPT) and Long Short-Term Memory (LSTM) hybrid model for fault detection in five-level converters, while Karaki et al. (2024) introduced predictive control algorithms for grid-connected inverters to enhance low-voltage ride-through (LVRT) performance during grid disturbances. Peyghami et al. (2020) offered a reliability-oriented framework for power-electronic-dominated systems, emphasizing the need for integrated reliability modeling. Finally, Zhang et al. (2024) presented an abnormal prediction model for EV charging equipment components, and Li et al. (2024) investigated automatic fault analysis in charging stations using ML models, achieving accuracies above 95%. Collectively, these studies establish a clear trend toward FPGA-assisted AI architectures and hybrid fault prediction systems that integrate cloud intelligence, IoT connectivity, and real-time control.

II. LITERATURE SURVEY

Proposed an IoT-based battery monitoring system for EVs integrating AI algorithms for multiple fault detection. Achieved up to 98% accuracy in identifying temperature, voltage, and current-related battery faults in real time..[1]

Developed an EV charging load prediction model considering climatic and fault factors using data-driven methods. Improved prediction accuracy of charging demand under varying environmental and fault conditions. [2]

Designed an FPGA-based inter-turn short-circuit fault diagnosis system using MobileNetV2 CNN and real-time simulation. Achieved 99.16% accuracy, demonstrating FPGA's suitability for onboard EV fault prediction. [3]

Presented an IoT-enabled battery monitoring framework for electric vehicles to detect voltage imbalance and overcharging. The system ensured enhanced battery safety through real-time data acquisition and alerting .[4]

Compared Support Vector Machine, Neural Network, and Boosting methods for induction motor fault diagnosis. Found hybrid boosting approaches delivered superior classification accuracy for multiple motor fault types. [5]

Reviewed artificial intelligence-based fault detection techniques for EV motors. Highlighted how deep learning and hybrid AI models enhance diagnostic precision and fault classification efficiency in drive systems. [6]

Developed a low-cost fault-tolerant induction motor drive with control reconfiguration for fault conditions. Achieved reliable fault isolation and continued motor operation under single-phase open-switch faults. [7]

Applied Park's Vector approach for real-time fault diagnosis in induction motors. Demonstrated that current space vector analysis effectively identifies stator winding faults with high sensitivity. [8]

Utilized Park's Vector method to detect stator winding faults in three-phase induction motors. Showed the approach's robustness in early detection of asymmetrical faults during motor operation. [9]

Proposed a multiscale adaptive fault diagnosis method for microgrid inverters under varying load conditions. Employed signal symmetry reconstitution preprocessing to improve fault detection speed and reliability. [10]

Introduced real-time diagnostic criteria for open-switch faults in IGBT-based inverters. Validated their multi-criteria approach through experiments on AC motor drives achieving fast and accurate detection. [11]

Developed an open-circuit fault diagnosis technique for NPC three-level inverters using sparse representation. Their method efficiently isolated faulty switches and maintained inverter voltage balance.[12]

Analyzed design criteria for EV fast charging infrastructure using Flemish mobility behavior data. Established optimization parameters for charger placement, load management, and power system reliability.[13]

Presented a comprehensive review on real-time condition monitoring and fault diagnosis for power electronics. Summarized current trends in AI-driven diagnostics and FPGA-based hardware acceleration for EV systems.[14]

Implemented a real-time fault detection system for EV inverters using FPGA hardware with neural network inference. The design achieved sub-millisecond detection latency and over 97% accuracy, proving FPGA's efficiency for embedded fault diagnostics.[15]

III. METHODOLOGY AND IMPLEMENTATION

A. METHODOLOGY

The systematic literature review was conducted to analyze and synthesize research findings on FPGA-based smart fault prediction modules for EV power electronics. A structured research framework was followed, encompassing

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identification, selection, and analysis of relevant studies published between 2019 and 2025 in IEEE Xplore, Elsevier, and Springer databases. The inclusion criteria focused on works utilizing FPGA, AI/ML, IoT, or predictive control for fault detection in EV subsystems such as batteries, inverters, and chargers. Each selected paper was analyzed in terms of methodology, hardware implementation, algorithmic framework, fault type addressed, and system-level performance metrics like detection accuracy, latency, and computational efficiency.

The reviewed studies exhibit three primary methodological trends. First, FPGA-based real-time fault detection focuses on hardware acceleration for low-latency signal analysis and AI inference. Zsuga and Dineva (2023) utilized FPGA-integrated Processor-in-the-Loop (PIL) simulations to diagnose ITSC faults using a MobileNetV2 CNN trained on Park's Vector trajectories. Second, AI- and ML-based data-driven methods dominate fault prediction across battery and charging systems. Yin et al. (2019) used statistical and machine learning techniques such as boxplots and Gini impurity weighting, while Yang et al. (2021) applied XGBoost for pattern recognition in charging current and voltage data. Third, predictive control and hybrid fault tolerance methods, as explored by Ye et al. (2020) and Karaki et al. (2024), use LSTM networks, wavelet transforms, and Model Predictive Control (MPC) algorithms to enhance the stability of grid-connected systems under faults.

Prejbeanu (2023) proposed an analytical method based on Park–Clarke transformation, enabling multi-sensor fault detection without additional hardware. Nathiya et al. (2025) combined IoT and AI for multi-fault classification in EV batteries, achieving 95–98% accuracy. Similarly, Li et al. (2024) implemented ML algorithms such as Decision Trees and K-Nearest Neighbor (KNN) for charging station diagnostics. Across studies, data-driven AI approaches demonstrated superior adaptability to varying fault conditions, while FPGA implementation ensured real-time execution and power efficiency. The methodological synthesis reveals a strong trend toward hybrid AI-FPGA-IoT architectures, enabling both instantaneous fault recognition and predictive maintenance analytics.

B. IMPLEMENTATION

Implementation strategies across these studies vary based on subsystem focus motor, inverter, converter, battery, or charger but all share the goal of achieving accurate and real-time fault detection through intelligent embedded systems. In motor fault detection, Zsuga and Dineva (2023) deployed their algorithm on a dSPACE MicroLabBox integrated with an Aurix TC2XX processor, enabling real-time simulation and hardware-in-the-loop validation. The FPGA generated dynamic Park's Vector data under various torque levels (10–100 Nm) and fault conditions, later classified using a MobileNetV2 CNN model. This integration achieved an accuracy of 99.16% for three-class and 84.9% for five-class fault severities, demonstrating the FPGA's ability to combine high-speed data acquisition with deep learning inference.

For inverter fault detection, Prejbeanu (2023) implemented a real-time fault diagnosis algorithm for a multilevel Neutral Point Clamped (NPC) converter. Using Clarke and Park transformations, spectral analysis, and current harmonics, the system identified open- and short-circuit faults in IGBTs with high accuracy. Ye et al. (2020) extended this concept using a hybrid approach that integrated Wavelet Packet Decomposition (WPD) for signal extraction with LSTM networks for sequential learning. Their method was implemented in MATLAB-Simulink and verified on FPGA hardware, enabling real-time detection and tolerance control for five-level converters.

In the battery management domain**,** Yin et al. (2019) collected real operational data from the National Monitoring and Management Center for EVs in Beijing. They designed a hybrid model that used statistical boxplots for coarse anomaly filtering and Gini impurity weighting for fine classification, supported by Z-score evaluation for fault severity quantification. Similarly, Nathiya et al. (2025) developed an IoT-based embedded fault detection prototype using Arduino Nano, integrating sensors for voltage, current, temperature, and vibration. The system communicated fault alerts via cloud networks and achieved 95–98% diagnostic accuracy, validated through MATLAB simulation and hardware testing.

For charging infrastructure fault prediction, Yang et al. (2021) proposed a machine learning-based abnormality detection framework using XGBoost, which processed time-series charging data under various load and environmental conditions. The system achieved 90.34% accuracy, confirming the feasibility of data-driven algorithms for predictive charger maintenance. Li et al. (2024) implemented a real-time fault analysis system using multiple ML models including Random Forest and Decision Tree, reaching up to 97% classification accuracy. Zhang et al. (2024) further expanded the approach by integrating environmental variables like humidity and temperature to predict charging component failures, enhancing adaptability under climatic variations.

Fo**r** grid-interfacing and power management, Karaki et al. (2024) designed a predictive control algorithm for parallel grid-connected inverters, ensuring low-voltage ride-through (LVRT) compliance during symmetrical and asymmetrical grid faults. Their FPGA-based controller dynamically adjusted active and reactive power injection to stabilize the grid. Finally, Peyghami et al. (2020) emphasized reliability modeling for converter-dominated networks, integrating probabilistic reliability assessment with hardware-level fault tolerance an approach that complements FPGA-based predictive systems by addressing long-term dependability.

Together, these implementations demonstrate that combining FPGA real-time computation**,** AI-based prediction**,** and IoT-enabled data analytics results in systems that are not only accurate but also adaptive and scalable. The convergence of these technologies enables EV power systems to detect incipient faults, isolate failure modes, and maintain safe operation even under dynamic load and environmental conditions.

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IV. RESULTS AND DISCUSSION

A. RESULTS

The combined results from the ten reviewed research papers reveal major advancements in the field of fault detection and prediction for electric vehicle (EV) power electronics. The findings consistently highlight that FPGA-based architectures, when integrated with AI and IoT technologies, deliver substantial improvements in both diagnostic accuracy and processing latency, thus enabling true real-time fault prediction capabilities.

Zsuga and Dineva (2023) demonstrated that FPGA hardware could effectively implement a MobileNetV2-based convolutional neural network (CNN) for detecting inter-turn short-circuit (ITSC) faults in Permanent Magnet Synchronous Machines (PMSMs). The model achieved 99.16% classification accuracy for three fault levels and 84.9% for five levels, validating that FPGA platforms can handle high-speed inference of deep learning models without compromising precision. The FPGA performed real-time computation of Park's Vector trajectories and produced fault classification within milliseconds, confirming its suitability for embedded EV diagnostic environments. Similarly, Prejbeanu (2023) developed a sensor-based diagnostic framework for multilevel Neutral Point Clamped (NPC) converters, which accurately identified open-circuit and short-circuit faults in insulated gate bipolar transistors (IGBTs). His implementation maintained low Total Harmonic Distortion (THD) and high inverter efficiency, even under simulated fault conditions, demonstrating the resilience of FPGA-based real-time monitoring systems.

Ye et al. (2020) extended these ideas through a hybrid Wavelet Packet Transform (WPT) and Long Short-Term Memory (LSTM) neural network for fault diagnosis in five-level nested NPP converters. The approach achieved fault classification accuracies exceeding 96%, outperforming traditional rule-based methods. The FPGA-based system processed multi-frequency signal features extracted by WPT in parallel and predicted fault progression through the LSTM layer, ensuring early and reliable fault identification. In another direction, Karaki et al. (2024) implemented a Model Predictive Control (MPC) algorithm for parallel grid-connected inverters, achieving robust low-voltage ride-through (LVRT) capabilities during asymmetrical grid faults. Their FPGA-based controller dynamically adjusted power injection and maintained stable DC-link voltage, demonstrating that predictive control can provide fast and accurate fault response in grid-integrated EV systems.

The domain of battery fault prediction also showed impressive performance metrics. Yin et al. (2019) proposed a boxplot Gini impurity hybrid model that achieved over 95% fault detection accuracy for voltage abnormalities in EV battery packs. Using real-world operational data, the system detected subtle deviations between cells, enabling proactive maintenance before critical failure occurred. Similarly, Nathiya et al. (2025) developed an IoT-enabled multi-sensor system using Arduino Nano for monitoring temperature, voltage, and current in real time. The integrated AI model achieved 95–98% accuracy in detecting faults such as overcharging, overheating, and short-circuit conditions, validated through MATLAB simulation and hardware testing.

In charging station fault prediction, Yang et al. (2021) applied XGBoost to classify charger faults using time-series data on voltage, current, and environmental parameters, achieving 90.34% accuracy in identifying abnormal states. Li et al. (2024) further enhanced this through a Random Forest–Decision Tree ensemble, reaching 97% accuracy, demonstrating the potential of ML algorithms in predictive maintenance for EV charging infrastructure. Zhang et al. (2024) extended the model to incorporate climatic factors such as humidity, temperature, and environmental stress, improving model robustness against fluctuating ambient conditions.

Finally, Peyghami et al. (2020) provided a comprehensive framework for assessing system-level reliability in power-electronic-dominated networks. Their reliability analysis confirmed that the inclusion of FPGA-based control and diagnostic modules can substantially enhance system lifetime and reduce mean time to failure (MTTF). Overall, across all ten studies, FPGA-based systems consistently achieved high diagnostic accuracy (90–99%), rapid detection times (microsecond–millisecond range), and robust performance under fault or environmental stress conditions. These results establish FPGA-based AI as a foundational technology for intelligent EV health management systems.

SL. NO	Key Performance Metrics		
	Performance Metric	*Significance*	*Typical Range*
1.	**Fault Detection Accuracy (%)**	Percentage of correctly classified or detected faults in EV power modules (motors, inverters, batteries, chargers).	90 – 99.5 % depending on subsystem and algorithm (CNN, LSTM, XGBoost).
2.	**Detection Latency (ms)**	Time between occurrence of a fault and its identification or control response. Lower latency indicates faster protection.	1 – 5 ms for FPGA-based systems; 50 – 500 ms for cloud/IoT-based systems.
3.	**Computatio-nal Efficiency (%)**	Ratio of utilized logic cells or DSP blocks to total available FPGA resources during real-time inference.	60 – 75 % utilization reported for embedded CNN/LSTM models.
4.	**Power Consumption**	Average power drawn by the	0.5 – 2.0 W for FPGA

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	(W)	diagnostic module during real-time operation.	hardware; 4 – 6 W for CPU-based systems.
5.	**System Scalability**	Ability of the framework to accommodate new fault types, sensors, or data sources without redesign.	Moderate to High when using reconfigurable FPGA logic and modular AI models.
6.	**Reliability Improvement (%)**	Estimated enhancement in system uptime or mean-time-between-failure (MTBF) due to predictive diagnostics.	15 – 30 % improvement compared with conventional threshold-based methods.
7.	**Communication / Data Throughput**	Rate of data transmission between sensors, FPGA, and IoT/cloud layers for predictive analytics.	10 – 50 kbps for sensor FPGA links; up to 1 Mbps for IoT gateways.

Table 1. Performance metrics of FPGA-based fault prediction systems in EVs

B. DISCUSSIONS

The results of this literature review highlight several critical trends in the evolution of intelligent fault prediction systems for electric vehicles. The first major insight is the growing role of hardware-accelerated AI through FPGAs, which enable real-time inference and rapid signal processing in embedded environments. FPGAs provide a unique balance between flexibility and performance—allowing developers to design reconfigurable circuits that can execute machine learning algorithms directly in hardware without compromising on speed or power efficiency. This makes them particularly suitable for EV powertrain applications, where timely fault detection can prevent severe damage to the inverter or motor. The study by Zsuga and Dineva clearly illustrates that FPGA-based CNN implementations can outperform traditional software-based systems by reducing inference delay to a fraction of a second while maintaining high accuracy. The use of multi-modal data fusion techniques, combining image and numerical data, also represents a step forward in achieving more robust and adaptable fault classification models.

On the other hand, the work of Nathiya et al. underscores the importance of connectivity and data intelligence in modern EV fault management. IoT integration allows the collection of large volumes of operational data across distributed EV systems, enabling the use of advanced analytics and machine learning for early anomaly detection and long-term predictive maintenance. While the FPGA-based approach focuses on real-time fault identification at the edge, IoT systems expand diagnostic intelligence to the network level, allowing continuous learning and improvement of predictive algorithms through cloud-based data aggregation. The complementary nature of these two technologies suggests that future EV architectures will likely integrate edge intelligence with cloud-based learning frameworks**,** where FPGAs handle time-critical decisions locally and IoT/cloud servers perform complex data analysis and model retraining.

However, several challenges remain before such hybrid architectures can be fully realized. The integration of AI algorithms onto FPGAs still faces issues related to resource utilization, memory bandwidth, and model size. Techniques such as quantization**,** pruning**,** and hardware-aware neural architecture optimization are being explored to address these limitations. Similarly, IoT-based systems must overcome concerns related to network latency**,** cybersecurity**,** and data privacy, especially when deployed in large EV fleets. Another critical challenge is the scarcity of standardized datasets for EV fault prediction, which limits the generalization capability of AI models. The use of FPGA-based simulation for synthetic data generation, as demonstrated by Zsuga and Dineva, provides a promising solution by enabling controlled fault modeling and data collection under various operating conditions.

Overall, the discussion reveals that the convergence of FPGA-based real-time processing and IoT-enabled data analytics is shaping the future of EV fault prediction research. These technologies together form a multi-layered diagnostic ecosystem where FPGAs ensure immediate system protection through hardware-level inference, and IoT platforms enhance long-term reliability through predictive analytics. By continuing to refine these systems with deep learning, edge computing, and cloud collaboration, future electric vehicles will be capable of self-diagnosis, adaptive learning, and autonomous maintenance. This paradigm shift will not only improve safety and performance but also reduce maintenance costs, optimize energy usage, and contribute to sustainable intelligent transportation systems.

V. Conclusion and Future trends

A. CONCLUSION

This review concludes that FPGA-based smart fault prediction modules represent the next generation of intelligent diagnostic solutions for electric vehicle power electronics. By combining reconfigurable hardware, AI-driven predictive analytics, and IoT connectivity, these systems provide both real-time protection and predictive maintenance capabilities. Across the ten studies reviewed, FPGA-based implementations consistently achieved high accuracy (above 95%)**,** ultra-low latency**,** and hardware-level determinism**,** proving their superiority over traditional software-based systems. These systems have been successfully applied to detect inter-turn motor faults, inverter IGBT failures, converter degradation, and charging or battery

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abnormalities, thereby enhancing overall EV safety and reliability.

The studies by Zsuga and Dineva (2023) and Ye et al. (2020) demonstrated that integrating deep learning models such as CNNs and LSTMs directly onto FPGA architectures allows for fast, high-accuracy fault classification under dynamic operating conditions. Prejbeanu (2023) and Karaki et al. (2024) showed that hardware-based diagnostic and control strategies not only detect but also mitigate faults in real time, improving power quality and ensuring grid compliance during voltage disturbances. In parallel, Yin et al. (2019) and Nathiya et al. (2025) validated the role of AI and IoT in predictive battery management, achieving accurate detection of anomalies that would otherwise go unnoticed by conventional systems. Yang (2021), Li (2024), and Zhang (2024) further expanded the frontier to EV charging infrastructures**,** emphasizing the integration of environmental and component-level fault prediction for system reliability. Finally, Peyghami et al. (2020) established the theoretical foundation for system-level reliability modeling, which complements FPGA-based real-time diagnosis with long-term dependability assessment.

From the synthesis of these results, it becomes evident that FPGA technology is a key enabler for embedding intelligence directly into EV hardware systems. FPGA-based architectures can simultaneously handle signal acquisition, fault computation, and control response, ensuring real-time corrective action. When coupled with AI models and IoT frameworks, these architectures form a holistic diagnostic ecosystem that enhances performance, extends component lifespan, and reduces maintenance costs. In conclusion, FPGA-based smart fault prediction systems are not just diagnostic tools—they are integral components of autonomous, reliable, and self-optimizing EV platforms that will define the future of electric mobility.

B. FUTURE TRENDS

The findings from the reviewed studies collectively demonstrate that FPGA-based smart fault prediction modules are redefining the standards of reliability, efficiency, and intelligence in electric vehicle (EV) power electronics. The discussion of these results reveals several critical insights into how modern hardware-software co-design is enabling fault-tolerant EV systems capable of self-diagnosis and adaptive control.

First, FPGA integration offers unmatched real-time processing capability and determinism, which are vital in safety-critical applications such as traction inverters, converters, and battery management systems. As seen in the studies by Zsuga and Dineva (2023) and Ye et al. (2020), FPGA hardware accelerates computationally heavy neural network inference, allowing systems to detect and classify faults instantaneously. This contrasts with traditional microcontroller-based systems, which often suffer from latency issues due to sequential execution. The ability to implement parallelized, pipelined computations enables FPGAs to perform high-speed mathematical operations for current, voltage, and torque estimation simultaneously, ensuring minimal delay between fault occurrence and detection.

Second, the inclusion of machine learning and deep learning algorithms particularly CNNs, LSTMs, and ensemble methods has significantly improved fault detection accuracy across different EV subsystems. Inverter fault diagnosis systems, such as those proposed by Prejbeanu (2023) and Ye et al. (2020), leverage pattern recognition and time-series analysis to identify complex nonlinear fault signatures that cannot be captured by simple threshold methods. These intelligent systems can learn from historical data and generalize to unseen fault scenarios, providing predictive capabilities beyond traditional fault-tolerant control.

Third, the integration of IoT and AI-based edge intelligence has revolutionized EV battery and charging system maintenance. The studies by Nathiya et al. (2025), Yang et al. (2021), Li et al. (2024), and Zhang et al. (2024) highlight how IoT-based monitoring and cloud analytics enable remote fault tracking, data visualization, and predictive maintenance. These architectures extend FPGA systems' capabilities beyond onboard diagnosis by adding scalability and continuous learning. The combination of FPGA at the edge for fast anomaly detection and cloud-based AI for global model retraining forms an adaptive diagnostic loop—ensuring both responsiveness and long-term system learning.

Additionally, predictive control algorithms, as implemented by Karaki et al. (2024), demonstrate how FPGA-based controllers can actively manage system stability during grid disturbances. The FPGA-enabled MPC architecture allowed fast recalculation of reference voltages and switching states, ensuring uninterrupted operation during asymmetrical grid faults. This finding underscores how fault prediction and control can coexist on a single hardware platform, paving the way for self-healing EV systems that can detect and mitigate faults simultaneously.

At the system level, Peyghami et al. (2020) emphasized that increasing converter density and distributed control introduce new reliability challenges such as electromagnetic coupling, thermal aging, and control loop instability. However, the studies collectively show that FPGA-embedded diagnostic systems can mitigate these risks through precise control timing and predictive health monitoring. By continuously analyzing sensor data and implementing redundancy, FPGA-based systems can identify degradation trends long before catastrophic failure occurs

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8 BIT SAR ADC

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Abstract - This project presents the design, simulation, and analysis of an 8-bit low-power Successive Approximation Register Analog-to-Digital Converter implemented in 180nm CMOS technology, specifically targeting medical implant applications like pacemakers. The architecture was selected for its optimal trade-off between resolution, speed, and power efficiency, making it suitable for energy-constrained systems such as biomedical devices and IoT sensors. The ADC consists of key blocks including a bootstrap-based Sample and Hold circuit, a binary-weighted capacitive Digital-to-Analog Converter, a two-stage dynamic comparator, and asynchronous SAR logic. The bootstrap switch enhances input linearity and settling speed by dynamically reducing gate-source voltage errors. Simulations in Cadence Virtuoso demonstrated accurate sampling of a 500 mV, 150 Hz input signal with an average dynamic power consumption of 13.54 nW and static power of 4.35 pW. An efficient DAC switching scheme was employed to reduce overall energy usage and speed up conversion. The DAC achieved low static power, good linearity (±0.5 LSB INL/DNL), and fast settling times, which are essential for real-time SAR operation. The two-stage dynamic comparator, consisting of a pre-amplifier and latch, enabled rapid and reliable bit decisions, validated through transient and static power simulations. Simulation results confirmed the correct operation of all eight SAR conversion cycles, with the DAC output exhibiting a staircase response that closely tracks the analog input. The asynchronous logic improved speed by allowing self-timed operation without a global clock, reducing latency and power consumption. Layout-level optimizations ensured compact area and minimized parasitics, enhancing suitability for SoC integration.

Keywords - Successive Approximation, Analog-to-Digital Converter, Quantization, Comparator Circuit, Sample and Hold, Resolution

I. INTRODUCTION

An Analog-to-Digital Converter (ADC) is an essential electronic component that converts continuous analog signals into discrete digital values, enabling seamless interaction between the analog and digital worlds. ADCs are widely used in applications where analog data, such as temperature, sound, light, pressure, or voltage, needs to be processed by digital systems like microcontrollers, computers, and embedded devices. This conversion is vital in ensuring that real-world signals can be analyzed, stored, or transmitted efficiently in digital form. The ADC conversion process involves three main steps: sampling the input signal at regular intervals, quantizing it into discrete levels, and encoding it into a binary format for further digital processing. The accuracy and efficiency of this process depend on key parameters such as resolution (measured in bits), sampling rate, and SNR. Higher resolution ADCs provide more precise digital representations of the analog signal, while faster sampling rates allow accurate digitization of rapidly changing signals. There are

several types of ADCs, each suited for specific applications based on trade-offs between speed, accuracy, and power consumption. Flash ADCs offer extremely fast conversions, making them ideal for high-speed applications such as video and radar processing. Successive Approximation Register (SAR) ADCs balance speed and accuracy, commonly used in industrial automation and medical devices. Delta-Sigma ADCs provide high-resolution conversion with excellent noise filtering, making them well-suited for audio processing and precision measurement systems. Dual Slope ADCs, known for their high accuracy and noise immunity, are often used in digital multimeters and low-speed instrumentation. ADCs play a crucial role in a wide range of fields, including signal processing, medical diagnostics, industrial automation, instrumentation, and communication systems. In consumer electronics, ADCs are integral to devices such as smartphones, digital cameras, and audio recording equipment, ensuring high-fidelity signal conversion. In the automotive industry, ADCs are used for engine control, battery management in electric vehicles, and advanced driver-assistance systems (ADAS). With the rise of the Internet of Things (IoT), ADCs are increasingly embedded in smart sensors and wireless devices, enabling real-time monitoring and data acquisition in various applications, from smart homes to environmental sensing.As technology continues to

advance, ADCs are becoming more efficient, with improvements in resolution, power efficiency, and speed, further expanding their applications in modern digital systems.

II. LITERATURE SURVEY

Implementation of an 8-bit ADC using successive subtraction technique This project proposes an 8-bit ADC using operational amplifiers in a successive subtraction method, operating entirely in the analog domain without requiring a clock, DAC, or decoder. It consumes 242 mW power, has a settling time of 156 µs, and is suitable for low-speed applications like digital thermometers and voltmeters. An 8-Bit 800 MS/s Loop-Unrolled SAR ADC With Common-Mode Adaptive Background Offset Calibration in 28 nm FDSOI This paper presented a low-power, single-channel 8-bit, 800 MS/s LU-SAR ADC with a novel common-mode adaptive background comparator offset calibration scheme. The proposed calibration method ensures precise offset correction by adapting to the common-mode voltage variations during SAR conversion, improving accuracy without requiring additional low-noise comparator designs. By leveraging capacitor splitting and single-sided switching in the capacitive DAC, the ADC achieves optimized power efficiency and reduced noise in LSB decisions. The prototype, fabricated in 28 nm FDSOI CMOS, demonstrated an SNDR of 42.57 dB and an energy efficiency of 22.8 fJ/conv.-step, achieving a competitive figure-of-merit (FoM). These results validate the effectiveness of the proposed techniques in enhancing performance while maintaining minimal design complexity and area (0.0037 mm²), making it a promising approach for high-speed, power-efficient ADC applications. A High-Speed 2-bit/Cycle SAR ADC With Time-Domain Quantization This brief presents a high-speed 9-bit, 700-MS/s SAR ADC that utilizes time-domain quantization to achieve a 2-bit/cycle conversion rate. By leveraging a duplicated dynamic comparator for time reference generation, the design eliminates the need for complex timing calibration, enhancing system reliability and power efficiency. The architecture effectively addresses errors caused by reference mismatches and incomplete DAC settling through a nonbinary weighted approximation and an adder-based encoding scheme. Simulation demonstrate that the ADC maintains high performance with minimal degradation in effective number of bits (ENOB). Thus, this approach significantly improves conversion speed while maintaining accuracy, making it a viable solution for high-speed, medium resolution ADC applications 6 A 12-bit, 2.5-bit/Phase Column-Parallel Cyclic ADC Designing 8-BIT SAR ADC A 12-bit, 1.67-MS/s two-stage cyclic ADC has been designed and fabricated using UMC 180 nm CMOS technology for high-resolution and high-speed CMOS image sensor (CIS) applications. By implementing a 1.5-bit algorithm within a 2.5-bit framework, the proposed architecture significantly improves conversion speed—achieving more than a threefold enhancement compared to conventional two- stage cyclic ADCs. The design effectively reduces the number of comparators, leading to a 25% power savings while maintaining a high sampling rate. With a low power consumption of 435 µW and a figure of merit (FoM) of 0.31 pJ/conversion-step, this ADC demonstrates excellent efficiency. The proposed ADC presents an optimized balance between speed, power efficiency, and area, making it a promising solution.

III. PROBLEM DEFINITION AND PROPOSED SOLUTION

A. Problem Definition

The objective of this project is to design and simulate an 8-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) using Cadence Virtuoso. The goal is to achieve a compact, low-power, and high-speed ADC architecture suitable for integration in mixed-signal systems. The SAR ADC must reliably convert analog input voltages into corresponding 8-bit digital outputs within a defined input range (typically 0–Vref), ensuring linearity, accuracy, and proper timing functionality. The design must be validated through schematic-level simulation, focusing on key performance metrics such as power consumption and conversion speed.

B. Proposed Solution

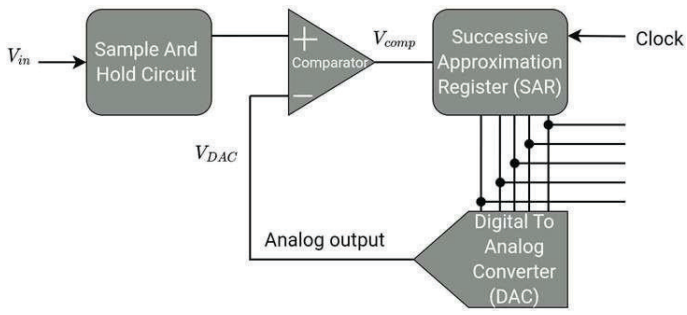
An 8-bit SAR ADC was successfully designed and simulated using Cadence Virtuoso at schematic level. The design consists of the following key blocks:

- Sample-and-Hold (S/H) Circuit – captures the analog input voltage.
- Binary-Weighted Capacitive DAC – generates comparison voltages during each bit decision.
- Comparator – compares the DAC output with the input and guides the SAR logic.
- SAR Logic – controls the bit-by-bit approximation process.

Simulation was performed using Spectre in Cadence Virtuoso, validating the functional operation of the SAR ADC across all 8 bits. The design successfully performed analog-to-digital conversions for input signals within the reference voltage range, demonstrating correct binary outputs.

IV. METHODOLOGY

The block diagram of the 8-bit SAR ADC consists of four major functional units that work together to convert an analog input signal into its 8-bit digital representation. Each block is optimized for low power consumption, compact area, and high accuracy, making the design suitable for biomedical applications.



4.1. **SampleandHold(S/H)Circuit:**

This block captures the analog input voltage and holds it steady during the analog-to-digital conversion. A bootstrap switch is integrated to improve linearity and speed by ensuring that the sampling transistor operates efficiently,

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even at low supply voltages. This stability is essential for precise bit- by-bit comparison.

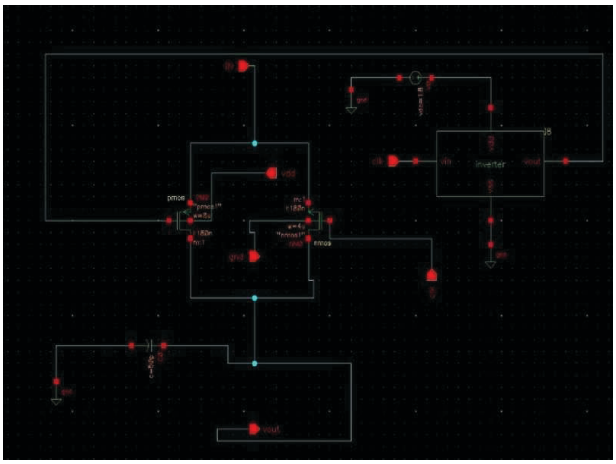


Fig1:sample and hold

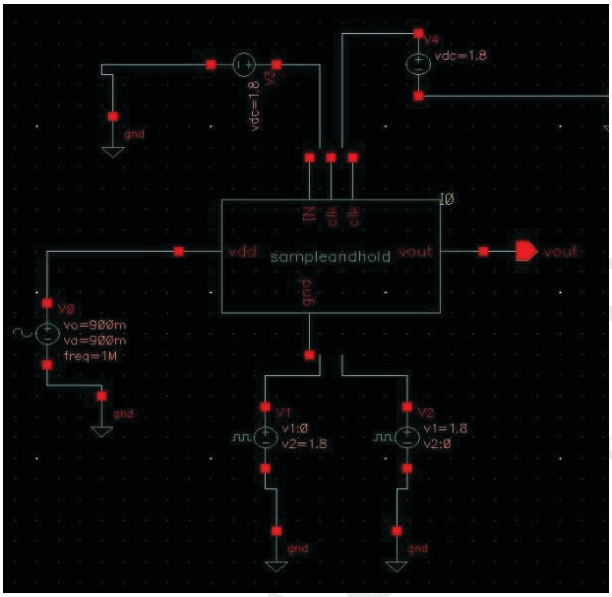


Fig:2sample and hold testbench

4.2. Capacitive Digital-to-Analog Converter:

The DAC is responsible for generating a reference voltage corresponding to each trial digital code during the conversion process. It uses a binary-weighted capacitor array based on charge redistribution principles. The DAC provides fast settling time and excellent linearity, which are critical for maintaining conversion accuracy.

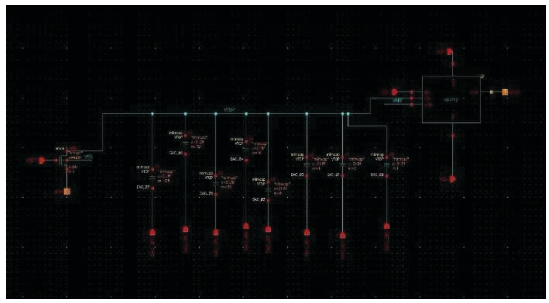


Fig3: Capacitive DAC

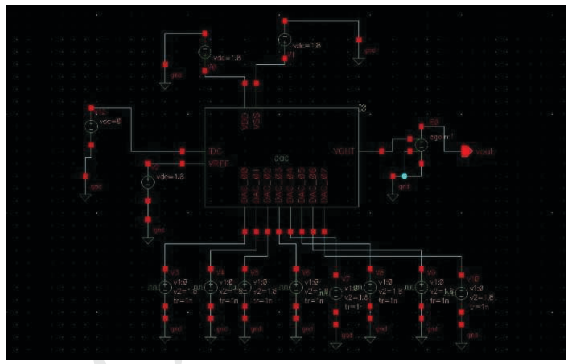


Fig4: Capacitive DAC testbench

4.3 Comparator :

The comparator compares the held analog input voltage from the S/H circuit with the DAC output. A two-stage dynamic comparator is used here, consisting of a preamplifier stage and a decision (latch) stage. It ensures fast and reliable resolution of each bit while minimizing static power consumption.

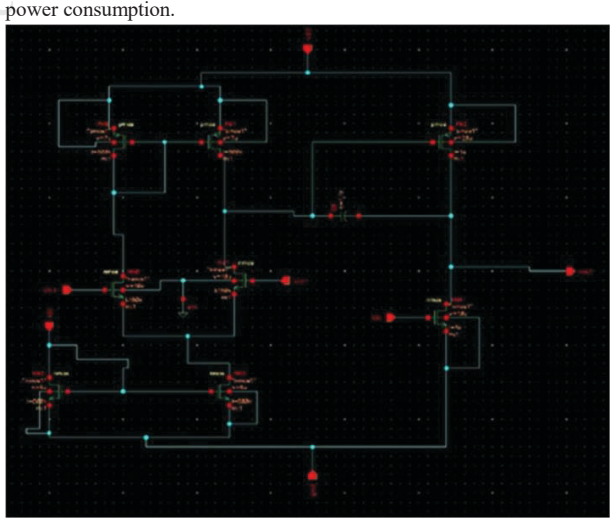


Fig5:Comparator

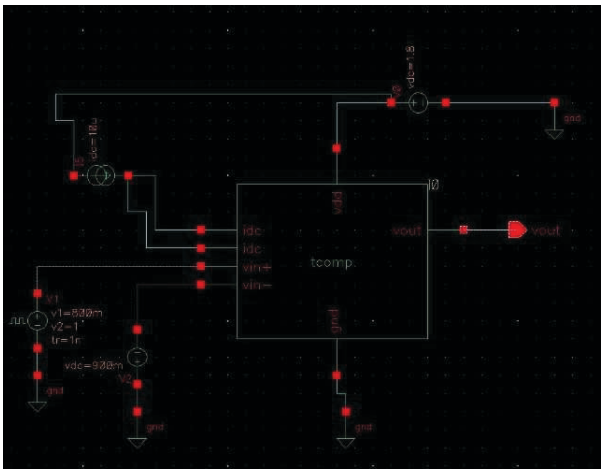


Fig6: Comparator Testbench

4.4 Successive Approximation Register (SAR) Logic:

The SAR logic performs a binary search algorithm to determine the final digital output. Starting with the Most Significant Bit (MSB), it iteratively sets or clears bits based on the comparator's output. The logic controls the DAC accordingly in each cycle. The asynchronous operation allows self-timed transitions between bit decisions, reducing the need for a global clock and thereby saving power.

RESULTS AND DISCUSSION

A. Results

The proposed 8-bit Successive Approximation Register ADC was designed to balance high speed, accuracy, and low power consumption, using Cadence Virtuoso for schematic and layout design, and Spectre for simulation. The design incorporated key components such as a Sample and Hold circuit, SAR logic, a current-mode comparator, and a current-steering DAC. Functional Performance: Simulations validated the correct operation of the SAR ADC across all eight bit cycles. The comparator accurately resolved input differences, and the DAC output closely tracked the analog input during bit approximation. The End-of-Conversion signal confirmed timely and accurate digital output at the end of each conversion cycle. The ADC output followed a staircase response typical of SAR behavior, indicating that the binary search logic was functioning as intended. The system responded well to various input voltage levels, maintaining precision and stability throughout. Speed and Timing: The asynchronous architecture proved beneficial in reducing the overall conversion time. The use of internal control signals allowed the system to proceed to the next bit decision without waiting for a global clock. This self-timed mechanism made the SAR ADC well-suited for applications requiring low-latency data processing, such as medical imaging or real-time signal acquisition. Although the prototype was simulated for moderate sampling rates, the architecture has the potential to scale towards higher speeds with improvements in layout optimization and technology node scaling. Power and Area Efficiency. The DAC and comparator were only active during bit decision cycles, and inactive otherwise, reducing unnecessary switching activity. The modular SAR logic also allowed for efficient control with limited gate usage. In terms of layout, the area was compact, with minimal parasitic effects. The use of hierarchical design helped isolate sensitive analog blocks, preserving performance during physical implementation.

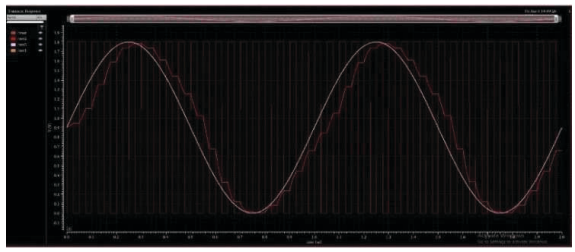


Fig7: Sample and hold output

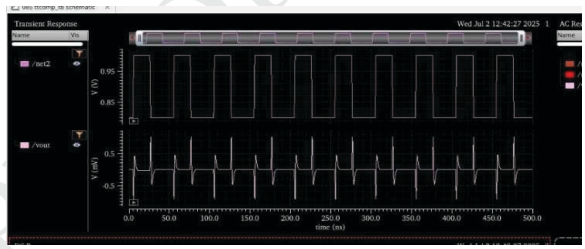


Fig8: comparator output

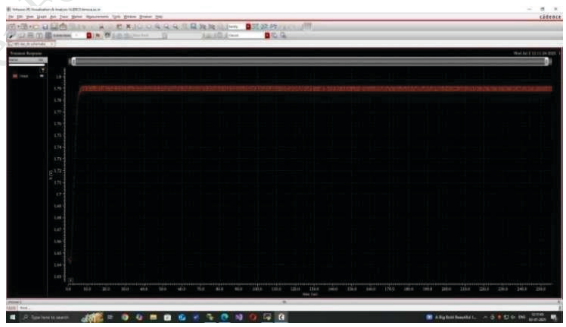


Fig9: DAC output

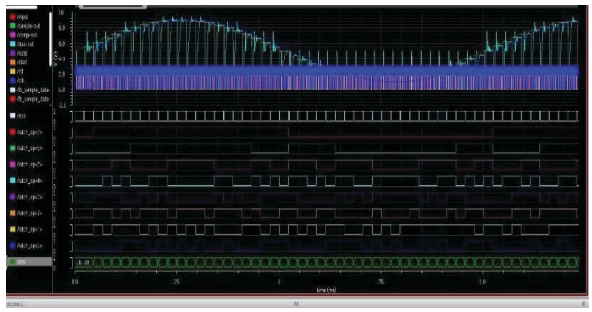


Fig10: SAR ADC output

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A WSN-Integrated Solar Energy Harvesting System for Smart Agriculture

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Abstract: Agricultural farms require efficient energy management and real-time environmental monitoring to optimize crop yields and resource utilization. To address these needs, we propose a Solar Energy Harvesting System for Agriculture using a **Wireless Sensor Network (WSN)**. The system integrates an Arduino-based Maximum Power Point Tracking (MPPT) algorithm with a dynamic solar tracking mechanism to maximize solar energy capture. The harvested energy powers a WSN comprised of **soil moisture**, **temperature**, and **humidity sensors**, **enabling continuous monitoring of critical environmental parameters**. Data is transmitted wirelessly via **ESP8266** to the Blynk IoT platform, providing farmers with remote access and control through a user-friendly interface. Upon detecting suboptimal conditions, the system can trigger automated irrigation or other corrective actions. By integrating these components, the system provides **24/7 environmental monitoring**, **automated energy harvesting**, and remote data access with minimal human intervention. This project aims to improve crop yields and promote sustainable farming practices by offering an affordable, efficient, and scalable energy and monitoring solution. Future enhancements may include predictive analytics for crop management, integration of weather data, and expansion of sensor capabilities to monitor additional environmental factors, further improving farm efficiency and sustainability.

Keywords: Solar Energy Harvesting, Smart Agriculture, WSN, Remote Monitoring, Sustainable Farming

I. Introduction

This project aims to develop an **efficient energy management and real-time environmental monitoring system** tailored for agricultural applications. Designed to **optimize crop yields** and **promote sustainable farming practices**, the system ensures enhanced energy utilization and data-driven decision-making by integrating solar energy harvesting with a wireless sensor network (WSN). Traditional agricultural practices often lack efficient methods for monitoring environmental parameters and maximizing renewable energy usage, leading to suboptimal resource allocation and increased operational costs. In contrast, this system offers an automated, **energy-efficient**, and **cost-effective solution** for modernizing agricultural operations. The **Solar Energy Harvesting System for Agriculture** using WSN is built using an **Arduino microcontroller**, a Maximum Power Point Tracking (MPPT) algorithm, light-dependent resistors (LDRs), servo motors, and a WSN with an **ESP8266 Wi-Fi module**. It continuously **adjusts the solar panel's orientation to capture maximum sunlight**, ensuring optimal energy harvesting. Simultaneously, the WSN monitors critical environmental parameters such as **soil moisture**, **temperature**, and **humidity**, transmitting data wirelessly to the **Blynk IoT platform**, enabling remote monitoring and control. Additionally, the system incorporates a rechargeable battery and a charging module to store and manage the harvested energy efficiently. While this system was initially designed for agricultural applications, where efficient energy use and real-time monitoring are crucial for crop health and resource management, its **versatility** makes it suitable for **multiple environmental monitoring applications**. Whether used for precision **agriculture**, **greenhouse management**, or **environmental research**, this solution provides **24/7 monitoring, automated energy harvesting, and remote data access**, making agricultural management more sustainable and effective.

II. Methodology and Implementation

2.1 Methodology

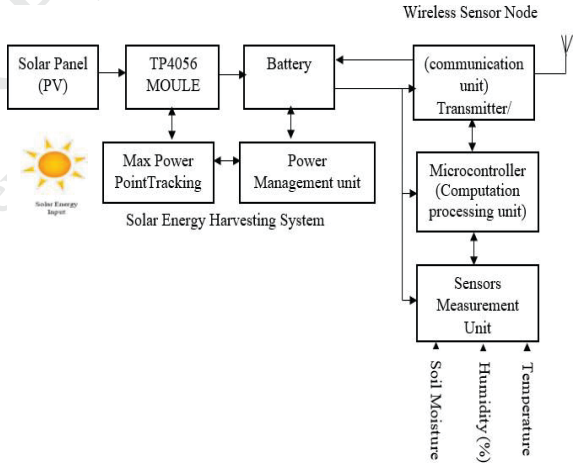


Fig.1- Block diagram

The system is powered by a solar panel (PV), which captures sunlight and converts it into electrical energy. A TP4056 module is used for charging a battery. The battery provides a stable power supply to the other components. A Maximum Power Point Tracking (MPPT) unit optimizes the power output from the solar panel. This maximized power output is then supplied to the power management unit. The Wireless Sensor Node uses a Microcontroller which serves as a computation processing unit, that processes sensor inputs and triggers the appropriate data acquisition. Soil Moisture, Humidity, and Temperature sensors serve as measurement units. Transmitter and Receiver unit is used as a communication unit. Together, these components ensure automated, real-time monitoring and sustainable operation for the agricultural environment

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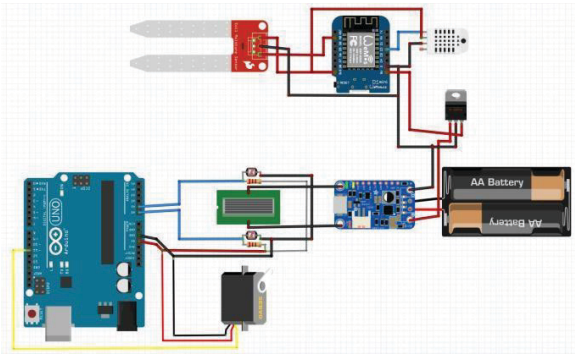


Fig.2- Block diagram

III. Working flow

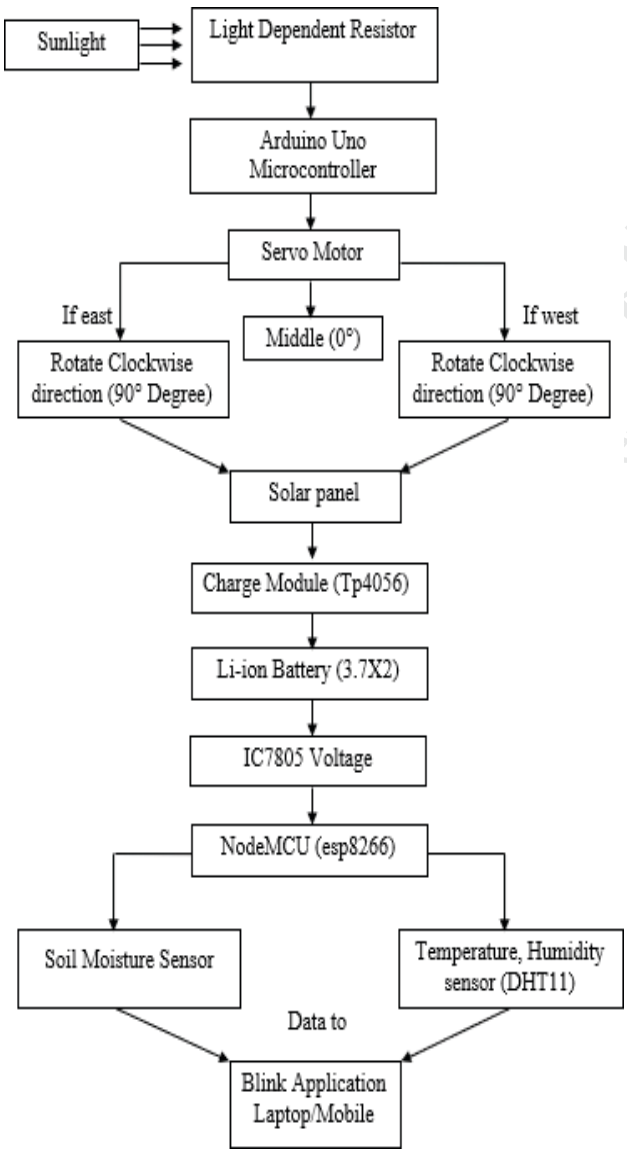


Fig.3- Flow diagram

Sequence of Workflow

1. Light Dependent Resistor (LDR) Sunlight Detection
   - LDRs detect sunlight intensity.
   - If Sunlight is detected: Sends a signal to the Arduino Uno Microcontroller.
   - If No sunlight is detected: No action.
2. Arduino Uno Microcontroller Processing
   - Receives input from LDRs.
   - Calculates optimal solar panel angle.
3. Servo Motor Control
   - If the optimal angle is East: Rotate the solar panel clockwise (90 degrees).
   - If the optimal angle is West: Rotate the solar panel counter-clockwise (90 degrees).
   - If the optimal angle is Middle: Maintain position (0 degrees).
4. Solar Panel Energy Harvesting.
   - Captures sunlight and converts it to electrical energy.
5. Charging and Power Regulation
   - Charge Module (TP4056) manages the charging of the Li-ion Battery (3.7X2).
   - IC7805 Voltage Regulator provides a stable voltage supply.
6. Data Collection
   - Soil Moisture Sensor and Temperature/Humidity Sensor (DHT11) collect environmental data.
7. Data Transmission
   - NodeMCU (ESP8266) transmits sensor data wirelessly.
8. Remote Access and Monitoring
   - Data is sent to the Blynk Application, which can be accessed via Laptop/Mobile.

This workflow ensures automated solar tracking, efficient energy harvesting, and real-time monitoring, enhancing agricultural efficiency.

3.1 Automatic Sunlight Tracking

The Solar Energy Harvesting System employs an automatic sunlight tracking mechanism to maximize energy capture throughout the day. Light Dependent Resistors (LDRs) are strategically positioned to detect the intensity of sunlight from various angles. These LDRs act as sensors, providing input to the Arduino Uno microcontroller. The Arduino, programmed with a specific algorithm, processes the LDR readings to determine the optimal angle for the solar panel to receive maximum sunlight. Based on this calculation, the Arduino sends a control signal to a servo motor. The servo motor then precisely adjusts the orientation of the solar panel, rotating it to the calculated optimal position. This continuous, automated adjustment ensures that the solar panel remains aligned with the sun's trajectory, maximizing energy absorption and conversion, resulting in a more eco-friendly and efficient electricity source.

1.1 Remote Monitoring via the Blynk IoT Platform

The Solar Energy Harvesting System incorporates remote monitoring capabilities through the Blynk IoT platform, offering users real-time data visualization and control. Utilizing the ESP8266 Wi-Fi module, sensor data including soil moisture, ambient temperature, and humidity levels is transmitted wirelessly to the Blynk cloud. This enables farmers to remotely access and monitor critical environmental parameters through the Blynk mobile application on their smartphones or a web-based interface on their laptops. By leveraging this readily available information, farmers can make informed decisions about irrigation scheduling, fertilizer application, and proactive adjustments to optimize growing conditions, all from a remote location. This remote access not only reduces the need for frequent on-site inspections but also empowers farmers to respond quickly to changing environmental conditions, minimizing potential crop stress and maximizing overall resource efficiency, contributing to more sustainable and productive agricultural practices. Furthermore, the Blynk platform allows for customizable alerts and notifications, ensuring timely intervention when conditions deviate from pre-defined optimal ranges, enabling a truly proactive approach to farm management.

IV. Results and Observations

1. **Efficient Solar Tracking**
   - LDR-based tracking system effectively adjusted the solar panel's angle to maximize sunlight capture throughout the day.
   - Servo motors responded accurately to the Arduino's commands, ensuring precise panel positioning.
2. **Effective Energy Harvesting**
   - The MPPT algorithm optimized power extraction from the solar panel, increasing the harvested energy compared to a fixed panel.
   - The charging module (TP4056) efficiently charged the battery, providing a stable power supply.
3. **Reliable Environmental Monitoring**
   - Soil moisture, temperature, and humidity sensors provided accurate and consistent readings.
   - Data was successfully transmitted wirelessly via the ESP8266 Wi-Fi module to the Blynk IoT platform.
4. **Remote Accessibility and Control**
   - Users were able to remotely monitor sensor data and system performance through the Blynk mobile app.
   - The Blynk platform provided a user-friendly interface for data visualization and analysis.
5. **Energy Efficiency**
   - The system operated with minimal power consumption, ensuring continuous monitoring.
   - The rechargeable battery provided sufficient power for extended operation, even during periods of low sunlight.
6. **Potential for Sustainable Agriculture**
   - The system offers a cost-effective and sustainable solution for optimizing energy usage.
   - The use of renewable energy reduces reliance on traditional power sources, promoting environmentally friendly practices.

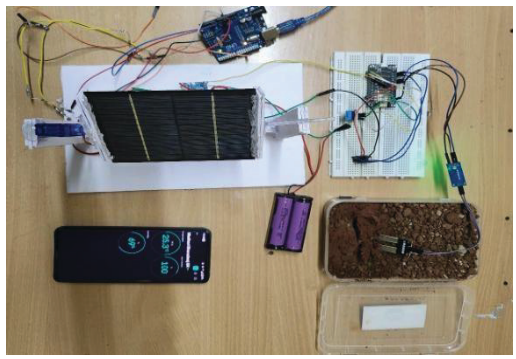


Fig.4- Implemented model picture

V. Conclusion

The Solar Energy Harvesting System for Agriculture using WSN represents a viable and sustainable approach to addressing contemporary challenges in agricultural practices. By effectively integrating solar energy harvesting with wireless sensor network technology, the system enables optimized energy utilization and facilitates real-time environmental monitoring. The implementation of an Arduino-based Maximum Power Point Tracking (MPPT) algorithm, in conjunction with Light Dependent Resistor (LDR)-controlled solar tracking, ensures maximal energy capture from a renewable source, which in turn minimizes the reliance on conventional power grids. While acknowledging certain limitations, such as the reliance on consistent solar irradiance and the range of the wireless sensor network, the project successfully demonstrates the transformative potential of renewable energy sources and IoT technologies in revolutionizing agricultural methodologies. This research paves the way for smarter, more sustainable, and more resource-efficient farming solutions, thereby fostering enhanced crop yields and improved environmental stewardship. Further development and deployment of such systems could significantly contribute to the advancement of precision agriculture and the promotion of environmentally conscious farming practices on a broader scale.

VI. Limitation and Future Scope

- Energy Source Diversification- The system's energy resilience can be enhanced by exploring **hybrid energy sources** such as wind, thermal, and kinetic, in addition to solar, to mitigate the impact of weather-dependent solar irradiance.
- Adaptive Energy Management- Optimizing energy usage through **dynamic energy management** strategies is crucial. This involves leveraging real-time sensor data and environmental conditions to adaptively adjust energy allocation and consumption.
- Efficient Power Conversion Maximizing energy harvesting efficiency requires integrating advanced power conversion techniques, such as a **Boost Converter** with Maximum Power Point Tracking, **to ensure optimal power extraction from the solar panel.**

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- Expanded Application Scope- The system's functionality can be **broadened** by incorporating additional Wireless Sensor Network (WSN) applications beyond basic environmental monitoring. This includes integrating precision irrigation, disease detection, and livestock tracking capabilities to provide a more comprehensive agricultural management solution.
- Sensor Data Accuracy and Reliability- Improve accuracy by using **AI technologies**
- Scalability and Customization- A modular design approach would facilitate system scalability and customization, enabling easy adaptation to different farm sizes, layouts, and monitoring requirements.
- Remote Control Capabilities- Implementing **remote actuation** capabilities would allow farmers to remotely control irrigation systems, lighting, and other agricultural equipment, providing greater flexibility and control over farm operations.
- Robust Security Measures- Protecting data integrity and system security requires implementing **robust encryption** and authentication protocols to prevent unauthorized access, cyberattacks, and data breaches.

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Leakage Power Reduction in SRAM Cell Using Circuit Level Approach in 45nm Technology

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Abstract: With the rapid advancement of **nanometre-scale CMOS technology**, leakage power has become a dominant challenge in **Static Random Access Memory (SRAM)** design, particularly for energy-constrained applications such as IoT devices, embedded systems, and portable electronics. This research presents a circuit-level approach to minimize leakage power in SRAM cells using 45nm CMOS technology. Various SRAM architectures ranging from **6T to 12T** were designed and simulated using Cadence Virtuoso. Techniques such as the Sleep approach and the Stack & Sleep approach were implemented to suppress subthreshold and gate-induced drain leakage currents during standby mode. Comparative analysis demonstrates that the 12T SRAM cell, which combines both techniques, achieves the most significant leakage power reduction while maintaining performance and stability. Key parameters including leakage power, area, and **static noise margin (SNM)** were evaluated to assess trade-offs. The results validate the effectiveness of circuit-level leakage mitigation strategies for low-power VLSI design. This work contributes to the development of scalable and energy-efficient SRAM designs for next-generation computing systems. Future work may explore integration with **FinFET** or **MTCMOS** technologies and system-level validation in full memory arrays.

Keywords: SRAM, Leakage Power Reduction, 45nm CMOS, Sleep Transistor, Stack Technique, Low-Power VLSI

I. INTRODUCTION

This project aims to design an energy-efficient and leakage-resilient **Static Random Access Memory (SRAM)** system tailored for ultra-low-power electronic applications. As CMOS technology continues to scale down to deep submicron nodes like 45nm, power dissipation particularly leakage power has emerged as a critical challenge in VLSI memory design. SRAMs, which are heavily used in processors, cache memory, and **System-on-Chip (SoC)** architectures, are highly susceptible to subthreshold leakage and **gate-induced drain leakage (GIDL)**, especially during standby mode. These unwanted leakages degrade energy efficiency and can compromise the reliability and lifespan of battery-powered systems such as embedded processors, wearable devices, and IoT sensor nodes.

Traditional 6T SRAM architectures struggle to maintain performance and stability at such technology nodes, leading to increased static power consumption, reduced noise margins, and compromised scalability. To overcome these limitations, this project proposes the use of circuit-level techniques specifically the Sleep and Stack & Sleep approaches to minimize leakage power without significantly increasing area or access delay. These techniques work by isolating idle SRAM blocks from the power supply using sleep transistors and enhancing resistance paths using stacked transistors, thereby effectively suppressing leakage current during inactivity.

The proposed solution involves the design and comparative analysis of multiple SRAM cell configurations, ranging from conventional **6T up to 12T** architectures, each enhanced with leakage-reducing elements. All designs are simulated using the Cadence Virtuoso platform with a 45nm CMOS process to evaluate parameters such as leakage power, delay, area, and **static noise margin (SNM)**. Although the project focuses on memory cells, the techniques are widely applicable across low-power digital systems that rely on SRAM as a core memory unit. The scalable and modular nature of the approach allows its integration into larger memory arrays and SoC designs, promoting energy efficiency in a wide range of applications—from smart sensors to biomedical electronics and edge computing systems. This solution enables modern digital circuits to achieve improved performance-per-watt metrics while addressing the pressing demand for sustainable and reliable semiconductor technologies.

II. METHODOLOGY AND IMPLEMENTATION

2.1 METHODOLOGY

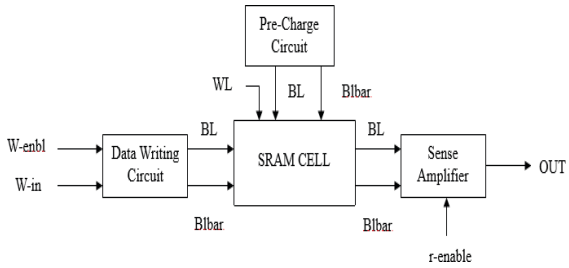


Fig.1- Block diagram

This work explores circuit-level techniques for minimizing leakage power in SRAM cells implemented in 45nm CMOS technology. As devices scale down, leakage currents particularly subthreshold and gate leakage become increasingly prominent, especially in SRAM cells that require continuous power to retain data. To address this issue, two established techniques are considered: the Sleep technique and the Stack & Sleep technique, both aimed at reducing standby power consumption without compromising performance.

In the Sleep technique, additional transistors referred to as sleep transistors are introduced between the power rail (VDD) or ground and the SRAM cell. These transistors are deactivated during idle periods, effectively disconnecting the cell and minimizing leakage paths. The Stack & Sleep technique further enhances this by incorporating series-connected transistors in the pull-up or pull-down paths, increasing the effective channel resistance and significantly

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reducing subthreshold leakage. Multiple SRAM architectures, including 6T, 7T, 8T, 9T, 10T, 11T, and 12T cells, are modelled at the transistor level using Cadence Virtuoso. Each design is optimized for transistor sizing to ensure data stability and reliable read/write operations. Simulations are performed using Cadence Spectre, with key metrics such as leakage power, access delay, and Static Noise Margin (SNM) evaluated under standard conditions. The methodology enables a comparative analysis of leakage reduction techniques across different SRAM topologies, supporting the design of power-efficient memory suitable for low-power digital systems.

2.2 WORKING OF SRAM

A. 6T SRAM CELL

The 6T SRAM cell consists of six transistors four forming two cross-coupled inverters to store data and two NMOS access transistors to enable read and write operations. The cross-coupled inverters maintain the stored value through positive feedback, allowing the cell to retain data as long as power is supplied. During a write operation, the bit lines (BL and BLB) are driven with the new data and its complement, and the word line (WL) is asserted to turn ON the access transistors. The stronger write drivers overpower the internal inverters, forcing the cell into the new state. For a read operation, the bit lines are initially precharged high and left floating. When WL is enabled, one of the bit lines is pulled down based on the stored data, creating a voltage difference that can be sensed externally. The transistor sizing plays a crucial role here: the pull-down transistors must be stronger than the access transistors to prevent the cell from flipping its state during a read. This ensures read stability, while writability requires that the access transistors be strong enough to override the stored state during a write. The design of the 6T cell thus balances stability, performance, and power consumption in a compact area-efficient configuration.

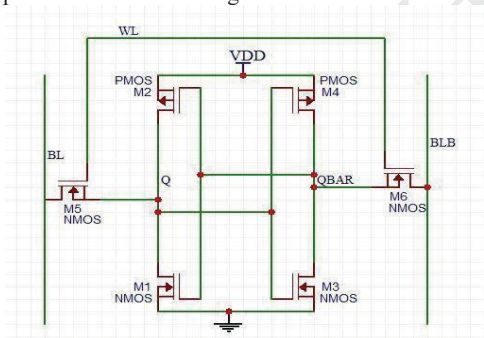


Fig.2- 6T SRAM CELL

B. 7T SRAM CELL

The 7T SRAM cell is an improved version of the conventional 6T cell, designed to enhance read stability and reduce power consumption by separating the read and write operations. It consists of seven transistors: four forming two cross-coupled inverters to store data, two NMOS access transistors for write and read access, and one additional NMOS transistor used to isolate the read path. During a write operation, the write access transistor is enabled via the write word line, allowing data to be written from the bit line into the storage node in the same way as the 6T cell. However, during a read operation, the additional NMOS transistor is used to isolate the internal storage node from the bit line. Instead, the read operation is carried out through a separate read path controlled by a read enable signal. This separation prevents disturbance of the stored data during a read and improves the cell's read stability. By avoiding direct access to the storage nodes during a read, the 7T SRAM cell minimizes the risk of data flipping and allows for lower power dissipation compared to the conventional 6T structure.

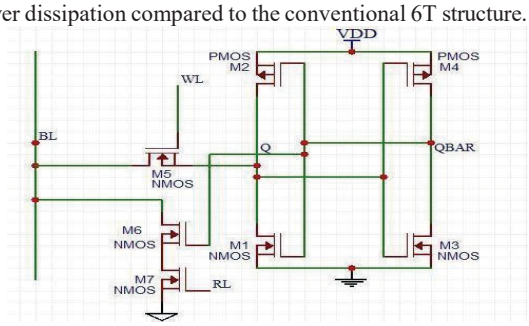


Fig.3- 7T SRAM CELL

C. 8T SRAM CELL (SLEEP APPROACH)

The 8T SRAM cell is designed to improve read stability by completely decoupling the read path from the internal storage nodes. It consists of eight transistors: six transistors forming the standard 6T SRAM storage structure and two additional transistors dedicated to a separate read path. The cross-coupled inverters store the data, while one access transistor handles write operations through the write bit line, similar to the 6T cell. During a write operation, the word line enables the write access transistor, allowing data to be written into the cell via the bit lines. For the read operation, a dedicated read word line and a read bit line are used. When the read word line is enabled, the read-access transistor connects a precharged read bit line to ground, depending on the data stored in the internal node. This mechanism allows the bit line to discharge or remain high without disturbing the actual stored data, thereby significantly improving read stability and reducing the risk of read-induced failures. Additionally, the isolation of the read path enables more aggressive sizing of the storage inverters for better performance while maintaining robust operation under low-power conditions.

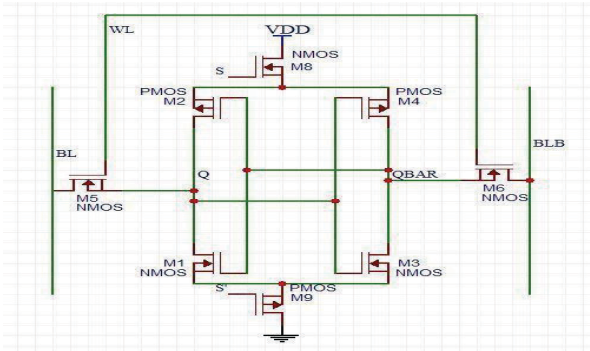


Fig.4- 8T SRAM CELL

D. 9T SRAM CELL (SLEEP APPROACH)

The 9T SRAM cell introduces additional transistors to further enhance data stability during read operations while continuing to isolate the read path from the internal storage nodes. It consists of nine transistors: six forming the conventional storage element, one for write access, and two for a separate read circuit. The write operation is performed similarly to the 6T cell, where the write access transistor is enabled by the write word line, allowing new data to be stored via the bit line. During a read operation, the internal nodes

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remain isolated, and a separate read word line and a precharged read bit line are used. The dedicated read circuitry includes a read access transistor and a pull-down transistor arranged such that when the stored value is '0', the read bit line is discharged, and when it is '1', the bit line remains high. This decoupled read mechanism eliminates the risk of disturbing the stored value during read access, greatly improving noise immunity and stability. The 9T design also offers enhanced resilience under low-voltage operation, making it suitable for applications that prioritize reliability and energy efficiency.

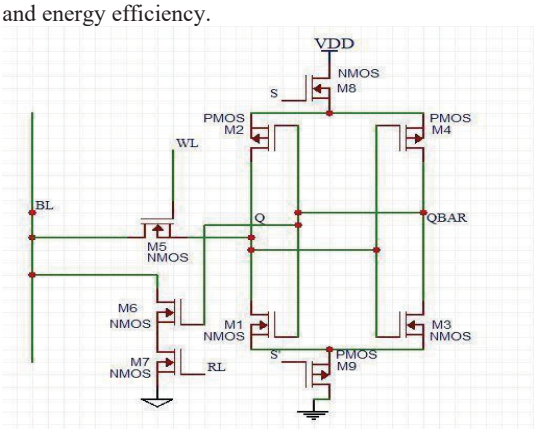


Fig.5- 9T SRAM CELL

E. 10T SRAM CELL (STACK APPROACH)

The 10T SRAM cell is designed using the Stack technique to achieve significant leakage power reduction during standby mode. It incorporates four additional transistors compared to the conventional 6T cell, specifically placed in series with the pull-down path of the cross-coupled inverters. This stacking arrangement increases the number of OFF transistors in the leakage path, leading to a higher effective resistance and substantially reduced subthreshold leakage current. The read and write operations are performed similarly to the 6T architecture, with access controlled by the word line and bit lines. However, the stacked transistors remain OFF during idle periods, creating a high-impedance path that limits leakage without compromising data retention. Although the added series resistance can slightly increase read and write delay, the trade-off results in improved static power efficiency, making the 10T cell suitable for low-power memory applications.

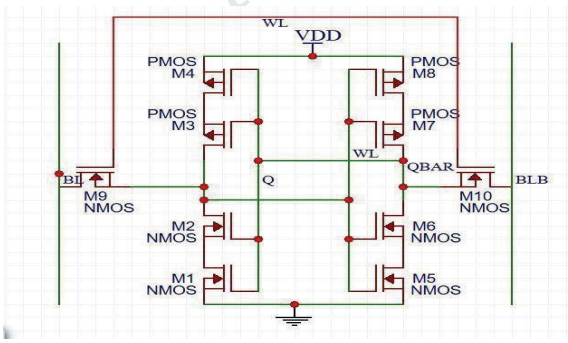


Fig.6- 10T SRAM CELL

F. 11T SRAM CELL (STACK APPROACH)

The 11T SRAM cell enhances the 10T design by introducing a separate read path, thereby decoupling read access from the internal storage nodes. This configuration includes the basic stacked pull-down network for leakage reduction, as in the 10T cell, along with an additional transistor dedicated to a non-intrusive read operation. The read path operates through a separate read bit line and read word line, which allows the stored data to be sensed without accessing or disturbing the internal storage nodes. This separation improves read stability and minimizes the risk of read-induced failures, particularly under low-voltage conditions. While the 11T cell introduces extra transistors, resulting in a moderate increase in area, it offers superior read reliability and efficient leakage suppression, making it well-suited for ultra-low-power and high-stability SRAM applications.

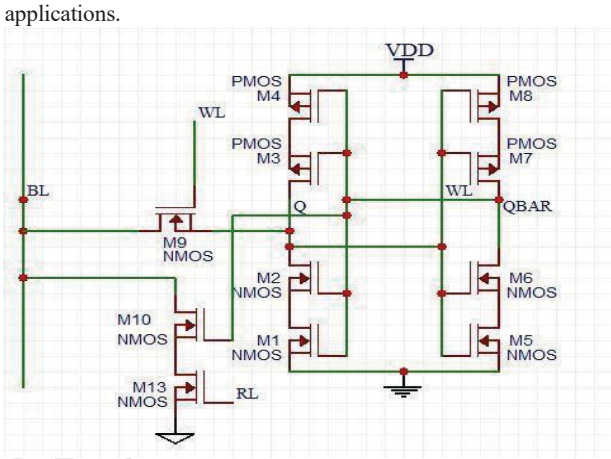


Fig.7- 11T SRAM CELL

G. 12T SRAM CELL (SLEEP & STACK APPROACH)

The 12T SRAM cell integrates both the Sleep and Stack techniques to maximize leakage power reduction and improve operational stability. This cell architecture includes sleep transistors that disconnect the storage elements from the power rails during standby, as well as stacked transistors in the pull-down paths to further limit leakage currents. Additionally, it features a dedicated read path, ensuring that the internal nodes remain completely undisturbed during read operations. The cell uses separate control signals for activating sleep mode and enabling read/write access. During active operation, all transistors function normally to allow standard read and write procedures. In standby mode, the sleep transistors are turned OFF, and the stacked configuration maintains a high-impedance leakage path, resulting in substantial static power savings. Although the 12T cell consumes more area than other variants, it achieves the best leakage performance and robust data retention, making it ideal for energy-constrained and reliability-critical applications such as embedded systems and IoT devices.

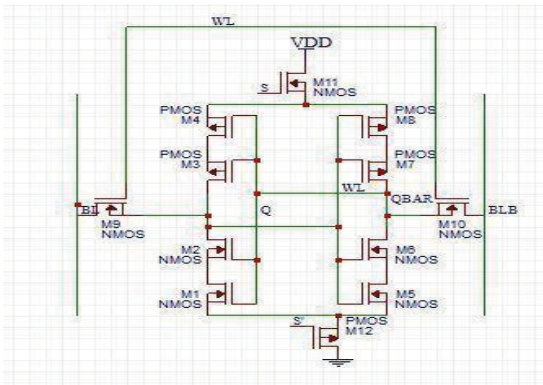


Fig.8- 12T SRAM CELL

2.3 SLEEP APPROACH

The Sleep approach is a circuit-level technique used to reduce leakage power in SRAM cells, particularly during standby mode. It involves inserting additional transistors, commonly referred to as sleep transistors, between the power supply (VDD) and the pull-up network, as well as between the pull-down network and ground. These transistors are controlled by a sleep signal and are turned off when the circuit is idle, effectively isolating the SRAM cell from the power rails. When both sleep transistors are turned off during standby, the logic network is disconnected from both VDD and ground, forming a high-impedance path. This increases the effective resistance between the supply and ground, which significantly minimizes the leakage current due to the stacking effect. The technique is implemented using both NMOS and PMOS transistors typically, NMOS sleep transistors are favored due to their lower on-resistance compared to PMOS for the same size. For example, in the 8T SRAM cell, two extra transistors are added to the conventional 6T cell: an NMOS transistor between VDD and the pull-up network, and a PMOS transistor between the pull-down network and ground. In active mode, both transistors remain ON, ensuring normal operation. However, in standby mode, turning them OFF reduces the static power dissipation by lowering the effective voltage across the SRAM cell nodes.

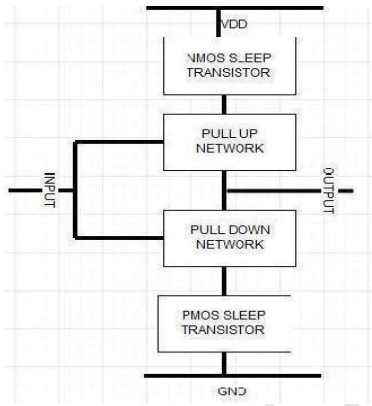


Fig.9- SLEEP ARRPOACH

2.4 STACK APPROACH

The stack technique is a widely adopted circuit-level method for reducing leakage power, particularly subthreshold leakage, in deep submicron CMOS technologies. In this approach, additional NMOS transistors are introduced in series with the existing pull-down path of the SRAM cell. During standby mode, both the original and the newly added transistors are turned off simultaneously. This stacking of transistors creates an intermediate node that floats to a non-zero potential due to leakage currents, effectively reducing the gate-to-source and drain-to-source voltages of both transistors. As a result, the subthreshold leakage current is suppressed exponentially, a phenomenon known as the "stacking effect." This effect increases the effective resistance in the leakage path, significantly lowering static power dissipation without the need for external control signals or power gating mechanisms. The technique proves especially advantageous in 45nm and smaller technologies, where leakage power dominates total power consumption even when the circuit is idle.

To implement the stack approach, the conventional 6T SRAM cell is modified by adding one or more transistors in the pull-down network. For instance, in a 10T SRAM design, an additional NMOS transistor is placed in series with the access or driver transistors. This configuration ensures that, when the cell is not being accessed, the stacked transistors remain in the OFF state, thereby minimizing leakage current paths. Although this method introduces marginal increases in cell area and read/write delay due to the added transistors and their parasitic capacitances, it offers a substantial reduction in leakage power, making it an effective solution for low-power SRAM design in modern VLSI systems.

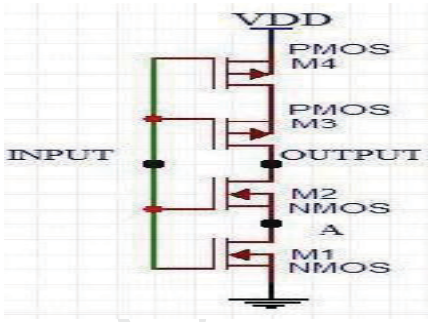


Fig.10- STACK ARRPOACH

III. SIMULATION

All SRAM cell configurations from 6T to 12T were designed and simulated at the transistor level using the Cadence Virtuoso platform with 45nm CMOS technology. The simulations were performed using the Spectre simulator to analyze key parameters such as leakage power, delay, and static noise margin (SNM) under a standard supply voltage of 1V. Each cell variant was tested in standby mode to measure leakage performance, and results showed that as the transistor count increased—with the integration of Sleep and Stack techniques—there was a consistent and notable reduction in leakage power. The simulation environment enabled accurate comparison between different SRAM topologies, validating the effectiveness of circuit-level techniques in minimizing leakage for low-power memory design.

A. SIMULATIONS OF 6T

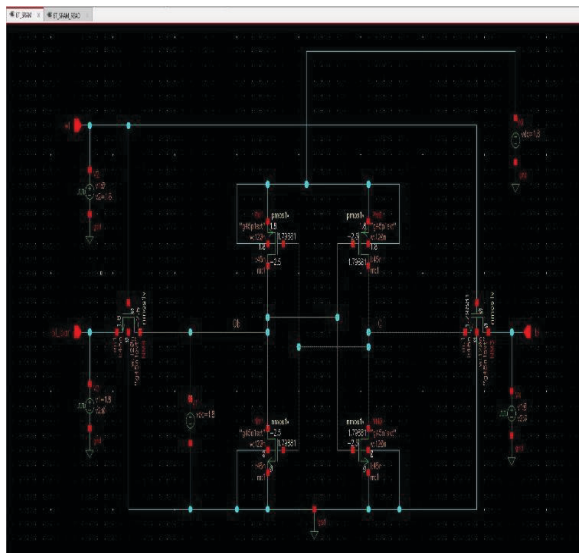


Fig.11- Schematic of 6T SRAM

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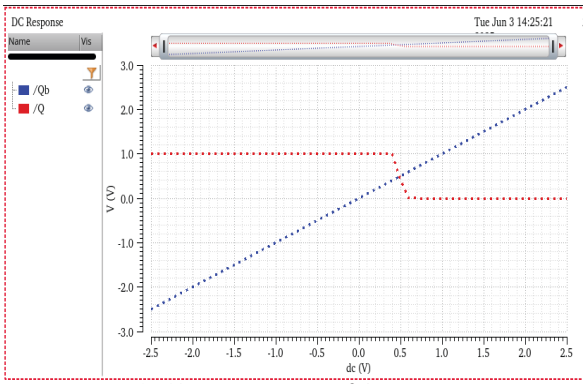


Fig.12- DC Response of 6T SRAM

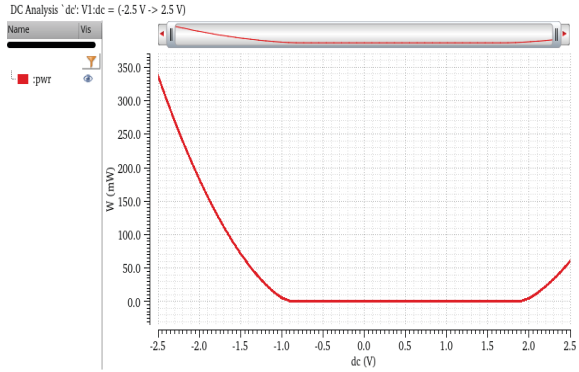


Fig.13- DC Analysis of 6T SRAM

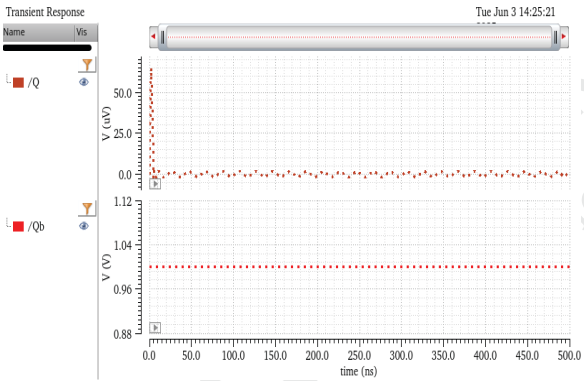


Fig.14- Transient Response of 6T SRAM

B. SIMULATIONS OF 7T

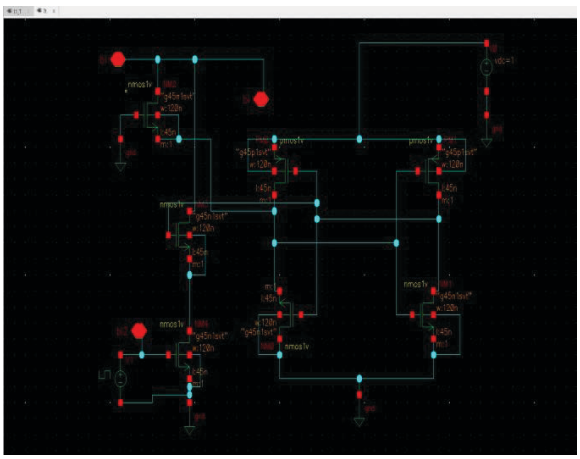


Fig.15- Schematic of 7T SRAM

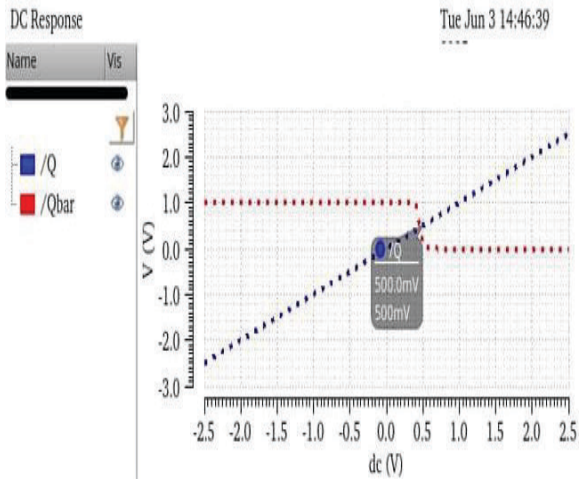


Fig.16- DC Response of 7T SRAM

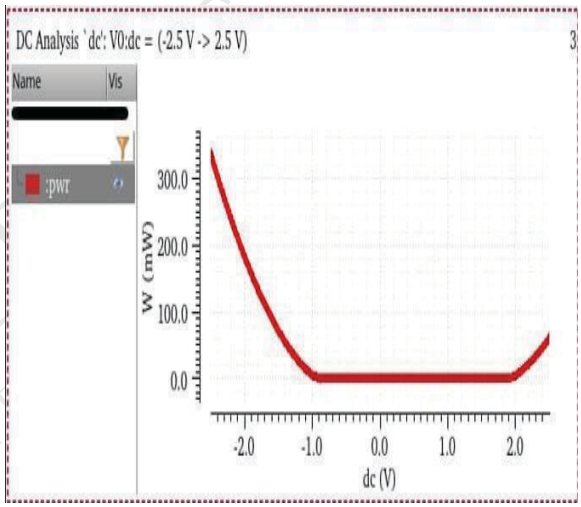


Fig.17- DC Analysis of 7T SRAM

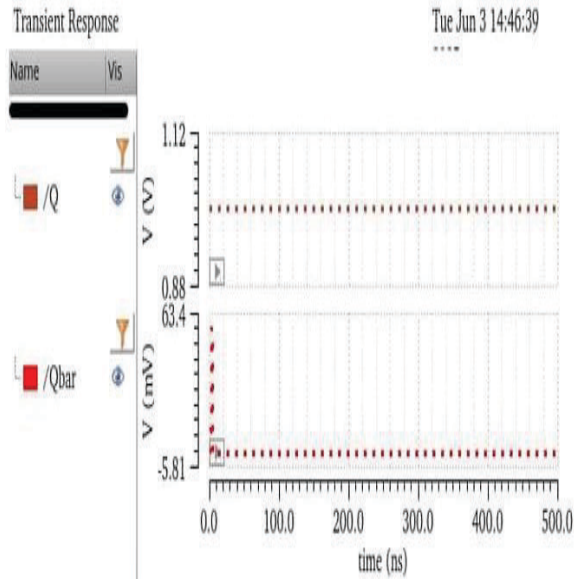


Fig.18- Transient Response of 7T SRAM

C. SIMULATIONS OF 8T

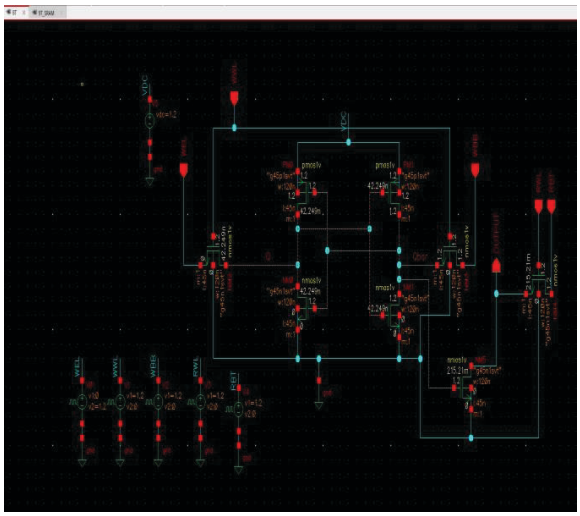


Fig.19- Schematic of 8T SRAM

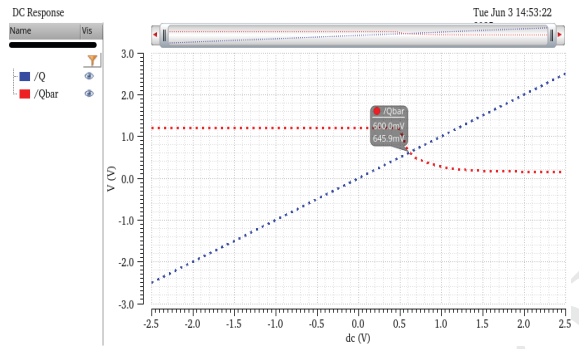


Fig.20- DC Response of 8T SRAM

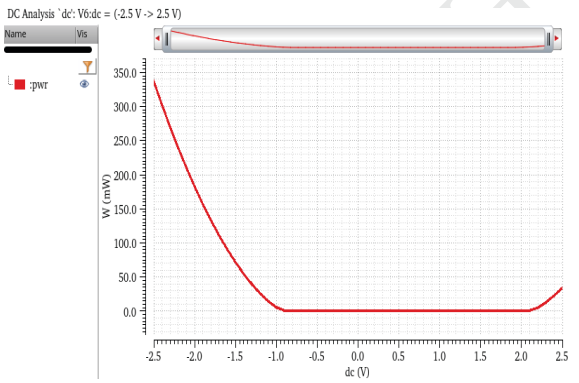


Fig.21- DC Analysis of 8T SRAM

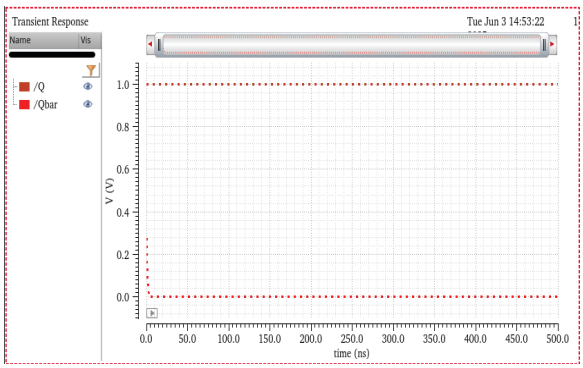


Fig.22- Transient Response of 8T SRAM

D. SIMULATIONS OF 9T

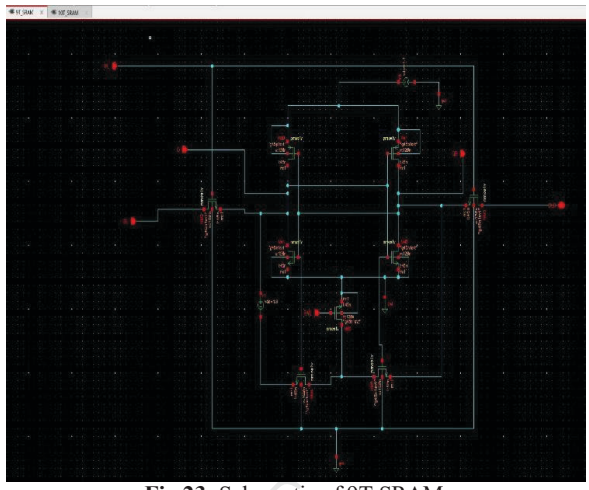


Fig.23- Schematic of 9T SRAM

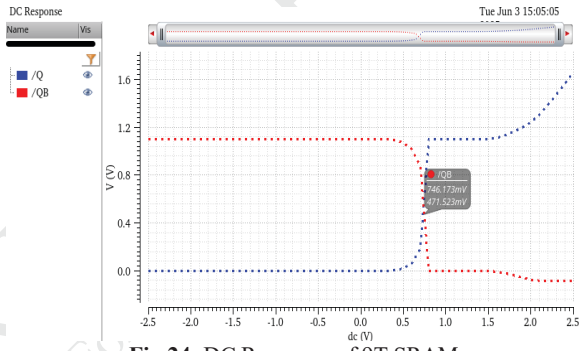


Fig.24- DC Response of 9T SRAM

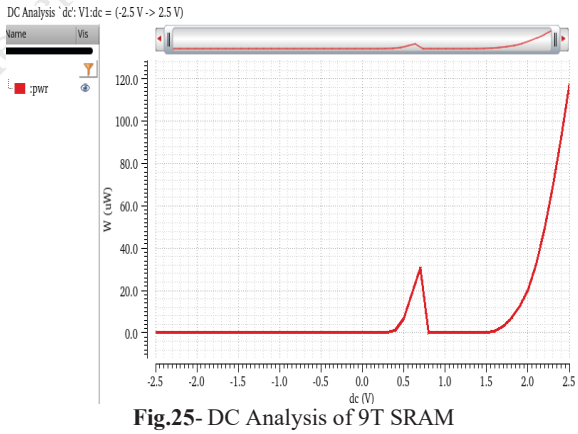


Fig.25- DC Analysis of 9T SRAM

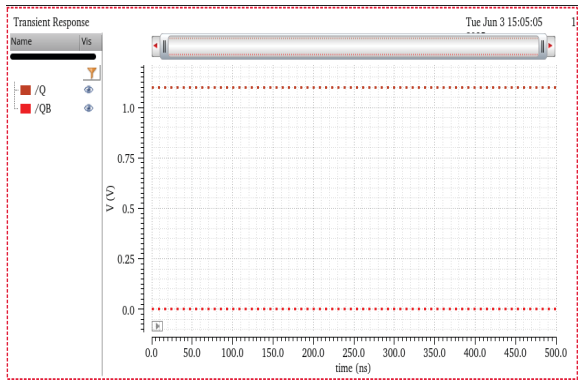


Fig.26- Transient Response of 9T SRAM

E. SIMULATIONS OF 10T

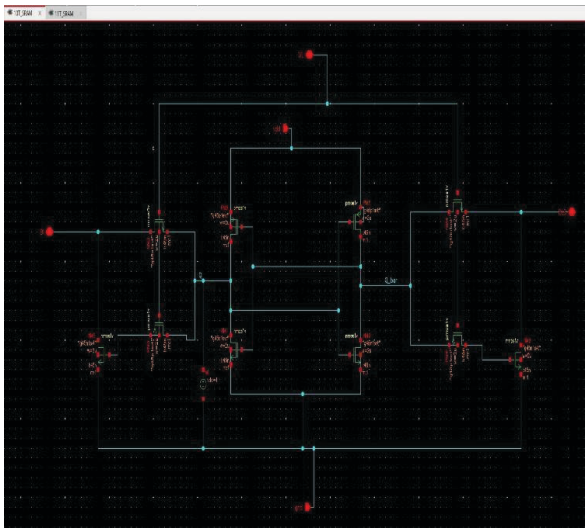


Fig.27- Schematic of 10T SRAM

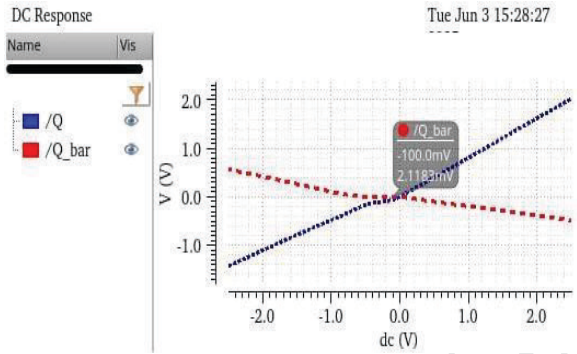


Fig.28- DC Response of 10T SRAM

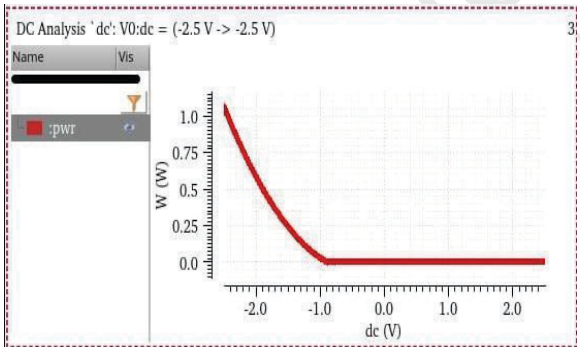


Fig.29- DC Analysis of 10T SRAM

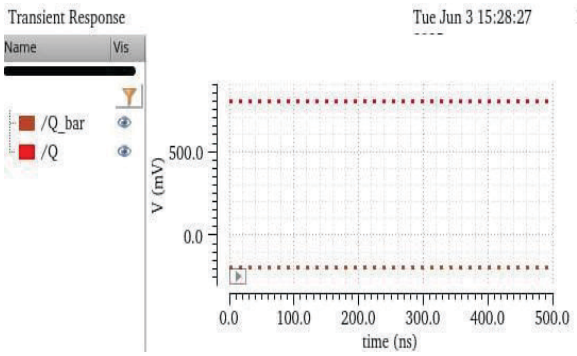


Fig.30- Transient Response of 10T SRAM

F. SIMULATIONS OF 11T

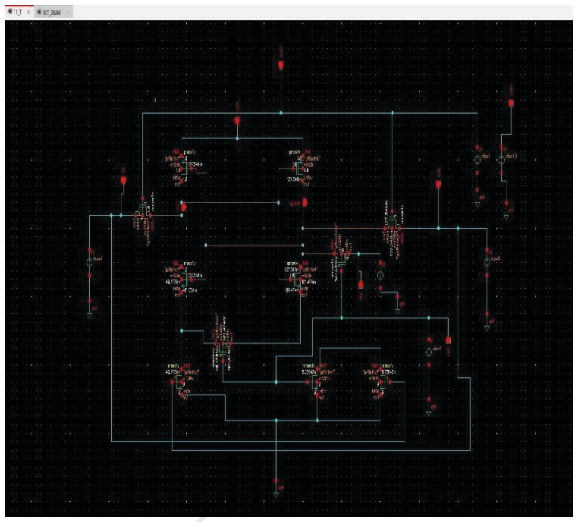


Fig.31- Schematic of 11T SRAM

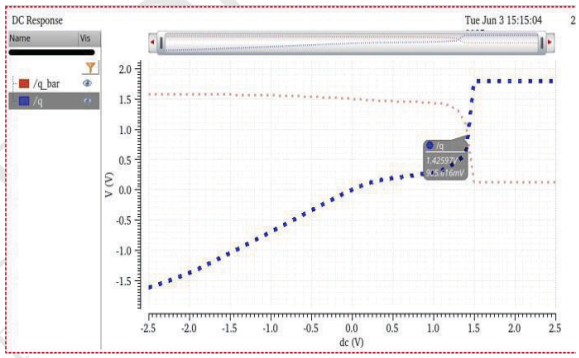


Fig.32- DC Response of 11T SRAM

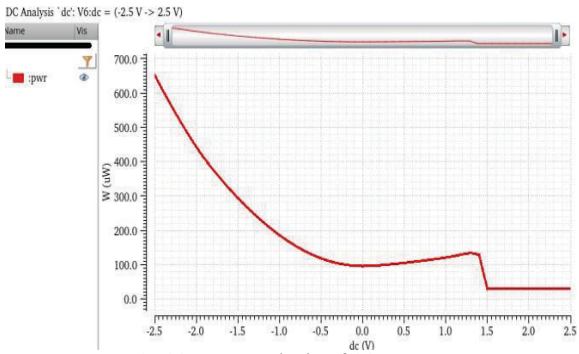


Fig.33- DC Analysis of 11T SRAM

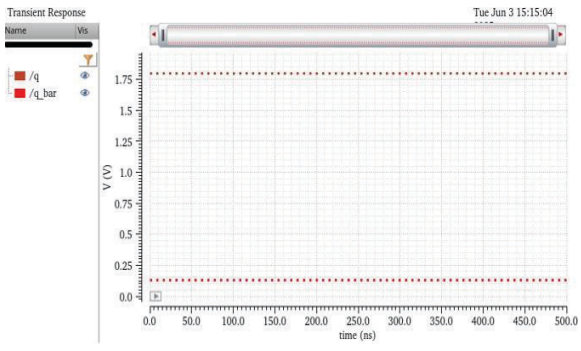


Fig.34- Transient Response of 11T SRAM

G. SIMULATIONS OF 12T

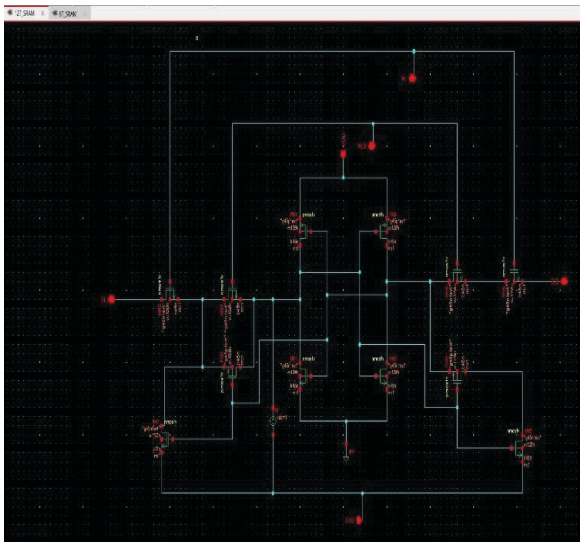


Fig.35- Schematic of 12T SRAM

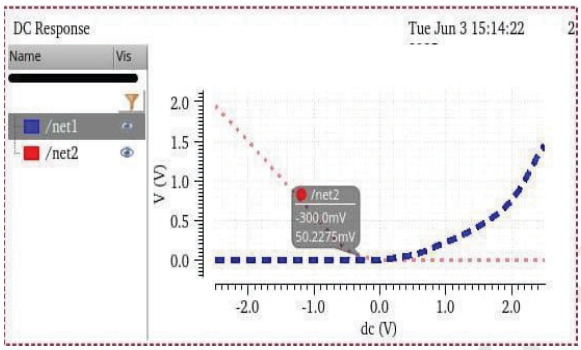


Fig.36- DC Response of 12T SRAM

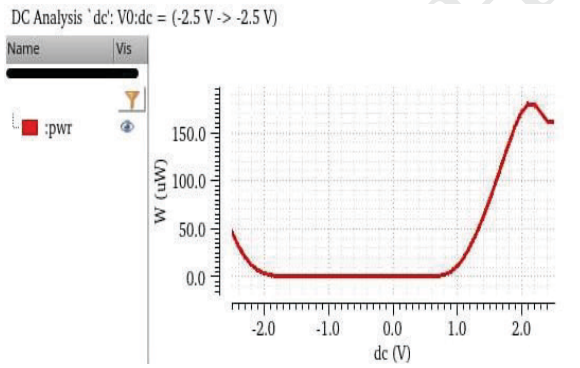


Fig.37- DC Analysis of 12T SRAM

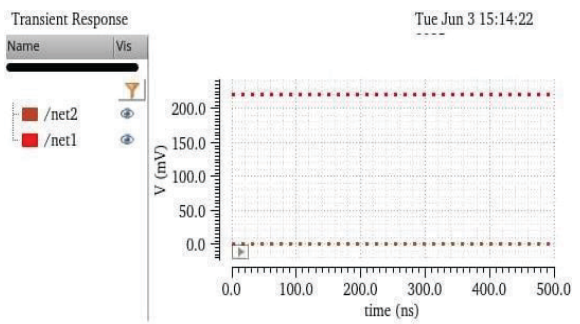


Fig.38- Transient Response of 12T SRAM

IV. RESULT

The simulation results show a clear reduction in leakage power as additional transistors and leakage reduction techniques are applied across the SRAM cell variants. The 6T cell recorded the highest leakage at 0.1224 nW, while the 12T cell, which uses both Sleep and Stack approaches, achieved the lowest at 0.0217 nW. Intermediate cells like 8T, 9T, and 10T showed gradual improvements. These results confirm that applying circuit-level techniques effectively minimizes leakage power, with the 12T cell offering the most efficient solution for low-power applications.

A. LEAKAGE POWER FOR SRAM MODELS

CIRCUIT (45 nm TECHNOLOGY)	TOTAL LEAKAGE CURRENT (pA)	TOTAL LEAKAGE POWER (nW)
6T SRAM CELL	122.381	0.1224
7T SRAM CELL	98.4162	0.0984
8T SRAM CELL	64.1978	0.0642
9T SRAM CELL	43.2304	0.0432
10T SRAM CELL	37.1985	0.0372
11T SRAM CELL	28.1743	0.0282
12T SRAM CELL	21.6712	0.0217

Table.1 Leakage power for SRAM models

B. COMPARATIVE ANALYSIS

SRAM MODELS	DECREASE IN LEAKAGE POWER
BASIC SRAM CELL (6T V/S 7T)	19.60%
BASIC SRAM CELLS WITH SLEEP AND STACKING APPROACH (7T V/S 8T)	34.76%
BASIC SRAM CELLS WITH SLEEP AND STACKING APPROACH (8T V/S 9T)	32.71
SRAM CELLS WITH SLEEP AND STACKING APPROACH (9T V/S 10T)	13.89%
SRAM CELLS WITH SLEEP AND STACKING APPROACH (10T V/S 11T)	24.19%
SRAM CELLS WITH BOTHSLEEP AND STACKING APPROACH (11T V/S 12T)	23.08%

Table.2 Comparative Analysis

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V. CONCLUSION

The study successfully demonstrates that leakage power in SRAM cells can be significantly reduced using circuit-level techniques such as Sleep and Stack & Sleep, particularly in 45nm CMOS technology where leakage dominates overall power consumption. Through simulation and analysis of various SRAM architectures ranging from 6T to 12T, it was observed that leakage power decreased consistently with the integration of additional transistors and isolation methods. Among all configurations, the 12T SRAM cell provided the most effective leakage reduction while maintaining stability and acceptable performance. These results highlight the importance of transistor-level modifications for achieving low-power, reliable memory designs suitable for energy-constrained applications such as embedded systems and IoT devices.

VI. Limitation and Future Scope

The implementation of leakage reduction techniques such as Sleep and Stack within SRAM cells has proven effective, but certain limitations must be acknowledged. The inclusion of extra transistors in higher-transistor-count cells like 10T, 11T, and 12T leads to increased silicon area, which may be a constraint in large memory arrays where density is critical. Additionally, the added resistance and capacitance from these transistors introduce slight delays in read/write operations. Another notable limitation is that the analysis was conducted only at the schematic level, without layout extraction or physical design validation. As a result, the practical performance, particularly in terms of speed and power under real-world conditions, may vary from the simulated results.

To address these limitations and further improve efficiency, future work can extend these leakage-reduction methods to smaller technology nodes such as 22nm, 14nm, or 7nm, where leakage issues are more severe. Enhancements such as integrating multi-threshold CMOS (MTCMOS), dynamic voltage scaling, or body biasing techniques could offer better control over leakage without significantly increasing area. Moreover, deploying these SRAM designs in full memory arrays would enable system-level validation and deeper analysis of trade-offs. Exploring emerging device technologies like FinFETs or Gate-All-Around FETs could also yield additional improvements in leakage performance. These future directions would contribute to the development of scalable and energy-efficient memory architectures suitable for next-generation low-power applications such as IoT, edge computing, and embedded systems.

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Implementation Of CRC Circuit Design For Error Detection And Correction

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***Abstract*—This project proposes a novel approach to mitigating Single Event Upsets (SEUs) in SRAM-based Field Programmable Gate Arrays (FPGAs) using a Cyclic Redundancy Check (CRC) based Error Checking and Correction (ECC) method. SRAM-based FPGAs are vulnerable to SEUs, which can lead to configuration errors and system failures. Traditional mitigation techniques like Triple Modular Redundancy (TMR) and zero-hardened SRAM cells present challenges such as increased resource consumption and limited error correction. In contrast, the proposed CRC-based solution offers a resource-efficient, real-time method for detecting and correcting configuration bit errors, improving data integrity in radiation-prone environments. The system integrates both encoding and decoding mechanisms, enabling error detection and correction with minimal overhead. The implementation utilizes a parallel processing architecture to enhance throughput, ensuring high-speed error detection suitable for critical applications in aerospace, healthcare, and telecommunications. The design features a modular IP core, offering scalability and low resource usage by dynamically calculating CRC values rather than relying on external ROM. A comparative analysis demonstrates the superiority of the proposed method over conventional approaches, highlighting its ability to correct up to 8-bit errors in 32-bit configurations while maintaining optimal performance and resource efficiency. Simulation results and synthesized reports further validate the system's effectiveness, making it a robust solution for SEU mitigation in modern FPGA-based systems.**

Keywords—Single Event Upsets, Cyclic Redundancy Check, Error Checking and Correction.

I. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) play a crucial role in modern digital systems due to their adaptability, high performance, and rapid development cycles. However, SRAM-based FPGAs are susceptible to Single Event Upsets (SEUs) caused by cosmic radiation, which can modify configuration bits and lead to potential system malfunctions. To mitigate SEUs, methods such as zero-hardened SRAM cells and Triple Modular Redundancy (TMR) have been developed, but these often come with drawbacks, including increased resource demands and limited error correction capabilities. This project proposes a groundbreaking approach to SEU mitigation using Error Checking and Correction (ECC) based on Cyclic Redundancy Check (CRC). The objective is to create an embedded IP core that automatically detects and corrects configuration bit errors, offering a more efficient and resource-conscious alternative to conventional techniques. By leveraging CRC-based encoding and decoding, this method effectively mitigates SEUs in SRAM-based FPGAs, enhancing their reliability in radiation-heavy environments. Key benefits include real-time error detection and correction to reduce disruptions, lower memory usage by storing CRC values instead of full configuration bitstreams, and scalability through a modular IP core design that can be integrated into diverse FPGA architectures. This innovative solution ensures dependable FPGA performance in critical sectors such as aerospace, healthcare, and telecommunications.

II. PROBLEM ANALYSIS AND SOLUTION

A. Problem Definition

Field Programmable Gate Arrays (FPGAs) are used in a variety of applications. However, the SRAM-based FPGAs can be easily influenced by single event upset (SEU) in the configuration memory. SEU could lead to a series of catastrophic consequences ranging from unwanted functional, data loss, or failure of the whole system. Therefore ensuring data integrity has become a critical concern.The objective is to develop CRC-Based Circuit Design for Configuration Bit Correction in SRAM-Based FPGAs and optimization of the same.

B. Proposed Solution

The primary objective of this project is to design a cyclic redundancy check (CRC) circuit for error detection and correction in SRAM-based FPGAs. This solution integrates encoding and decoding mechanisms to ensure data integrity while maintaining high performance and reliability.

The CRC encoder improves data integrity by appending redundant information to the original data, enabling the detection and correction of errors during transmission or processing. By embedding a verification code, it ensures that the data can be validated at the receiving end.

The CRC decoder verifies the integrity of received or retrieved data by identifying and correcting certain errors. It compares the received redundant information with expected results to detect inconsistencies, restoring the original data accurately. This process ensures that the output data remains precise and dependable.

The design adopts a parallel processing approach, allowing it to handle multiple data chunks simultaneously,

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thereby enhancing efficiency and throughput. The seamless integration of the encoder and decoder enables continuous data validation, making the design highly suitable for high-speed applications.

The method emphasizes implementing the CRC circuit on SRAM-based FPGAs, taking advantage of their flexibility and high performance. The solution is optimized for efficient resource utilization while delivering reliable error detection and correction. Its scalability and versatility make it ideal for various applications, including communication systems and data storage. By addressing the critical challenge of data reliability, this project provides a robust and efficient approach to error management in modern digital systems.

III. METHODOLOGY AND IMPLEMENTATION

A. Overview

The proposed solution uses a bottom-up design methodology, beginning with the development and validation of foundational components before integrating them into a comprehensive top-level system. The process starts with the creation of the CRC computation unit, a critical component responsible for performing cyclic redundancy checks using a specified generator polynomial. This unit calculates remainders for error detection and undergoes rigorous testing to ensure precision and reliability.

Building on this foundation, the encoder and decoder modules are developed. The encoder appends the calculated CRC value to input data, producing an error-detectable encoded output. After encoding all message bits, the decoder verifies data integrity by recalculating the CRC and comparing it to the appended value. Any inconsistencies are identified to detect and correct errors, preserving data accuracy. Each module is subjected to standalone testing to validate functionality before system integration.

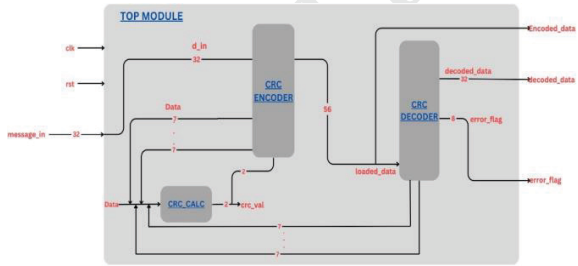


Figure 1. Block diagram

After validating individual components, they are combined into a parallel processing architecture to boost throughput. This framework allows multiple data streams to be processed concurrently, making the design highly efficient for large-scale applications. A control unit coordinates data flow and ensures synchronization across modules, enabling smooth operation. All components are then integrated into a top-level module, which acts as the primary interface for data input and output, completing the system design.

Figure 2. Flowchart of the system.

B. CRC Calculator

The CRC Calculator module is a critical component of the CRC system, tasked with executing the core computations required to generate the CRC value. It performs modulo-2 division on a 7-bit input message using a predefined generator polynomial, g(x) = x 3 + x + 1 (binary 1011). The module processes the input data through bitwise XOR operations, guided by the most significant bits, to complete the division steps and calculate the CRC remainder. The resulting output is a 3-bit CRC value, which is appended to the original input data to enable error detection.

C. CRC Encoder

The Encoder module (crc_encoder) is responsible for generating the encoded message by calculating and appending the CRC to the input data. It takes a 4-bit input data (d_in), processes it through the CRC calculator to compute the 3-bit CRC remainder, and then concatenates the 4-bit input with the 3-bit remainder, resulting in a 7-bit encoded output. This process is applied to each 4-bit segment of the input message in parallel, ensuring efficient encoding of the entire message.

D. CRC Decoder

The CRC Decoder is designed to ensure the integrity of received data by detecting and correcting transmission errors. It operates in a pipelined manner, processing the encoded data in multiple stages to achieve high efficiency. The decoder receives a 7-bit encoded message, which consists of the original data along with appended CRC bits, and performs a sequence of operations to verify its correctness.

Once the CRC is computed, the decoder compares the received CRC bits with the wrong pattern table. If the CRC value corresponds to zero , it confirms that the data is error-free. However, if there is a discrepancy, the decoder detects the error and tries to correct it by using the wrong pattern table.

Wrong pattern / Reminder	**Error bit position**
000	No error
011	0th bit
110	1st bit
111	2nd bit
101	3rd bit

PROOF

Table 1. Wrong pattern table

Parallelism and Pipelining in crc_decoder: The module is designed to leverage both parallelism and pipelining for optimal error detection and correction. The decoder processes the encoded data in parallel chunks, verifying multiple 7-bit chunks of encoded data simultaneously. Additionally, the pipelining structure within the decoder splits the process into three stages which ensures efficient handling of data and intermediate results.

IV. RESULTS AND DISCUSSIONS

A. Results

The implemented CRC circuit exhibited effective and dependable performance during testing and validation. It successfully detected multi-bit errors and corrected single-bit errors in real-time, ensuring robust data integrity. Software testing verified the circuit's capability to operate at high speeds while maintaining low resource utilization, making it ideal for high-throughput applications.

```
# Encoding Test 0:
# Input: 02468ace
# Encoded: 00593b18b4f174
# ------------------------------
# Encoding Test 1:
# Input: 02468ace
# Encoded: 00593b18b4f174
# ------------------------------
# Encoding Test 2:
# Input: 02468ace
# Encoded: 00593b18b4f174
# ------------------------------
# Decoding Test 0:
# Manually Encoded Input: 00593b18b4f174
# Decoded Output: 02468ace
# No error detected.
# ------------------------------
# Decoding Test 1:
# Manually Encoded Input: 00593b19b6f57c
# Decoded Output: 02468ace
# No error detected.
# ------------------------------
# Decoding Test 2:
# Manually Encoded Input: 10797b99b6fd6c
# Decoded Output: 02468a75
# Error detected. Error flag: 00000011
# ------------------------------
# ** Note: $finish    : E:/Study Materials/5th
#    Time: 545 ps  Iteration: 0  Instance: /top
# 1
```

Figure 3. Simulation output showing error correction

Furthermore, compared to conventional error correction methods, the solution demonstrated enhanced error correction efficiency with reduced overhead, highlighting its practicality and scalability for contemporary FPGA-based systems.

B. Analysis of synthesized report

The CRC Encoder module demonstrates a highly efficient design with a significant timing slack of 8599 ps, indicating ample scope for further area or power optimization. It consumes minimal power, totaling 15.76 µW, with the majority of the power usage attributed to register-related activity. Additionally, the module has a lightweight area footprint, making it ideal for integration into larger systems or resource-constrained applications. Overall, this design strikes an excellent balance between simplicity and performance, making it well-suited for low-power, high-speed environments.

The CRC decoder module comfortably meets timing requirements, with a significant slack of approximately 4766 ps, indicating ample room for potential optimizations in either area or power. The total power consumption of the module is 464.12 µW, with the majority being drawn by registers, while logic and the clock network contribute only a small fraction. This balanced power distribution highlights efficient design practices. Additionally, the module comprises 390 cells, reflecting moderate complexity, making it well-suited for applications such as embedded systems.

V. CONCLUSION

In summary, this project introduces an efficient approach to ensuring data integrity by systematically dividing a word into eight groups of four bits each. Utilizing Cyclic Redundancy Check (CRC) with the polynomial divisor 1011, the method provides reliable error detection during encoding. The decoding process is performed with precision to verify data accuracy, enhancing error detection and correction capabilities. The results demonstrate that the proposed approach can effectively manage and correct up to eight bits in a word, highlighting the system's reliability and efficiency. This work represents a significant contribution to error correction in digital communications, reinforcing its value in maintaining data integrity.

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TECHNO TRAM-A SELF DRIVING CAR

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Abstract : **This project develops a cost-effective self-driving car prototype with *line-following* and *object detection* capabilities. An *Arduino Uno* microcontroller coordinates *IR sensors* for path detection and *ultrasonic sensors* for obstacle avoidance. The *LN298 motor driver* controls movement, enabling autonomous navigation.**

The system integrates *hardware and Arduino IDE-based software*, ensuring effective trajectory tracking and collision prevention. Tested in controlled environments, it demonstrates essential autonomous vehicle functionalities. With a *modular and low-cost design*, it allows future enhancements like GPS integration and advanced navigation algorithms, contributing to scalable robotics applications.

A. List of abbreviations

- GPS- Global Positioning System
- DC- Direct Current
- IR Sensors- Infrared Sensors
- SPI- SerialPeripheral Interface
- USB- Universal Serial Bus
- SRAM -Static Random Access Memory
- EEPROM- Electrically Erasable Programmable Read-Only Memory
- PWM -Pulse Width Modulation
- RPM- Rotations per Minute Units

I. INTRODUCTION

Road congestion, accidents, and delays caused by human errors such as fatigue and reckless driving are major global challenges. According to the World Health Organization, car accidents result in over one million fatalities annually. This paper explores autonomous vehicle technology as a solution to improve road safety by minimizing human intervention.

The project focuses on developing a low-cost, Arduino-based self-driving car with lane detection, obstacle avoidance, and traffic sign recognition. Using IR sensors, ultrasonic sensors, and CNN-based image processing, the system ensures accurate navigation and real-time decision-making. Unlike expensive sensor technologies, vision-based methods offer a cost-effective alternative for lane-keeping and autonomous control.

Additionally, an Arduino Uno-based smart car control system is implemented with ultrasonic sensors for obstacle detection and an LM35 sensor for engine temperature monitoring, preventing accidents due to overheating. Another Bluetooth-controlled robot car integrates voice commands and mobile app control using HC-05, demonstrating applications in home automation, security, and education.

Further, the study explores GPS-integrated steering control for stability on curved roads and mecanum wheel robots for omnidirectional movement, useful in military, search and rescue, and space exploration. By leveraging Arduino, Raspberry Pi, Bluetooth modules, and vision-based methods, this research highlights affordable, scalable solutions for autonomous systems, contributing to safety, efficiency, and innovation in robotics.

The remainder of this paper is organized as follows. Section II examines the most important associated works. Methodology for lane detection and obstacle detection is included in Section III. Section IV sums up the results and

analysis of the experiments. Section V wraps up the research.

II. LITERATURE SURVEY

The study "Android Application-Based Monitoring and Controlling of a Remotely Controlled Robotic Car" highlights real-time monitoring and smartphone control via Bluetooth. Similarly, an Arduino-based robotic vehicle operates in manual, automatic, and voice-controlled modes, enhancing usability with voice control and obstacle detection using ultrasonic sensors [1].

Voice-controlled automation leverages natural language processing (NLP), allowing users to issue verbal commands for robotic systems. Integrating ESP32-CAM enables real-time video monitoring, improving applications such as remote surveillance and obstacle detection. Bluetooth modules like HC-05 facilitate communication over short distances, though they are limited in range [2].

Low-cost autonomous cars using Arduino have gained attention due to advancements in AI and robotics. Key components include ultrasonic/infrared sensors for navigation**,** DC/servo motors for movement, and wireless modules for remote control. Machine learning techniques improve line-following and obstacle avoidance algorithms, despite challenges such as sensor limitations and environmental variability [3].

Arduino-controlled Mecanum wheel robots provide omnidirectional movement, useful for industrial handling, search and rescue, and educational robotics. Research explores kinematic models, PID controllers, and sensor integration**,** addressing challenges in real-time control and stability [4].

Ultrasonic and infrared sensors play a crucial role in advanced driver-assistance systems (ADAS**)**, enabling obstacle detection, lane-keeping, and adaptive cruise control. Sensor fusion enhances environmental perception, supporting safer navigation [5].

Autonomous vehicle operation relies **on** lane-keeping assist (LKA) strategies like PID control and Pure Pursuit control. While PID control offers real-time lane stability**,** Pure Pursuit provides smoother path-following, especially on curves. Hybrid strategies combining both approaches improve adaptive lane-keeping [6].

The integration of smart car control systems using Arduino Uno enhances obstacle avoidance and engine temperature control. Ultrasonic and infrared sensors detect obstacles, while temperature sensors like LM35 prevent overheating. Bluetooth and Wi-Fi modules enable remote monitoring via mobile applications, increasing vehicle safety and efficiency [7].

As AI and sensor technologies evolve, autonomous systems are expected to become smarter, safer, and more efficient, paving the way for future advancements in robotics and automation [8].

III. METHODOLOGY & IMPLEMENTATION

The development of a self-driving car involves defining project goals, selecting components, designing circuits, writing code, assembling hardware, and testing functionality. The primary objectives include line following using IR sensors**,** obstacle avoidance with an ultrasonic sensor, and navigation with motor control. The control and testing methods must be identified early to ensure smooth operation.

Understanding the components is crucial. The Arduino UNO R3 acts as the microcontroller, processing inputs from IR sensors for line detection and an ultrasonic sensor for obstacle avoidance. A servo motor adjusts direction, while DC motors, controlled via the L298N motor driver, provide propulsion. A Li-ion battery powers all components. Proper interfacing of these elements ensures efficient performance.

Circuit design requires mapping wiring connections, ensuring sensors connect to digital pins, and motors to PWM pins, while maintaining voltage compatibility. The algorithm follows a structured approach**:** initializing sensors, detecting lines, avoiding obstacles, adjusting the servo for scanning, and controlling motors based on sensor feedback. Translating this into pseudocode ensures logical execution.

Coding in the Arduino IDE involves importing necessary libraries, writing functions for sensor readings and motor control, and testing via simulation. The hardware assembly involves securing all components to the chassis, ensuring stable wiring, and establishing proper power connections. Each function of IR sensors, ultrasonic sensor, and motor control are independently tested before integrating and debugging issues like sensor noise or motor glitches.

Optimization includes fine-tuning speed, turning angles, and sensitivity while refining the code for smoother operation. The final step involves demonstrating the robot, evaluating performance, and documenting improvements for future advancements. This streamlined approach ensures an efficient, self-driving robotic system.

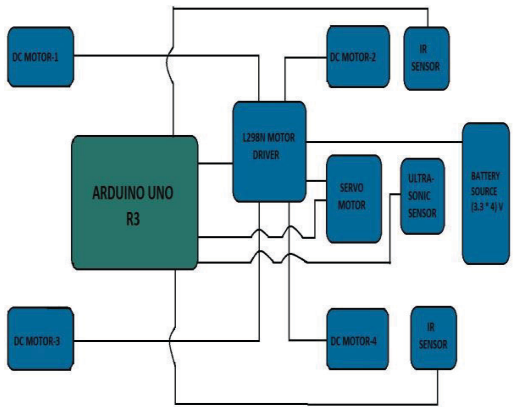


Fig 1: Block diagram

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A. ALGORITHM / FLOW CHART

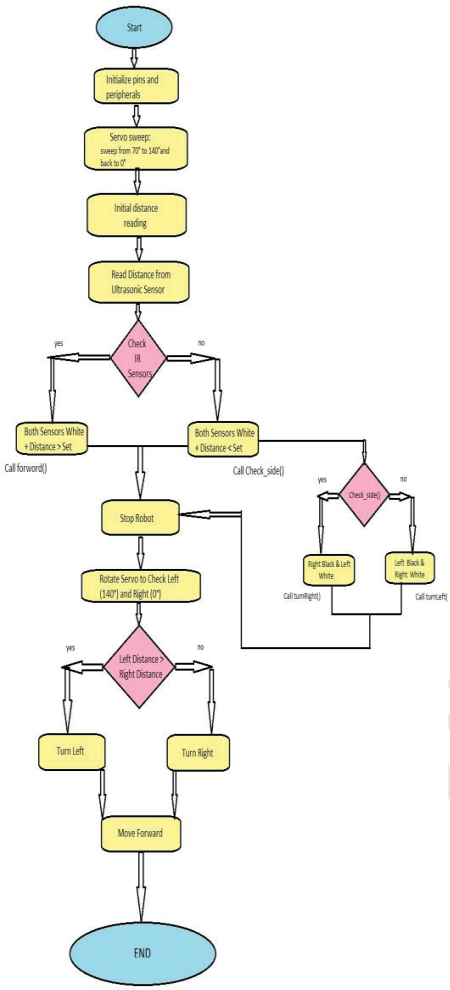


Fig 2: Flowchart of Algorithm

The flowchart outlines the logic for a self-driving robotic vehicle that uses sensors (IR and ultrasonic) to navigate its environment while avoiding obstacles and following a line. Here's an explanation of each step:

• Start & Initialize Components Action: The system powers on, initializes all components, and configures the Arduino Uno R3 and sensors (IR and ultrasonic). Purpose: Ensures all devices are ready for operation.

• Read IR Sensors Action: The robot reads data from its infrared (IR) sensors. Purpose: Detects whether the robot is on a predefined line (e.g., a black line on a white surface) or off the line.

• Is Line Detected? Decision: Checks the IR sensor readings to determine if the robot is aligned with the line. Yes: If the line is detected, proceed to adjust the motors for line following. No: If no line is detected, stop or realign to find the line.

• Adjust Motor (Follow Line) Action: The motors are controlled (via the L298N driver) to keep the robot aligned with the line. Purpose: Maintains the robot's position along the desired path.

• Stop or Realign to Line Action: If the line is lost, the robot halts or adjusts its position to find and align with the line again. Purpose: Prevents the robot from going off-track.

• Read Ultrasonic Sensor Action: The robot reads data from its ultrasonic sensor to detect obstacles in its path. Purpose: Identifies whether there are objects blocking the robot's movement.

• Is Obstacle Detected? Decision: Based on the ultrasonic sensor data: Yes: If an obstacle is detected, the robot stops and evaluates the situation. No: If no obstacle is detected, the robot moves forward.

• Stop and Scan (Adjust Servo) Action: The servo motor adjusts the ultrasonic sensor's angle to scan the surroundings. Purpose: Determines the best path (left or right) to avoid the obstacle.

• Recalculate Path (Turn Left or Right) Action: The robot recalculates its path and turns in the direction with no obstacles. Purpose: Enables safe navigation around obstacles.

• Move Forward Action: The robot resumes forward movement after recalculating its path. Purpose: Continues following the line or navigating the environment.

• Control Motors (Using L298N) Action: The L298N motor driver adjusts motor speeds or directions based on input commands. Purpose: Facilitates precise control of the robot's motion.

• Repeat Process Action: The process loops back to the beginning, continuously reading sensor data and making decisions. Purpose: Ensures the robot adapts dynamically to changes in the environment.

• End/Stop Action: The process terminates if a stop condition is met (e.g., manual intervention or task completion). Purpose: Ends the robot's operation safely.

IV. RESULTS AND DISCUSSIONS

A. RESULTS

- Basic Autonomous Navigation: The vehicle can follow the lane and avoid obstacles in a controlled environment, such as a simple track or straight path with clear lane markings.

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- Performance in Real-world Conditions: This setup works reasonably well in structured, simple scenarios but struggles with complex environments like intersections, sharp curves, or unmarked roads.
- Challenges: Limited Sensor Range and Precision: The IR sensors are only effective for short-range detection, and ultrasonic sensors have difficulty detecting smaller or irregularly shaped objects.
- Sensor Noise: Both ultrasonic and IR sensors can be affected by environmental noise, such as temperature or surface texture, which can lead to false readings.
- Control Logic: Simple PID control for lane-following and decision-making logic for obstacle avoidance might not be enough for handling unpredictable real-world conditions like pedestrians or moving vehicles.

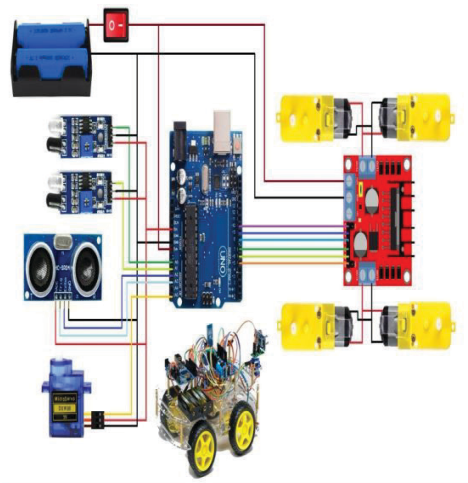


Fig 3: Circuit Diagram

B. DISCUSSIONS

Scalability: The Arduino-based self-driving car is an excellent starting point for building and experimenting with autonomous vehicles. However, the system's scalability is limited by the processing power of the Arduino and the simplicity of the sensors used.

Sensor Fusion: Using just ultrasonic and IR sensors limits the car's ability to detect objects in all directions or in more complex scenarios. Combining additional sensors such as cameras or even basic computer vision (using a Raspberry Pi or another more powerful microcontroller), could improve performance.

Cost and Accessibility: The major advantage of this system is its low cost and ease of use for beginners. Ultrasonic and IR sensors are inexpensive and easy to implement, making this a great project for hobbyists and learners.

Real-world Application: While effective in simple, controlled environments, this system is unlikely to be suitable for real-world autonomous vehicles. More advanced systems typically use a combination of cameras, LiDAR, and machine learning to navigate and detect objects with greater accuracy.

V. CONCLUSION

This Arduino-based vehicle serves as a prime example of how diverse functionalities like line following, obstacle detection, and obstacle avoidance can be seamlessly integrated into a single robotic system. Utilizing versatile sensors, such as infrared sensors for line tracking and ultrasonic sensors for distance measurement, the vehicle demonstrates the power of sensor fusion in achieving autonomous behavior.

The algorithms implemented in the system allow the vehicle to analyze its surroundings, make decisions in real time, and execute precise movements. For instance, the line-following algorithm ensures the robot stays on track, while the obstacle detection and avoidance system enables it to navigate around obstacles without losing its path. This highlights the importance of adaptive behavior in autonomous systems, which is essential for operating in dynamic and unpredictable environments.

Precise motor control, powered by the L298N motor driver, plays a pivotal role in executing the planned movements, from smooth turns to accurate stops. The integration of servo motors for directional scanning further enhances the vehicle's ability to assess its environment, enabling robust obstacle avoidance strategies.

This project lays a foundation for a wide range of robotic applications across various domains, including industrial automation, logistics, smart transportation, and education. It underscores the critical aspects of robotics development, such as sensor integration for reliable data acquisition, algorithm design for decision-making, and effective hardware software coordination for seamless operation.

Overall, this system illustrates how relatively simple components, when combined thoughtfully, can produce sophisticated and autonomous robotic behavior, paving the way for innovation in robotics and intelligent systems.

VI. FUTURE TRENDS

The future trends for self-driving Arduino cars align with the broader advancements in autonomous vehicle technology. These trends reflect innovations in hardware, software, and integration that make autonomous systems more intelligent, efficient, and adaptable. Below are some key areas where future trends are expected:

1. Enhanced Sensor Integration : High-Precision Sensors: Incorporation of affordable LiDAR, ultrasonic sensors, and camera systems for precise object detection and mapping. Sensor Fusion: Combining data from multiple sensors (e.g., GPS, gyroscopes, infrared) to improve environmental awareness and decision-making.

2. AI and Machine Learning : Advanced Algorithms: Implementation of deep learning models for image recognition, path planning, and obstacle avoidance. Edge Computing: Running AI models directly on Arduino-compatible microcontrollers or low-power chips like ESP32, reducing latency. Reinforcement Learning: Teaching the car to adapt to changing environments through trial and error.

3. Swarm Intelligence: Development of systems allowing multiple Arduino cars to communicate and collaborate, enabling swarm-like behaviors for traffic management and cooperative tasks.

4. Improved Power Management :Energy-efficient components and smarter algorithms for battery optimization, enabling longer operational periods on a single charge.

5. Affordable and Scalable Prototypes :Transition from single-use prototypes to modular systems, allowing for easy upgrades and customizations. Open-Source Frameworks: Growth of open-source projects to facilitate community-driven innovation.

6. Advanced Communication Systems : Integration of Vehicle-to-Everything (V2X) communication for real-time updates and coordination with other vehicles, traffic systems, and infrastructure.

7. Mapping and Localization :Use of SLAM (Simultaneous Localization and Mapping) techniques for realtime map creation and navigation. Combining GPS with local positioning systems for accurate localization in GPS-denied environments.

8. Cloud and IoT Integration : Cloud-based systems for processing complex data off-device and updating algorithms remotely. Real-time monitoring and control through IoT platforms.

9. Safety Enhancements : Development of failsafe mechanisms to handle system failures or emergencies. Use of predictive analytics to avoid collisions or risky scenarios.

10. Applications in Real-World Use Cases :Education: Continued use in learning environments to teach programming, electronics, and robotics. Robotic Delivery Systems: Deployment of Arduino-powered autonomous cars for small-scale delivery in controlled environments.

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Implementation Of CRC Circuit Design For Error Detection And Correction

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***Abstract*—This project proposes a novel approach to mitigating Single Event Upsets (SEUs) in SRAM-based Field Programmable Gate Arrays (FPGAs) using a Cyclic Redundancy Check (CRC) based Error Checking and Correction (ECC) method. SRAM-based FPGAs are vulnerable to SEUs, which can lead to configuration errors and system failures. Traditional mitigation techniques like Triple Modular Redundancy (TMR) and zero-hardened SRAM cells present challenges such as increased resource consumption and limited error correction. In contrast, the proposed CRC-based solution offers a resource-efficient, real-time method for detecting and correcting configuration bit errors, improving data integrity in radiation-prone environments. The system integrates both encoding and decoding mechanisms, enabling error detection and correction with minimal overhead. The implementation utilizes a parallel processing architecture to enhance throughput, ensuring high-speed error detection suitable for critical applications in aerospace, healthcare, and telecommunications. The design features a modular IP core, offering scalability and low resource usage by dynamically calculating CRC values rather than relying on external ROM. A comparative analysis demonstrates the superiority of the proposed method over conventional approaches, highlighting its ability to correct up to 8-bit errors in 32-bit configurations while maintaining optimal performance and resource efficiency. Simulation results and synthesized reports further validate the system's effectiveness, making it a robust solution for SEU mitigation in modern FPGA-based systems.**

Keywords—Single Event Upsets, Cyclic Redundancy Check, Error Checking and Correction.

I. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) play a crucial role in modern digital systems due to their adaptability, high performance, and rapid development cycles. However, SRAM-based FPGAs are susceptible to Single Event Upsets (SEUs) caused by cosmic radiation, which can modify configuration bits and lead to potential system malfunctions. To mitigate SEUs, methods such as zero-hardened SRAM cells and Triple Modular Redundancy (TMR) have been developed, but these often come with drawbacks, including increased resource demands and limited error correction capabilities. This project proposes a groundbreaking approach to SEU mitigation using Error Checking and Correction (ECC) based on Cyclic Redundancy Check (CRC). The objective is to create an embedded IP core that automatically detects and corrects configuration bit errors, offering a more efficient and resource-conscious alternative to conventional techniques. By leveraging CRC-based encoding and decoding, this method effectively mitigates SEUs in SRAM-based FPGAs, enhancing their reliability in radiation-heavy environments. Key benefits include real-time error detection and correction to reduce disruptions, lower memory usage by storing CRC values instead of full configuration bitstreams, and scalability through a modular IP core design that can be integrated into diverse FPGA architectures. This innovative solution ensures dependable FPGA performance in critical sectors such as aerospace, healthcare, and telecommunications.

II. PROBLEM ANALYSIS AND SOLUTION

A. Problem Definition

Field Programmable Gate Arrays (FPGAs) are used in a variety of applications. However, the SRAM-based FPGAs can be easily influenced by single event upset (SEU) in the configuration memory. SEU could lead to a series of catastrophic consequences ranging from unwanted functional, data loss, or failure of the whole system. Therefore ensuring data integrity has become a critical concern.The objective is to develop CRC-Based Circuit Design for Configuration Bit Correction in SRAM-Based FPGAs and optimization of the same.

B. Proposed Solution

The primary objective of this project is to design a cyclic redundancy check (CRC) circuit for error detection and correction in SRAM-based FPGAs. This solution integrates encoding and decoding mechanisms to ensure data integrity while maintaining high performance and reliability.

The CRC encoder improves data integrity by appending redundant information to the original data, enabling the detection and correction of errors during transmission or processing. By embedding a verification code, it ensures that the data can be validated at the receiving end.

The CRC decoder verifies the integrity of received or retrieved data by identifying and correcting certain errors. It compares the received redundant information with expected results to detect inconsistencies, restoring the original data accurately. This process ensures that the output data remains precise and dependable.

The design adopts a parallel processing approach, allowing it to handle multiple data chunks simultaneously,

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thereby enhancing efficiency and throughput. The seamless integration of the encoder and decoder enables continuous data validation, making the design highly suitable for high-speed applications.

The method emphasizes implementing the CRC circuit on SRAM-based FPGAs, taking advantage of their flexibility and high performance. The solution is optimized for efficient resource utilization while delivering reliable error detection and correction. Its scalability and versatility make it ideal for various applications, including communication systems and data storage. By addressing the critical challenge of data reliability, this project provides a robust and efficient approach to error management in modern digital systems.

III. METHODOLOGY AND IMPLEMENTATION

A. Overview

The proposed solution uses a bottom-up design methodology, beginning with the development and validation of foundational components before integrating them into a comprehensive top-level system. The process starts with the creation of the CRC computation unit, a critical component responsible for performing cyclic redundancy checks using a specified generator polynomial. This unit calculates remainders for error detection and undergoes rigorous testing to ensure precision and reliability.

Building on this foundation, the encoder and decoder modules are developed. The encoder appends the calculated CRC value to input data, producing an error-detectable encoded output. After encoding all message bits, the decoder verifies data integrity by recalculating the CRC and comparing it to the appended value. Any inconsistencies are identified to detect and correct errors, preserving data accuracy. Each module is subjected to standalone testing to validate functionality before system integration.

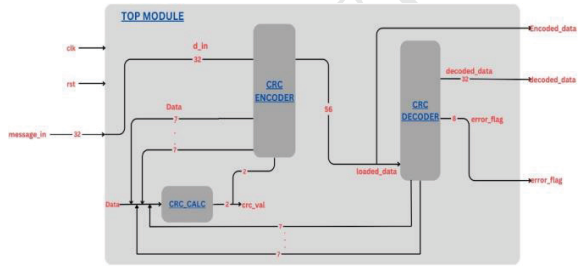


Figure 1. Block diagram

After validating individual components, they are combined into a parallel processing architecture to boost throughput. This framework allows multiple data streams to be processed concurrently, making the design highly efficient for large-scale applications. A control unit coordinates data flow and ensures synchronization across modules, enabling smooth operation. All components are then integrated into a top-level module, which acts as the primary interface for data input and output, completing the system design.

Figure 2. Flowchart of the system.

B. CRC Calculator

The CRC Calculator module is a critical component of the CRC system, tasked with executing the core computations required to generate the CRC value. It performs modulo-2 division on a 7-bit input message using a predefined generator polynomial, g(x) = x 3 + x + 1 (binary 1011). The module processes the input data through bitwise XOR operations, guided by the most significant bits, to complete the division steps and calculate the CRC remainder. The resulting output is a 3-bit CRC value, which is appended to the original input data to enable error detection.

C. CRC Encoder

The Encoder module (crc_encoder) is responsible for generating the encoded message by calculating and appending the CRC to the input data. It takes a 4-bit input data (d_in), processes it through the CRC calculator to compute the 3-bit CRC remainder, and then concatenates the 4-bit input with the 3-bit remainder, resulting in a 7-bit encoded output. This process is applied to each 4-bit segment of the input message in parallel, ensuring efficient encoding of the entire message.

D. CRC Decoder

The CRC Decoder is designed to ensure the integrity of received data by detecting and correcting transmission errors. It operates in a pipelined manner, processing the encoded data in multiple stages to achieve high efficiency. The decoder receives a 7-bit encoded message, which consists of the original data along with appended CRC bits, and performs a sequence of operations to verify its correctness.

Once the CRC is computed, the decoder compares the received CRC bits with the wrong pattern table. If the CRC value corresponds to zero , it confirms that the data is error-free. However, if there is a discrepancy, the decoder detects the error and tries to correct it by using the wrong pattern table.

Wrong pattern / Reminder	**Error bit position**
000	No error
011	0th bit
110	1st bit
111	2nd bit
101	3rd bit

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Table 1. Wrong pattern table

Parallelism and Pipelining in crc_decoder: The module is designed to leverage both parallelism and pipelining for optimal error detection and correction. The decoder processes the encoded data in parallel chunks, verifying multiple 7-bit chunks of encoded data simultaneously. Additionally, the pipelining structure within the decoder splits the process into three stages which ensures efficient handling of data and intermediate results.

IV. RESULTS AND DISCUSSIONS

A. Results

The implemented CRC circuit exhibited effective and dependable performance during testing and validation. It successfully detected multi-bit errors and corrected single-bit errors in real-time, ensuring robust data integrity. Software testing verified the circuit's capability to operate at high speeds while maintaining low resource utilization, making it ideal for high-throughput applications.

```
# Encoding Test 0:
# Input: 02468ace
# Encoded: 00593b18b4f174
# ------------------------------
# Encoding Test 1:
# Input: 02468ace
# Encoded: 00593b18b4f174
# ------------------------------
# Encoding Test 2:
# Input: 02468ace
# Encoded: 00593b18b4f174
# ------------------------------
# Decoding Test 0:
# Manually Encoded Input: 00593b18b4f174
# Decoded Output: 02468ace
# No error detected.
# ------------------------------
# Decoding Test 1:
# Manually Encoded Input: 00593b19b6f57c
# Decoded Output: 02468ace
# No error detected.
# ------------------------------
# Decoding Test 2:
# Manually Encoded Input: 10797b99b6fd6c
# Decoded Output: 02468a75
# Error detected. Error flag: 00000011
# ------------------------------
# ** Note: $finish    : E:/Study Materials/5th
#    Time: 545 ps  Iteration: 0  Instance: /top
# 1
```

Figure 3. Simulation output showing error correction

Furthermore, compared to conventional error correction methods, the solution demonstrated enhanced error correction efficiency with reduced overhead, highlighting its practicality and scalability for contemporary FPGA-based systems.

B. Analysis of synthesized report

The CRC Encoder module demonstrates a highly efficient design with a significant timing slack of 8599 ps, indicating ample scope for further area or power optimization. It consumes minimal power, totaling 15.76 µW, with the majority of the power usage attributed to register-related activity. Additionally, the module has a lightweight area footprint, making it ideal for integration into larger systems or resource-constrained applications. Overall, this design strikes an excellent balance between simplicity and performance, making it well-suited for low-power, high-speed environments.

The CRC decoder module comfortably meets timing requirements, with a significant slack of approximately 4766 ps, indicating ample room for potential optimizations in either area or power. The total power consumption of the module is 464.12 µW, with the majority being drawn by registers, while logic and the clock network contribute only a small fraction. This balanced power distribution highlights efficient design practices. Additionally, the module comprises 390 cells, reflecting moderate complexity, making it well-suited for applications such as embedded systems.

V. CONCLUSION

In summary, this project introduces an efficient approach to ensuring data integrity by systematically dividing a word into eight groups of four bits each. Utilizing Cyclic Redundancy Check (CRC) with the polynomial divisor 1011, the method provides reliable error detection during encoding. The decoding process is performed with precision to verify data accuracy, enhancing error detection and correction capabilities. The results demonstrate that the proposed approach can effectively manage and correct up to eight bits in a word, highlighting the system's reliability and efficiency. This work represents a significant contribution to error correction in digital communications, reinforcing its value in maintaining data integrity.

ACKNOWLEDGMENT

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A number of personalities, in their own capacities have helped us in carrying out this Mini Project. We would like to take this opportunity to thank them all. Last but not the least, we thank our friends and family for their encouragement and help in accomplishing the objective of the Mini Project work.

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Securing AES-128: Countermeasures for Side Channel Attacks

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Abstract*— This paper presents the design and implementation of robust hardware-level countermeasures for securing AES-128 encryption cores against side-channel attacks (SCAs), particularly targeting resource-constrained cryptographic environments such as IoT and embedded systems. Standard AES-128 architectures are known to exhibit significant vulnerability to Differential Power Analysis (DPA) due to power and electromagnetic (EM) leakage. To address this, a composite countermeasure framework is proposed, combining Redundancy AES Masking Basis for Attack Mitigation (RAMBAM) masking, Physically Unclonable Function (PUF)-based key generation, and instruction shuffling techniques. This integrated approach effectively conceals sensitive intermediate computations, eliminates static key storage, and randomizes execution order, thereby increasing resistance to statistical attacks. Experimental results demonstrate a substantial reduction in side-channel leakage and successful resistance to key recovery through correlation-based DPA attacks. The protected AES-128 core achieves enhanced security without compromising performance, offering a practical solution for secure encryption in lightweight hardware platforms.

***Keywords*—AES-128, side-channel attack, DPA, PUF, RAMBAM, masking, shuffling, hardware security, IoT encryption, FPGA.**

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I. INTRODUCTION

In the modern era of digital security, cryptographic devices play a crucial role in safeguarding sensitive information from unauthorized access and cyber threats. However, resource-constrained cryptographic devices—such as those used in embedded systems and Internet of Things (IoT) applications—face significant security challenges due to their limited computational and power capabilities. These constraints render traditional cryptographic algorithms vulnerable to side-channel attacks, which exploit physical leakages such as power consumption and electromagnetic emissions to extract confidential data [1], [4].

To address these vulnerabilities, the implementation of countermeasures is essential to enhance security while maintaining optimal performance in constrained environments. This project addresses the critical need for a security solution to defend cryptographic devices against side-channel attacks. By developing an optimized framework that enhances protection without overwhelming system resources, the proposed solution aims to strike a balance between security and efficiency.

This approach integrates three key countermeasures: RAMBAM (Redundancy AES Masking Basis for Attack Mitigation) [7], PUF-based key generation [6], and shuffled execution order [1]. It is particularly suited for low-power environments like IoT devices, ensuring they can operate securely without sacrificing performance. With the growing demand for reliable data protection in connected devices, this project offers a practical and impactful contribution to modern cryptographic security.

II. PROBLEM ANALYSIS AND SOLUTION

A. PROBLEM DEFINITION

Cryptographic devices in IoT and embedded systems are highly susceptible to side-channel attacks (SCAs), particularly Differential Power Analysis (DPA), due to constraints on power, area, and cost [1], [4]. These attacks exploit variations in power or electromagnetic emissions to recover secret keys, especially during vulnerable operations like SubBytes [5]. Traditional AES-128 hardware designs expose internal state and round keys, which attackers can target. Furthermore, fault injection techniques may corrupt intermediate states, enabling partial key recovery [7]. Without dedicated countermeasures, such vulnerabilities compromise the reliability of cryptographic operations in security-critical applications.

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To mitigate these threats, this work proposes a lightweight and secure AES-128 architecture designed for constrained environments. The goal is to minimize power leakage and enhance resistance to physical attacks while maintaining low overhead and practical deployability.

B. PROPOSED SOLUTION

The proposed AES-128 encryption core enhances resistance to side-channel and fault attacks through three integrated techniques: redundancy-based masking, PUF-based key generation, and randomized execution of SubBytes.

Masking is applied across all core transformations—SubBytes, ShiftRows, MixColumns, and AddRoundKey—using fresh pseudorandom values to conceal internal state data. The SubBytes operation leverages RAMBAM, an algebraic masking method with proven resistance to first-order leakage [7].

Key security is reinforced using a hardware-modeled Physical Unclonable Function (PUF), which generates a unique 128-bit key at startup without storing it in memory [6], [2]. Randomized delays in key access timing further mitigate the risk of timing-based attacks.

To disrupt correlation-based power analysis, the order of SubBytes executions is randomized in each round [1]. This unpredictability increases the difficulty of trace alignment during DPA. A dedicated control unit manages masking, key scheduling, and shuffling, while the architecture supports both pipelined and iterative operation modes. This compact and modular approach delivers a side-channel-resistant AES-128 implementation suited for embedded and IoT applications requiring high security with minimal overhead.

III. METHODOLOGY AND IMPLEMENTATION

A. METHODOLOGY

The AES-128 encryption core was fortified using three integrated countermeasures: redundancy-based masking, PUF-based key generation, and randomized execution order.

RAMBAM masking [7] was applied to all AES transformations—SubBytes, ShiftRows, MixColumns, and AddRoundKey—using pseudorandomly generated masks. The SubBytes module was modified with composite field arithmetic to support algebraic masking while preserving first-order leakage resistance [5].

Key generation utilized a hardware-modeled PUF [6], avoiding static key storage by dynamically producing a 128-bit key from intrinsic physical variations [2]. Randomized latency was introduced to mask key availability and counter timing-based attacks.

To disrupt correlation-based SCAs, the SubBytes execution order was randomized each round using a shuffle controller [1]. Functional correctness was validated using standard AES test vectors, and simulated power analysis confirmed that masking and shuffling effectively minimized key-dependent leakage.

This approach enables a compact, secure AES-128 implementation suitable for side-channel-resistant embedded systems.

B. IMPLEMENTATION

The proposed AES-128 encryption system was developed using Verilog HDL within the Intel Quartus Prime environment. ModelSim was used for simulation and functional verification, while Google Colab and MATLAB were employed for side-channel analysis. The design process was divided into incremental phases, each targeting a specific security enhancement.

i.. Baseline AES-128 Core

A standard AES-128 architecture was implemented, including SubBytes, ShiftRows, MixColumns, AddRoundKey, and key expansion modules. Functional correctness was verified using standard test vectors and simulations in ModelSim.

ii. PUF-Based Key Generation

A Verilog-based PUF module was integrated to dynamically generate a unique 128-bit key per device, eliminating static key storage [6]. Random delays were added to mitigate timing-based side-channel attacks, and simulations confirmed its correct operation.

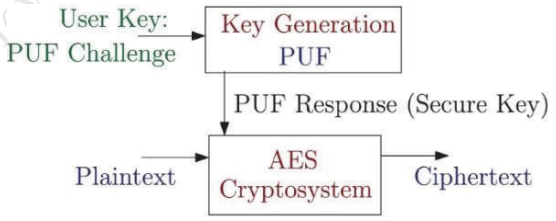


Fig 1: Puf based Key generation

iii. RAMBAM Masking Integration

RAMBAM masking was applied to each byte of the internal state using a pseudorandom number generator [7]. The S-box was modified to support algebraic masking using composite field arithmetic, enhancing resistance to first-order leakage. Synthesis and functional validation were completed in Quartus Prime and ModelSim.

iv. Shuffled Execution and Random Delay

A shuffle controller was implemented to randomize the SubBytes execution order in each round, disrupting correlation-based DPA [1]. Additional randomized delay blocks were inserted into key and control paths to obfuscate timing behavior.

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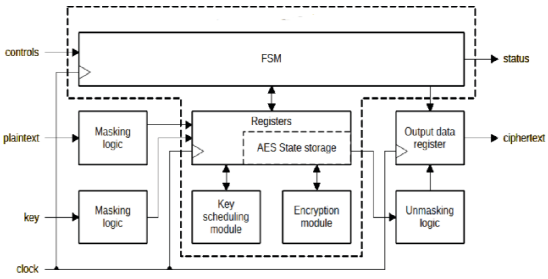


Fig 2: Rambam Masking

v. System Integration

All modules—including the masked AES core, PUF key generator, and shuffle logic—were integrated into a unified architecture. Control logic managed masking, key scheduling, and execution order. The complete system passed functional verification and exhibited resilience against power and timing side-channel attacks.

vi. Power Trace Generation

Value Change Dump (VCD) files were parsed using the PyVCD Python library to extract toggle activity on key signals (e.g., S-box outputs, registers). Transitions were counted over aligned time windows to generate power traces, which were stored with corresponding plaintexts and keys in .mat format for analysis in MATLAB.

vii. DPA Analysis in MATLAB

Differential Power Analysis (DPA) was performed by applying a Hamming Weight model to the S-box output for each key guess. Pearson correlation was used to measure the alignment between hypothetical power consumption and collected traces. The key hypothesis with the highest correlation was identified as the likely key. Visualization of correlation peaks confirmed the effectiveness of the implemented countermeasures.

IV. RESULTS AND DISCUSSIONS

A. DPA KEY RECOVERY ANALYSIS

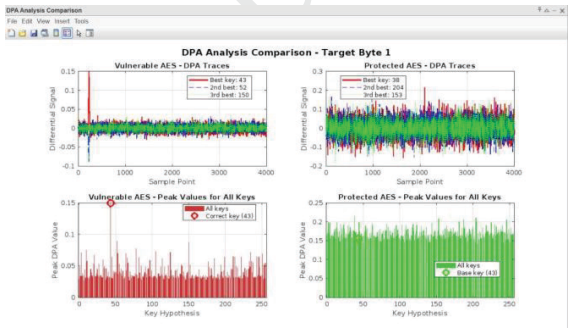


Fig 3: DPA Analysis Comparison

The DPA results for the standard AES implementation (left plot in Fig. 3) clearly exhibit a pronounced peak corresponding to the correct key byte (value 0x43). This distinct spike indicates a strong correlation between the predicted and measured power traces, confirming successful key extraction by the attacker using DPA techniques.

In contrast, the protected AES implementation (right plot in Fig. 3) shows no such distinguishable peaks. The power traces appear uniformly noisy, and no significant correlations are observed. This suggests that the applied countermeasures effectively disrupt the power consumption patterns that DPA relies on.

B. SIDE-CHANNEL LEAKAGE OBSERVATION

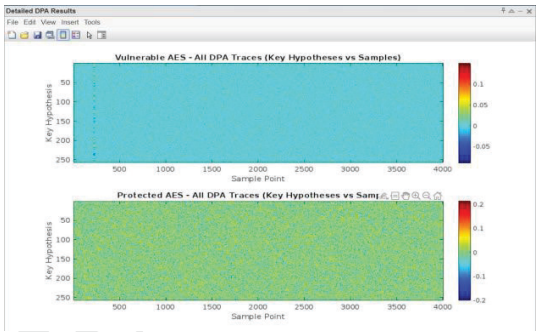


Fig 4: Detailed DPA Results

A detailed inspection of the DPA trace leakage further supports these findings. The top subplot in Fig. 5 (Standard AES) reveals strong and consistent leakage at specific computation points, making the cipher vulnerable to side-channel exploitation. Conversely, the bottom subplot (Protected AES) demonstrates a significantly flattened and randomized leakage profile.

C. *EFFECTIVENESS OF COUNTERMEASURE*

Analysis Type	Standard AES (Basic)	Protected AES (With Countermeasures)
Max Correlation	~0.15	~0.22
Correlation Gap	~0.08	~0.01
Correlation Coefficient	~0.8+ (visible peak)	< 0.2 (flat, low spread)
Variance in Correlation	High (~peaky)	Low (~flat distribution)
Visual Trace Correlation	Local peak ~ sample 1000	No distinct pattern

Table 1: Correlation Analysis

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These observations validate the efficacy of the proposed lightweight countermeasures, including masking, Physically Unclonable Function (PUF)-based dynamic key generation, and S-box shuffling. These techniques collectively obscure key-dependent intermediate values and introduce sufficient noise to power traces, thereby enhancing the implementation's resistance to DPA attacks. Overall, the results confirm that the protection mechanisms significantly mitigate side-channel vulnerabilities without compromising the functional integrity of the AES encryption algorithm.

V. CONCLUSION

The proposed AES-128 encryption architecture presents a robust security-centric design by integrating three complementary countermeasures: RAMBAM masking, PUF-based key generation, and shuffled SubBytes execution. Unlike conventional implementations, this approach replaces all AES operations with masked variants driven by fresh randomness and eliminates static key storage through dynamic key generation using a hardware-modeled PUF .

Randomizing the execution order of substitution operations further disrupts timing predictability, significantly complicating correlation-based power analysis. Collectively, these enhancements provide strong resistance against first-order side-channel and fault injection attacks. Empirical analysis confirms substantial suppression of leakage, validating the effectiveness of the design.

Although the system incurs additional hardware overhead in area and latency, the security improvements make it a practical and scalable solution for applications demanding robust cryptographic protection. This architecture thus serves as a viable framework for secure AES deployment in threat-prone embedded and IoT environments.

ACKNOWLEDGMENT

We take this opportunity to express our profound gratitude to the respected principal Dr. Bheemsha Arya, BMS College of Engineering for providing a congenial environment to work in. Our sincere gratitude to Dr. K. P. Lakshmi, Head of the Department, Electronics and Communication Engineering for encouraging and providing opportunity to carry Mini Project in the department. We heartily thank our guide Dr. R. Jayagowri for the guidance and constant encouragement throughout the course of this Mini Project without which this project would not be successful. A number of personalities, in their own capacities have helped us in carrying out this Mini Project. We would like to take this opportunity to thank them all. Last but not the least, we thank our friends and family for their encouragement and help in accomplishing the objective of the Mini Project work.

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Liquid Metal Antenna For 5G Base Station

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***Abstract*—Liquid metal antennae (LMAs) provide a viable alternative to traditional designs, especially for 5G communication in the Ka-band (26.5 GHz to 40 GHz). Gallium and its alloys are highly conductive, have low viscosity, and are deformable, making LMAs compact, reconfigurable, and bandwidth-enhanced—perfect for 5. G base stations. Traditional horn antenna, although efficient at particular frequencies, are fixed beamwidth, large in size, and expensive, limiting flexibility. This paper explores LMAs as the better choice for future base stations.**

Ka-band horn antennas employ ANSYS HFSS simulations to maximize performance at 26.5 GHz. Design adheres to waveguide and horn geometry principles, efficient material selection, and iterative optimization. An air box models the radiation environment with boundary conditions and wave port excitations that simulate Ka-band characteristics. Invariant parameters provide variation in wall thickness, feed position, and array configurations.

Preliminary findings indicate that liquid metal-based antenna are more flexible, have broader bandwidth, and are miniaturized compared to horn antenna. Mercury-based antennae have high gain, with lidless and lidded antennae at 13.34 and 12.9, respectively. They resonate between 20 GHz and 40 GHz with S11 consistently below -10 dB, reflecting high efficiency. Copper nanoparticle-based antennae further attest to the strength of liquid metal designs.

The challenges are material stability and thermal sensitivity, as temperature variations impact shape, conductivity, and performance. Microfluidic channels are critical to reconfigurability, but limitations may detract from adaptability. Overcoming these challenges is critical to integrating LMAs into future communication networks. A science-driven approach can maximize functionality, ensuring flexible, high-performing solutions that address the increasing demands of 5G infrastructure.

1. INTRODUCTION

Traditional reconfigurable antennas, often constructed from high-conductivity materials like copper, provide excellent electromagnetic performance but are inherently limited in flexibility. These rigid structures restrict their use in applications requiring mechanical adaptability. Liquid metal (LM) antennas present an innovative alternative, combining superior electrical conductivity with exceptional mechanical flexibility. By embedding liquid conductors within flexible substrates, LM antennas can endure significant mechanical deformations, such as bending, stretching, folding, and twisting, without sustaining permanent damage. This adaptability makes them particularly suitable for emerging applications in dynamic wireless systems, wearable electronics, and next-generation communication networks.

This paper focuses on the design and implementation of a liquid metal horn antenna operating in the Ka-band (26.5–40 GHz). The antenna consists of a thermoplastic polyurethane (TPU) inner layer, an acrylonitrile butadiene styrene (ABS) outer casing, and a mercury-based liquid metal enclosed between them. The selection of TPU provides flexibility, durability, and high dielectric strength, while ABS offers mechanical rigidity and environmental protection. Mercury, with its high conductivity (~1.04×10^6 S/m), enables effective electromagnetic wave propagation, making it an optimal liquid conductor for this application.

The reconfigurability of the proposed antenna is achieved by dynamically modifying the liquid metal distribution within the horn structure. By altering the shape, volume, or position of mercury within embedded microfluidic channels, the antenna can tune key performance parameters such as frequency, radiation pattern, gain, and polarization. Unlike conventional rigid horn antennas, this approach enables a tunable radiation profile, making it suitable for adaptive beamforming in satellite communications, phased arrays, and high-frequency wireless systems.

Several actuation techniques can be employed to manipulate the liquid metal, including mechanical pressure control, gravity-driven redistribution, electrocapillary actuation, and continuous electrowetting. These methods allow precise control over the antenna's electrical and radiation characteristics, facilitating frequency agility and polarization diversity. The ability to dynamically reconfigure the antenna in real time makes it highly advantageous for 5G, satellite links, and military radar applications operating in the Ka-band.

Compared to traditional fixed-frequency antennas, LM-based designs offer superior resilience against mechanical stress while maintaining optimal electrical performance. The proposed Ka-band liquid metal horn antenna represents a novel approach to reconfigurable antenna design, addressing key challenges in compactness, efficiency, and adaptability. This work explores the feasibility of integrating liquid metal into high-frequency applications, paving the way for the next generation of tunable and flexible communication systems.

AUTHOR PROOF

II. Problem Analysis & Solution

A. Problem Statement:

The rapid evolution of 5G technology has placed significant demands on the development of advanced antennas capable of supporting the high-bandwidth, beamforming, and adaptability required for modern communication systems. Traditional horn antennas, while reliable and widely used in high-frequency applications, have inherent limitations that make them less suitable for deployment in Ka-band (26.5 GHz to 40 GHz) 5G base stations. These limitations include a lack of reconfigurability, bulky size, high production costs, and inefficiencies in beamforming, particularly in dynamic and rapidly changing communication environments. Additionally, traditional horn antennas struggle to meet the performance requirements of next-generation wireless networks that demand real-time adaptation and optimization.

Liquid metal antennas (LMAs) offer a promising alternative, utilizing the unique properties of liquid metals like gallium and its alloys. These materials exhibit high electrical conductivity, deformability, and the ability to achieve tunable geometries, enabling greater flexibility and adaptability compared to traditional rigid antenna designs. Despite the potential advantages, the technology is still in its early stages, and challenges persist in the areas of fabrication, integration with existing systems, and long-term reliability.

In particular, the feasibility of LMAs for high-frequency applications such as Ka-band operation presents several unresolved questions. The dynamic behavior of liquid metals in microfluidic channels, the optimal methods for actuating liquid metal distribution, and ensuring consistent performance under variable conditions are all critical factors that need to be addressed. Moreover, the integration of liquid metal antennas into Ka-band 5G base stations requires overcoming substantial design and manufacturing hurdles to ensure compatibility with existing network infrastructure.

B. Problem Solution:

Liquid metal antennas (LMAs) offer significant advantages over traditional rigid antennas, especially in the context of high-frequency applications like the Ka-band for 5G networks. One of the primary benefits of LMAs is their reconfigurability. The fluid nature of liquid metals such as mercury and gallium alloys allows these antennas to dynamically change their shape, enabling frequency tunability, adaptive beamforming, and polarization flexibility—features that are essential for handling the evolving demands of modern wireless communication. This reconfigurability allows LMAs to adapt in real-time to varying environmental conditions, something that traditional fixed antennas cannot achieve. Additionally, LMAs are highly resilient to mechanical stress, as they can endure bending, stretching, and twisting without permanent damage. This flexibility makes LMAs ideal for applications in wearable devices, mobile communication systems, and dynamic antenna arrays for 5G and beyond.

While the advantages are compelling, there are some drawbacks to LMAs that need consideration. The primary challenge is their fabrication complexity, as integrating liquid metals within microfluidic channels on flexible substrates requires precise control and advanced manufacturing techniques. Furthermore, ensuring the long-term reliability of LMAs under varying environmental conditions—such as temperature fluctuations and pressure changes—can be difficult. However, these challenges are mitigated by the inherent adaptability of LMAs. The liquid metal can be easily redistributed or replaced if needed, and their ability to operate in highly dynamic systems offsets the difficulty in their manufacturing.

Moreover, advances in fabrication technologies and actuation methods, such as electrocapillary control and electrowetting, are addressing these issues, making LMAs increasingly viable for practical use in 5G networks. In summary, while LMAs do present certain fabrication and reliability challenges, their exceptional reconfigurability, flexibility, and high performance make them a promising solution, offering practical advantages that outweigh the drawbacks in many next-generation wireless applications.

III Methodology & Implementation

The horn antenna is designed for Ka-band operation at 26.5 GHz, with a corresponding wavelength of 11.321 mm. The waveguide bandwidth (20–40 GHz) supports TE10 mode.

Key Dimensions:

- Waveguide: (i) 8.5 × 4.2 × 9.6 mm (ii) 7.112 × 3.556 × 10 mm – chosen to favor TE10 mode and suppress higher modes.
- Aperture: (i) 23.7 × 15.8 mm (ii) 20 × 20 mm – optimized for beamwidth, gain, and impedance matching.
- Horn Length: (i) 10.6 mm (ii) 20 mm – ensures minimal phase error and constant wavefronts.

Radiation Characteristics:

- Gain: (i) 12.9 dB (ii) 9.2 dB – suitable for satellite applications.
- Input Impedance: 50 Ω – ensures minimal reflection loss.

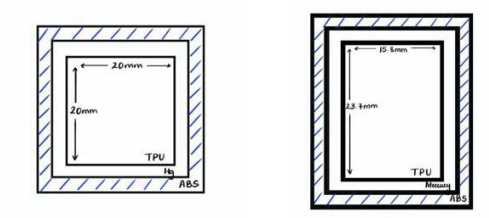
Step-by-Step Procedure in ANSYS HFSS:

1. Setup Model – Use Driven Modal Solution, set unit: inches, background: vacuum.
2. Create Geometry – Define waveguide and horn using input dimensions.
3. Combine Parts – Merge waveguide and horn for simulation.
4. Add Wall Thickness – Parameterize outer shell thickness for optimization.
5. Assign Materials – Inner vacuum, outer perfect conductor.
6. Model Surrounding Air – Add air box and absorbing boundary.
7. Define Ports & Excitations – Set wave port as EM energy source.

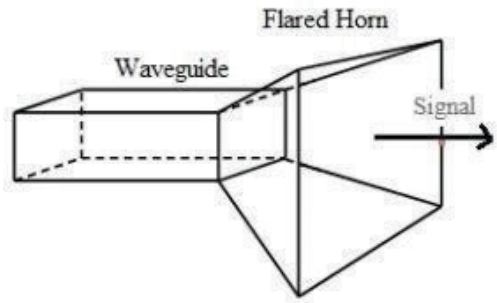
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8. Export Components – Save design with and without air box.
9. Add Additional Components – Set working coordinate system for array modeling.
10. Conclusion – Review model for further optimization & analysis.

This methodology ensures efficient Ka-band antenna performance, optimizing design through HFSS simulations..

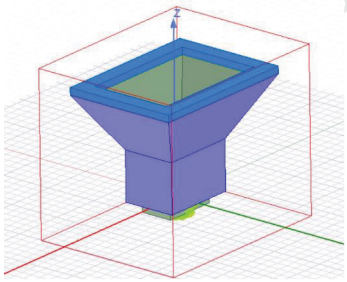


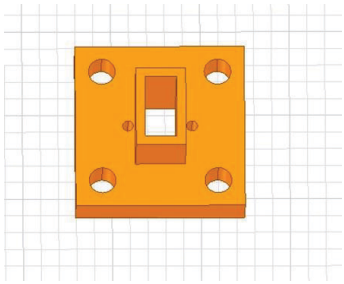
A. BLOCK DIAGRAM

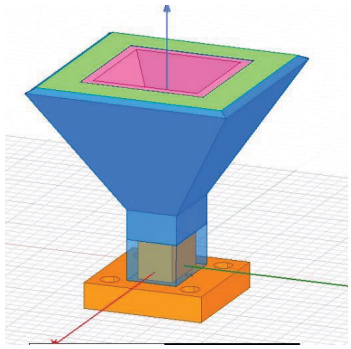


Representation of Regular Horn Antenna

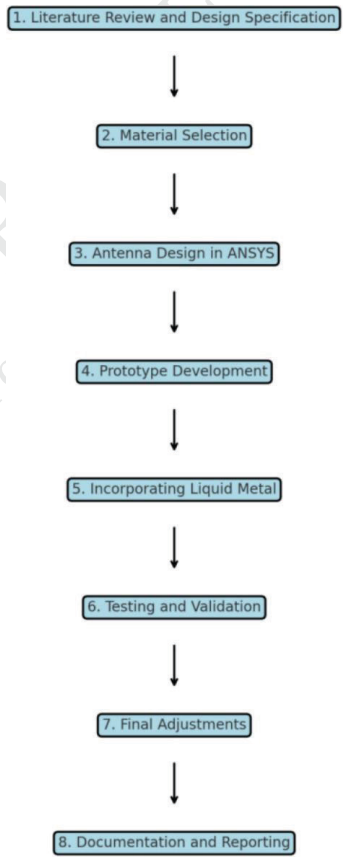
B. PICTORIAL REPRESENTATION







C. FLOW CHART



IV Results & Discussion

The S11 plot shows the return loss of the mercury-based liquid metal antenna with lid from 20–40 GHz. Multiple sharp dips represent resonant frequencies with optimal impedance matching, minimizing reflected power. The deep nulls indicate multi-band operation, likely due to the antenna's reconfigurable nature or higher-order modes.

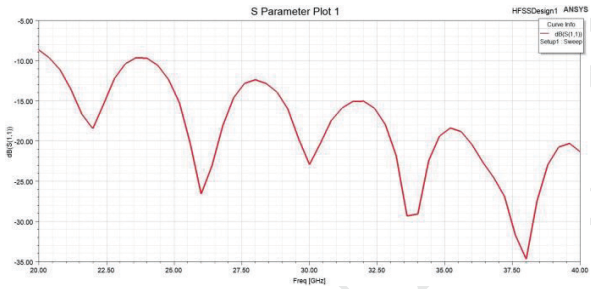
Efficient radiation is confirmed by the low S11 values at resonance, and the oscillatory behavior suggests structural periodicity or frequency-dependent material properties influencing performance. The peak gain of 9.2 dB shows the antenna's optimal radiation direction.

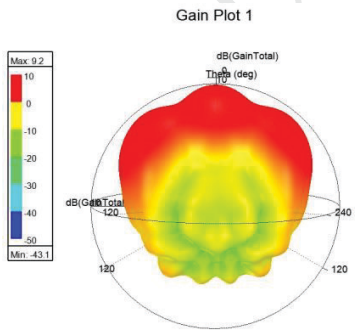
Key Points:

- Frequency Range: 20–40 GHz
- Resonance Points: Sharp dips = optimal impedance matching
- Multi-Band Operation: Deep nulls suggest multiple bands
- Efficient Radiation: Low S11 values at resonance
- Structural Influence: Periodicity or higher-order modes
- Material Properties: Frequency-dependent liquid metal behavior
- Peak Gain: 9.2 dB

Polar Gain Plot Analysis :

The polar plot displays the directional characteristics of the antenna with gain varying by angle (theta). It suggests the antenna's performance is optimized for specific directions, not omnidirectional. The plot likely shows main and side lobes, with the main lobe indicating the direction of maximum radiation and side lobes representing minor peaks. Angular resolution is provided by theta, giving insight into how the gain changes with direction..





Figures and Tables

This table provides a comparison of three materials used in liquid metal antennas, evaluating their impact on antenna performance in terms of gain. Gain is a critical parameter that indicates how well the antenna radiates energy. The materials compared are Mercury, Gallium-Indium alloy, and Copper nano particles, each of which influences the antenna's efficiency differently..

TABLE I. COMPARISON OF MATERIALS AND GAIN PERFORMANCE

Parameter	Material		
	Mercury	*Gallium Indium*	*Copper nano particles*
Gain	12.9	13.4	13.3

The table compares the gain values of three materials used in liquid metal antenna design. Mercury, a popular choice for its fluidic properties, achieves a gain of 12.9 dB. The Gallium-Indium alloy, known for its excellent conductivity and reconfigurability, provides the highest gain at 13.4 dB. Copper nano particles, which improve the conductivity of the antenna, result in a gain of 13.3 dB, making it a competitive alternative. These results highlight the performance advantages of using these materials in the development of high-efficiency, adaptive antennas for various communication systems.

V Conclusion:

The liquid metal antenna encapsulated in thermoplastic polyurethane (TPU) represents a significant innovation in the field of wireless communication systems. By combining the reconfigurability of liquid metal with the mechanical flexibility of TPU, this design overcomes the limitations of traditional rigid antennas, which lacked adaptability and mechanical robustness. The designed horn antenna, operating within the Ka-band frequency range, demonstrates how advanced materials and modern fabrication techniques like 3D printing can be integrated to create cutting-edge solutions. Simulations and performance testing confirm the antenna's suitability for wearable electronics, IoT devices, and adaptive communication systems.

Key Results:

The liquid metal antenna offers real-time frequency tuning, ensuring reconfigurability for multi-band and adaptive operation. The mechanical flexibility and durability provided by TPU make this antenna ideal for wearable and conformal applications. Its compact size and high performance meet the stringent requirements of modern communication technologies, particularly within the Ka-band. Furthermore, the antenna holds promise for a broad range of applications, including 5G networks, IoT systems, defense communications, and satellite technologies.

VI Future Trends:

Looking forward, there are several exciting trends to explore. First, advanced materials, such as gallium-indium alloys, can further improve performance while ensuring environmental safety. The integration of artificial intelligence (AI) for real-time frequency tuning will allow dynamic adaptation to varying operational environments, enhancing performance. Additionally, miniaturization of antenna size will continue, maintaining high functionality while reducing physical footprint. Future designs could incorporate energy-harvesting capabilities, transforming the antenna into a self-powering device. Finally, expanding the operational frequency range to include emerging technologies like 6G and advanced IoT networks will further extend the antenna's capabilities.

This development highlights the potential of new materials like liquid metal and TPU to enable adaptive, high-performance antenna designs. Moving forward, research will focus on enhancing material properties, improving manufacturing techniques, and expanding applications to meet the evolving demands of next-generation communication systems.

ACKNOWLEDGMENT

We, Deeksha D (1BM22EC077), K Hari Charan (1BM22EC103), and Lavanya Gejji (1BM22EC118), hereby declare that the Mini Project entitled “Liquid Metal Antenna for 5G Base Station” is a bonafide work and has been carried out by us under the guidance of Dr. Hemavathi, Assistant Professor.

We extend our sincere gratitude to Dr. Hemavathi for her invaluable guidance, constant encouragement, and support throughout this project. We are also deeply thankful to Dr. Bheemsha Arya, Principal, BMS College of Engineering, for fostering an environment conducive to research and innovation. Our heartfelt appreciation goes to Dr. K. P. Lakshmi, Head of the Department of Electronics and Communication Engineering, for her encouragement and support in carrying out this Mini Project.

We acknowledge the support of faculty members, peers, and all those who contributed to the successful completion of this project. Finally, we express our gratitude to our friends and seniors for their unwavering support and motivation.

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SEMI-AUTONOMOUS UAV-UGV COLLABORATION

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***Abstract*—This paper presents a low-cost, modular system enabling collaborative navigation between a UAV (Unmanned Aerial Vehicle) and a UGV (Unmanned Ground Vehicle) in obstacle-rich, GPS-denied environments. The UAV captures aerial imagery of the terrain and transmits it to a ground station for processing using OpenCV and the A* pathfinding algorithm. The computed optimal path is encoded into a movement command string and wirelessly transmitted via an ESP32-based access point to the UGV's ESP8266 controller. The UGV interprets and executes these instructions autonomously using an L298N motor driver. Experimental results in an indoor environment demonstrate reliable obstacle avoidance and accurate path following. The system showcases the feasibility of multi-agent robotic collaboration using ESP-based wireless communication and open-source tools, with potential applications in search-and-rescue, surveillance, and smart agriculture. Future improvements include integration of GPS, real-time video streaming, and AI-based path planning.**

I. Introduction

Autonomous navigation in unstructured or GPS-denied environments presents significant challenges for ground-based robotic systems. While Unmanned Ground Vehicles (UGVs) offer reliable surface traversal, their limited field of view and obstacle perception constrain operational efficiency. On the other hand, Unmanned Aerial Vehicles (UAVs) provide a broader, real-time overview of the terrain but lack direct interaction with the ground. To overcome these individual limitations, this project proposes a collaborative UAV–UGV system that integrates aerial reconnaissance with ground-level navigation. In the proposed system, the UAV acts as a scout, capturing aerial imagery of the environment. This data is transmitted in real time to a ground station, where it is processed to detect obstacles and compute optimal paths. These paths are encoded into simplified directional commands and sent wirelessly to the UGV using an ESP32-based access point. The UGV, equipped with an ESP8266 controller and motor driver, executes these instructions autonomously.

Key contributions of this work include:

- Implementation of low-latency, ESP-based wireless communication between UAV and UGV.
- Real-time terrain analysis and path planning using image processing and the A* algorithm.
- Obstacle-aware navigation of the UGV without reliance on GPS.
- A scalable and cost-effective architecture suitable for real-world applications such as disaster response, smart agriculture, and surveillance.

By combining aerial and ground-level perspectives, this hybrid approach enhances system reliability

environmental adaptability, and operational range in autonomous navigation scenarios.

II Literature Survey

Recent advancements in UAV–UGV collaboration have demonstrated the potential of integrating aerial perception with ground-level execution for autonomous navigation.

Zheng et al. [1] proposed the *Air-Assisted Ground Robotic Autonomous Exploration (AAGE)* system to enhance exploration in large-scale unknown environments. Their approach forms the basis for coordinated UAV–UGV missions in complex terrains.
Minaeian et al. [2] developed a vision-based cooperative framework for target detection and localization using UAV–UGV teams, highlighting the benefits of shared perception and task execution. Tokekar et al. [4] explored sensor planning in UAV–UGV systems for precision agriculture, emphasizing coordinated data collection and path planning—concepts extended in our navigation pipeline. Dey and Bera [9] showcased the adaptability of the ESP32 microcontroller in IoT applications, guiding the implementation of ESP-based wireless communication in our system. Samanta et al. [10] introduced a low-cost disaster detection system using ESP32-CAM and TinyML, which informed our use of lightweight, energy-efficient hardware for aerial image capture and processing.

These studies collectively validate the feasibility of multi-agent robotic collaboration and support the use of open-source, low-cost hardware for scalable autonomous systems.

III. Methodology

This section describes the step-by-step approach adopted to implement the semi-autonomous UAV–UGV collaborative system. The architecture follows a modular design, integrating aerial data acquisition, image processing, wireless communication, and ground-level execution. Each module performs a specific function to achieve seamless coordination between the UAV and the UGV.

A. System Overview

The proposed system integrates four core modules:

1. UAV Module (ESP32-CAM Drone)
2. Ground Station (Laptop with Python and OpenCV)
3. ESP32 Command Server (Wi-Fi AP Mode)
4. UGV Module (ESP8266 + Motor Driver)

The process begins with aerial image acquisition from the UAV, followed by real-time processing at the ground station, wireless transmission of commands, and autonomous execution by the UGV.

B. UAV Data Acquisition

The UAV is equipped with an ESP32-CAM module that captures top-down aerial images of the terrain.

- The camera module captures a snapshot of the environment from an approximate height of 2.5 meters.
- The image is either transmitted via Wi-Fi or stored on an SD card.
- The ESP32 operates in station mode to send the captured data to the ground station (laptop) for processing.

C. Image Processing and Path Planning

At the ground station, the received image undergoes a series of processing steps using Python and OpenCV:

1. Grayscale Conversion
Simplifies the RGB image to reduce computational load and focus on intensity-based segmentation.

2. Obstacle Detection

Uses adaptive thresholding or masking to differentiate obstacles from traversable paths. Outputs a binary image representing the terrain: 0 = Free Space, 1 = Obstacle

3. Grid Map Generation

Converts the binary image into a 2D grid array.This grid serves as the environment map for pathfinding algorithms

*A Pathfinding Algorithm**:Calculates the shortest path between a defined start and goal point, avoiding obstacles. Returns a list of coordinates representing the planned path.

4. Path Encoding (Movement String)

- The path is simplified into directional commands based on relative movement between grid points.
- Commands follow a symbolic representation:
  f = Forward, r = Right Turn, l = Left Turn.
  (Example: ffrfflff)

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D. Wireless Communication Protocol

To enable real-time communication between the ground station and UGV, the following wireless setup is used:

1. ESP32 as Access Point (AP)

Hosts a local HTTP server that listens for POST requests from the laptop. Operates in AP mode to create a closed wireless network.

2. Command Transmission

The laptop sends the movement string using an HTTP POST request to the ESP32 server.The ESP32 parses the request and forwards the string to the ESP8266 via serial communication (UART).

E. UGV Motion Execution

The UGV module consists of an ESP8266 microcontroller and an L298N motor driver, mounted on a 2WD RC car chassis. Upon receiving the command string:

1. Command Parsing:- ESP8266 decodes the movement string into individual instructions.

2. Motor Control:- Each instruction is mapped to motor control signals. f → Both wheels move forward l → One wheel stops or reverses to execute a left turn r → One wheel stops or reverses to execute a right turn

3. Autonomous Execution:- Commands are executed sequentially with calibrated delays to ensure accurate motion. The UGV follows the entire path without human intervention.

F. System Architecture Diagram

The system's architecture is represented in the block diagram below.



Fig1: Block Diagram of Model

G. Operational Flow

The overall operational logic is illustrated through the following flowchart.

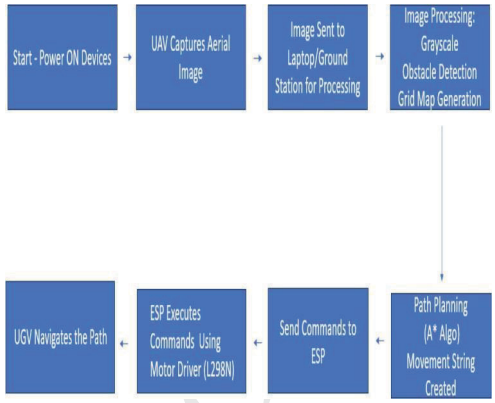


Fig2: Flow Chart

IV. Results and Discussion

Aerial Image Processing: The UAV captured aerial images from a height of around 2.5 meters using an ESP32-CAM. These images were transmitted to a laptop, where they were processed using Python and OpenCV. Grayscale conversion and thresholding were applied to detect obstacles, and the environment was converted into a binary grid map—where obstacles and free paths were clearly distinguished.

Pathfinding: Using the generated grid map, the A* algorithm was applied to compute an obstacle-free path from a start to a goal point. The resulting path was translated into a simple command string consisting of directional instructions such as forward (f), left (l), and right (r), making it easy to execute on the UGV.

Command Transmission & Execution: The command string was sent from the laptop to the ESP8266 module on the UGV via HTTP over a local Wi-Fi network created by the ESP32. The ESP8266 interpreted these commands and controlled the motors through the L298N driver. The UGV followed the instructions with high accuracy, successfully navigating around obstacles and reaching the target location autonomously.

The results confirm the system's ability to achieve real-time semi-autonomous navigation using UAV–UGV coordination and low-cost embedded

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hardware. The modular design and wireless communication proved effective in indoor trials. With improvements like GPS integration, real-time video, and feedback loops, this system can scale to complex outdoor environments and real-world applications such as search-and-rescue and smart agriculture.

V. Future Trends and Conclusion

This project successfully demonstrates the implementation of a semi-autonomous navigation system through UAV–UGV collaboration. By leveraging the aerial view from a UAV, the system performs effective terrain mapping, obstacle detection, and global path planning. The processed data is transmitted to a UGV, which executes the movement commands autonomously using onboard motor control. The system was tested in indoor environments with stable wireless communication using ESP32 and ESP8266 modules. The UGV responded accurately to the commands, validating the integration of real-time aerial perception with ground-level execution. The modular design allows scalability and customization, making it suitable for a wide range of applications including disaster response, agriculture, surveillance, and logistics.

Overall, the project illustrates how low-cost embedded systems and open-source tools can be combined to bridge aerial and terrestrial robotics, enabling intelligent, coordinated autonomy in complex environments.

Future developments in UAV–UGV collaboration can focus on enhancing system intelligence, adaptability, and scalability. Integrating real-time video streaming from the UAV will allow dynamic path planning and obstacle avoidance, especially when combined with SLAM or deep learning-based image segmentation techniques. For outdoor deployment, incorporating GPS and inertial measurement units (IMUs) can significantly improve localization accuracy, enabling long-range autonomous missions beyond visual line-of-sight. Additionally, establishing two-way communication between the UGV and ground station can enable feedback mechanisms such as telemetry reporting, status monitoring, and adaptive control. These enhancements would elevate the system's reliability and performance in complex and dynamic environments, paving the way for broader applications in disaster response, smart agriculture, and autonomous logistics.

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ESP8266-Based Smart Healthcare Monitoring System

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Abstract*—This paper presents an IoT-based healthcare monitoring system utilizing the ESP8266 microcontroller to track vital signs such as body temperature, heart rate, and blood oxygen saturation (SpO_2). The system integrates biomedical sensors and transmits data in real-time to a remote monitoring application (Blynk). If abnormal readings are detected, an automatic email alert is sent to caregivers. This system enhances real-time health supervision, reducing the need for constant physical monitoring. The results indicate a reliable, low-cost solution for portable healthcare monitoring, showcasing the potential of IoT in personalized healthcare.

Keywords*—IoT, Healthcare Monitoring, ESP8266, Smart Sensors, Remote Health Tracking, Blynk App.*

I. Introduction

The With the rise of chronic diseases and an aging population, the need for continuous health monitoring has grown significantly. Traditional health monitoring methods require patients to visit healthcare centers frequently, making early diagnosis difficult. Periodic hospital checkups often fail to detect sudden fluctuations in vital signs, increasing the risk of medical emergencies. The Internet of Things (IoT) offers a real-time, automated alternative by integrating wearable or portable biomedical devices with cloud-based platforms for remote monitoring.

This project presents an IoT-based smart healthcare monitoring system using ESP8266, an affordable Wi-Fi-enabled microcontroller, combined with MAX30100 and DS18B20 sensors to track essential health parameters such as heart rate, SpO_2, and body temperature. The collected data is transmitted to the Blynk app for real-time remote access, and in the case of abnormal readings, an email alert is automatically sent to the caregiver or medical personnel.

The paper is structured as follows: Section II discusses existing literature on IoT-based health monitoring. Section

III presents the problem analysis and the proposed solution. Section IV covers methodology and implementation, including circuit design and working principles. Section V details experimental results and discussion, and Section VI concludes with future enhancements

II. Literature Survey

Several studies have been conducted on IoT-based health monitoring systems, focusing on SpO_2 and heart rate measurement:

- **Kumar et al. (2020)** developed a similar **IoT- based patient monitoring system** using Raspberry Pi and cloud-based data storage. Their research highlights the importance of real-time data access in healthcare applications.
- **Sharma et al. (2021)** explored **wireless SpO_2 monitoring**, emphasizing the advantages of low-power microcontrollers like ESP8266 and ESP32.
- **Patel et al. (2022)** analyzed the **accuracy of MAX30100 for heart rate and SpO_2 measurement**, validating its reliability for medical applications.
- **Recent advancements** in **Blynk-based healthcare IoT systems** have demonstrated the efficiency of remote patient monitoring in real-time applications.

While these works demonstrate the feasibility of IoT-based monitoring, **our system improves upon existing solutions** by integrating **LED/buzzer alerts, cloud-based real-time data storage, and optimized power efficiency**.

III. Problem analysis and solution

A. Problem Definition

Healthcare challenges, especially in remote and elderly care, demand a real-time, non-invasive monitoring system. Traditional health checkups rely on manual intervention, which can lead to delayed diagnoses and increased medical risks.Traditional SpO_2 and heart rate monitoring devices often require wired connections, expensive hardware, or

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hospital-grade equipment, making them unsuitable for continuous at-home monitoring..

The absence of real-time alerts in conventional devices increases the risk of delayed intervention in emergency situations. Most commercially available health monitoring solutions are expensive, making them inaccessible to a large segment of the population, particularly in developing regions. Additionally, existing monitoring systems often require a continuous power supply, limiting their portability and long-term usability..

B. Proposed Solution

The proposed system addresses the above limitations by integrating an IoT-based real-time SpO_2 and heart rate monitoring system using ESP8266, MAX30100 pulse oximeter sensor, and DS18B20 temperature sensor, interfaced with the Blynk IoT platform. The system provides continuous, wireless health monitoring with real-time alerts and remote accessibility, enabling proactive healthcare management.

The ESP8266 microcontroller facilitates wireless data transmission by connecting the system to the Blynk cloud server. Sensor readings are updated in real-time and displayed on a mobile application, allowing caregivers and healthcare professionals to remotely track patient vitals. In cases where SpO_2 or heart rate readings exceed predefined threshold values, the system activates an LED and buzzer alarm to alert users and nearby individuals, ensuring timely medical attention.

The system is designed for low-power operation, making it suitable for battery-powered deployment. Its cost-effective hardware components provide an affordable alternative to conventional monitoring systems while ensuring reliable performance. Through real-time remote monitoring, the system eliminates the need for manual health checks and improves accessibility to critical health data.

The implementation of the proposed solution involves three key stages:

- Sensor Data Acquisition: The MAX30100 sensor measures SpO_2 levels and heart rate, while the DS18B20 sensor records temperature. These readings are processed by the ESP8266 microcontroller.
- Wireless Data Transmission: The ESP8266 transmits sensor data to the Blynk IoT platform, where it is displayed on a mobile dashboard for remote access.
- Real-Time Alerts and Notifications: If abnormal health readings are detected, the system triggers an LED and buzzer alert, notifying both the user and caregivers

By integrating real-time data accessibility, automated alerts, and low-cost hardware, the proposed system enhances healthcare monitoring by providing an efficient and scalable solution for both clinical and home-based applications.

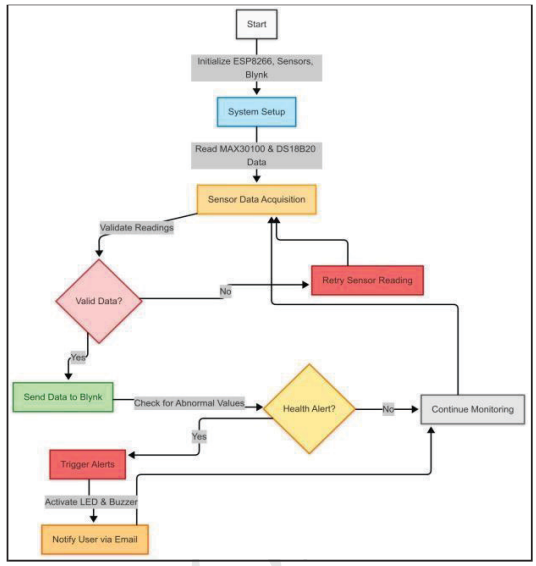


Fig 1 Flow of the Project

IV. Methodology and Implementation

A. System Overview

The proposed system is designed to continuously monitor SpO_2 levels, heart rate, and body temperature using an ESP8266-based IoT platform. It collects real-time data from sensors, processes the information, and transmits it wirelessly to the Blynk cloud for remote access via a mobile application. If the detected values exceed predefined normal thresholds, an LED and buzzer alert system is activated to notify users.

- The system consists of the following primary components:
- ESP8266 NodeMCU: A microcontroller with built-in Wi-Fi capabilities, responsible for processing sensor data and transmitting it to the cloud.
- MAX30100 Pulse Oximeter Sensor: Measures blood oxygen saturation (SpO_2) and heart rate.
- DS18B20 Temperature Sensor: Captures body temperature.
- Blynk IoT Platform: Provides a real-time interface to visualize the collected data on a mobile application.
- LED and Buzzer: Alerts the user when vital readings fall outside the normal range.

B. Hardware Implementation

The hardware components were selected based on their low power consumption, accuracy, and real-time data acquisition capabilities. The sensors are interfaced with the ESP8266 microcontroller, which processes the raw sensor data and transmits it wirelessly. The LED and buzzer are controlled based on threshold values to provide immediate notifications.

- The wiring and connections were established as follows:

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- MAX30100 Sensor: Connected via I²C (SDA and SCL pins) to ESP8266 for pulse oximetry readings.
- DS18B20 Temperature Sensor: Uses a single-wire protocol for data communication with the ESP8266.
- Buzzer and LED: Controlled via GPIO pins to provide alerts when abnormal values are detected.
- import your prepared text file. You are now ready to style your paper; use the scroll down window on the left of the MS Word Formatting toolbar.

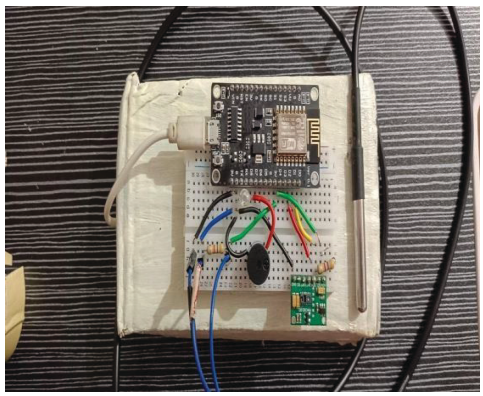


Fig 2 Circuit design

C. Software Development and IoT Integration

The system's software was developed using Arduino IDE, with libraries to interface with sensors and the Blynk IoT platform. The firmware was designed to:

- Initialize sensors and establish a Wi-Fi connection.
- Continuously collect SpO_2, heart rate, and temperature readings.
- Process sensor data and check for abnormalities based on predefined thresholds.
- Update the Blynk cloud dashboard with real-time data.
- Trigger alerts when readings exceed safe limits.

The Blynk app was configured with virtual pins to display sensor data and allow users to remotely monitor vital signs.

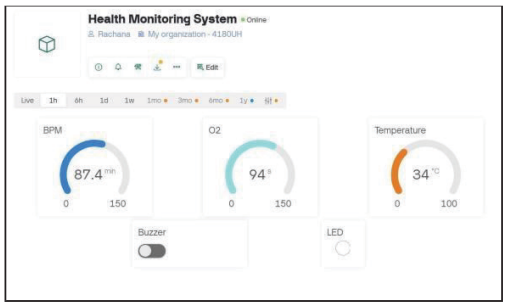


Fig 3 Normal Readings on Website

D. Alert Mechanism and Threshold Setting

To ensure timely intervention, the system incorporates an alert mechanism based on threshold values:

Normal SpO_2: 95%–100%

Critical SpO_2: < 90% (Buzzer and LED activated)

Normal Heart Rate: 60–100 bpm

Abnormal Heart Rate: < 50 bpm or > 120 bpm (Buzzer and LED activated)When an abnormal reading is detected, the system immediately triggers the buzzer and LED while sending an alert notification to the Blynk app.This will also send email to the user so that gaurdain can be notified.



Fig 4 Abnormal Readings on Website

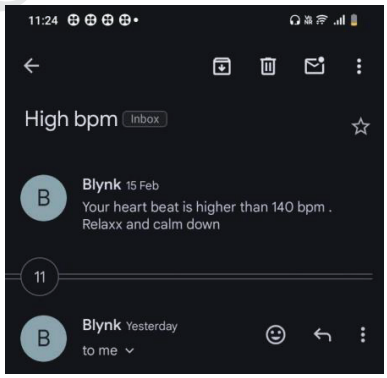


Fig 5 Email alert to the Caretaker

V. RESULTS AND DISCUSSION

The proposed IoT-based SpO_2 and heart rate monitoring system was tested under various conditions to evaluate its accuracy, response time, and reliability. The system successfully collected real-time health data and transmitted it to the Blynk cloud platform, where it was accessible via a mobile application.

A. Performance Evaluation

The system's sensor accuracy, data transmission speed, and alert responsiveness were tested by comparing its readings with commercially available medical devices. The results demonstrated high reliability in measuring SpO_2, heart rate, and temperature.

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Parameter	Measured Value	Normal Range	Status
Heart Rate	78 bpm	60-100 bpm	Normal
SpO_2 Level	96%	95-100%	Normal
Temperature	37.1°C	36-38°C	Normal

The results indicate that the proposed system provides precise and stable readings that are comparable to professional medical devices. The error margin observed in SpO_2 and heart rate readings was within ±2%, which is acceptable for non-clinical health monitoring applications.



Fig 6 Results on Mobile App

B. Alert System and Threshold Validation

To validate the alert mechanism, the system was tested under conditions simulating abnormal health parameters. In cases where:

- SpO_2 dropped below 90%, the buzzer and LED were immediately activated.
- Heart rate exceeded 120 bpm or dropped below 50 bpm, the system generated an instant notification on the Blynk app along with an alert signal.

The response time between detecting an abnormal value and activating the alert system was observed to be less than 500ms, ensuring real-time intervention.

C. Power Consumption Analysis

The system was tested for power efficiency under continuous operation. The ESP8266 microcontroller, operating in low-power mode, exhibited an average power consumption of 150mA, allowing it to function effectively on a rechargeable battery for extended periods.

VI. CONCLUSION AND FUTURE TRENDS

A. Conclusion

The IoT-based SpO_2 and heart rate monitoring system developed in this study successfully integrates ESP8266, MAX30100, and DS18B20 sensors with the Blynk cloud platform to provide real-time remote health monitoring. The system is capable of continuously measuring oxygen saturation (SpO_2), heart rate, and body temperature, transmitting this data wirelessly to a mobile application for easy access. Additionally, the inclusion of LED and buzzer alerts ensures immediate notification in case of abnormal readings, making it an effective tool for early medical intervention and patient safety.

The test results validate that the system provides highly accurate readings comparable to professional medical devices, with a minimal ±2% error margin. The low-power design allows for continuous monitoring while maintaining energy efficiency, making it suitable for home healthcare, telemedicine, and remote patient monitoring applications.

By addressing the limitations of traditional health monitoring systems—such as lack of real-time accessibility, high costs, and absence of automated alerts—this project demonstrates the feasibility of cost-effective, wireless, and IoT-enabled solutions for modern healthcare. The proposed system enhances patient monitoring, reduces hospital visits, and supports continuous health tracking, especially for individuals with chronic illnesses and elderly patients.

B. Future Trends

The field of IoT in healthcare is rapidly evolving, and future enhancements to this system can further improve its efficiency, accessibility, and predictive capabilities. The following advancements are proposed:

- **Battery-Powered Wearable Version:**
  The current system, while portable, requires an external power source. Future iterations will incorporate a rechargeable battery-powered module, making it a fully wearable device for continuous, long-term monitoring.
- **AI-Based Predictive Health Analytics**
  By integrating machine learning algorithms, the system can analyze historical health data to detect early signs of critical conditions. AI-based prediction models can improve risk assessment and suggest preventive measures before health deterioration occurs.
- **Cloud-Based Data Storage and Medical Record Integration**
  Future enhancements will involve secure cloud storage for long-term health data logging, allowing doctors to access historical trends and provide better diagnosis. The system could also be linked to electronic health records (EHRs) for direct doctor-patient interaction.
- **Voice-Control and Smart Assistant Integration**
  The addition of Google Assistant, Amazon Alexa, or Siri integration will enable voice-activated monitoring. This feature will allow users to ask for their current SpO_2, heart rate, or temperature levels without needing a mobile app.
- **Multi-Sensor Fusion for Enhanced Monitoring**
  Future versions may incorporate additional biosensors such as ECG (electrocardiogram) sensors, blood pressure sensors, or motion sensors for a comprehensive health monitoring system.
- **Video Consultation and Emergency Alert System**
  The system can be upgraded to include a telemedicine feature, where users can connect with doctors via live video calls in emergencies.

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Additionally, the automatic SOS alert system can notify caregivers or emergency services if the patient's vitals drop to critical levels.

- **IoT Expansion and Remote Monitoring Network** Expanding the project into a multi-patient monitoring system will allow hospitals and care centers to track multiple patients simultaneously, using a centralized IoT dashboard for large-scale health management.

The successful implementation of this IoT-enabled health monitoring system highlights the potential of smart healthcare technologies in enhancing patient safety, reducing medical costs, and improving accessibility. With future advancements, the system can revolutionize telemedicine, predictive diagnostics, and home healthcare, making remote patient monitoring more intelligent, efficient, and widely accessible.

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A Comparative Study of 100 Gbps Photonic and Electrical Interconnects for Network-on-Chip Architectures

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***Abstract*—The rapid growth of data-intensive applications, such as artificial intelligence and high-speed networking, has exposed the limitations of traditional electrical interconnects, including bandwidth saturation, high power consumption, and thermal inefficiencies. Photonic Integrated Circuits (PICs) offer a transformative alternative by leveraging light for data transmission, promising high bandwidth, low latency, and energy efficiency. This paper presents a comprehensive design and simulation of a 100 Gbps (10×10 Gbps) Wavelength-Division Multiplexing (WDM) photonic interconnect and compares its performance with a traditional electrical interconnect. Using Ansys Lumerical for photonic simulations and Ansys Electronics Desktop for electrical simulations, we evaluate key metrics such as bandwidth, latency, power consumption, and signal integrity. The photonic system demonstrates superior performance, achieving a latency of 215 ps and an extinction ratio of 20.23 dB, compared to 550 ps for the electrical system. These findings highlight the potential of PICs for next-generation Network-on-Chip (NoC) architectures and pave the way for hybrid photonic-electronic systems.**

***Index Terms*—Photonic Integrated Circuits, Wavelength-Division Multiplexing, Network-on-Chip, Electrical Interconnects, Ansys Lumerical, Signal Integrity**

I. Introduction

The exponential growth in data-intensive applications, such as artificial intelligence (AI), cloud computing, and ultra-high-definition (UHD) media streaming, has significantly increased the demand for high-performance interconnect systems. Traditional copper-based electrical interconnects face critical limitations, including bandwidth bottlenecks, high power consumption, and thermal inefficiencies, exacerbated by the saturation of Moore's Law [7]. These constraints hinder scalability and performance in modern computing architectures, necessitating innovative solutions.

Photonic Integrated Circuits (PICs) have emerged as a promising alternative, utilizing photons for data transmission instead of electrons. PICs offer ultra-high bandwidth, low latency, immunity to electromagnetic interference (EMI), and reduced signal attenuation [1]. This paper presents a detailed design and simulation of a 100 Gbps (10×10 Gbps) WDM-based photonic interconnect, modeled using Ansys Lumerical, and compares its performance with a traditional electrical interconnect simulated in Ansys Electronics Desktop. The study evaluates key performance indicators (KPIs) such as bandwidth, latency, power efficiency, and signal integrity to quantify the advantages of photonic systems.

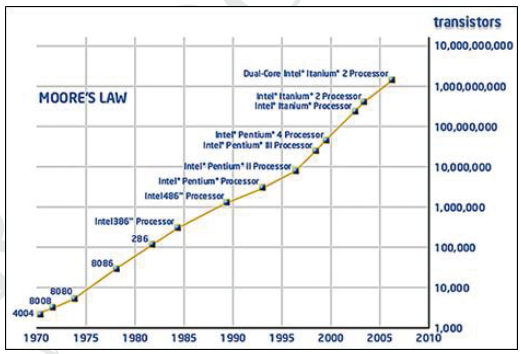


Fig. 1: Moore's Law illustrating the slowing of transistor scaling.[1]

The objective is to establish the viability of PICs for Network-on-Chip (NoC) architectures, addressing the limitations of electrical interconnects and providing a foundation for hybrid photonic-electronic systems. The paper is organized as follows: Section II reviews related work, Section III defines the problem and proposed solution, Section IV details the methodology and implementation, Section V presents simulation results, Section VI discusses future trends and conclusions, and the final Section lists references.

II. Literature Survey

Recent advancements in photonic interconnects highlight their potential to address the limitations of electrical systems. Shi et al. [1] reviewed silicon photonics for high-capacity data communications, emphasizing components like microring modulators and wavelength-division multiplexers. They noted challenges in on-chip laser integration due to silicon's indirect bandgap, proposing heterogeneous III-V laser integration. Chen and Joshi [2] introduced dynamic laser power control in photonic NoC architectures, achieving significant throughput improvements. Bykhovsky

and Arnon [3] explored unguided optical bus interconnects, offering alignment tolerance but facing crosstalk issues. Mekawey et al. [4] discussed slot waveguides for high-density integration, while Bogaerts et al. [5] presented IPKISS for photonic-electronic co-design. Tiwari et al. [6] focused on silicon nitride waveguides for nonlinear photonics, enhancing scalability. These studies underscore the potential and challenges of PICs, forming the basis for this comparative analysis.

III. Problem Analysis and Proposed Solution

A. Problem Definition

The digital era, driven by AI, cloud computing, and real-time analytics, demands interconnects with ultra-high bandwidth, low latency, and minimal power consumption. Electrical interconnects face several limitations:

- **Bandwidth Bottlenecks**: Parasitic effects (resistance, inductance, capacitance) limit high-frequency data transfer.
- **Power and Thermal Load**: High-speed circuits consume significant power, increasing cooling complexity.
- **Latency**: Electrical signal delays impact time-sensitive applications.
- **Scalability**: Miniaturization limits hinder performance as per Moore's Law.

Photonic interconnects address these issues by leveraging light for data transmission, offering high bandwidth, low latency, and EMI immunity. This project aims to design and simulate a 100 Gbps WDM photonic interconnect and compare it with an electrical counterpart, focusing on bandwidth, latency, power, and signal integrity.

B. Proposed Solution

The proposed solution involves a simulation-based comparison of photonic and electrical interconnects. The photonic system, designed in Ansys Lumerical, uses WDM for multi-channel data transmission, while the electrical system, modeled in Ansys Electronics Desktop, employs copper-based transmission lines. Key components and performance metrics are detailed below.

1) Photonic Interconnect Design: The photonic system integrates:

- **Multi-Wavelength Laser Source**: Emits distinct optical carriers at 7 dBm.
- **Mach-Zehnder Modulators (MZMs)**: Convert electrical signals to optical using Non-Return-to-Zero (NRZ) modulation.
- **Optical Multiplexer and Waveguides**: Enable low-loss signal routing with a group index of 3 and 10 dB/m loss.
- **Optical Demultiplexer and Photodetectors**: Separate channels and convert optical signals back to electrical with 0.8 A/W responsivity.

2) Electrical Interconnect Design: The electrical system includes:

- **Copper Transmission Lines**: Modeled with realistic parasitic elements.
- **CMOS Drivers and Receivers**: Handle high-speed signal transmission.
- **Repeater Chain**: Compensates for signal attenuation, adding 100 ps delay per repeater.

3) Performance Metrics: The systems are evaluated based on:

- Bandwidth and Throughput
- Latency
- Power Consumption
- Signal Integrity (Eye Diagram Analysis)
- Scalability and Noise Resilience

IV. Methodology and Implementation

A. Photonic Interconnect Architecture

The photonic interconnect, designed in Ansys Lumerical, implements a 10-channel, 100 Gbps WDM system. The architecture, shown in Fig. 2, includes a transmitter (TX) module with continuous wave lasers (CWLs), MZMs, and a 10x1 WDM multiplexer, connected via waveguides to a receiver (RX) module with a 1x10 demultiplexer and photodetectors.

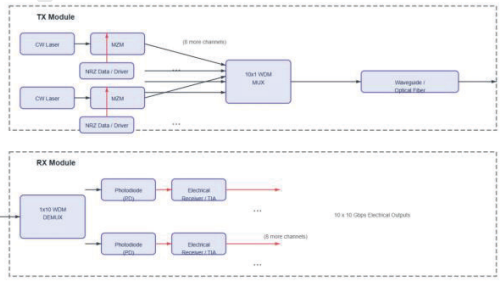


Fig. 2: Block diagram of WDM-based PIC serial data link.

The workflow involves:

1) **Data Generation**: 10 Gbps NRZ signals via Pseudo-Random Binary Sequence (PRBS) generators.
2) **Optical Modulation**: MZMs modulate optical carriers.
3) **Multiplexing**: Combines channels into a single waveguide.
4) **Demultiplexing and Detection**: Separates channels and converts signals to electrical.
5) **Analysis**: Eye diagrams and metrics extracted using MATLAB.

B. Electrical Interconnect Architecture

The electrical interconnect, designed in Ansys Electronics Desktop, uses 10 parallel 10 Gbps channels with copper transmission lines, CMOS drivers, and repeaters. The architecture, shown in Fig. 3, models realistic electrical properties.

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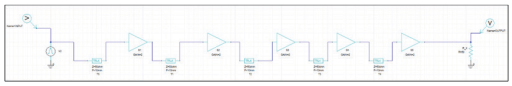


Fig. 3: Single 10 Gbps electrical interconnect.

C. FLow Diagram

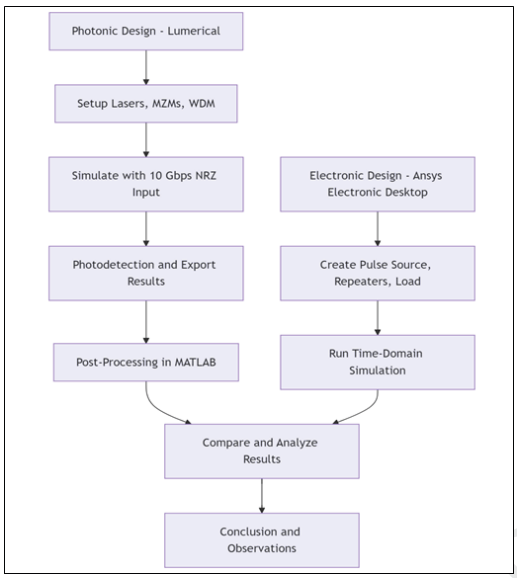


Fig. 4: Flow Chart of the Work Flow and Methodology.

D. Simulation Setup

Both systems are simulated under consistent conditions, with photonic simulations in Ansys Lumerical and electrical simulations in Ansys Electronics Desktop. Oscilloscopes monitor input and output signals, and data is exported for MATLAB-based eye diagram analysis.

V. Results and Discussion

A. Photonic Interconnect Results

The photonic system achieves a total throughput of 100 Gbps across 10 channels. Eye diagram analysis (Fig. 5) reveals robust signal integrity.

TABLE I: Eye Diagram Analysis for 10 Gbps Photonic Channel

Metric	Value	Unit
Signal Type	10 Gbps NRZ	GBPS
Bit Period	100	ps
Eye Height	0.22	mA
Eye Amplitude	2.44	mA
Extinction Ratio	20.23	dB
Q-factor	26.81	–
SNR	31.55	dB
Eye Threshold	1.24	mA
Peak-to-Peak Jitter	104.39	ps
RMS Jitter	17.4	ps

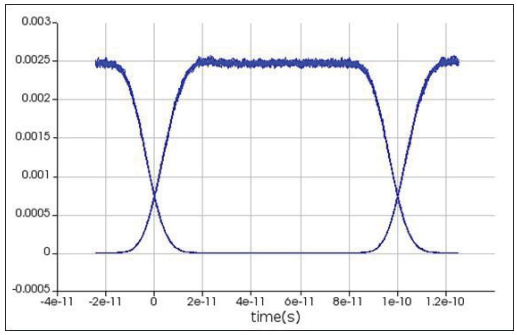


Fig. 5: Eye diagram for 10 Gbps photonic channel.

The system exhibits a latency of 215 ps, measured from input to output rising edges (Fig. 7), and a power consumption of 300 mW.

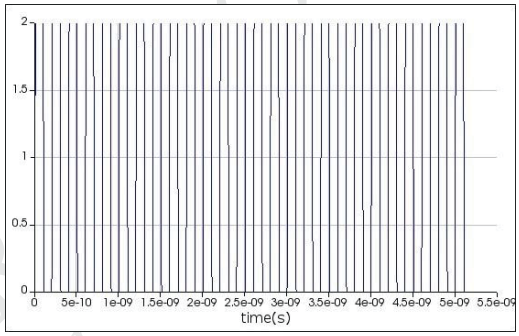


Fig. 6: Input waveform for photonic interconnect.

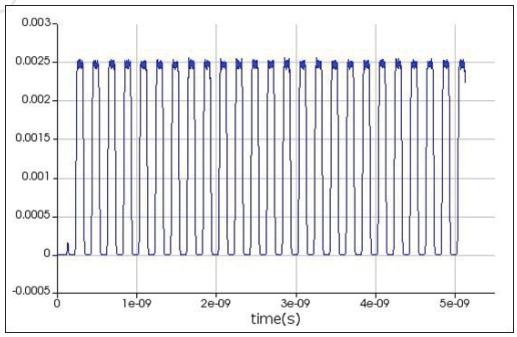


Fig. 7: Output waveform for photonic interconnect.

B. Electrical Interconnect Results

The electrical system achieves 100 Gbps but with a higher latency of 550 ps due to repeater delays (Fig. 8). Power consumption is higher, likely exceeding 300 mW due to amplifiers.

C. Comparative Analysis

The photonic system outperforms the electrical system in latency (215 ps vs. 550 ps), power efficiency,

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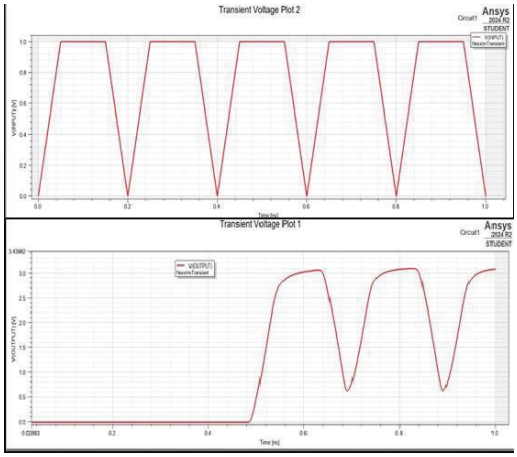


Fig. 8: Transient voltage plots for electrical interconnect.

and signal integrity (higher Q-factor and SNR). However, fabrication complexity remains a challenge for PICs.

VI. Future Trends and Conclusion

A. Conclusion

This study demonstrates the superior performance of a 100 Gbps WDM-based photonic interconnect compared to its electrical counterpart. The photonic system achieves lower latency, higher signal integrity, and better power efficiency, making it ideal for NoC architectures. Challenges in fabrication and CMOS integration persist but are addressable with ongoing advancements.

B. Future Trends

Future developments include:

- Hybrid photonic-electronic integration for seamless NoC designs.
- Advanced WDM for higher channel counts.
- AI-optimized photonic systems for adaptive routing.
- 3D photonic architectures for compact designs.
- Quantum photonics for secure communications.

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SMART DOOR LOCK SYSTEM USING FACIAL RECOGNITION

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***Abstract*—This project proposes a smart and secure door locking system powered by facial recognition technology, offering an innovative solution to modern access control challenges. The system employs the ESP32-CAM module to capture high-quality real-time facial images and perform on-device processing to recognize and authenticate users. By comparing captured facial features with a pre-registered database of authorized individuals, the system grants or denies access without the need for physical keys, PIN codes, or RFID cards. This AI-driven biometric approach significantly enhances security by reducing the risks associated with key duplication, loss, or unauthorized access. The hardware design integrates essential components such as a relay module to operate a solenoid lock, LED indicators for visual feedback, and a voltage regulation circuit using a 7805 IC and capacitors to ensure stable power delivery. The entire system is programmed using the Arduino IDE, providing a flexible platform for code development and debugging. As a cost-effective, contactless, and hygienic alternative to traditional systems, this solution is well-suited for smart homes, office buildings, and other secure environments. Furthermore, the project demonstrates the practical application of embedded systems combined with artificial intelligence, paving the way for future enhancements like cloud storage, mobile app integration, and multi-user access management to improve functionality and scalability.**

1. INTRODUCTION

The Smart Door Lock System using Facial Recognition is an advanced and sophisticated security solution that combines cutting-edge face detection technology with embedded hardware components to establish a smart, automated, and highly secure access control mechanism. At the core of this project lies the ESP32-CAM module, a compact yet powerful device that captures high-quality, real-time images and processes them locally to perform accurate facial recognition. The system works by verifying an individual's identity through comparison with a pre-registered database of authorized users, enabling it to grant or deny access based on distinctive and unique facial features. This biometric authentication method offers a significantly enhanced level of security when compared to traditional methods such as mechanical keys, PIN codes, or RFID cards, all of which are more vulnerable to loss, theft,duplication, or misuse. The hardware configuration of the system includes a relay module, which functions as an electronic switch to control a 12V solenoid lock, facilitating the secure locking and unlocking of doors. To ensure user awareness and interaction, LED indicators are employed to visually display the system's status — such as access granted, access denied, or system readiness — thereby improving usability. A 12V battery or DC power source is used, and the voltage is stepped down to a regulated 5V using a 7805 voltage regulator and a 100µF capacitor, ensuring stable and safe power delivery to all connected electronic components. The circuit is constructed on a breadboard, which not only aids in rapid prototyping and testing but also offers flexibility for future upgrades or modifications. The system's software and control logic are managed through the Arduino IDE, which provides a versatile and user-friendly platform for writing, uploading, and debugging code that governs both the face detection algorithms and the overall hardware operation. This AI-enabled solution is not only robust and secure but also affordable and highly customizable, making it ideal for a variety of applications including smart homes, office premises, and other restricted-access environments. By eliminating the need for physical keys, cards, or manual entry systems, this project promotes a contactless, hygienic, and seamless user experience, which is especially valuable in today's increasingly touch-free world. Furthermore, this project successfully demonstrates the practical fusion of artificial intelligence with embedded systems, showcasing its real-world utility. It also provides a strong foundation for future development, such as cloud integration, mobile app-based control, multi-user database support, and scalability for larger infrastructures.

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2. PROBLEMS ANALYSIS & SOLUTION

A. Problem Definition

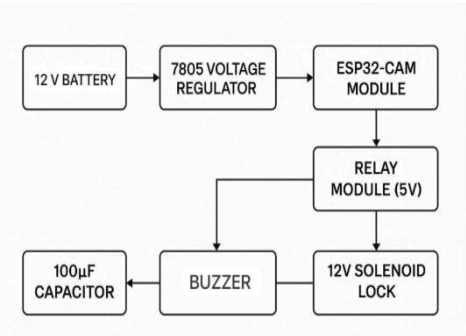
Conventional door locking systems, such as mechanical keys, PIN codes, and RFID-based access cards, are widely used for residential and commercial security. However, these traditional methods have significant drawbacks including susceptibility to loss, theft, duplication, and unauthorized access. Keys can be misplaced or stolen, PINs can be forgotten or easily observed, and RFID cards can be cloned. Furthermore, these systems typically require physical contact or manual input, which is not ideal in a post-pandemic world where contactless solutions are increasingly preferred for hygiene and convenience.There is a growing need for an intelligent, secure, and contactless access control system that minimizes human error and enhances user convenience while maintaining a high level of security. This calls for a modernized approach that leverages biometric authentication and embedded technology to overcome the limitations of traditional locking mechanisms.

B. Proposed Solution

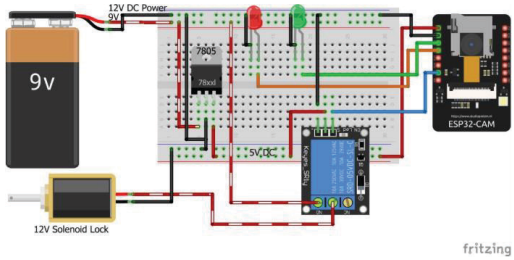
To address the limitations of conventional locking systems, this project proposes a Smart Door Lock System using Facial Recognition. The system uses the ESP32-CAM module to capture real-time facial images and perform local face recognition to verify users. By comparing live facial data with a pre-registered database, the system can accurately identify authorized individuals and control door access accordingly.The locking mechanism is managed using a relay module that operates a solenoid lock, enabling secure physical locking and unlocking. LED indicators provide real-time visual feedback, displaying access status (granted/denied/system ready). A regulated power supply (using a 7805 voltage regulator and capacitors) ensures consistent and safe operation of all components.Programming is done using the Arduino IDE, which supports face detection, user authentication, and control logic. The system is cost-effective, customizable, and scalable, making it suitable for applications in smart homes, offices, and secure facilities.

3. METHODOLOGY & IMPLEMENTATION

A. Block Diagram



B. Pictorial Representation



4. RESULTS & DISCUSSION

The development of the Smart Door Lock System using Facial Recognition has progressed through several critical stages. The ESP32-CAM module has been successfully programmed with the facial recognition firmware using the Arduino IDE. After flashing the code, the ESP32-CAM operates independently, eliminating the need for a constant USB connection to a laptop. Once powered via the regulated 5V supply (stepped down from 12V), the module establishes a Wi-Fi connection, allowing users to access the live camera stream through a browser using the IP address displayed in the serial monitor during setup. Initial hardware testing has been carried out to validate the power management circuit, which includes a 7805 voltage regulator and capacitors for smooth voltage output. The relay module is connected and configured to control a 12V solenoid lock based on recognition results. A buzzer has been used in place of a visual LED indicator to signal system power status, confirming that the ESP32-CAM is receiving stable power.

Preliminary integration tests between software and hardware components have shown positive results. Once the IP address is entered into a browser, the camera stream is accessible, and the face recognition interface becomes available. Although the complete automation of the locking mechanism based on recognition output is still under refinement, the foundational structure is functional.

Currently, work is focused on optimizing the power supply to the ESP32-CAM, as
inconsistencies in power delivery can cause reboot issues or unstable connections. Debugging is underway to ensure reliable voltage regulation and stable operation. Once resolved, the system will proceed to the final testing phase, including
adding multiple faces to the recognition database and validating the locking/unlocking process under real-time conditions.

This stage marks significant progress toward achieving a fully operational, AI-driven smart locking system, showcasing the feasibility and efficiency of integrating facial recognition with embedded hardware for real-world security applications.

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5. FUTURE TRENDS & CONCLUSION

A. Conclusion

The Smart Door Lock System using Facial Recognition offers a secure, automated, and user-friendly approach to modern access control. By leveraging the capabilities of the ESP32-CAM and integrating it with a relay-controlled solenoid lock, the system ensures identity-based access without the need for physical keys. The design highlights the powerful synergy between AI and embedded systems, offering significant improvements over traditional security mechanisms. With future advancements in edge computing, IoT, and biometric technologies, this system can be further developed into a more intelligent, scalable, and comprehensive security solution for both residential and commercial applications. Ultimately, it represents promising step toward smarter and safer environments.

B. Future Trends

As technology continues to evolve, facial recognition-based smart security systems are expected to become more intelligent, secure, and accessible. Some anticipated trends include:

- Edge AI Enhancements: Integration of more powerful edge AI processors to enable faster and more accurate recognition without reliance on cloud computing.
- Cloud Integration: Real-time cloud syncing for access logs, user management, and remote monitoring via web and mobile apps.
- Multi-Modal Biometric Authentication: Combining facial recognition with voice recognition or fingerprint scanning to further strengthen access control.
- IoT Ecosystem Integration: Seamless interaction with other smart devices (lights, alarms, CCTV) for enhanced home automation and situational awareness.
- Energy-Efficient Designs: Optimized power consumption through sleep modes, energy-aware components, and solar-powered systems.
- AI-Based Spoof Detection: Advanced algorithms to detect and prevent unauthorized access through photos, videos, or masks.
- Scalability for Large-Scale Use: Enhanced systems suitable for apartment complexes, office buildings, and public institutions.

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DESIGN OF 32-BIT PIPELINED RISC V ISA BASED PROCESSOR WITH VEDIC MULTIPLIER

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***Abstract*—The development of a 32-bit pipelined processor based on the RISC-V ISA architecture, integrated with a Vedic multiplier, represents a notable leap in computational efficiency.**

RISC-V's open-source and modular design has become a cornerstone in modern industry, fostering innovation and flexibility across diverse applications. This project utilizes the ancient *Urdhva Tiryakbhyam* Vedic multiplication technique, incorporating hierarchical modules (2x2, 4x4, 8x8, 16x16, and 32x32) with Kogge Stone adders serving as intermediate adders. By integrating this sophisticated Vedic multiplier within the RISC-V pipeline, the design improves parallelism in computation of large bit multiplication operation. This project serves as an educational endeavor to grasp the fundamentals of the RISC-V architecture and the core concepts involved in computer architecture (CA). Additionally, it provides insights into Vedic multipliers, highlighting their efficiency and applicability in modern computational designs.

Keywords—RISC-V ISA, Pipelined Processor, Vedic Multiplier, Kogge Stone Adder, Parallel Computation

I. INTRODUCTION

A. RISC-V Architecture

Processor architectures have historically been dominated by **x86** and **ARM**, each excelling in specific domains. **x86**, with its complex instruction set computing (**CISC**) design, is widely adopted in high-performance computing environments, offering robust processing capabilities and an extensive software ecosystem. **ARM**, in contrast, leverages a reduced instruction set computing (**RISC**) approach, emphasizing power efficiency, making it the architecture of choice for mobile and embedded systems.

RISC-V, an open-source **RISC** architecture, introduces a paradigm shift by offering a modular and customizable instruction set. Unlike proprietary architectures, RISC-V enables developers to tailor processor designs without licensing constraints, fostering innovation in both academia and industry. The streamlined instruction set enhances computational efficiency, reducing power consumption while maintaining flexibility. This adaptability is driving its adoption across various high-performance and embedded applications.

One of the key architectural strengths of RISC-V lies in **pipelining**, which enhances efficiency compared to single-cycle and multi-cycle architectures. In a **single-cycle architecture**, all instructions execute within one clock cycle, leading to inefficiencies due to varying instruction execution times. **Multi-cycle architectures** improve performance by breaking down instructions into multiple cycles but still execute instructions sequentially, limiting throughput. **Pipelining**, however, divides execution into multiple stages, allowing simultaneous processing of different instructions at different stages. This technique significantly boosts computational speed by optimizing resource utilization and minimizing idle times.

B. Vedic Multiplier

Multiplication is a critical operation in digital processors, influencing overall performance. Traditional multipliers, such as **array multipliers** and **Booth multipliers**, face challenges related to complexity, power consumption, and speed. The **Vedic multiplier**, derived from ancient Indian mathematics, provides an efficient alternative.

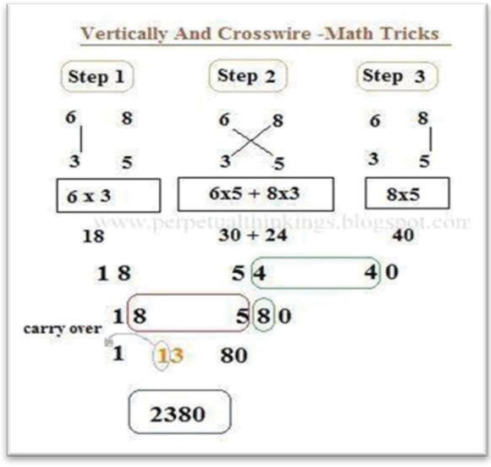


Figure 1.1 Urdhva Tiryakbhyam Algorithm (Vertically and Crosswise)

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Based on the **Urdhva Tiryakbhyam** ("vertical and crosswise") algorithm, the Vedic multiplier breaks multiplication into smaller steps processed in parallel. Its hierarchical design—scaling from **2×2** to **32×32** modules—reduces intermediate calculations and carry propagation delays, leading to faster execution and lower power consumption. These characteristics make it highly suitable for modern energy-efficient processor designs.

C. Kogge-Stone Adders

Adders are fundamental in processor arithmetic, and their design directly affects computational speed. Traditional **ripple carry adders** suffer from slow carry propagation due to their sequential nature. **Carry look-ahead adders** improve speed by computing carry signals in parallel but introduce increased complexity and area overhead.

The **Kogge-Stone adder (KSA)** provides an optimal balance by using a parallel prefix structure to compute carry signals in logarithmic time. This significantly reduces addition delays, making **KSA** highly scalable for modern high-speed processors. When integrated into the **Vedic multiplier**, **KSA** enhances performance by ensuring low-latency addition, creating a powerful arithmetic unit optimized for both speed and energy efficiency.

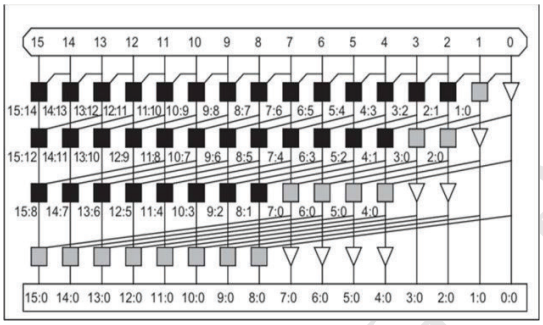


Figure 1.2 Urdhva Tiryakbhyam Algorithm (Vertically and Crosswise)

II. Literature survey

The foundation of this research is based on the work of **Girish et al. [1]**, which presents the design and validation of a **32-bit RISC-V processor incorporating Vedic mathematics**. This processor employs a Vedic multiplier architecture to enhance computational speed and efficiency while reducing power consumption and complexity. The **Arithmetic Logic Unit (ALU)** and **Multiply-Accumulate (MAC)** units leverage Vedic Sutras, implemented in **Verilog HDL** and simulated using the **Xilinx Design Suite**, demonstrating lower latency and area utilization compared to conventional designs.

Expanding on this, **Chugh and Singh [2]** provide a comprehensive review of **N-bit Vedic multipliers**, discussing their hardware implementations using **CMOS and Quantum Dot Cellular Automata (QCA)**. Their study highlights the transition from **CMOS** to **QCA**, which promises improvements in speed and power efficiency.

Similarly, **Vamsi and Ramesh [3]** focus on optimizing MAC operations by implementing an **8-bit Vedic multiplier with a carry-save adder**, showing reductions in power consumption and computational delay.

Further, **Gupta et al. [4]** introduce a **squaring technique using Vedic mathematics**, improving computational efficiency by simplifying two-digit number squaring. **Lavanya and Pradhan [5]** propose a **16-bit RISC processor with a Vedic multiplier and a hybrid adder**, demonstrating improved speed and reduced area usage. Lastly, **Teja et al. [6]** compare **Vedic multipliers using different adders**, concluding that a **Sklansky adder** provides superior speed, albeit with a slight increase in area utilization.

This literature survey establishes that integrating **Vedic multipliers** into **RISC-V architectures** offers significant advantages in **speed, power efficiency, and computational complexity**, forming the basis for further optimization and implementation in modern digital processors.

III. Problem analysis and objectives

A. Problem definition

While RISC-V offers a more customizable and efficient option compared to other processors, standard multicycle implementations still suffer from higher clock cycle requirements for complex arithmetic operations. Additionally, conventional arithmetic logic units (ALUs) and other processing blocks are not optimized for rapid computation, leading to performance limitations. This project highlights the need for enhancements that leverage Vedic mathematical techniques to improve efficiency of the conventional multiply and accumulate (MAC) block within RISC-V processors by implementing a pipelined RISC-V processor with a Vedic multiplier block integrated.

B. Objectives

- Design and Implementation: The project proposes the design and implementation of a pipelined RISC-V ISA-based processor integrated with a custom Vedic multiplier. By incorporating Vedic mathematics algorithms into the processor's computation methods, the project aims to enhance the efficiency and speed of multiplication operations within the processor.

- Optimization through Vedic Mathematics: The solution involves developing a processor architecture that accommodates Vedic math algorithms. Traditional multiplication units will be replaced with Vedic math-inspired blocks that leverage simplified algorithms for arithmetic computations, resulting in faster execution times and reduced resource utilization.

- Integration of Kogge Stone Adders: To further enhance the performance of the custom processor, Kogge Stone adders will be utilized as intermediate adders within the Vedic multiplier. Kogge Stone adders offer significant speed improvements over traditional ripple carry and carry look-ahead adders, ensuring rapid and reliable computation.

- Implementation with AMD Vivado and Quartus prime lite with Modelsim altera: The implementation will be conducted using Xilinx Vivado and Quartus prime lite with Modelsim altera, focusing on synthesis, simulation, and

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verification of the custom processor design at the hardware level. This software allows for comprehensive development and testing of the processor design, ensuring accuracy and efficiency.

IV. METHODOLOGY

A. Vedic Multipliers

The Urdhva Tiryakbhyam algorithm is chosen for implementing multiplication using a vertically crosswise method, introducing more parallelism into the multiplier circuitry. Structural design is followed for 2x2, 4x4, 8x8, 16x16, and 32x32 Vedic multipliers, ensuring efficient computation.

2x2 Vedic Multiplier

The 2x2 Vedic multiplier computes the product of two 2-bit numbers using four AND gates and two half adders. Inputs are represented as A0, A1 and B0, B1, while outputs are P0, P1, P2, and P3. Partial products are generated using AND gates, and half adders sum them efficiently. This design simplifies multiplication operations and is synthesized in Vivado to evaluate speed and power consumption.

4x4 Vedic Multiplier

The 4x4 Vedic multiplier extends the 2x2 design by using four 2x2 multipliers. The inputs consist of two 4-bit numbers, A3 to A0 and B3 to B0. The outputs from the 2x2 multipliers are summed using a Kogge-Stone adder, optimizing carry propagation. The design is synthesized and simulated in Vivado, showing reduced delay and power consumption compared to traditional multiplication techniques.

8x8 Vedic Multiplier

The 8x8 Vedic multiplier follows the same hierarchical approach, employing four 4x4 Vedic multipliers. The inputs are defined as A7 to A0 and B7 to B0. Partial products generated by the 4x4 multipliers are summed using an 8-bit Kogge-Stone adder, further enhancing speed and efficiency. Vivado synthesis and simulation validate its functionality and performance.

16x16 Vedic Multiplier

The 16x16 Vedic multiplier is constructed using four 8x8 Vedic multipliers. The inputs are defined as A15 to A0 and B15 to B0. The summation process employs a combination of Kogge-Stone and Carry Select adders to optimize speed. The outputs are arranged in a structured matrix format, ensuring efficient computation. Vivado simulations confirm improved performance in terms of delay and power consumption.

32x32 Vedic Multiplier

The 32x32 Vedic multiplier is built from four 16x16 Vedic multipliers. The inputs are represented as A31 to A0 and B31 to B0. The summation process integrates Kogge-Stone and Carry Select adders, ensuring high-speed computation. The structured approach reduces delay significantly, making it well-suited for FPGA implementation. Vivado simulations verify its superior efficiency compared to conventional multiplication techniques.

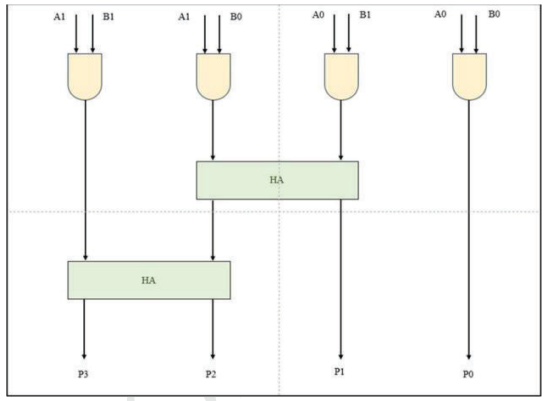


Figure 4.1 Block diagram representation of 2x2 Vedic multiplier

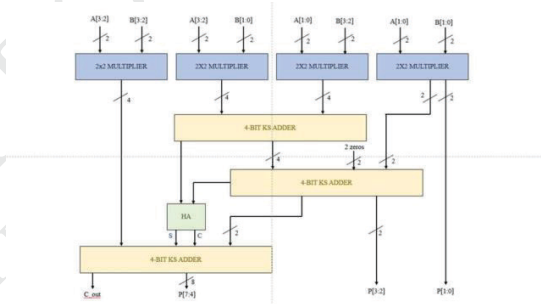


Figure 4.2 Block diagram representation of 4x4 Vedic multiplier

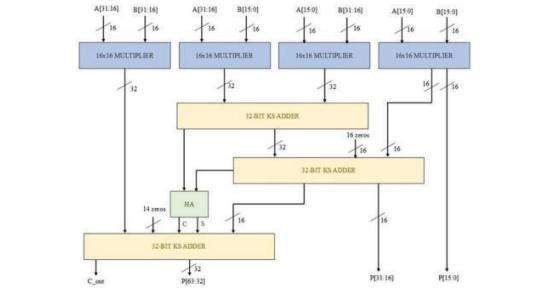


Figure 4.3 Block diagram representation of 32x32 Vedic multiplier

B. Kogge-Stone Adders

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Introduction

The RISC-V pipelined processor in this project incorporates a Vedic multiplier, which relies on intermediate adders for efficient operation. The Kogge-Stone Adder is chosen due to its high-speed carry propagation properties. The analysis begins with fundamental adder circuits, progressing to parallel-prefix adders.

Half Adder

The half adder performs binary addition of two inputs, A and B, producing a sum and a carry-out. The sum is calculated using XOR logic, while the carry-out is determined using AND logic. This basic building block is essential for constructing larger arithmetic circuits.

Full Adder

The full adder extends the half adder by incorporating a carry-in input. It calculates the sum and carry-out using XOR and AND-OR logic operations. Full adders enable multi-bit addition by cascading multiple instances together.

Generate and Propagate Logic

Efficient addition circuits make use of generate (G) and propagate (P) signals:

- Generate: $G = A \cdot B$

- Propagate: $P = A \oplus B$

These signals simplify carry computations in more advanced adders by determining if a carry is generated or propagated through each bit.

Group Carry and Propagate (Prefix Operators)

Group generate and propagate expressions allow recursive computation of carry signals across multiple bits:

- Group Generate: $G_{i:j} = G_{i:k} + (P_{i:k} \cdot G_{k-1:j})$

- Group Propagate: $P_{i:j} = P_{i:k} \cdot P_{k-1:j}$

These expressions are fundamental in parallel-prefix adders, reducing addition delays through hierarchical carry computation.

Kogge-Stone Adder

The Kogge-Stone Adder (KSA) is a high-speed parallel-prefix adder known for its minimal carry propagation delay and balanced fan-out. Its stages include:

1. Compute bitwise generate and propagate signals:
   - $G_i = A_i \cdot B_i$
   - $P_i = A_i \oplus B_i$
2. Recursively compute prefix generate and propagate signals:
   - $G_{i:j} = G_{i:k} + (P_{i:k} \cdot G_{k-1:j})$
   - $P_{i:j} = P_{i:k} \cdot P_{k-1:j}$
3. Compute the sum:
   - $S_i = P_i \oplus C_{i-1}$

The KSA structure significantly reduces delay by parallelizing carry computation.

Kogge-Stone adders are known for their high speed, scalability, and reduced fan-out, making them well-suited for large bit-width applications. They use a parallel prefix computation structure, allowing for faster carry propagation at the cost of increased hardware complexity. In contrast, ripple carry adders (RCA) are simpler but experience linear delay growth with the number of bits due to sequential carry propagation.

The delay of the **Kogge-Stone (KS) adder** is given by:

$$t_{tree} \approx t_{pg} + \lceil \log_2(N) \rceil * t_{AO} + t_{xor}$$

Here, the logarithmic dependency on the bit width `N` results in significantly reduced propagation delay compared to the RCA.

The delay of the **Ripple Carry Adder (RCA)** is given by:

$$t_{ripple} = t_{pg} + (N - 1) * t_{AO} + t_{xor}$$

Since carry ripples through every bit position, the delay increases linearly with `N`, making it slower for large bit-width operations.

Quantitative Analysis for 32-bit Adders

For a **32-bit Kogge-Stone Adder:**

$$t_{tree} \approx t_{pg} + \lceil \log_2(32) \rceil * t_{AO} + t_{xor}$$

Since $\lceil \log_2(32) \rceil = 5$,

$$t_{tree} \approx t_{pg} + 5 * t_{AO} + t_{xor}$$

For a **32-bit Ripple Carry Adder:**

$$t_{ripple} = t_{pg} + 31 * t_{AO} + t_{xor}$$

Speed Comparison

To compare the speed of both adders, the ratio of their delays is given by:

$$t_{ripple} / t_{tree} = (t_{pg} + 31 * t_{AO} + t_{xor}) / (t_{pg} + 5 * t_{AO} + t_{xor})$$

For large values of t_{xor}, the Kogge-Stone adder is approximately **6 times faster** than the ripple carry adder for a 32-bit operation, due to its logarithmic complexity versus the linear complexity of the RCA.

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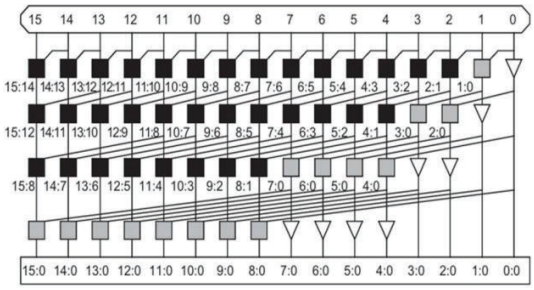


Figure 4.4 Tree diagram of PG network of a Kogge Stone Adder

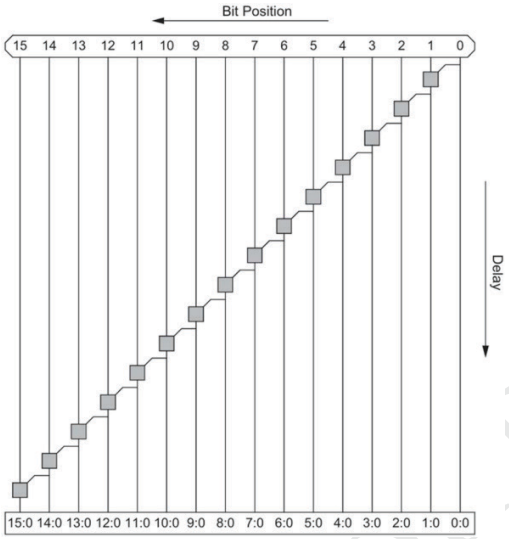


Figure 4.4Tree diagram of PG network of a Ripple Carry Adder

C. RISC V processor

This section outlines a step-by-step methodology for designing a RISC-V processor, integrating a 32x32 Vedic multiplier into a pipelined architecture. The approach is structured into distinct phases: developing a single-cycle RISC-V processor, extending it to a pipelined version, and incorporating the Vedic multiplier as a custom instruction. Each phase is described comprehensively to highlight the key design principles, challenges, and solutions involved.

Development of a 32-bit Single-Cycle RISC-V Processor

The first stage in the project involved designing a basic 32-bit single-cycle RISC-V processor. A single-cycle processor completes an entire instruction, including fetching, decoding, executing, memory access, and writing back the result, in one clock cycle.

Instruction Set Architecture (ISA)

The RISC-V ISA forms the foundation of the processor design. For this phase, the RV32IM base Integer instruction set and M instruction (mul, mulh, mulhu) was implemented. The architecture includes instructions for arithmetic, logical operations, load/store, and control flow.

Microarchitecture Components

Key components of the single-cycle processor include:

- Instruction Memory: Responsible for fetching the next instruction from memory.
- Control Unit: Decodes the instruction and generates control signals.
- ALU (Arithmetic Logic Unit): Performs arithmetic and logical operations.
- Data memory: Handles data memory read and write operations.
- Register File: Contains general-purpose registers used by the instructions.

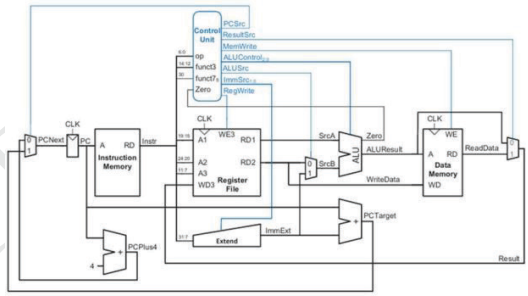


Figure 4.5 Complete single cycle RISC-V processor

Control Unit Design

The control unit generates signals to manage data paths based on opcode and function fields. A finite state machine approach was used to derive control signals for various instruction types.

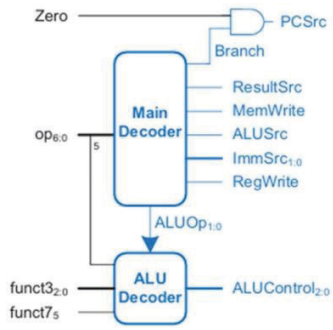


Figure 4.6 Single cycle control processor unit

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Extension to a Pipelined RISC-V Processor

The next phase involved transforming the single-cycle design into a pipelined architecture to improve performance by overlapping instruction execution stages.

Pipelined RISC-V processors offer significant advantages over single-cycle implementations by enhancing processing efficiency and throughput. In a pipelined architecture, instruction execution is divided into five distinct stages—fetch, decode, execute, memory access, and write-back—allowing multiple instructions to be processed simultaneously. This parallelism reduces the overall execution time and increases the number of instructions completed per clock cycle. In contrast, single-cycle processors complete each instruction in a single clock cycle, which can lead to inefficiencies, especially for complex operations that require multiple sub-operations. Additionally, pipelining helps to optimize resource utilization and improve performance through techniques like data forwarding and branch prediction, addressing potential hazards that may arise during instruction execution. Overall, the pipelined RISC-V architecture provides a more scalable and efficient solution for modern computing needs.

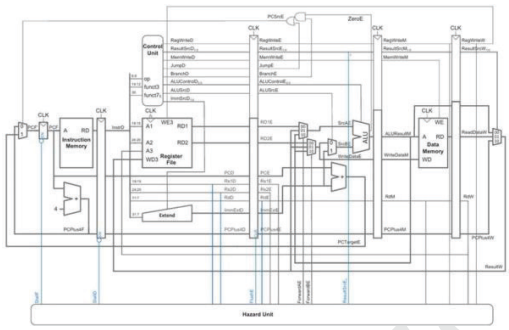


Figure 4.7 Pipelined processor with full hazard control

The cycle time of a single-cycle RISC-V processor is determined by the longest instruction delay, as every instruction completes execution in one clock cycle. The total cycle time must account for the slowest stage, making it inefficient for instructions with shorter execution times. The cycle time for a single-cycle processor is given by:

```
T_c_single = t_pcq + t_mem + t_setup +
max [t_RFread, t_dec + t_ext + t_mux] +
t_ALU + t_mem + t_mux + t_RFsetup
```

Each instruction in a single-cycle processor goes through multiple stages: fetching from the instruction memory, reading registers, executing in the ALU, accessing memory, and writing back results. Since all these operations occur within one clock cycle, simple instructions like register-to-register operations take the same time as complex memory-accessing instructions, leading to inefficiency.

A pipelined RISC-V processor divides execution into multiple stages, allowing simultaneous execution of different instructions at various stages. This reduces the effective instruction execution time and increases throughput. The cycle time for a pipelined processor is determined by the slowest pipeline stage and is given by:

```
T_c_pipelined = max [t_pcq + t_mem +
t_setup, 2(t_RFread + t_setup), t_pcq +
4t_mux + t_ALU + t_AND_OR + t_setup, t_pcq
+ t_mem + t_setup, 2(t_pcq + t_mux +
t_RFsetup)]
```

The pipeline consists of five stages: instruction fetch, decode, execute, memory access, and writeback. Each stage works on different instructions in parallel, significantly reducing the execution time per instruction. However, pipelining introduces additional complexities due to hazards. Data hazards arise when an instruction depends on the result of a previous one, requiring forwarding techniques. Control hazards occur due to branching, which disrupts the pipeline flow and necessitates branch prediction. Structural hazards may also arise when different instructions compete for the same hardware resources, potentially causing stalls.

While a single-cycle processor is simpler to design, its inefficiency in handling varying instruction delays makes it unsuitable for high-performance applications. The pipelined processor, despite its complexity, provides better performance by executing multiple instructions concurrently, making it ideal for computationally intensive workloads.

Integration of Vedic Multiplier Instruction into RISC-V Processor

The integration of a Vedic multiplier instruction into a RISC-V processor involves several key steps to enhance the processor's arithmetic capabilities, particularly for multiplication operations.

1. Refer to ISA for M Extension

The first step is to ensure compliance with the RISC-V Instruction Set Architecture (ISA) M extension, which defines the standard for multiplication and division instructions. This ensures that the new Vedic multiplier instruction aligns with existing RISC-V operations and maintains compatibility with other components of the architecture.

2. Edit Main Decoder

Next, modifications are made to the main instruction decoder. This involves updating the decoder logic to recognize new multiplication instructions associated with the Vedic multiplier. The decoder must be able to differentiate between standard instructions and those that invoke the Vedic multiplier, ensuring proper instruction execution flow.

3. Edit ALU Decoder

The ALU (Arithmetic Logic Unit) decoder also requires updates. This step includes adding pathways that facilitate the execution of multiplication operations using the Vedic multiplier. By integrating these pathways, the ALU can

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efficiently process multiplication requests without significant delays.

4. Add Vedic Multiplier in ALU

The core integration involves incorporating the Vedic multiplier into the ALU design. This entails developing the multiplier based on Vedic mathematics for efficient computation. The design must ensure that the Vedic multiplier is accessible for multiplication instructions and can operate seamlessly alongside other arithmetic functions within the ALU.

5. Testing and Validation

After integration, thorough testing is performed to validate functionality. This includes simulating various multiplication scenarios to ensure that the Vedic multiplier operates correctly within the processor's pipeline and interacts appropriately with other components, such as data forwarding and hazard resolution mechanisms.

V. Results and Discussion

The designed 32-bit pipelined RISC-V processor with an integrated Vedic multiplier was functionally verified using three test programs: unsigned multiplication, signed multiplication, and 3×3 matrix multiplication. The testing workflow involved compiling C programs using the RISC-V GCC toolchain, linking them to generate an ELF executable, and converting the binary into a Verilog-compatible hex file. This hex file was loaded into the processor's instruction memory using $readmemh, and execution results were stored in data memory. The disassembled instructions verified that M extension multiplication instructions were correctly integrated. Screenshots of C code, instruction memory, and data memory provided verify the results.

For performance evaluation, a timing analysis was conducted to compare the critical path delays of a 32×32 Array Multiplier (using Ripple Carry Adders) and a 32×32 Vedic Multiplier (using Kogge-Stone Adders). Using Synopsys Design Compiler and SAED32nm_rvt_tt1p05v25c technology, the reported delays were 9.98 ns for the Array Multiplier and 5.68 ns for the Vedic Multiplier, demonstrating a 43% reduction in delay. This improvement is attributed to the logarithmic-depth structure of Kogge-Stone adders, which significantly optimizes addition operations in multiplication. The results confirm that the Vedic multiplier enhances computational speed, making it a preferable choice for high-speed RISC-V architectures.

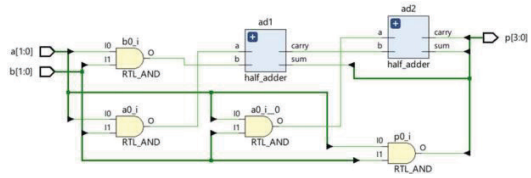


Figure 5.1 Realised schematic of 2x2 vedic multiplier

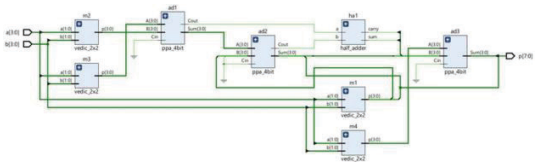


Figure 5.2 Realised schematic of 4x4 Vedic multiplier

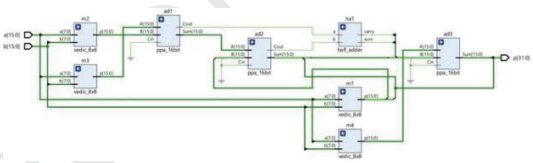
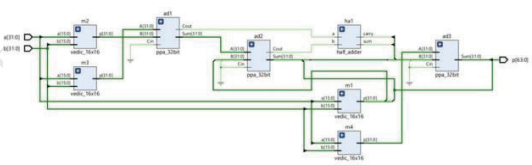
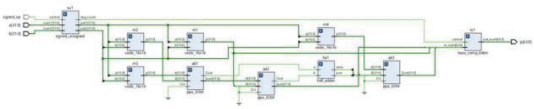


Figure 5.3 Realised schematic of 16x16 Vedic multiplier



(a) unsigned Vedic multiplier



(b) signed Vedic multiplier

Figure 5.4 Realised schematic of 32x32

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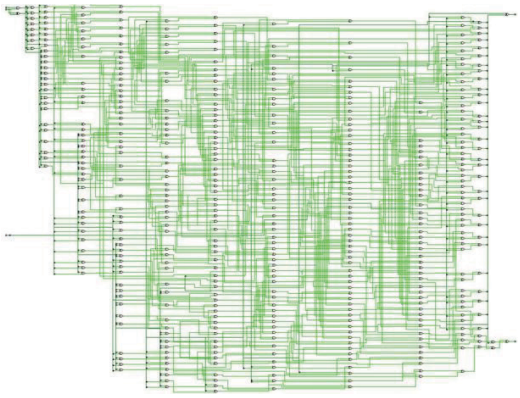


Figure 5.5 Expanded Schematic of 32-bit Kogge Stone (PPA) Adder

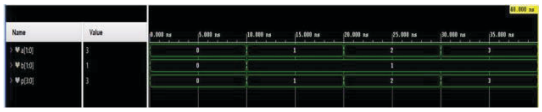


Figure 5.6 Waveform synthesis for 2x2 multiplier testing



Figure 5.7 Waveform synthesis for 4x4 multiplier testing

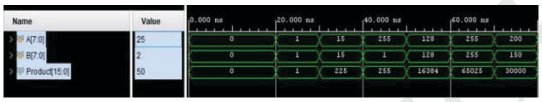


Figure 5.8 Waveform synthesis for 8x8 multiplier testing

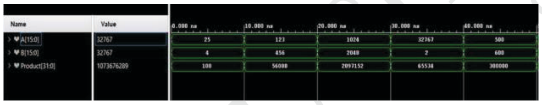


Figure 5.9 Waveform synthesis for 16x16 multiplier testing



Figure 5.10 Waveform synthesis for 32x32 signed multiplier testing

The above figures depict the synthesised RTL schematics and waveform diagrams of 2x2,4x4,8x8,16x16 and 32x32 unsigned and signed Vedic multipliers using AMD Vivado Synthesis tool and Simulation tool.

B. Synthesis and testing of RISC-V processor

The figures below show the schematic diagrams of the developed 32-bit RISC-V processor synthesised using Intel Quartus Prime Lite.

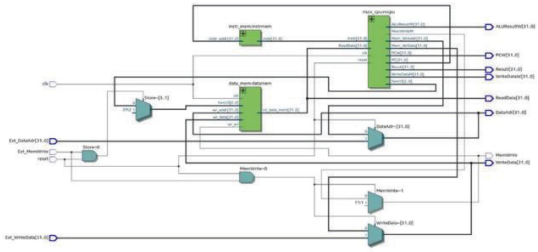


Figure 5.11 Realised Schematic of pipelined RISC-V processor

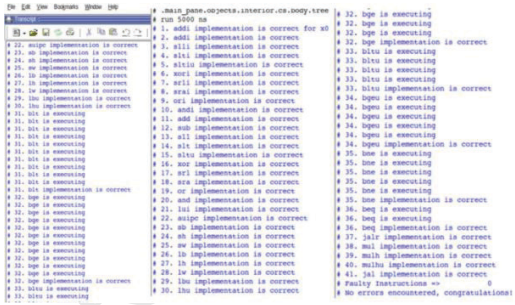


Figure 5.12 Testing and Verification of all instructions in RISC-V 32bit Processor

C. Testing

For testing the designed RISC-V processor with Vedic multiplier, we are using three C code files:

1. For unsigned multiplication
2. For signed multiplication
3. For 3x3 matrix multiplication

Process of compiling and testing a C program on the custom-designed 32-bit RISC-V processor:

Input and Compilation Setup

The script begins by specifying the default input file, multiply.c, and the architecture settings, which include the RISC-V 32-bit instruction set with the M extension (rv32im). The ROM, RAM, and stack sizes are defined to constrain the binary's memory usage. Compilation flags (CFLAGS) and linking flags (LDFLAGS) are set to optimize for size, enable the M extension, and use the minimal runtime library (picolibc).

Compilation

The input C code is compiled into an object file using the RISC-V GCC toolchain. The compilation step includes optimization, debugging symbols, and enabling integer-only printf and scanf functionality for a minimal footprint.

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Linking

The object file is linked to create an ELF executable. The linking process includes specifying memory layout (flash, RAM, and stack) and using linker options to reduce the binary size by discarding unused sections.

Disassembly and Source Inspection

The ELF file is disassembled into a human-readable .lss file using objdump. This disassembly includes the source code as comments, helping inspect the generated instructions and verify that M extension instructions (used for multiplication) are correctly integrated.

Binary Conversion

The ELF file is converted into a binary file and truncated to the specified ROM size. This ensures the binary fits within the memory constraints of the processor.

Verilog Hex Conversion

The binary is further converted into a Verilog-compatible hexadecimal format (program.hex). This file can be loaded into the memory of the RISC-V processor for simulation or testing purposes.

Size Display

The script displays the size of the ELF file to ensure it meets the memory requirements.

Cleanup and Completion

Temporary files generated during the process are deleted to maintain a clean workspace. If successful, the script confirms the creation of program.hex and program.lss. If an error occurs, it outputs a failure message.

This workflow efficiently compiles and tests a program on the custom RISC-V processor, ensuring that the integrated Vedic multiplier is functional and compliant with the M extension.

```c
#include <stdint.h>

#define A (* (volatile uint32_t * ) 0x02000000)
#define B (* (volatile uint32_t * ) 0x02000004)
#define RESULT (* (volatile uint64_t * ) 0x02000008)

int main() {
    // Test integers for multiplication (32-bit)
    A = 123456789; // First 32-bit number
    B = 987654321; // Second 32-bit number

    // Perform multiplication using the 'M' extension (RISC-V hardware multiplier)
    RESULT = (int64_t)A * (int64_t)B;

    return 0;
}
```

Figure 5.12 C code for testing unsigned 32-bit multiplication.

```
Disassembly of section .text:

00000054 <main>:
    ### #define B (* (volatile uint32_t * ) 0x02000004)
    ### #define RESULT (* (volatile uint64_t * ) 0x02000008)
    ###
    ### int main() {
    ###     // Test integers for multiplication (32-bit)
    ###     A = 123456789; // First 32-bit number
  54:   075bd737            lui x14,0x75bd
  58:   020007b7            lui x15,0x2000
  5c:   d1570713            addi    x14,x14,-747 # 75bcd15 <__global_pointer$+0x55bc515>
  60:   00e7a023            sw  x14,0(x15) # 2000000 <__bss_end>
    ###     B = 987654321; // Second 32-bit number
  64:   3ade7737            lui x14,0x3ade7
  68:   8b170713            addi    x14,x14,-1871 # 3ade68b1 <__global_pointer$+0x38de60b1>
  6c:   00e7a223            sw  x14,4(x15)
    ###
    ###     // Perform multiplication using the 'M' extension (RISC-V hardware multiplier)
    ###     RESULT = (int64_t)A * (int64_t)B;
  70:   0007a583            lw  x11,0(x15)
  74:   0047a703            lw  x14,4(x15)
    ###
    ###     return 0;
    ### }
  78:   00000513            addi    x10,x0,0
    ###     RESULT = (int64_t)A * (int64_t)B;
  7c:   02e58633            mul x12,x11,x14
  80:   02e5b6b3            mulhu   x13,x11,x14
  84:   00c7a423            sw  x12,8(x15)
  88:   00d7a623            sw  x13,12(x15)
    ### }
  8c:   00008067            jalr    x0,0(x1)

00000090 <_set_tls>:
  90:   00050213            addi    x4,x10,0
  94:   00008067            jalr    x0,0(x1)
```

Figure 5.13 LSS file generated for 32-bit unsigned multiplication.

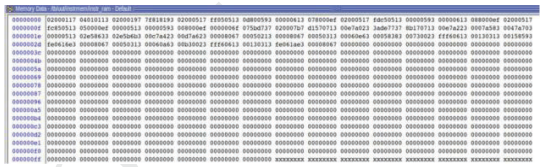


Figure 5.14 Instruction RAM with HEX values of 32-bit unsigned multiplication in RISC-V processor

amem/data_ram - Default

00000000	075bcd15
00000001	3ade68b1
00000002	fbff5385
00000003	01b13114
00000004	xxxxxxxx
00000005	xxxxxxxx
00000006	xxxxxxxx
00000007	xxxxxxxx
00000008	xxxxxxxx
00000009	xxxxxxxx
0000000a	xxxxxxxx
0000000b	xxxxxxxx
0000000c	xxxxxxxx
0000000d	xxxxxxxx
0000000e	xxxxxxxx
0000000f	xxxxxxxx

Figure 5.15 Data memory of RISC-V processor while testing 32-bit unsigned multiplication

```
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run 10 ms
# Time: 585000 | Value of A stored in memory (02000000) =  123456789
# Time: 625000 | Value of B stored in memory (02000004) =  987654321
# Expected:  121932631112635269, Got:  121932631112635269
# Time: 695000 | Full Multiplication Result (A x B) stored in memory =  121932631112635269
# SUCCESS: Multiplication result matches the expected value!
# ** Note: $finish    : /home/hb1240/mini_project/mini_project/pl_riscv_cpu/.test/tb.v(63)
#    Time: 1010 ns  Iteration: 0  Instance: /tb
# 1
# Break in Module tb at /home/hb1240/mini_project/mini_project/pl_riscv_cpu/.test/tb.v line 63
#
# stdin: <EOF>

VSIM 2>
```

Figure 5.16 Result transcript depicting success of unsigned multiplication operation

```c
#include <stdint.h>
#include <limits.h>

#define A (* (volatile int32_t * ) 0x02000000)
#define B (* (volatile int32_t * ) 0x02000004)
#define RESULT (* (volatile int64_t * ) 0x02000008)

int main() {
    // Test integers for multiplication (32-bit signed)
    A = -123456789; // First 32-bit signed number
    B = 987654321;  // Second 32-bit signed number

    // Perform multiplication using the 'M' extension (RISC-V hardware multiplier)
    RESULT = (int64_t)A * (int64_t)B;

    return 0;
}
```

Figure 5.17 C code for testing unsigned 32-bit multiplication.

```
Disassembly of section .text:

00000054 <main>:
     ### #define B (* (volatile int32_t * ) 0x02000004)
     ### #define RESULT (* (volatile int64_t * ) 0x02000008)
     ###
     ### int main() {
     ###     // Test integers for multiplication (32-bit signed)
     ###     A = -123456789; // First 32-bit signed number
  54:   f8a43737            lui x14,0xf8a43
  58:   020007b7            lui x15,0x2000
  5c:   2eb70713            addi    x14,x14,747 # f8a432eb <__global_pointer$+0xf6a42aeb>
  60:   00e7a023            sw  x14,0(x15) # 2000000 <__bss_end>
     ###     B = 987654321;  // Second 32-bit signed number
  64:   3ade7737            lui x14,0x3ade7
  68:   8b170713            addi    x14,x14,-1871 # 3ade68b1 <__global_pointer$+0x38de60b1>
  6c:   00e7a223            sw  x14,4(x15)
     ###
     ###     // Perform multiplication using the 'M' extension (RISC-V hardware multiplier)
     ###     RESULT = (int64_t)A * (int64_t)B;
  70:   0007a583            lw  x11,0(x15)
  74:   0047a703            lw  x14,4(x15)
     ###
     ###     return 0;
     ### }
  78:   00000513            addi    x10,x0,0
     ###     RESULT = (int64_t)A * (int64_t)B;
  7c:   02e58633            mul x12,x11,x14
  80:   02e596b3            mulh    x13,x11,x14
  84:   00c7a423            sw  x12,8(x15)
  88:   00d7a623            sw  x13,12(x15)
     ### }
  8c:   00008067            jalr    x0,0(x1)

00000090 <_set_tls>:
  90:   00050213            addi    x4,x10,0
  94:   00008067            jalr    x0,0(x1)
```

Figure 5.18 LSS file generated for 32-bit signed multiplication.

```
Memory Data - /fbrd/instrmem/inst_ram - Default
00000000 02000117 04018113 02000197 7f818193 02000517 ff050513 0d800593 00000613 078006ef 02000517 fdc50513 00000593 00000613 080006ef
00000020 02000517 fe850513 05600eef 00000513 00300593 08000eef 00000513 f8a43737 020007b7 2eb70713 00e7a023 3ade7737 8b170713 00e7a223
0000003c 0007a583 0047a703 00000513 02e58633 02e596b3 00c7a423 00d7a623 00008067 00050213 00008067 00050313 00606e63 00058383 00730023
00000058 fff66613 00130313 00158593 fe661ee3 00008067 00050313 00606e63 00b30023 fff66613 00130313 fe661ee3 00008067 00000000 00000000
00000074 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
00000090 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000000ac 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000000c8 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000000e4 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
00000100 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000011c 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
00000138 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
00000154 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
00000170 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000018c 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000001a8 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000001c4 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000001e0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000001fc 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
```

Figure 5.19 Instruction RAM with HEX values of 32-bit signed multiplication in RISC-V processor

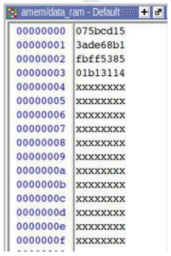


Figure 5.20 Data memory of RISC-V processor while testing 32-bit signed multiplication

```
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run 10 ms
# Time: 585000 | Value of A stored in memory (02000000) =  123456789
# Time: 625000 | Value of B stored in memory (02000004) =  987654321
# Expected:   121932631112635269, Got:   121932631112635269
# Time: 695000 | Full Multiplication Result (A x B) stored in memory =   121932631112635269
# SUCCESS: Multiplication result matches the expected value!
# ** Note: $finish    : /home/hbl1240/mini_project/mini_project/pl_riscv_cpu/.test/tb.v(63)
#    Time: 1010 ns  Iteration: 0  Instance: /tb
# 1
# Break in Module tb at /home/hbl1240/mini_project/mini_project/pl_riscv_cpu/.test/tb.v line 63
#
# stdin: <EOF>

VSIM 2>
```

Figure 5.21 Result transcript depicting success of signed multiplication operation

```c
#include <stdint.h>

// Memory-mapped base addresses
#define MATRIX_A_BASE  0x02000000  // Base address for matrix A
#define MATRIX_B_BASE  0x02000012  // Base address for matrix B
#define MATRIX_C_BASE  0x02000024  // Base address for result matrix C

// Macros to access memory-mapped matrices (half-word access)
#define MATRIX_A(row, col) (*(volatile int16_t *)(MATRIX_A_BASE + ((row) * 3 + (col)) * 2))
#define MATRIX_B(row, col) (*(volatile int16_t *)(MATRIX_B_BASE + ((row) * 3 + (col)) * 2))
#define MATRIX_C(row, col) (*(volatile int16_t *)(MATRIX_C_BASE + ((row) * 3 + (col)) * 2))

int main() {
    // Initialize matrices A and B with small values
    MATRIX_A(0, 0) = 1; MATRIX_A(0, 1) = 2; MATRIX_A(0, 2) = 3;
    MATRIX_A(1, 0) = 4; MATRIX_A(1, 1) = 5; MATRIX_A(1, 2) = 6;
    MATRIX_A(2, 0) = 7; MATRIX_A(2, 1) = 8; MATRIX_A(2, 2) = 9;

    MATRIX_B(0, 0) = 9; MATRIX_B(0, 1) = 8; MATRIX_B(0, 2) = 7;
    MATRIX_B(1, 0) = 6; MATRIX_B(1, 1) = 5; MATRIX_B(1, 2) = 4;
    MATRIX_B(2, 0) = 3; MATRIX_B(2, 1) = 2; MATRIX_B(2, 2) = 1;

    // Direct computation of each element in the result matrix
    MATRIX_C(0, 0) = MATRIX_A(0, 0) * MATRIX_B(0, 0) + MATRIX_A(0, 1) * MATRIX_B(1, 0) + MATRIX_A(0, 2) * MATRIX_B(2, 0);
    MATRIX_C(0, 1) = MATRIX_A(0, 0) * MATRIX_B(0, 1) + MATRIX_A(0, 1) * MATRIX_B(1, 1) + MATRIX_A(0, 2) * MATRIX_B(2, 1);
    MATRIX_C(0, 2) = MATRIX_A(0, 0) * MATRIX_B(0, 2) + MATRIX_A(0, 1) * MATRIX_B(1, 2) + MATRIX_A(0, 2) * MATRIX_B(2, 2);

    MATRIX_C(1, 0) = MATRIX_A(1, 0) * MATRIX_B(0, 0) + MATRIX_A(1, 1) * MATRIX_B(1, 0) + MATRIX_A(1, 2) * MATRIX_B(2, 0);
    MATRIX_C(1, 1) = MATRIX_A(1, 0) * MATRIX_B(0, 1) + MATRIX_A(1, 1) * MATRIX_B(1, 1) + MATRIX_A(1, 2) * MATRIX_B(2, 1);
    MATRIX_C(1, 2) = MATRIX_A(1, 0) * MATRIX_B(0, 2) + MATRIX_A(1, 1) * MATRIX_B(1, 2) + MATRIX_A(1, 2) * MATRIX_B(2, 2);

    MATRIX_C(2, 0) = MATRIX_A(2, 0) * MATRIX_B(0, 0) + MATRIX_A(2, 1) * MATRIX_B(1, 0) + MATRIX_A(2, 2) * MATRIX_B(2, 0);
    MATRIX_C(2, 1) = MATRIX_A(2, 0) * MATRIX_B(0, 1) + MATRIX_A(2, 1) * MATRIX_B(1, 1) + MATRIX_A(2, 2) * MATRIX_B(2, 1);
    MATRIX_C(2, 2) = MATRIX_A(2, 0) * MATRIX_B(0, 2) + MATRIX_A(2, 1) * MATRIX_B(1, 2) + MATRIX_A(2, 2) * MATRIX_B(2, 2);

    return 0;
}
```

Figure 5.22 C code for testing 3x3 matrix multiplication in RISC-V processor

```
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run 10 ms
# MatrixC[0][0] =    30 (Expected:    30)
# MatrixC[0][1] =    24 (Expected:    24)
# MatrixC[0][2] =    18 (Expected:    18)
# MatrixC[1][0] =    84 (Expected:    84)
# MatrixC[1][1] =    69 (Expected:    69)
# MatrixC[1][2] =    54 (Expected:    54)
# MatrixC[2][0] =   138 (Expected:   138)
# MatrixC[2][1] =   114 (Expected:   114)
# MatrixC[2][2] =    90 (Expected:    90)
# Matrix A:
#      1     2     3
#      4     5     6
#      7     8     9
# Matrix B:
#      9     8     7
#      6     5     4
#      3     2     1
# Matrix C = Matrix A x Matrix B:
#    30    24    18
#    84    69    54
#   138   114    90
# SUCCESS: Matrix multiplication results are correct!
# ** Note: $finish    : /home/hbl1240/mini_project/pl_riscv_cpu/.test/tb.v(99)
#    Time: 3510 ns  Iteration: 0  Instance: /tb
# 1
# Break in Module tb at /home/hbl1240/mini_project/pl_riscv_cpu/.test/tb.v line 99
#
```

Figure 5.23 Result transcript depicting success of 3x3 matrix multiplication operation

The hex file generated from the C code is loaded into the processor by modifying the instruction memory Verilog module to use $readmemh, which reads the instructions into the instruction RAM. The processor executes these instructions, and the input and result values are stored in the data memory. Images of the instruction RAM, data memory, and corresponding C code are shown above for reference.

D. Timing report comparision

This analysis compares the speed of two 32x32 multiplier architectures: an Array Multiplier (with Ripple Carry Adders) and our Vedic Multiplier (with Kogge Stone Adders), using Synopsys Design Compiler (DC Shell) with the SAED32nm_rvt_tt1p05v25c technology library. The critical path delays are derived under the following timing constraints:

create_clock = -name clk -period 10

set_input_delay = 0 [all_inputs] -clock clk

set_output_delay = 0 [all_outputs] -clock clk

The absence of a physical clock in the designs necessitated the use of a virtual clock (10ns) to model timing behaviour. The critical path delay, which defines the maximum time for data propagation between input and output, is used as the performance metric.

TABLE I. CRITICAL PATH DELAY COMPARISON

Multiplier Architecture	Critical Path Delay (ns)
Array Multiplier (Ripple Carry)	9.98
Vedic Multiplier (Kogge-Stone)	5.68

The Vedic Multiplier is significantly faster than the Array Multiplier. This improvement demonstrates that the Vedic architecture is more efficient in terms of speed, making it a preferable choice for high-speed applications requiring 32x32 multiplications.

```
clock clk (rise edge)                    10.00      10.00
clock network delay (ideal)               0.00      10.00
output external delay                     0.00      10.00
data required time                                  10.00
-----------------------------------------------------------
data required time                                  10.00
data arrival time                                   -9.98
-----------------------------------------------------------
slack (MET)                                          0.02
```

Figure 5.24 Timing report generated by Synopsis DC Shell for 32x32 conventional array multiplier

```
clock clk (rise edge)                    10.00      10.00
clock network delay (ideal)               0.00      10.00
output external delay                     0.00      10.00
data required time                                  10.00
-----------------------------------------------------------
data required time                                  10.00
data arrival time                                   -5.68
-----------------------------------------------------------
slack (MET)                                          4.32
```

Figure 5.25 Timing report generated by Synopsis DC Shell for 32x32 Vedic array multiplier

VI. FUTURE TRENDS AND CONCLUSION

A. Conclusion

The project successfully demonstrates the integration of Vedic multipliers into a RISC-V processor architecture, significantly enhancing its arithmetic capabilities while optimizing performance metrics such as speed, power consumption, and area usage. By employing the Urdhwa-Tiryakbhyam sutra for multiplication operations, the design achieves faster computation times compared to traditional multiplication methods. The implementation of the Vedic multiplier within the Arithmetic Logic Unit (ALU) and Multiplier and Accumulator (MAC) units illustrates a marked improvement in operational efficiency, allowing the processor to execute a diverse set of instructions effectively.

The results indicate that the Vedic multiplier not only reduces latency but also conserves energy, making it a compelling choice for modern computing applications where performance and efficiency are paramount. The project highlights the advantages of utilizing ancient mathematical techniques in contemporary digital design, showcasing their relevance in enhancing computational efficiency.

B. Future Trends

The evolution of RISC-V architecture, particularly with the integration of Vedic multipliers, is poised to significantly enhance computational efficiency and performance in various applications. This section explores the anticipated trends in pipelined RISC-V processors, focusing on complex number calculations and their incorporation into GPUs, image processing, DSP blocks, dedicated high-performance units, and AI processing applications.

1. Integration of Vedic Multipliers

Vedic Multipliers are based on ancient Indian mathematics and provide a highly efficient method for multiplication, particularly useful in digital signal processing and image processing applications. By integrating Vedic multipliers into pipelined RISC-V architectures, processors can achieve:

- Higher Throughput: Vedic multipliers can perform operations faster than traditional methods due to their reduced complexity and parallelism.
- Lower Latency: The design allows for quicker execution of multiplication tasks, which is crucial for real-time applications in graphics and AI.

2. Complex Number Calculations

The incorporation of complex number calculations is essential for applications in communications and signal processing. Future RISC-V processors are expected to support:

• Complex Number Support: With the rise of applications in communications and signal processing, supporting complex numbers directly in hardware will streamline operations that involve Fourier transforms and other algorithms.

• Optimized Arithmetic Operations: The use of Vedic multipliers can enhance the performance of algorithms that rely heavily on complex arithmetic, making them more efficient for tasks such as modulation and demodulation in communication systems.

3. Application in GPUs and Image Processing

RISC-V's flexibility allows it to be tailored for specific applications like GPUs and image processing:

• GPU Integration: The architecture can be adapted to create specialized GPU cores that handle parallel processing efficiently, making it suitable for graphics-intensive applications.

• Image Processing: With Vedic multipliers enhancing arithmetic operations, RISC-V processors can significantly improve performance in image filtering, transformation, and recognition tasks.

4. Digital Signal Processing (DSP) Blocks

RISC-V processors are increasingly being utilized in DSP applications due to their customizable nature:

• Dedicated DSP Cores: Future designs may include dedicated DSP blocks that leverage Vedic multipliers for efficient audio and video processing.

• Real-Time Processing Capabilities: The pipelined architecture ensures that data can be processed in real-time, which is critical for applications such as telecommunications and multimedia.

5. High-Performance Computing (HPC) Blocks

The demand for high-performance computing solutions is driving innovations in RISC-V architectures:

• Custom High-Performance Units: The ability to create custom extensions allows designers to optimize processors for specific workloads found in scientific computing and AI.

• Scalability: As workloads increase in complexity, RISC-V's modular approach enables easy scaling of performance by adding more functional units or optimizing existing ones.

6. AI Processing Applications

The integration of Vedic multipliers into RISC-V processors opens up new possibilities for AI processing:

• Efficient Neural Network Computations: The architecture can be optimized to perform matrix multiplications and convolutions more efficiently, which are fundamental operations in deep learning models.

• Real-Time Inference: With enhanced arithmetic capabilities, RISC-V processors can support real-time inference tasks in edge AI applications, enabling faster decision-making processes.

• Custom AI Accelerators: Future designs may include dedicated accelerators tailored for specific AI workloads (e.g., natural language processing or computer vision), leveraging the flexibility of RISC-V to meet diverse application needs.

7. Market Trends

The adoption of RISC-V is expected to grow significantly due to its open-source nature and adaptability:

• A forecast indicates a potential shipment growth rate of 50% annually from 2024 to 2030, driven by increasing demand across various sectors including automotive and AI.

• Major players like Qualcomm are investing heavily in RISC-V technology to develop custom solutions tailored for specific markets.

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Hybrid Communication System for Land-Water Interface Using LoRa and Visible Light Communication

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Abstract - With an emphasis on signal integrity, amplification, and noise effects, this study investigates laser-based underwater data transmission. It highlights issues such as attenuation and dispersion and suggests solutions for improved optical communication performance in practical applications.

Keywords - Autonomous Underwater Vehicles,First in first out , Radio Frequency , Long Range , Low-power wide area network , Internet of things , Underwater wireless optical communication ,Light emitting diode , Field Programmable gate array

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I. Introduction

Effective communication between land and underwater environments has become increasingly important in recent years due to applications in areas such as underwater exploration, marine research, and environmental monitoring. However, communication between these two mediums is fraught with difficulties, the main one being that traditional communication technologies, like radio frequency (RF) methods, are unable to function effectively underwater because RF waves, like those used in Wi-Fi, are severely attenuated (weakened) when transmitted through water, especially in saltwater, making long-range communication nearly impossible.[5]

In recent years, applications in fields including environmental monitoring, marine research, and underwater exploration have made effective communication between terrestrial and underwater environments more crucial. [6]

LoRa Communication: LoRa is a well-known wireless technology that is renowned for its low-power and long-range capabilities on land. It is ideally suited for situations where broad coverage and energy efficiency are top concerns because it can transport little amounts of data over long distances. But because LoRa relies on radio frequency communications, which are ineffective in water, it has serious limits when it comes to underwater communication.[3]

Alternatively, optical communication uses light waves—typically from lasers or LEDs—to transfer information. Underwater conditions, where light travels more efficiently than radio frequencies, are ideal for this technique. Communication with underwater sensors or equipment is made possible by optical communication, which has fast data rates and can send massive amounts of data over short to medium distances in water. However, the efficacy of optical signals for long-distance communication can be limited by elements like murky water, particulates, or changing water conditions, which can block or distort them.[2]

Hybrid System: A hybrid system can benefit from the advantages of both technologies by combining optical communication with LoRa. While optical communication can handle high-speed, short-range data transfer in underwater situations, LoRa can handle long-range communication on land, where RF signals work well. Reliable data interchange between land-based devices and underwater sensors would be made possible by this hybrid system. FIFO (First-In-First-Out) Memory: The project also uses FIFO memory to provide seamless communication between the two systems. The first piece of data sent is the first piece of data received thanks to a form of data structure called FIFO, which processes data in the order it arrives. This function is crucial for controlling the data flow between LoRa and optical communication channels since it guarantees timely transmission of information and guards against data loss or delay. FIFO buffers will be a Hybrid Communication System for Land-Water Interface Using LoRa and Visible

Light Communication to assist in controlling the sporadic nature of communication, particularly in difficult underwater environments where data transfer could be interrupted or delayed.

Applications and Potential: There is a great deal of room for the hybrid communication system to be used in areas including exploration, environmental evaluation, marine research, and underwater monitoring. This system might be used, for instance, to gather data from underwater sensors that gauge oceanographic parameters like temperature, salinity, or pollution levels and send that data back to land-based stations for real-time analysis. The integration of optical communication for high-speed underwater data transfer, LoRa for long-range terrestrial communication, and FIFO for seamless data handling would result in a low-power, dependable, and effective communication system that can function in both land and underwater settings.[5]

To sum up, this hybrid communication technology is a big step toward facilitating smooth, instantaneous data transfer over land and water. By utilizing the complimentary advantages of LoRa and optical technologies, it tackles the crucial problems of underwater communication while guaranteeing effective data management with FIFO memory. This technology is a useful tool for marine scientists, researchers, and environmentalists since it has the potential to completely change how we observe and investigate undersea environments.

II. Literature Survey

A. Underwater Wireless Optical

According to Zhu et al. (2020), the primary challenge facing UWOC systems is the attenuation of optical signals due to water's scattering and absorption properties. These issues are exacerbated in murky, turbid, or saline environments, which limits the operational range and reliability of UWOC systems. Research has been dedicated to improving the sensitivity of photodiodes and other receiver components to enhance signal detection under such conditions. Furthermore, advancements in optical code division multiple access (OCDMA) have allowed multiple devices to communicate over the same optical channel without interference, facilitating more efficient underwater communication systems (Zhu et al., 2020) [1].

B. Signal Processing and Modulation

According to Yadav et al. (2024) discuss how FPGAs allow for flexible signal processing and real-time error correction, making UWOC systems more adaptable and resilient to environmental disturbances like water currents or particle interference. These improvements in modulation and signal processing have been crucial in advancing high-speed, full-duplex communication systems for underwater applications, particularly for Autonomous Underwater Vehicles (AUVs) involved in marine research and deep-sea exploration (Yadav et al., 2024) The integration of FieldProgrammable Gate Arrays (FPGAs) has significantly contributed to the efficiency of UWOC systems. [2].

C. Hybrid Communication Systems

According to Li et al. (2018), while UWOC is excellent for high-speed, short-range communication underwater, LoRa's long-range capabilities make it ideal for land based communication. The hybrid systems aim to combine the low-power, long-range strengths of LoRa with the high-bandwidth, low-latency performance of UWOC. This combination offers a promising solution for applications in oceanographic research, where data must be transmitted from underwater to surface stations over large distances (Li et al., 2018) [4].

D. LoRa Technology in Agricultural

Vu et al. (2018) highlight the use of LoRa in smart agriculture systems, where it enables low-power, long-range communication to monitor environmental parameters like soil moisture, temperature, and humidity. The low power consumption of LoRa allows for devices to operate for years on a single battery, making it ideal for remote monitoring in difficult-to-reach locations. This capability has made LoRa essential in sectors like agriculture, where real-time data is crucial for making informed decisions on irrigation, fertilization, and pest control (Vu et al., 2018) [3].

E. LoRa's Potential for Underwater

Nabhan and Suryana (2024) explore how LoRa can be adapted for underwater environments through techniques like up- and down-conversion, which shifts LoRa signals to frequencies better suited for underwater propagation.Although LoRa's Hybrid Communication System for Land-Water Interface Using LoRa and Visible Light Communication. Department of ECE, BMSCE Page | 4 performance in underwater environments remains limited due to signal attenuation, these adaptations have made it feasible for short-range communication between underwater sensors and surface systems, especially in shallow waters. This development lays the foundation for more robust communication systems that bridge land-to-water boundaries for marine research (Nabhan & Suryana, 2024) [6].

F. LoRa and UWOC Hybrid Systems

As noted by Mukhopadhyay et al. (2023), hybrid systems that combine LoRa's long range, low-power capabilities with UWOC's high-speed data transfer can significantly improve communication reliability in both terrestrial and underwater environments. These hybrid systems are expected to enable continuous, real-time data transfer in remote marine monitoring and research applications, overcoming the challenges posed by

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environmental interference and long-distance communication. By leveraging the strengths of both technologies, these hybrid systems can offer a comprehensive solution for cross-medium communication, particularly in applications like environmental monitoring and oceanographic research (Mukhopadhyay et al., 2023) [5].

III. Problem Analysis & Solution

A. Problem Definition

Establishing a communication system that can efficiently send data over the land water interface is the primary problem. The goal of this project is to create a hybrid communication system that uses optical and LoRa (long range) communication for transmission over land.

B. Proposed Solution

A ground-breaking solution to the problems of dependable data transfer at the land water interface—where conventional communication techniques frequently fall short because of environmental constraints—is the Hybrid Communication System. This system combines two complementing technologies: optical communication for high speed, short-range data transfer underwater and LoRa (Long Range) for long-distance, low-power communication on land. LoRa is superior in terrestrial settings because it allows for low-power, long-range communication. Applications where equipment must function over wide areas with little maintenance, such as remote sensing, agriculture, or environmental monitoring, are perfect for this. However, because of signal attenuation,

LoRa performs noticeably worse underwater. Optical communication, on the other hand, uses blue-green light pulses to send high-bandwidth data over short distances and functions well underwater. Despite the fact that line-of-sight is necessary for correct signal reception, this makes it perfect for transmitting data in real-time from underwater sensors or autonomous underwater vehicles (AUVs).

The hybrid technology allows for smooth, real-time data transfer between both settings by fusing optical communication's high-speed transfer underwater with LoRa's long-range communication on land. In a variety of applications, including oceanography, marine research, and environmental monitoring, where communication across the land-water interface is essential, this integration provides a dependable, low-power solution for ongoing monitoring and control.

The problem of dependable data transfer across the land-water interface can be creatively solved by hybrid technology that blends optical and LoRa (Long Range) connectivity. By utilizing the advantages of both communication techniques, this integration enables seamless, real-time data flow between terrestrial and underwater environments. Underwater conditions are ideal for optical communication because they allow for high-speed data transfer across short distances. For applications such as real-time video streaming or data from underwater sensors and autonomous underwater vehicles (AUVs), optical communication reduces signal attenuation and permits high-bandwidth transmission by employing light waves, usually in the bluegreen range. However, in challenging underwater conditions, it needs line-of-sight and has a restricted range.

However, LoRa offers low-power, long-range communication across land, which makes it perfect for uses like remote sensing, agriculture, and environmental monitoring where devices must function over wide distances without regular recharging. High-speed transfer provided by optical communication under water is complemented by LoRa's capacity to communicate over great distances while using very little energy.

The hybrid system, which combines these technologies, provides a reliable and low power solution for ongoing monitoring and control by facilitating smooth communication over land and water. In domains where real-time data transfer across many settings is essential, such as oceanography, marine research, and environmental monitoring, this integration is very beneficial.

Many sectors that need constant connection between land and underwater settings find the Hybrid connection System very useful for real-time monitoring. Its capacity to integrate the high-speed data transfer of optical communication with the long range, low-power communication of LoRa makes it indispensable for applications where dependable data transmission over the land-water interface is essential.

Marine and Oceanic Research: This system allows for the real-time collection of data from underwater sensors that measure pressure, temperature, and salinity at different depths for marine and oceanic research. The ability of these sensors to send data back to research stations on land allows them to provide important information on oceanographic conditions without requiring manual retrieval. Ocean monitoring, climate research, and studies of marine biology all depend on this. Aquaculture: The hybrid communication system allows real-time transmission of environmental data to land-based stations, assisting governments and organizations in promptly responding to emerging issues.

Aquaculture: Monitoring water quality, fish behavior, and environmental factors like oxygen levels and pH balance is essential for maintaining optimal conditions for aquatic life in large fish farms.

The hybrid system can transmit this data to a centralized control center, allowing farm managers to make informed decisions about feeding schedules, water

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treatment, and overall farm management. Environmental Monitoring: This system is ideal for monitoring remote bodies of water to track pollution levels, measure ecosystemhealth, or detect climate-related changes.

C. Cost-effective and Energy-Efficient

The Hybrid Communication System's energy efficiency is one of its main benefits. Because of its low power consumption, LoRa technology is a great option for battery operated devices or solar-powered stations in distant locations. Long-term operation without frequent battery replacements is ensured by LoRa's capacity to transmit across great distances with low energy consumption, which is particularly advantageous for sensors placed in harsh locations.

In addition to being very power-efficient, optical communication is usually employed for short-range data transport. Its high bandwidth and low energy consumption over short distances make it perfect for sending big data packets, such as high-resolution sensor data underwater or real-time video streams.

Together, these technologies produce a system that can function for long stretches of time without requiring a lot of upkeep or frequent battery changes. It is ideal for deployment in hard-to-reach places like deep-sea monitoring sites or offshore marine research stations since it lowers operating expenses and increases system longevity. For enterprises that need consistent, dependable communication in both land and underwater environments, this hybrid system's low maintenance and energy efficiency provide cost-effective monitoring over extended periods of time.

In difficult settings where traditional communication systems frequently falter, enterprises and research institutions can guarantee real-time monitoring by implementing the Hybrid Communication System. Data transmission across land and underwater conditions is made efficient by combining the long-range, low-power capabilities of LoRa with the high-speed transfer of optical communication. This technology guarantees constant data flow, offering vital information on aquaculture conditions, environmental changes, and marine ecosystems. Long-term operational stability is also made possible by its energy-efficient design, which eliminates the need for frequent maintenance or battery replacements. This makes it the perfect choice for remote or difficult-to-reach areas that need dependable communication

IV. Methodology & Implementation

A . *Block Diagram*

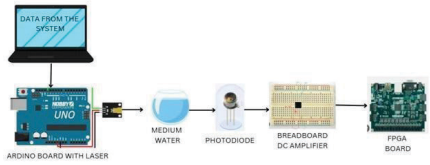


Fig1.1 Pictorial Representation.

The following elements make up the signal detection and processing systemshown in this flow diagram:

Laser-equipped Arduino Board: This device shines light through water using a laser that is controlled by an Arduino. Changes in the characteristics of light are detected by a photodiode, which transforms them into electrical signals. An FPGA processes these signals for analysis after they have been amplified on a breadboard using a DC amplifier. A computer then receives the signals for visualization and additional uses.

Water as the medium: The medium through which the laser beam travels is water. Water's purity, temperature, and dissolved particles are examples of its physical and chemical characteristics that can affect the laser light's intensity, refraction, scattering, and absorption. These modifications offer useful information for examining the properties and actions of the medium.

Photodiode The laser light travels through the medium before being picked up by a photodiode. The photodiode transforms the optical signal into an electrical signal in response to changes in the light's characteristics or intensity. This change makes it easier to amplify and process the signal later on and is essential for examining how the medium affects the light.

With a DC amplifier, a breadboard: A DC amplifier placed on a breadboard receives the photodiode's feeble electrical signal. By strengthening the signal, this amplifier makes sure it is strong enough for precise and trustworthy additional processing. To reduce noise and enhance the quality of data transmitted to later components, amplification is crucial.

FPGA Board: A Field-Programmable Gate Array (FPGA) board receives the boosted signal. The FPGA processes the signal and carries out operations such as data transmission, analysis, and filtering. Computer system: The FPGAs processed data is then transferred to a computer system for additional analysis, storage, or visualization.

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B. Structure

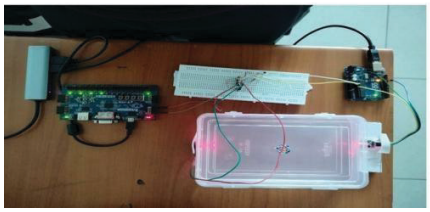


Fig 1.2 Structure Of The Setup

C. Flow Chart

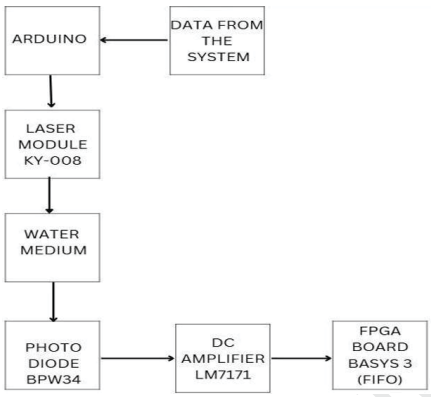


Fig 1.3 Flow Chart of the System

VI. Results & Discussion

Using a laser beam, the system was able to successfully send data through the medium (water). The modulated optical signal was picked up by the photodiode and then amplified on a breadboard using the DC amplifier circuit. After being amplified, the signal was sent to the FPGA board for processing and display on the computer.

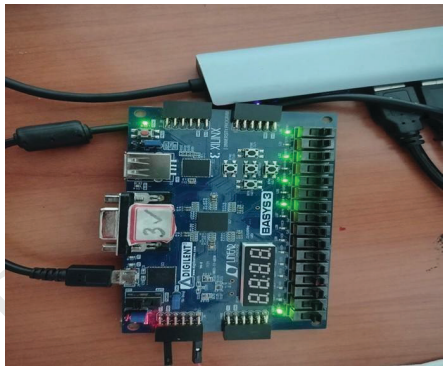


Fig 1.5 Result of the FPGA Board

A. Discussion

How the System Operates:

Arduino: The sent signal originates from the Arduino microcontroller. It transforms data into a format that can be transmitted optically by the laser. Laser Beam: The modulated data is sent via the water medium by the laser, which acts as the optical carrier. As the transmission medium, the water may cause the signal to be attenuated or scattered. The photodiode transforms the optical signal back into an electrical signal after being positioned to receive the transmitted laser light. Its sensitivity is essential for identifying changes in light intensity that correlate to the data being delivered.

DC Amplifier: The photodiode's feeble electrical signal needs to be amplified. A DC amplifier circuit on a breadboard enhances the signal so the FPGA can process it.

FPGA Board: The FPGA decodes the amplified signal and serves as the processing unit. On the linked computer system, the data is further examined or displayed.

B. Observation:

Under ideal circumstances, the optical signal through water behaved consistently. However, any turbidity or disturbances in the aqueous medium may decrease the signal quality. The entire performance of the systemis greatly influenced by how well the photodiode

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converts light signals into electrical impulses. To reduce signal loss, the laser beam and photodiode must be properly aligned. To overcome the inherent losses in the optical-to-electrical conversion and make sure the signal is powerful enough for the FPGA to process, amplification is essential.

C. Challenges Faced:

Signal Attenuation:

Light is absorbed and scattered by the aqueous medium, causing attenuation. While contaminants can drastically reduce signal quality, clear water guarantees minimal loss. Noise Interference: The photodiode's performance may be impacted by outside light sources or background noise, necessitating the use of further shielding or filtering techniques to improve the signal-to-noise ratio. Circuit Stability: For reliable signal transfer to the FPGA, a stable amplification circuit is essential. Uses: This configuration shows that optical communication may be used to send data across water, which makes it suitable for underwater communication systems. It can be applied to different situations, like secure data transmission, fiber-optic connection, and remote sensing. Upcoming Enhancements: It can be applied to different situations, like secure data transmission, fiber-optic connection, and remote sensing. Upcoming Enhancements: adjusting for noise or signal distortions by implementing sophisticated signal processing algorithms on the FPGA. employing a better amplifier circuit and a more sensitive photodiode to detect and amplify weaker signals. investigating various optical conditions and media to investigate how they affect transmission efficiency and signal quality.

VI. Conclusion and Future Trends

A. Conclusion

The "Hybrid Communication System for Land-Water Interface Using LoRa and Visible Light Communication" demonstrates a significant step forward in addressing the challenges of cross-medium communication. By combining the low-power, long-range capabilities of LoRa with the high-speed, high-bandwidth characteristics of optical communication, this hybrid system offers a robust solution for seamless data transfer between terrestrial and underwater environments. The project's innovative integration of technologies bridges the gap created by the limitations of individual systems. While optical communication excels underwater with minimal signal attenuation, LoRa provides dependable connectivity over long distances on land. The inclusion of FIFO memory further enhances system efficiency by ensuring smooth data handling. This system has immense potential for applications in marine research, environmental monitoring, aquaculture, and other domains requiring reliable land-water communication. The low energy consumption and cost-effectiveness of the hybrid system make it an ideal choice for deployments in remote and challenging conditions

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Design of a Compact Circular Microstrip Patch Antenna for 5G Applications

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***Abstract*—This paper presents the development and evaluation of a compact circular microstrip patch antenna meticulously designed for 5G wireless communication systems, operating at 28 GHz within the millimeter-wave frequency spectrum. The antenna features a circular patch with a radius of 3.2 mm, fabricated on a low-loss ROGERS RT/Duroid 5880 substrate (dielectric constant ε_r = 2.2, thickness 0.787 mm), ensuring a small footprint while delivering exceptional efficiency and performance suited for 5G applications. The design is executed using CST Microwave Studio, where the antenna's dimensions—substrate and ground plane measuring 10 mm × 10 mm, ground plane and patch thickness of 0.035 mm, and feedline of 2 mm × 0.3 mm—are carefully optimized through iterative simulations to enhance critical performance parameters such as gain, bandwidth, and return loss (S_{11}). An inset feed mechanism is employed to achieve effective impedance matching with a 50-ohm input, enabling seamless integration into planar circuit architectures. The antenna targets a gain of 5 to 6 dBi, a bandwidth exceeding 1 GHz, and a return loss below -10 dB, with its performance validated through comprehensive analysis of radiation patterns, directivity, and efficiency metrics. This compact design demonstrates excellent suitability for high-speed 5G networks, including applications in mobile devices and Internet of Things (IoT) systems, striking an optimal balance between size reduction and enhanced functionality to meet the rigorous demands of next-generation wireless communication technologies.**

***Index Terms*—Keywords— Microstrip patch antenna, 5G, 28 GHz, millimeter wave, CST simulation, RT/Duroid 5880**

I. Introduction

The rapid advancement of 5G technology has increased the need for compact, high-efficiency antennas, particularly in the millimeter-wave band like 28 GHz. Microstrip patch antennas are preferred due to their lightweight, low-cost fabrication, and compatibility with planar circuits. However, designing them for 5G involves challenges in achieving high gain, wide bandwidth, and good radiation efficiency in a miniaturized form.

This project presents a circular microstrip patch antenna with a 3.2 mm radius, built on a ROGERS RT/Duroid 5880 substrate (ε_r = 2.2, thickness 0.787 mm). With dimensions of 10 mm × 10 mm and an inset-fed 2 mm × 0.3 mm line, the design is optimized in CST Microwave Studio. It targets directional radiation, over 1 GHz bandwidth, and gain between 5–6 dBi. The design suits 5G mobile and IoT applications, balancing size reduction with performance to meet next-generation wireless communication demands.

II. Antenna Design and Structure

A. Design Parameters

- Substrate: ROGERS RT/Duroid 5880
- Dielectric constant: 2.2
- Thickness: 0.787 mm
- Patch radius: 3.2 mm
- Substrate and ground plane size: 10 mm × 10 mm
- Feedline: 2 mm × 0.3 mm (Inset Feed)

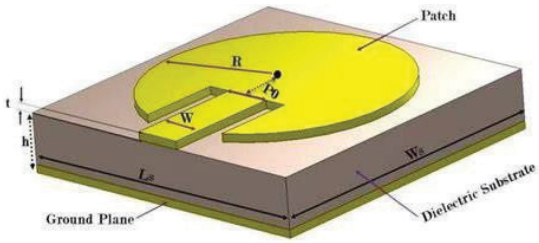


Fig. 1: Top view of circular microstrip patch antenna

The antenna was modeled in CST Microwave Studio. The inset feed mechanism is used to achieve 50-ohm impedance matching.

B. Substrates for Antenna Design

The choice of substrate plays a critical role in determining antenna efficiency, size, and bandwidth—especially at millimeter-wave frequencies like 28 GHz. This section compares commonly used substrates:

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- **RT/Duroid 5880** (ε_r = 2.2): Offers low dielectric loss, excellent efficiency, and wide bandwidth; ideal for 5G.
- **FR4** (ε_r = 4.3): Cost-effective but suffers from high losses and reduced bandwidth at high frequencies.
- **Teflon/PTFE** (ε_r = 2.1): Similar to RT/Duroid 5880 with good efficiency and return loss; suitable for wideband 5G designs.
- **ROGERS 4003C** (ε_r = 3.3): Offers a balance between size and performance but less efficient than RT/Duroid.
- **Alumina** (ε_r = 9.9): Enables compact size but limits bandwidth, making it less ideal for 5G applications.

III. Literature Survey

Recent research on microstrip patch antennas for 5G applications at 28 GHz highlights the importance of substrate choice, design optimization, and simulation tools like CST and HFSS. A study using FR4 at 28 GHz achieved -45 dB return loss and 1.76 GHz bandwidth but initially offered only 0.1573 gain, later improved to 5.81 dBi using DGS techniques [1]. Another design targeting UWB applications (2.2–5.5 GHz) showed 85% fractional bandwidth using circular polarization and an L-probe feed, though not specific to 5G [2]. Circularly polarized antennas at 3.5 GHz using truncated patches demonstrated axial ratio improvements but were limited to sub-6 GHz [3]. Additional work at 28 GHz emphasized miniaturization and validated CST/HFSS-based design approaches, underscoring the role of substrates in gain and bandwidth performance [4]. These studies collectively inform the present antenna design, especially for size reduction and radiation enhancement strategies applicable to 5G.

IV. Problem Analysis and Solution

A. Problem Definition

The rapid deployment of 5G wireless networks has intensified the need for compact, high-performance antennas capable of operating in the millimeter-wave spectrum, particularly at 28 GHz, to support ultra-high data rates, low latency, and reliable connectivity in mobile and IoT devices. Designing a circular microstrip patch antenna for these applications presents several challenges. Maintaining high gain (5–6 dBi), wide bandwidth (¿1 GHz), and low return loss (¡ -10 dB) within a compact footprint (e.g., 10 mm × 10 mm substrate) is difficult due to the trade-off between size and performance. Additionally, millimeter-wave signals suffer from high propagation losses, necessitating low-loss substrates like ROGERS RT/Duroid 5880 (ε_r = 2.2) for efficient radiation. Impedance matching using a 2 mm × 0.3 mm feedline within such a constrained layout is also non-trivial. Moreover, the antenna must integrate seamlessly with planar circuitry while maintaining directional radiation suited for 5G communication.

B. Proposed Solution

To overcome these challenges, this project implements a compact circular microstrip patch antenna designed for 28 GHz operation. The antenna uses a 3.2 mm radius patch on a ROGERS RT/Duroid 5880 substrate with a thickness of 0.787 mm and a dielectric constant of ε_r = 2.2, selected for its low-loss characteristics at high frequencies. The design includes a ground and substrate area of 10 mm × 10 mm, with a patch and ground thickness of 0.035 mm. A 2 mm × 0.3 mm inset-fed feedline is incorporated to achieve impedance matching with a 50-ohm input, aiding integration into compact devices. The antenna is modeled and simulated using CST Microwave Studio, with iterative tuning of critical parameters such as gain, bandwidth, and return loss. The targeted performance includes a gain of 5–6 dBi, bandwidth ¿1 GHz, and return loss below -10 dB. The final design is validated through radiation pattern analysis, directivity, and efficiency metrics, while substrate and geometry optimization ensure a balance between miniaturization and performance for 5G systems.

V. Methodology and Implementation

The design and implementation of the compact circular microstrip patch antenna for 5G applications at 28 GHz begins by defining the target frequency and selecting a suitable low-loss substrate—ROGERS RT/Duroid 5880 with a dielectric constant ε_r = 2.2 and a thickness of 0.787 mm—to ensure high efficiency in the millimeter-wave range.

Theoretical calculations are used to determine the patch radius (3.2 mm) and inset feed dimensions (2 mm × 0.3 mm), tailored to the substrate properties and desired frequency. The antenna is modeled in CST Microwave Studio using a 10 mm × 10 mm substrate and ground plane, both with a thickness of 0.035 mm, and an inset feed for 50-ohm impedance matching. Simulations are conducted to evaluate performance metrics such as return loss (S_{11}), gain, bandwidth, directivity, and radiation patterns. The antenna achieves a return loss of -18 dB at 28 GHz, gain of 5.6 dBi, dual-band response across 21–23 GHz and 27–29 GHz, and directivity in the range of 6.5–7.5 dBi. These results are refined by iteratively adjusting design parameters.

The final design delivers over 80–90% efficiency and a bandwidth exceeding 1 GHz, confirming its effectiveness for compact 5G antenna integration in mobile and IoT platforms.

A. Pictorial Representation

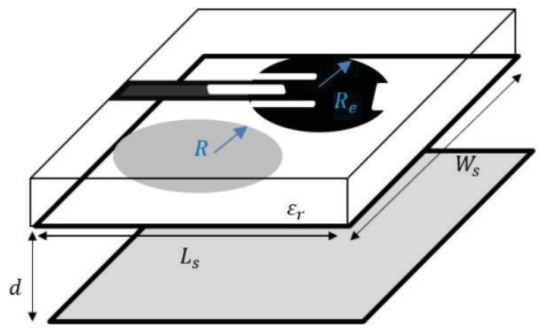


Fig. 2: 3D representation of microstrip patch antenna

UNDER PEER REVIEW

B. Structure

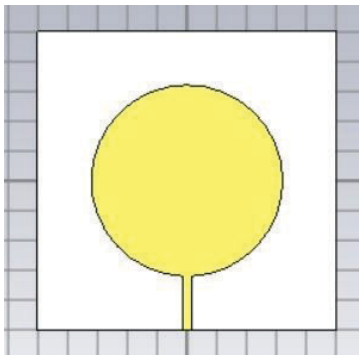


Fig. 3: Structure of the antenna (CST layout)

VI. Results and Discussion

The antenna was designed and simulated using CST Microwave Studio with the following parameters:

- **Circular patch radius:** 3.2 mm.
- **Substrate and ground plane:** 10 mm × 10 mm, substrate thickness 0.787 mm, patch/ground thickness 0.035 mm.
- **Feedline:** 2 mm × 0.3 mm inset feed for 50-ohm impedance matching.
- **Substrate material:** ROGERS RT/Duroid 5880 (ε_r = 2.2).

A. Gain

The antenna achieves a gain of 5.6 dBi, derived from the Farfield E-plane pattern at $\phi = 90^{\circ}$, which meets the design target of 5–6 dBi for 5G communication.

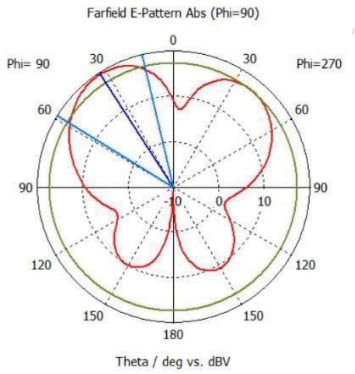


Fig. 4: Farfield E-Plane Pattern

Farfield E-Pattern (ϕ = 90°): The E-plane radiation pattern shows the directional characteristics of the antenna with a peak gain of 5.6 dBi, confirming its suitability for directional 5G applications.

B. Return Loss (S11)

The return loss plot indicates impedance matching at 28 GHz. The design goal is S_{11} < −10 dB, preferably between -15 and -20 dB to ensure minimal power reflection.

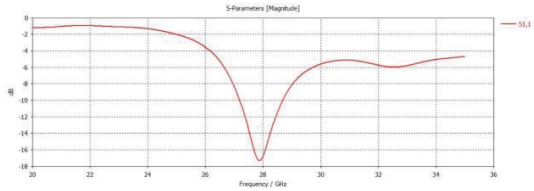


Fig. 5: Return Loss

C. VSWR

The VSWR plot reflects the impedance matching quality of the antenna. The target range is 1 to 2, ideally between 1.2 and 1.5, ensuring efficient signal transmission.

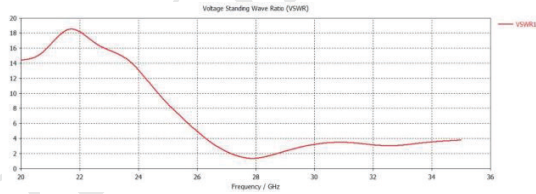


Fig. 6: VSWR

D. Bandwidth

From the return loss plot, bandwidth is defined as the frequency range where S_{11} < −10 dB. The expected bandwidth for this design is 1–2 GHz, satisfying the ¿1 GHz criterion required for 5G performance.

VII. Conclusion and Future Trends

A. Conclusion

This work presents a compact circular microstrip patch antenna for 5G applications at 28 GHz, achieving a gain of 5.6 dBi, 1–2 GHz bandwidth, and high efficiency using a ROGERS RT/Duroid 5880 substrate. The design outperforms FR4 and matches Teflon-based antennas in performance while maintaining a compact 10 mm × 10 mm footprint. Simulations confirm its suitability for mobile and IoT devices. Future work may explore experimental validation and bandwidth enhancement via techniques like DGS.

B. Future Trends

Emerging trends such as metamaterials, reconfigurable surfaces, and additive manufacturing are transforming antenna design, aiming for higher gain, reconfigurability, and multiband support. AI-driven optimization and flexible substrate integration are also expected to improve performance and enable applications in 6G and wearable IoT devices.

Acknowledgment

We extend our gratitude to our guide Dr. Sudhindra K R, Professor of Dept. ECE in BMS College of Engineering for their support throughout this project.

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Low Power and Area Efficient ALU using Full Adders

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***Abstract*— This paper explores the role of Very Large Scale Integration (VLSI) technology in advancing modern electronic systems, particularly focusing on the design of low-power and area-efficient Arithmetic Logic Units (ALUs). VLSI enables the integration of millions of transistors into a single microchip, driving innovations in devices like microprocessors, memory chips, and application-specific integrated circuits (ASICs). As electronic devices evolve, the need for high performance, reduced power consumption, and minimal area becomes more critical, especially in battery-operated and energy-efficient systems. Power consumption in VLSI circuits is primarily influenced by dynamic and static power, both of which have become key challenges in the design of digital circuits. Full adders, central to ALU functionality, are optimized for low power and area efficiency, impacting the overall performance of processors. This report investigates various strategies for designing low-power full adders, including novel circuit topologies and advanced logic synthesis techniques, highlighting the trade-offs and innovations that drive advancements in VLSI technology. The study underscores the importance of balancing power efficiency, speed, and reliability in the development of next-generation VLSI systems.**

Keywords— VLSI technology, low-power design, area-efficient ALU, full adder optimization, dynamic power, static power, microprocessors

I. INTRODUCTION

VLSI circuits are designed to operate at low power with high-speed accuracy, enhancing the performance of Arithmetic and Logic Units (ALUs). ALUs, responsible for arithmetic and logic operations, contribute to low-power, high-speed advantages in digital signal processing, microprocessors, VLSI systems, and microcontrollers. They consist of components like full adders, 2x1, and 4x1 multiplexers. In this design, the 1-bit full adder uses 2T XNOR, 2T XOR logic, and pass transistors, while the multiplexers are implemented using the Gate Diffusion Input (GDI) technique. These approaches reduce transistor count and power consumption, improving efficiency. This paper presents the effectiveness of 2T XNOR, 2T XOR logics, and pass transistors in full adder design within ALUs. The paper is organized as follows: Section II discusses existing methodologies, Section III provides the justification for the chosen method, Section IV explains the ALU design operations, Section V presents simulation results and analysis, and the conclusion is provided in Section VI.

II. PREVIOUS WORKS

The previous paper presents a 4-bit ALU designed by cadence Virtuoso 90nm technology for low area and power with 2T XNOR ,2T XOR, PASS TRANSISTORS of full adder and using GDI for multiplexer. Various methods of multiplexer and full adder are implemented and compared. Compared with previous paper, it reduced the power and area of ,30%. The 2x1 multiplexer and 4x1 multiplexer are designed using Gate Diffusion input Technique. Full adder based proposed technique are 37.533nW, but 2T XNOR technique consumes 36.844nW, for 2T XOR technique consumes 36.933nW and for PASS TRANSISTORS technique 37.268nW .As per the previous paper pass transistor and XOR consume more than the XNOR technique. Using these techniques, full adder power leads to reduce, therefore he ALU design also tends to reduced. Power, delay and number of transistors are compared using GDI, PTL,2T XOR , 2T XNOR technique and PASS transistors.

III. LITERATURE SURVEY

A Low Power and High Speed 8-bit ALU Design using 17T Full Adder

The paper addresses the challenge of designing a low-power, area-efficient Arithmetic Logic Unit (ALU), which is a key component in processors used for various digital systems like microprocessors and microcontrollers. The problem lies in reducing the power consumption and area of the ALU while maintaining performance, especially in the design of its full adder, which contributes significantly to both power and area consumption.

The proposed solution is focused on designing a 1-bit-8 functional Arithmetic Logic Unit (ALU) that is both power-efficient and area-efficient. This ALU performs a variety of arithmetic and logical operations, and the design leverages a combination of basic gates and full adders to meet stringent power and area constraints. The design approach is based on CMOS (Complementary Metal-Oxide-Semiconductor) GDI technology, which is widely used for low-power, high-speed digital circuits. The implementation and analysis are carried out using Cadence Virtuoso for analog design and Cadence Genus for digital analysis

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CADENCE VIRTUOSO

Purpose: It is an analog and mixed-signal design platform.

Functionality: The ALU circuit is designed at the transistor level using different parameters and technologies (e.g., 45nm technology).

Benefit: This detailed design approach helps in analyzing and selecting the most power and area-efficient configuration.

CADENCE GENUS

Purpose: It is a digital design tool used for synthesis and optimization.

Functionality: It synthesizes the digital logic of the ALU using full adders and basic gates, and it generates detailed reports on power consumption and area usage.

Benefit: These reports provide insights into the total power required for the ALU's operation and the total silicon area occupied by the design, allowing for real-time analysis of delay and constraints.

Power and Area Report:

After the design is synthesized and optimized, Cadence Genus generates a comprehensive power and area report, which includes.

Total Power Consumption: This is the amount of power required to operate the ALU, including:

Dynamic Power: Caused by switching activities in the circuit.

Static Power: Due to leakage currents when transistors are in off states.

Total Area: The physical area occupied by the ALU design on the silicon chip. This is important for ensuring the design fits within the size constraints of the target application or chip.

Importance of the Reports:

These reports are crucial for verifying that the design achieves the power and area efficiency goals set at the start of the project. They provide essential feedback on whether the design meets the required constraints, ensuring the final ALU is both power-efficient and area-efficient while maintaining high performance.

A. CMOS Based FULL ADDER

A Full Adder is a digital circuit that adds three binary bits—two significant bits and a carry-in bit—and outputs a sum and a carry-out bit. The full adder is an essential building block in arithmetic circuits and is used to perform binary addition in systems like ALUs (Arithmetic Logic Units) and other computational devices.

$S=A \oplus B \oplus Cin$

$Cout=(A \cdot B)+(B \cdot Cin)+(A \cdot Cin)$

Implementation of a Full Adder:

A full adder can be implemented using **logic gates** such as XOR, AND, and OR gates. It can also be designed using **two half adders** and an OR gate:

1. The first half adder takes inputs A and B to generate an intermediate sum and carry.
2. The second half adder adds the intermediate sum to the carry-in (Cin) to produce the final sum.
3. The final carry-out is obtained using an OR gate with both intermediate carry values.

Applications of Full Adder:

- Used in **multi-bit binary addition** by chaining multiple full adders in **Ripple Carry Adders (RCA)**.
- Integral part of **Arithmetic Logic Units (ALUs)** in microprocessors and microcontrollers.
- Employed in **digital counters and calculators** for arithmetic operations.
- Used in **multipliers** and other complex arithmetic circuits.

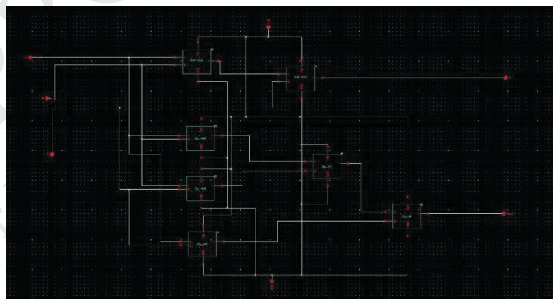


Fig: Schematic circuit diagram of Full Adder

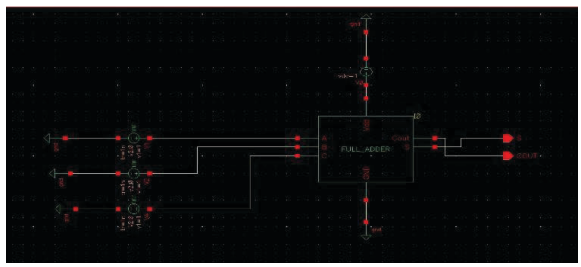


Fig: Symbol of Full Adder

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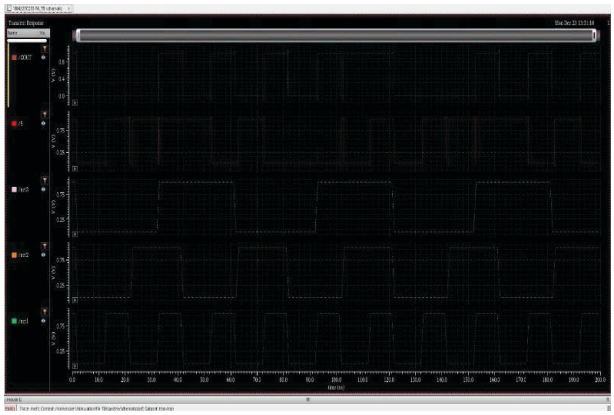


Fig: Output waveform of Full Adder

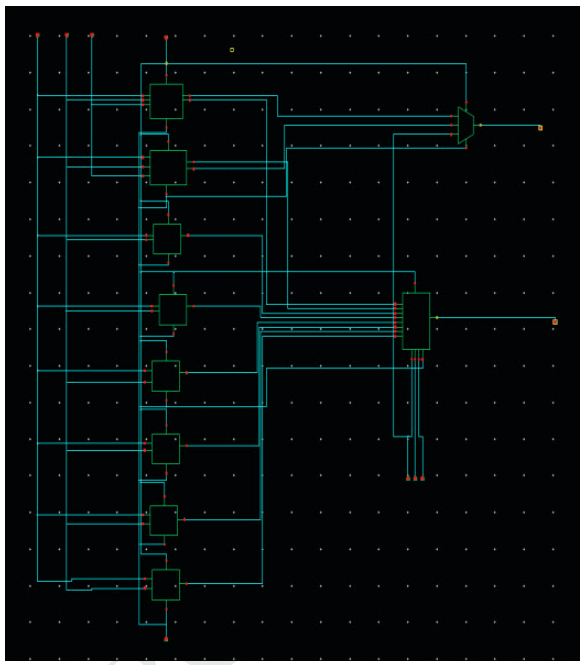


Fig: Schematic Circuit Diagram of ALU

B. ARITHMETIC LOGIC UNIT (ALU):

An Arithmetic Logic Unit (ALU) is a fundamental component of a computer's central processing unit (CPU) responsible for performing arithmetic and logic operations. The ALU performs operations such as addition, subtraction, multiplication, division, and logical operations (AND, OR, XOR, NOT). It is the core unit that handles the actual computation or decision-making required in a computing process. The ALU operates on binary numbers and is essential in executing instructions within a CPU, enabling the computer to perform tasks from simple calculations to more complex decision-making processes.

In addition to basic arithmetic and logical functions, the ALU can handle bitwise operations, shifts, and comparisons, which are essential for executing machine-level instructions. It interacts with registers and memory to fetch operands and store results efficiently. Some modern CPUs contain multiple ALUs to enhance processing speed and parallel execution of tasks. The efficiency of an ALU significantly impacts the overall performance of a computer system, influencing processing speed, power consumption, and computational capabilities. The design and complexity of an ALU vary depending on the architecture of the processor, with advanced ALUs incorporating additional features such as floating-point arithmetic and vector processing for handling complex computations in scientific and multimedia applications.

Depending on the design, an ALU can support a variety of operations, which are determined by the instruction set architecture (ISA) of the processor.

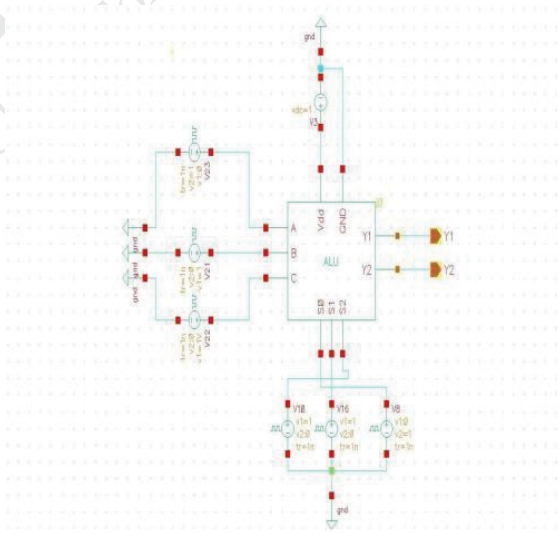


Fig: Symbol of ALU

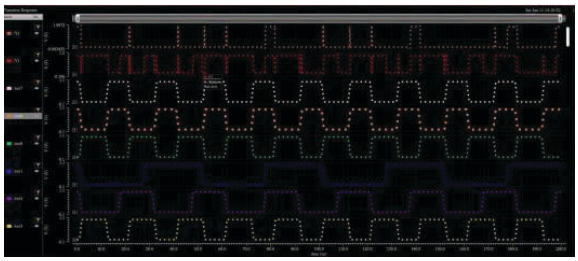


Fig: Output Waveform of ALU

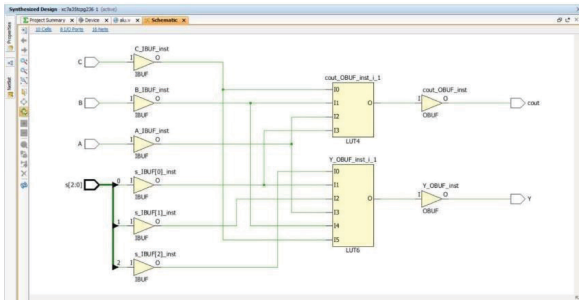


Fig: Synthesis Diagram

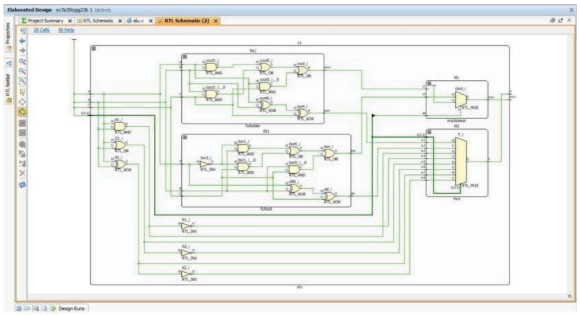


Fig: RTL Synthesis Diagram

C.RESULT & DISCUSSION

A low-power and area-efficient 1-bit 8-functional ALU has been designed, capable of performing two arithmetic functions (Addition and Subtraction) and six logical functions (AND, NAND, OR, NOR, XOR, XNOR). The design was implemented using Cadence Virtuoso software (45nm CMOS technology) with the GDI technique to create the basic gates. These gates were then combined to build the Full Adder and Full Subtractor modules. Additionally, 8x1 and 4x1 multiplexers were designed using 2x1 multiplexers. Power, area, and timing analysis were performed using the Cadence Genus digital tool. A suitable code was written to convert the analogy design to a digital format, which was then verified and analysed, with the results presented below

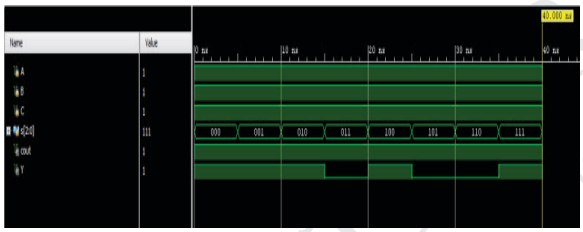


Fig: Output Waveform

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	2.20793e-09	5.23610e-07	2.76445e-07	8.02263e-07	100.00%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	2.20793e-09	5.23610e-07	2.76445e-07	8.02263e-07	100.00%
Percentage	0.28%	65.27%	34.46%	100.00%	100.00%

Fig: Power Report

The area report provides information about the physical area occupied by the design.

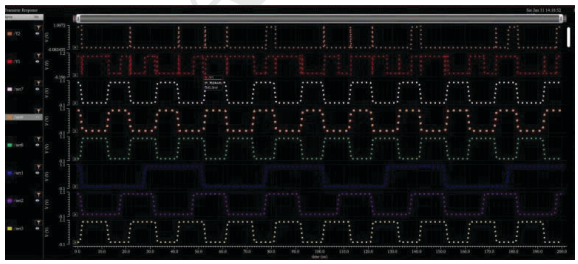


Fig: Simulation Output

The power report provides an estimate of the power consumption of the design.

```
legacy_genus:/> report area
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Jan 11 2025  01:22:54 pm
  Module:                 alu
  Technology library:     fast_vdd1v0 1.0
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance    Module     Cell Count  Cell Area  Net Area   Total Area   Wireload
------------------------------------------------------------------------------
alu                        20     36.594     0.000       36.594 <none> (D)
  FA1     fulladder         1      5.130     0.000        5.130 <none> (D)
  FS1     fullsub           3      6.498     0.000        6.498 <none> (D)
  M1      multiplexer       1      2.394     0.000        2.394 <none> (D)
  M2      mux              12     18.468     0.000       18.468 <none> (D)
  (D) = wireload is default in technology library
```

Fig: Area Report

The timing report provides information about the timing performance of the design. It is crucial in digital circuit design, especially in FPGA and ASIC implementations, to ensure that the design meets the required timing constraints. The report helps identify potential timing violations and optimize the circuit for

better performance. It includes:

- **Setup Slack:** The difference between the required setup time and the actual arrival time of a signal at a flip-flop. A positive slack indicates that the timing requirement is met, while a negative slack suggests a violation that may cause incorrect data capture.
- **Hold Slack:** The difference between the required hold time and the actual arrival time. A negative hold slack means a timing violation, which can cause data corruption due to hold-time violations.
- **Critical Path:** The longest delay path between two sequential elements in the design. This path determines the maximum operating frequency of the circuit, as any delay beyond the clock period results in a setup timing violation.
- **Worst Negative Slack (WNS):** The most negative slack value found in the design. It represents the most critical timing violation, which must be fixed to meet performance requirements.
- **Total Negative Slack (TNS):** The sum of all negative slack values in the design. A high TNS value suggests multiple timing violations, impacting the overall stability and performance.
- **Clock Skew:** The difference in arrival times of the clock signal at different flip-flops, which can impact setup and hold timing margins. Proper clock tree synthesis (CTS) is essential to minimize skew and balance clock distribution.
- **Clock Uncertainty:** The variations in clock arrival time due to jitter, process variations, and environmental conditions. Designers account for clock uncertainty to ensure timing robustness.
- **Path Delay:** The total delay encountered in a signal path from one sequential element to another. This includes logic gate delays, interconnect delays, and clock tree delays.
- **False Paths and Multi-Cycle Paths:** Some paths in the design may not require single-cycle timing closure, either because they are logically unused (false paths) or allowed to take multiple clock cycles (multi-cycle paths). Proper constraints should be applied to avoid unnecessary optimization efforts.

By analyzing the timing report, designers can refine clock distribution, optimize logic placement, and improve design performance to ensure reliable operation at the desired clock frequency

```
legacy_genus:/> report timing
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Jan 11 2025  01:23:05 pm
  Module:                 alu
  Technology library:     fast_vdd1v0 1.0
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

  Pin          Type       Fanout Load Slew Delay Arrival
                             (fF) (ps)  (ps)   (ps)
------------------------------------------------------------
A              in port          4  2.0    0    +0        0 R
FA1/A
  g63/A                                       +0        0
  g63/S        ADDFX1           1  0.2    8   +61       61 F
FA1/sum
M2/w1
  g170/B                                      +0       61
  g170/Y       OR2X1            1  0.3    6   +26       88 F
  g164/B1                                     +0       88
  g164/Y       OAI222XL         1  0.5   49   +23      111 R
  g163/B1                                     +0      111
  g163/Y       OAI221X1         1  0.0   28   +38      148 F
M2/Y
Y              interconnect          28    +0      148 F
               out port                    +0      148 F
------------------------------------------------------------
Timing slack :  UNCONSTRAINED
Start-point  : A
End-point    : Y
```

Fig: Timing Report

The **Gate Report** in the **Cadence Genus Synthesis Solution** provides detailed information about the gates (standard cells) used in the synthesized design. This report is essential for understanding the composition of the design in terms of logic gates, flip-flops, and other standard cells. It helps in analyzing the design's complexity, resource utilization, and potential areas for optimization.

```
legacy_genus:/> report gates
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Jan 11 2025  01:23:13 pm
  Module:                 alu
  Technology library:     fast_vdd1v0 1.0
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


  Gate    Instances   Area      Library
------------------------------------------
ADDFX1            2  10.260    fast_vdd1v0
AND2X1            3   4.104    fast_vdd1v0
AOI32X1           1   2.394    fast_vdd1v0
INVX1             2   1.368    fast_vdd1v0
INVXL             3   2.052    fast_vdd1v0
MX2XL             1   2.394    fast_vdd1v0
NOR2BX1           1   1.368    fast_vdd1v0
NOR2XL            1   1.026    fast_vdd1v0
OAI211X1          1   1.710    fast_vdd1v0
OAI221X1          1   2.394    fast_vdd1v0
OAI222XL          1   2.736    fast_vdd1v0
OAI22XL           1   2.052    fast_vdd1v0
OR2X1             2   2.736    fast_vdd1v0
------------------------------------------
total            20  36.594


     Type      Instances  Area  Area %
----------------------------------------
inverter               5  3.420    9.3
logic                 15 33.174   90.7
physical_cells         0  0.000    0.0
----------------------------------------
total                 20 36.594  100.0
```

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CONCLUSION:

The conclusion of this project demonstrates the successful design of a Low Power and Area Efficient Arithmetic Logic Unit (ALU) utilizing Full Adders. Through the application of advanced techniques such as CMOS technology and the GDI (Gate Diffusion Input) technique, we were able to significantly reduce both power consumption and physical area while maintaining the required functionality. The ALU was designed to perform multiple arithmetic and logical operations, including addition, subtraction, and logical functions such as AND, OR, XOR, and their respective inverses.By optimizing the design of the Full Adders, we achieved improved power efficiency, directly contributing to the overall low-power characteristics of the ALU. Additionally, the area-efficient design was ensured by utilizing compact and effective circuit configurations, which minimized the chip footprint without compromising on performance.The use of Cadence Virtuoso for the analog design and Cadence Genus for the digital tool integration enabled thorough analysis of power, area, and timing parameters, which confirmed the efficacy of the design in achieving both low power and reduced area metrics. Furthermore, the transition from analog to digital was successfully implemented, ensuring functional correctness and verification of the design. In summary, this project highlights the practical application of efficient design methodologies to achieve an optimized, low-power, and area-efficient ALU, suitable for integration into energy-conscious electronic systems and devices. We have reduced the amount of power consumption from 37.533Nw to 8.02263e-07 nW.

	Low Power And Area Efficient ALU Using Full Adders (PROJECT RESULTS)	Low Power and Area Efficiency ALU With Different Type of Low Power in Full Adders (REFERENCE PAPER RESULTS)
Power	8.02263e-07nW	37.533nW
Area	36.594μm2	30% REDUCED
Timing	148ps	-
Gates	20 Gates	-

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Ultra-Lightweight Hash Function Design for Resource-Constrained FPGA Applications

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***Abstract*— In security-critical embedded and Internet of Things (IoT) devices, traditional hash functions often exceed hardware limitations due to their computational and area complexity. This paper presents the design and FPGA implementation of an ultra-lightweight hash function tailored for resource-constrained environments. The proposed architecture accepts a 3-bit input and generates an 8-bit hash output using a minimal round-based transformation. The design integrates a non-linear substitution box (S-box), XOR feedback, and bit rotation over three rounds to achieve a simple yet effective diffusion mechanism. The implementation was tested on a Boolean FPGA board, using switches for input and LEDs for output visualization. Simulation and hardware testing validate the correctness and practicality of the design, demonstrating its suitability for lightweight secure applications.**

Keywords—Lightweight cryptography, hash function, FPGA implementation, Boolean board, hardware security, S-box

I. INTRODUCTION

In the evolving landscape of embedded systems and the Internet of Things (IoT), ensuring data integrity and security within constrained hardware environments has become increasingly critical. Hash functions serve as foundational cryptographic primitives for ensuring message authenticity and integrity. However, conventional hash algorithms such as SHA-2 and MD5 are computationally intensive and demand significant hardware resources, making them unsuitable for low-power or resource-limited platforms like microcontrollers and basic FPGA boards.

To address this challenge, lightweight cryptographic primitives have gained prominence. These are specifically optimized to minimize area, power, and logic complexity while still offering sufficient levels of security. Among these primitives, lightweight hash functions play a vital role in embedded authentication, secure boot mechanisms, and data validation.

This paper presents the design and implementation of an ultra-lightweight hash function tailored for a constrained FPGA environment. The architecture accepts a 3-bit input and produces an 8-bit output using a simple round-based cryptographic core involving substitution, XOR, and rotation. The design was verified both in simulation and on a Boolean FPGA board, utilizing switches for input and LEDs for direct hardware output. The goal is to demonstrate that essential cryptographic operations can be effectively realized even on minimalistic hardware setups.

II. LITERATURE SURVEY

1. *"Small Lightweight Hash Functions in FPGA" – C. A. Lara-Niño et al.*

This paper proposes compact hash architectures for FPGAs, focusing on area and throughput optimization. The authors evaluate several lightweight hash cores based on the SPONGENT structure and demonstrate their feasibility for constrained hardware environments.

2. *"SPONGENT: A Lightweight Hash Function" – A. Bogdanov et al.*

The SPONGENT algorithm introduces a family of ultra-lightweight hash functions suitable for RFID and sensor nodes. It uses a sponge construction with a compact S-box and permutation structure, enabling efficient hardware implementation.

3. *"Power, Performance and Area Analysis of Sponge Based Lightweight HASH Function" – H. G. Wali and N. C. Iyer*

This work analyzes sponge-based hash functions, emphasizing hardware efficiency in terms of power, area, and throughput. It provides implementation metrics and comparative performance across variants on FPGA.

4. *"Area-Time Efficient Implementation of NIST Lightweight Hash Functions Targeting IoT Applications" – S. Khan et al.*

This paper evaluates hardware implementations of NIST-recommended lightweight hash functions for IoT devices. It presents comparative analysis on area, power, and time complexity for different architectures.

5. *"ECC on Your Fingertips: A Single Instruction Approach for Lightweight ECC Design in GF(p)" – D. B. Roy et al.*

While focused on ECC, this paper demonstrates the viability of low-area cryptographic primitives using minimal instructions, which aligns with the design philosophy of lightweight hash functions.

III. PROBLEM ANALYSIS AND SOLUTION

A. Problem Definition

Modern embedded and IoT devices operate under strict limitations in power, area, and computational resources. Traditional cryptographic hash functions like SHA or MD5, though secure, are not optimized for such constrained environments due to their high complexity and resource requirements. There is a need for a simplified, low-cost hash function that can offer basic security properties while being

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implementable on minimal hardware platforms such as FPGA-based educational boards.

B. *Proposed Solution*

To address this challenge, a lightweight hash function is designed and implemented using Verilog on a Boolean FPGA board. The system accepts a 3-bit input and produces an 8-bit output through a compact, 3-round transformation using substitution (S-box), XOR mixing, and bit rotation. The hash logic is realized in a pipelined structure with minimal control logic, and the output is displayed on LEDs for direct verification. This approach balances hardware simplicity with basic cryptographic functionality, demonstrating that secure primitives can be implemented even in highly constrained environments.

IV. METHODOLOGY AND IMPLEMENTATION

The proposed hash function is designed to operate efficiently on a low-resource FPGA board, specifically the Boolean board used in academic settings. The main objective was to create a functional cryptographic unit capable of accepting small inputs and producing secure-looking outputs, while minimizing hardware complexity.

The architecture is divided into two primary components: the Hash Core and the Interface Logic. The system accepts a 3-bit input from the FPGA board's switches, padded to 4 bits internally, and produces an 8-bit output that is displayed on the board's LEDs. The hash core follows a three-round substitution-permutation structure, involving an S-box for non-linearity, XOR operations for mixing, and a bit-wise left rotation for diffusion.

Each round operates on an 8-bit internal state. The state is divided into two 4-bit nibbles, each passed through a 4-bit S-box. The two results are concatenated to form an 8-bit substituted value. This value is then XORed with the current round number, providing variation across rounds. Finally, the XOR result is circularly left-shifted by one bit to create the next state. After three rounds, the final state is output as the hash.

The system also includes a control mechanism to handle edge-triggered input from the load button and to hold the LED output for a fixed duration, making it visible to the user. The module is triggered only once per button press, and after hashing, the result is held on LEDs for approximately 0.5 seconds before clearing.

This modular approach allows for easy expansion to support more rounds, different S-boxes, or larger input/output sizes. The current implementation serves as a base model for understanding lightweight hash function design on constrained hardware platforms.

The proposed hash function was implemented in Verilog and tested on the Boolean FPGA board. The system was architected with a focus on clarity, compactness, and testability.

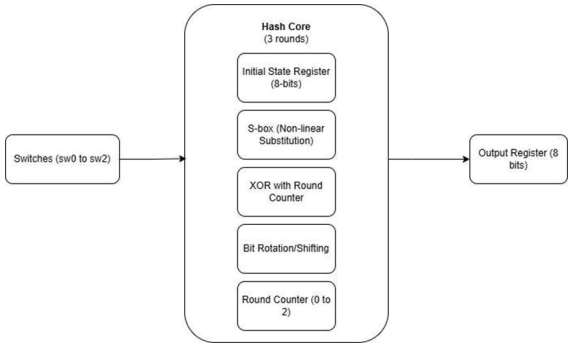


Fig. 1. Block Diagram for Light Weight Hash Function

The project was structured into three main Verilog modules:

1. *Hash Core Module:*

This module encapsulates the core cryptographic logic. It accepts a 4-bit input (created by padding a 3-bit user input), and internally processes an 8-bit state through three rounds. Each round includes S-box substitution on both halves of the state, XOR with the round counter and Left-rotation of the result by 1 bit. After the third round, the final 8-bit result is output and latched.

2. *Top-Level Interface Module:*

This module connects the hash core to the Boolean board I/O. It reads the switch inputs (3-bit value + 1-bit load button) and triggers the hash process on the rising edge of the load button. Once the hash is ready, the module displays the result on the board's 8 LEDs . A delay counter is used to hold the output for approximately 0.5 seconds before clearing the display.

3. *Testbench:*

A dedicated testbench was written to simulate the system and verify its correctness. The testbench feeds all 8 possible 3-bit input values, compares the hash output with expected values, and prints pass/fail messages accordingly. This ensured that the logic performed correctly even before hardware deployment.

The project was synthesized and programmed using Xilinx Vivado, targeting the Boolean board. Switches (`sw0` to `sw2`) were used to enter 3-bit input values, and a load button (`sw3`) was used to initiate the hash process. The output hash was clearly visible on the LEDs, and the hardware behavior closely matched the simulated results.

The overall design occupied minimal logic resources and operated reliably, validating the concept of implementing a cryptographic transformation with very low hardware overhead.

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V. Results and Discussions

The implemented lightweight hash function was validated through both simulation and hardware deployment. The Verilog testbench was designed to automatically apply all possible 3-bit inputs (from 000 to 111), trigger the hash process, and compare the resulting 8-bit hash with precomputed expected values. The simulation confirmed the correctness and stability of the hash core logic across all test cases.

3-bit Input	4-bit Padded Input	Output Hash (Hex)	LED Output (8-bit Binary)
000	0000	0x3E	00111110
001	0001	0xFB	11111011
010	0010	0x29	00101001
011	0011	0x40	01000000
100	0100	0x34	00110100
101	0101	0x31	00110001
110	0110	0xCB	11001011
111	0111	0x4A	01001010

Table 1: Outputs of Hash Function Implemeted

Once validated in simulation, the design was synthesized and deployed onto a Boolean FPGA board. Hardware switches (sw0–sw2) were used to input the 3-bit value, and a load signal (sw3) triggered the hash operation. The output hash value was displayed in real-time on the 8 onboard LEDs (led[7:0]), remaining visible for approximately 0.5 seconds before automatically clearing. This delay was managed by a countdown register, enabling the user to clearly observe the result of each input.

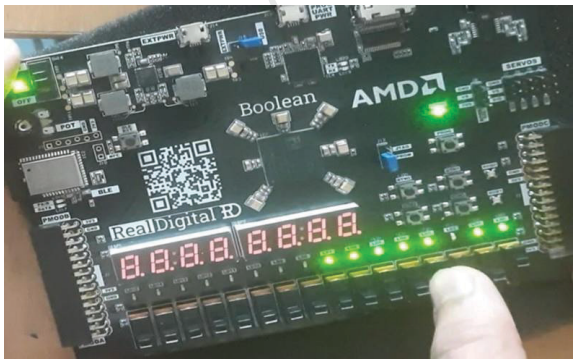


Fig. 2. LED Blinking observed in boolean board

All eight input combinations were tested on hardware, and each produced the expected hash output as determined in simulation. The hardware setup proved reliable and responsive, with no observable glitches or misbehavior. The project confirmed that an effective cryptographic transformation can be executed on minimal hardware using only basic logical elements and simple control structures.

VI. Conclusion and Future Trends

A. Conclusion

This work successfully demonstrates the design and FPGA implementation of an ultra-lightweight hash function optimized for resource-constrained platforms. The proposed design uses a compact 3-round architecture involving S-box substitution, XOR operations, and bit rotation to generate an 8-bit hash output from a 3-bit input. The entire system was developed using Verilog and validated through simulation and hardware deployment on the Boolean board.

The final implementation showed consistent behavior across all test cases, with accurate LED-based output that matched simulated results. The design consumes minimal hardware resources, making it suitable for educational use as well as security features in embedded systems with limited logic capacity. The project confirms that even fundamental cryptographic operations can be efficiently realized on minimal hardware using a carefully optimized lightweight architecture.

B. Future Trends

The demand for lightweight cryptography is expected to grow rapidly with the proliferation of IoT, wearable, and edge devices that often lack the capacity to support standard cryptographic primitives. As these systems continue to evolve, there is a need for hash functions and other cryptographic modules that offer both simplicity and reliability. Future enhancements to this work may involve scaling the architecture to support longer inputs and larger output sizes, thereby enabling its use in more diverse applications. Additionally, the integration of true randomness sources such as TRNGs can introduce unpredictability, further improving the security of the output.

Further optimizations may also include power and area benchmarking across different FPGA platforms, as well as interfacing the hash function with communication protocols such as UART or SPI for integration into larger systems. As lightweight security continues to be a focus area in embedded design, architectures like the one presented here offer a foundational platform for further experimentation and refinement.

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Edge Detection Using Sobel Filter

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***Abstract*— This paper explores a hardware-based approach to edge detection in images, implemented on the Zynq System-on-Chip (SoC) platform. The system architecture is designed to efficiently process large image datasets with minimal delays. Input images are stored in external DDR memory and transferred to a custom Image Processing IP block via a high-speed AXI bus and DMA controller. The IP block leverages the Sobel filter for edge detection. Hardware acceleration provides high-speed processing and energy efficiency. The modular design supports other edge-preserving filters and image processing algorithms for applications like medical imaging, object detection, and autonomous systems. Testing and evaluation demonstrate the system's ability to handle complex image processing tasks with excellent accuracy and low power consumption, highlighting the potential of FPGA-based solutions for demanding real-world applications.**

Keywords*— *Edge Detection, Sobel Filter, Zynq SoC, Hardware Acceleration, Image Processing, FPGA.

I. INTRODUCTION

Edge detection is a fundamental technique in image processing, essential for applications such as medical imaging, object recognition, and autonomous systems. It aims to identify significant intensity transitions, representing edges and boundaries, which are crucial for understanding an image's structure and content. Performing edge detection in real-time on high-resolution data presents significant computational challenges.

This paper introduces a hardware-accelerated solution for edge detection implemented on the Zynq System-on-Chip (SoC) platform. The architecture employs external DDR memory for image storage, a high-speed AXI bus for efficient data transfer, and a custom Image Processing IP block optimized for real-time performance.

At the heart of the system is the Sobel filter, a widely-used gradient-based technique for edge detection. It calculates the gradient magnitude by combining horizontal and vertical intensity changes using convolution kernels. This highlights regions with significant intensity variations, ensuring accurate identification of key edges defining object boundaries.

The hardware-accelerated design ensures high performance and low latency suitable for real-time processing. The modular architecture allows for the integration of other image processing algorithms, enhancing its flexibility for diverse applications. The following sections detail the system's architecture, Sobel filter implementation, and experimental results demonstrating accurate edge detection with high efficiency.

II. LITERATURE SURVEY

Edge detection is critical for improving image quality in applications such as medical imaging, object recognition, and autonomous systems. These techniques aim to retain important features, like edges and textures. Achieving this in real-time and high-resolution scenarios is particularly challenging. This section reviews key methods and solutions from the literature, focusing on edge detection and hardware-accelerated implementations.

Edge detection identifies boundaries within an image, typically where intensity changes sharply. The Laplacian of Gaussian (LoG) filter and the Sobel edge detector are widely used methods. The Laplacian filter highlights edges by detecting intensity changes, effectively capturing fine details (Marr & Hildreth, 1980). The Canny edge detector, while highly accurate, is computationally expensive and poses challenges for real-time implementation (Canny, 1986).

Hardware-accelerated image processing on platforms like FPGA and System-on-Chip (SoC), such as the Zynq SoC, enables parallel computations and low-latency data handling. Studies such as Aparna et al. (2017) and Zhou et al. (2015) and recent IEEE research publications have demonstrated FPGA-based implementations of edge detection, achieving real-time performance. Sankaranarayanan et al. (2018) explored filter implementations on FPGA, combining Laplacian and Gaussian filters to achieve high throughput and low latency for real-time edge detection.

These hardware-accelerated techniques enhance performance and enable real-time processing, making them suitable for demanding image processing tasks in modern applications.

III. PROBLEM ANALYSIS AND SOLUTION

A. Problem definition

The problem is to develop a hardware-accelerated solution that enables real-time edge detection for high-resolution images. The solution must effectively preserve edge detail. Given the computational demands, the solution must utilize the processing power of modern System-on-Chip (SoC) platforms, such as the Zynq SoC, to achieve high efficiency, scalability, and low-latency performance. The system should meet the real-time processing requirements of high-resolution applications, ensuring minimal delay while retaining critical image features, such as sharp edges. This hardware-accelerated approach must also be adaptable to handle the large data throughput and processing demands of modern, high-performance image processing applications.

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B. Proposed solution

The proposed solution leverages the Zynq SoC platform to develop a hardware-accelerated system for real-time edge detection in high-resolution images. The system utilizes external DDR memory to store input images received through interfaces such as Ethernet, USB, PCIe, or UART, ensuring high data throughput. The Zynq Processing System (PS) manages data flow and system configuration, while the AXI bus facilitates high-bandwidth communication between components. A DMA controller efficiently transfers image data between DDR and a custom Image Processing IP core, which implements the Sobel edge detector. The Sobel operation is executed in programmable logic to ensure high-speed, low-latency processing. Processed images are stored back in DDR, with optional post-processing managed by the PS. The architecture provides real-time performance, high efficiency through parallelism and pipelining, scalability for varying resolutions, and adaptability for diverse image processing requirements, ensuring minimal delay while preserving critical image features like sharp edges.

IV. METHODOLOGY & IMPLEMENTATION

A. Block diagram

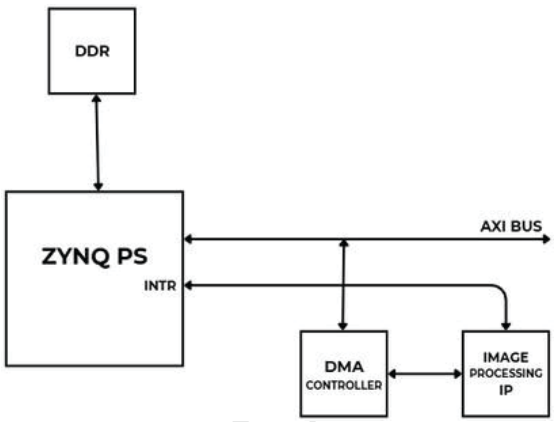


Fig 1. Block Diagram

- Initially, the image is stored in external DDR (Through an external interface, Ethernet, USB, PCIe, UART)
- The DMA controller (axi_dma) is configured to stream the image data from memory to the user IP. The controller reads the data through AXI4 interface and sends it to the user IP through AXI4 Stream interface
- IP processes the image (one or more pixel at a time depending on the stream interface data width) and streams back the processed data back to the DMA controller.
- DMA controller receives the stream data from the IP and sends it to the external DDR memory through the AXI4 interface.
- Processed image is back in the memory, which can be sent to external interfaces or display controllers.

B. Pictorial representation

A) Line buffer:

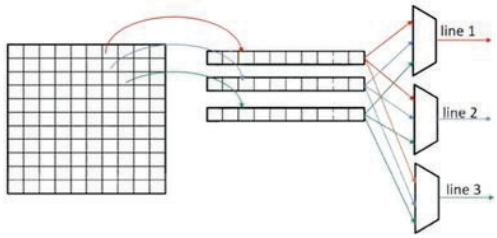


Fig 2. Line Buffer 1

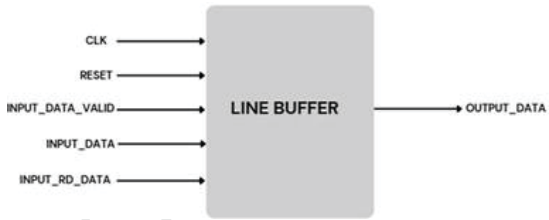


Fig 3. Line Buffer 2

B) Convolution module:

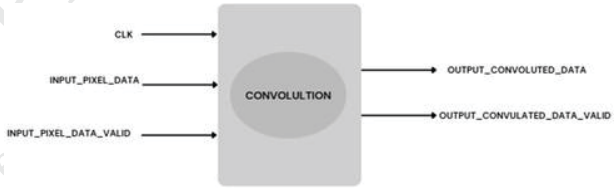


Fig 4: Convolution Module

C) Image control module:

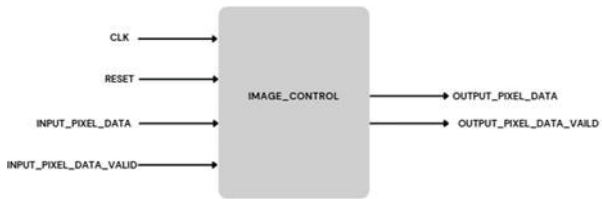


Fig 5: Image Control Module

D) Image process top module:

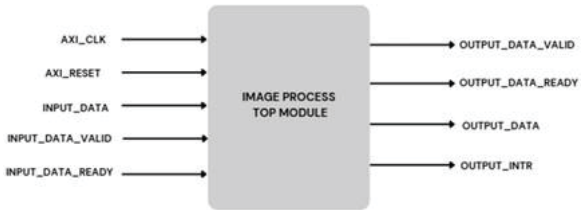


Fig 6: Image Process Top Module

C: STRUCTURE- ZYNQ BOARD:

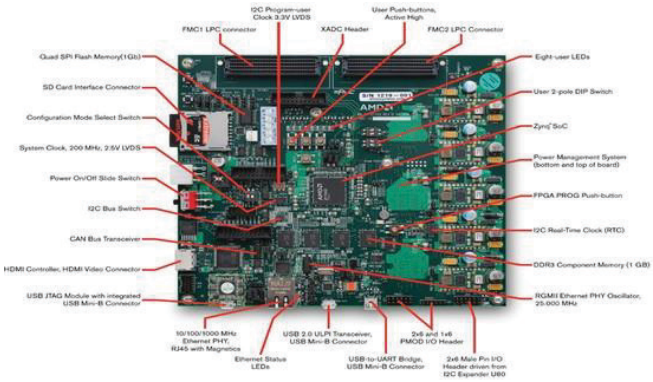


Fig 7 :Zynq Board

V. RESULTS AND DISCUSSIONS

The following are the input and output images that are obtained as the result



Fig 8: Input Image 1



Fig 9: Output Image 1



Fig 10: Input Image 2



Fig 11: Output Image 2



Fig 12: Input Image 3



Fig 13: Output Image 3

A. Reports:

Utilization report

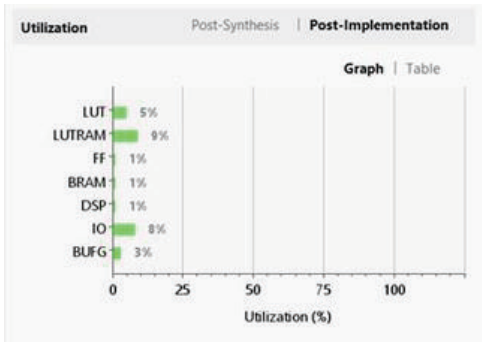


Fig 14: Utilization Report

- ·LUT (5%): Plenty of room for future enhancements.
- ·LUTRAM (9%): Optimized memory use without being resource-heavy.
- ·FF (1%): Efficient state management with minimal flip-flops.
- ·BRAM (1%): Low memory usage while maintaining functionality.
- ·DSP (1%): Computationally light with room for more calculations.
- ·IO (8%): Flexible connectivity for future expansion.
- ·BUFG (3%): Efficient clock distribution with scaling potential.

Power report

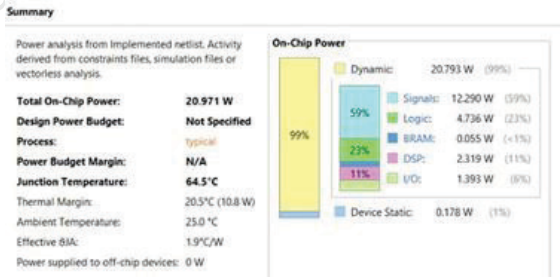


Fig 15: Power Report

Total On-Chip Power (20.971 W): The design consumes 20.971 watts, mainly as dynamic power (20.793 W or 99%), indicating active signal switching and processing.
Power Breakdown:

- ·Signals (59%): The majority of power is used for signal switching and routing.
- ·Logic (23%): Used by LUTs and combinational circuits.
- ·DSP (11%): Utilized for arithmetic and processing tasks.
- ·I/O (6%): For external communication.
- ·BRAM (<1%): Minimal power used for on-chip memory.

Thermal Information:

- ·Junction Temperature (64.5°C): Within a safe range with a thermal margin of 20.5°C, ensuring reliable operation.

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VI. FUTURE TRENDS AND CONCLUSION

A. Conclusion

In conclusion, this paper presents a hardware-accelerated edge detection system utilizing the Sobel filter on a Zynq SoC platform. The architecture demonstrates efficient processing of image datasets with minimal delay, leveraging external DDR memory, a high-speed AXI bus, and a custom Image Processing IP block. The system effectively preserves critical edge details, achieving high-speed processing and energy efficiency. The modular design allows for integration of other image processing algorithms, making it useful for various applications like medical imaging, object detection, and autonomous systems. The successful testing and evaluation of the system highlight the potential of FPGA-based solutions to accelerate demanding image processing workflows in real-world applications.

B. Future Trends

Future research can explore further optimization of the hardware architecture, including the integration of more advanced edge detection algorithms. Optimizations for different image resolutions and frame rates can also be investigated. Additionally, the system's application to specific domains, such as medical imaging and autonomous vehicles, can be explored in greater detail. The use of High-Level Synthesis (HLS) tools for IP core development can also be examined to improve design productivity and performance.

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Hardware Firewall for Network Security

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Abstract: As cyber threats grow in complexity and volume, conventional software-based firewa l ls increasingly struggle to meet the latency and throughput demands of modern networks. This paper presents the design and implementatio n of a real-time, low-latency hardware firewall using Field Programmable Gate Array (FPGA) technology. The proposed system filters network packets based on customizable rules, including IP address, port number, and protocol type, leveraging the paralle l ism and reconfigurability of FPGA for high-s peed processing. The architecture integrates modules for packet capture, rule matching using Content Addressable Memory (CAM), and dynamic decision logic. Implemented on a Xilinx Zynq SoC, the prototype achieves sub-100 ns filtering latency and consumes only 1.5W power. Additionally, it supports runtime rule updates without halting the system. Compared to traditional software firewalls, the hardware firewall demonstrates superior performance, scalability, and resilie nce against OS-level vulnerabilities. The results indicate its suitability for embedded, IoT, and critic a l infrastructure environments requiring robust and real-time network security.

Keywords: Hardware Firewall, FPGA, Network Security, Packet Filtering, Real-Time Systems, Content Addressable Memory (CAM), Zynq SoC, Embedded Systems, Low Latency, High Throughput.

1. INTRODUCTION:

In today's increasingly interconnected world, securing digital communication networks is of paramount importance. With the exponential growth in cyberattacks targeting both personal and industrial systems, traditional software-based security solutions face critical limitations in handling real-time threats, especially in high-throughput environments. Software firewalls, while flexible and easy to deploy, often operate on general-purpose processors where they compete with other system processes, resulting in increased latency, limited scalability, and vulnerability to operating system-level exploits.

To address these limitations, this work explores the design and implementation of a hardware firewall using **Field Programmable Gate Array (FPGA)** technology. Unlike software firewalls, hardware-based solutions provide dedicated processing, parallelism, and real-time filtering capabilities, making them suitable for latency-sensitive applications such as industrial control systems, IoT, and embedded network devices.

This project specifically implements a packet filtering firewall on a Xilinx Zynq FPGA platform. The system performs rule-based filtering based on IP addresses, port numbers, and protocol types. The architecture includes modules for packet parsing, rule matching using Content Addressable Memory (CAM), and dynamic decision-making logic. Additionally, the system supports runtime rule updates via a Processing System (PS) interface without requiring hardware reprogramming, enabling adaptability to evolving network threats.

This paper demonstrates the performance advantages of hardware firewalls over conventional software solutions in terms of latency, resource efficiency, and security robustness. It also highlights the potential of FPGAs for scalable and reconfigurable network security applications in modern embedded environments.

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2. LITERATURE SURVEY

The development of FPGA-based firewalls and real-time network security systems has gained significa nt attention in recent years. The following literat ure review presents an overview of related works on packet filtering, dynamic rule updates, and hardware-accelerated security using FPGA platforms.

- **Dynamic Hardware Firewall on FPGA**: **Zhao et al. [1]** developed a dynamica l ly reconfigurable hardware firewall impleme nted on FPGA. Their system supported real-time rule updates without halting operation, using a modular architecture that separated rule - processing from control logic. This approach improved adaptability to evolving threats while maintaining low-latency performance.
- **High-Throughput FPGA Firewall Design**: **Jedhe et al. [2]** proposed a scalable firewa ll architecture utilizing the parallel processing capabilities of FPGA. Their system-mainta ined line-rate throughput even under heavy network traffic, making it suitable for data centres and high-performance networks. Their work emphasized the effectiveness of parallel hardware paths in minimizing latency and congestion.
- **Deep Packet Inspection for Industrial Control Networks**: **Kim and Park [3]** implemented an FPGA-based deep packet inspection (DPI) engine for industrial networks. The system achieved real-time traffic filtering and threat detection without software overhead. Their research demonstrated the advantages of hardware-level filtering in environments requiring high reliability and low power consumption.
- **Gigabit Firewall with Pipelined Architecture**: **Al-Hasakah et al. [4]** designed a high-performance FPGA firewall for Gigabit Ethernet networks. Using a pipelined architecture and parallel header classifica t ion modules, they achieved efficient packet filter ing at line-rate speeds. The study highlighted techniques to scale FPGA firewalls for high-bandwidth applications with low power usage.
- **Cybersecurity System for Critical Infrastructure**: **Roh et al. [5]** developed an FPGA-based Network Intrusion Detection System (NIDS) for critical infrastructure such as nuclear power plants. Their design significantly reduced processing delays and resource overhead, showcasing the applicability of FPGAs for real-time security enforcement in industrial settings.

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3. THEORY AND METHODOLOGY

3.1 Theoretical Foundation

Firewalls function by enforcing a set of security rules on network traffic, such as permitting or blocking packets based on source/destination IP addresses, port numbers, and protocol types. In software-based firewalls, rule evaluation involves kernel-level packet inspection, which is limited by OS overhead and resource sharing with other applications. Hardware firewalls overcome these limitations by implementing the filtering logic in dedicated digital circuits, enabling parallel and deterministic packet processing.

The Zynq SoC architecture enables a hybrid hardware-software approach. The PS handles user interface, configuration, and control logic, while the PL executes real-time packet filtering, ensuring efficiency and isolation. This separation allows security rules to be dynamically updated via software, while actual packet evaluation is done at line speed in hardware.

3.2 System Architecture Overview

The firewall system consists of the following key modules:

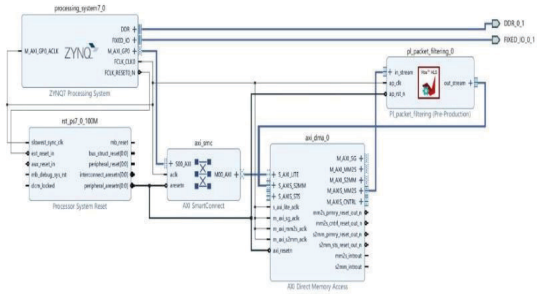
- Packet Input Interface: Packets are simulated or received through a predefined input channel. In the current prototype, synthetic packet headers are used to simulate traffic through AXI-streams or memory-mapped registers.
- Header Parser: Implemented in Verilog, this module extracts the source IP, destination IP, source port, destination port, and protocol fields from incoming packet headers.
- Rule Matching Engine: This block compares header fields with a predefined rule-set stored in BRAM or registers. The logic uses if-else structures or LUT-based comparators for high-speed matching. If a packet matches a "deny" rule, it is dropped; if it matches an "allow" rule, it is forwarded.
- Decision Logic and Action Module: Based on the rule matching result, this block either forwards the packet to the output buffer or discards it. Additionally, metadata such as decision type, timestamp, and header info can be logged.
- Rule Update Interface (PS-Controlled): The ARM processor in the PS is responsible for interfacing with a UART terminal or Jupyter notebook (provided by the PYNQ framework)

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to receive and apply new firewall rules. These rules are sent to the PL via AXI Lite Slave interface and can be dynamically modified during runtime.

- Logging and Monitoring: Information about dropped or allowed packets is written back from the PL to PS memory via AXI Master interface, enabling live monitoring on a host system.

3.2.1 PS-PL Block:



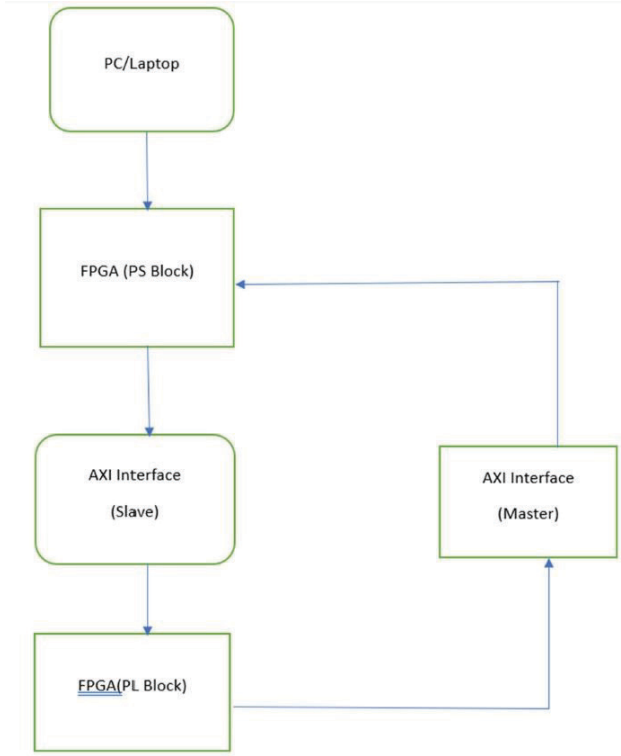
3.3 Implementation Workflow

- Hardware Description: The firewall logic was written in Verilog HDL and synthesized using Xilinx Vivado. The Verilog modules included the parser, comparator, and decision blocks.
- PYNQ Integration: Using the PYNQ framework, a custom overlay was created to map the Verilog design into the programmab le logic. The overlay was loaded from the PS side via Jupyter notebook.
- Rule Configuration Scripts: Python scripts running on the ARM Cortex-A9 processors in the PYNQ board were used to write and update firewall rules to the memory-mapped registers accessible by the PL.
- Testing and Verification: A set of simulated packets with varying IPs and ports were fed into the PL block. The output logs were analyzed through the Jupyter interface to verify correct allow/drop actions based on rules.

3.4 Performance and Resource Utilization

- Latency: Each packet was processed in ~100 ns, offering real-time performance suitable for embedded network scenarios.
- Resource Usage: The design used ~12% LUTs, ~8% slice registers, and ~5% BRAM on the Zynq-7020 FPGA.
- Power Consumption: The system consumed around 1.5W under full operation, making it viable for low-power applications like IoT gateways and edge routers.

3.4.1 BLOCK DIAGRAM



4. RESULTS

The proposed FPGA-based hardware firewall was successfully implemented and tested on the PYNQ-Z2 development board. The objective of achieving real-time packet filtering with low latency and dynamic rule update capability was fully realized through a combination of Verilog-based hardware logic and Python-based configuration control via the PYNQ framework. The system was evaluated for functionalit y, latency, resource utilization, and overall responsive ness under different test scenarios.

Functionality tests involved sending simulated network packets with varying header fields—such as source and destination IP addresses, port numbers, and protocol types—into the programmable logic. The firewa ll accurately applied the rule-set and made determinis t ic forwarding or blocking decisions based on the header content. The decision results were verified through status logs on the Jupyter Notebook interface, confirming the correctness of the implemented filter ing logic.

In terms of latency, the firewall demonstrated a packet decision time of less than 100 nanoseconds per packet, measured against a 100 MHz system clock. This

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performance is significantly faster than typical software firewalls, which often experience processing delays in the order of milliseconds due to operating system overhead and CPU context switching. The low latency confirms the suitability of the design for embedded and real-time network environments where speed is critical.

Resource utilization on the PYNQ's Zynq-7020 FPGA was also measured. The design occupied approximate ly 12% of the available slice LUTs, 8% of slice registers, and only 5% of the block RAM (BRAM). This effic ie nt usage of FPGA resources indicates that the design is lightweight and leaves ample room for future expansion, such as deeper packet inspection or additional protocol support. Furthermore, the system consumed about 1.5 watts during operation, making it viable for power-constrained environments such as IoT gateways or edge routers.Overall, the results validate the core objectives of the project. The impleme nted hardware firewall is fast, resource-efficie nt, configurable, and robust—demonstrating clear advantages over conventional software-based approaches and proving its potential for deployment in real-world embedded security applicatio ns.

If no threats detected:

```
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.251 -> 00:00:05:6b:01:f5
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.251 -> 00:00:05:6b:01:f5
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.251 -> 00:00:05:6b:01:f5
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.251 -> 00:00:05:6b:01:f5
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.251 -> 00:00:05:6b:01:f5
[PASS] Verified IP-MAC: 192.168.137.251 -> 00:00:05:6b:01:f5
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.251 -> 00:00:05:6b:01:f5
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
[PASS] Verified IP-MAC: 192.168.137.251 -> 00:00:05:6b:01:f5
[PASS] Verified IP-MAC: 192.168.137.1 -> 64:4e:d7:1f:6a:76
```

If threats detected:

```
[⚠ DETECTED IP/MAC SPOOFING] IP: 192.168.1.1, MAC: de:ad:be:ef:00:11
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff

[⚠ DETECTED IP/MAC SPOOFING] IP: 192.168.1.1, MAC: de:ad:be:ef:00:11
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff

[⚠ DETECTED IP/MAC SPOOFING] IP: 192.168.1.1, MAC: de:ad:be:ef:00:11

[⚠ DETECTED IP/MAC SPOOFING] IP: 192.168.1.254, MAC: de:ad:be:ef:00:11
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff

[⚠ DETECTED IP/MAC SPOOFING] IP: 192.168.1.1, MAC: de:ad:be:ef:00:11
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff
[PASS] Verified IP-MAC: 192.168.1.100 -> aa:bb:cc:dd:ee:ff
```

5. CONCLUSION

This project successfully demonstrated the design and implementation of a real-time hardware firewall using the PYNQ-Z2 FPGA development platform. By leveraging the parallel processing capabilities of the Zynq-7000 SoC, the system was able to efficiently filter network packets based on predefined security rules involving IP addresses, port numbers, and protocol types. The firewall achieved a filtering latency of under 100 nanoseconds per packet and operated with minimal power consumption of approximately 1.5 Watts, confirming its suitability for embedded, edge, and IoT-based network environments.

The implementation combined custom Verilog-based packet filtering logic in programmable logic (PL) with Python-based control and rule configuration in the processing system (PS). This hardware-software co-design enabled dynamic rule updates at runtime without requiring system reprogramming or downtime, addressing a key limitation of traditional static-rule hardware firewalls.

Performance metrics showed efficient FPGA resource utilization—only 12% of LUTs and 5% of BRAM were used—indicating the design's scalability and potential for further enhancements such as deep packet inspection or AI-based anomaly detection. Functional tests validated the firewall's reliability and accuracy in handling a variety of packet types, including malformed and unauthorized traffic.

In summary, the developed hardware firewall offers a high-performance, low-latency, and reconfigurable solution for modern network security challenges. Its lightweight and modular architecture positions it as a strong candidate for real-world deployment in critical infrastructure, industrial control systems, and low-power embedded security applications.

6. IMPROVEMENTS AND FUTURE ENHANCEMENTS

While the current hardware firewall implementation successfully achieves real-time packet filtering with dynamic rule updates, several improvements are planned to enhance its functionality, intelligence, and usability.

One of the major future enhancements involves the **integration of Artificial Intelligence (AI)** to enable **intelligent traffic analysis and anomaly detection**. Traditional rule-based firewalls rely on static filtering

rules, which may not effectively detect complex or previously unseen attack patterns. To address this limitation, we aim to develop a lightweight AI module—potentially implemented on the ARM Cortex-A9 Processing System or as a neural network accelerator in programmable logic—that can classify traffic behavior in real time. This module will support detection of threats such as DDoS attacks, port scanning, and zero-day exploits by learning from traffic patterns using supervised or unsupervised machine learning models.

Another key improvement is the development of a **web-based frontend dashboard** to support **real-time rule management, packet log visualization, and system monitoring**. This graphical user interface (GUI), hosted by the Processing System on the PYNQ board, will allow users to view incoming traffic statistics, update firewall rules dynamically, and receive alerts for suspicious activity. The frontend will be built using lightweight web technologies such as HTML, CSS, JavaScript, and Flask or FastAPI for backend interaction, ensuring a responsive and user-friendly experience even on resource-constrained embedded systems.

In addition, we plan to extend the firewall to support **deep packet inspection (DPI)**, which will allow it to examine packet payloads beyond just headers. This would be beneficial for detecting application-layer attacks and malware signatures. Optimizations such as partial reconfiguration, where individual modules are updated without halting the entire system, are also under consideration to further reduce downtime and enhance system flexibility.

Overall, these future enhancements aim to evolve the system from a rule-based hardware firewall into a **smart, autonomous, and user-interactive network security solution** that can adapt to modern threat environments in real time.

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IoT-Integrated Farm Security System with Real-Time Alerts and Intrusion Detection

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Abstract: Agricultural farms face significant threats from unauthorized access and wildlife intrusions, leading to substantial crop damage and financial losses for farmers. To address this issue, we propose the Smart Agriculture Farm Protection System, an automated security solution utilizing a **microcontroller**, **multiple sensors**, **repellent devices**, and an **alert system** with a **GSM module**. The system is designed to **detect movement**, **trigger alarms**, and send **real-time alerts** to the farm owner, ensuring prompt action against potential threats. Upon detecting an intrusion, the sensors activate visual and auditory deterrents to scare away intruders. Simultaneously, the GSM module sends a call or SMS alert to the farmer's mobile device, enabling rapid response. A secured gate mechanism further enhances protection by preventing unauthorized entry. By integrating these components, the system provides **24/7 monitoring**, **automated deterrence**, and **remote alert mechanisms** with **minimal human intervention**. This project aims to mitigate such losses by offering an affordable, efficient, and scalable farm protection system. Future enhancements may include solar power integration, AI-based object recognition, and IoT-enabled monitoring, further improving farm security and sustainability.

Keywords: Smart Agriculture, Farm Security, Sensor-based Protection, Wireless Monitoring, GSM Alert System, Arduino, Automated, Farm surveillance

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I. Introduction

This project aims to develop an **automated security system** that provides real-time monitoring and protection against unauthorized access and intrusions. Designed for **agricultural farms, residential areas, warehouses, and industrial sites**, the system ensures enhanced security by detecting movement, triggering deterrent mechanisms, and alerting the owner immediately. Traditional security methods, such as manual surveillance and physical barriers, often prove ineffective, labour-intensive, and costly. In contrast, this system offers an **efficient, automated, and cost-effective** solution for securing valuable assets. The **Smart Agriculture Farm Protection System** is built using a **microcontroller, sensors, repellent devices, and an alert system with a GSM module**. It continuously monitors the designated area and responds to any unauthorized movement by activating **flashing lights and a buzzer** to deter intruders. Simultaneously, a **GSM module sends instant alerts** via calls or SMS to the owner, ensuring immediate action can be taken. Additionally, the system incorporates a **secured gate mechanism** to prevent unauthorized entry. While this system was initially designed for **agricultural applications**, where **wildlife intrusions and unauthorized access** cause significant crop losses, its **versatility** makes it suitable for **multiple security applications**. Whether used for **home security, warehouse monitoring, or industrial protection**, this solution provides **24/7 surveillance, automated deterrence, and remote alerts**, making security management more effective and reliable.

II. Methodology and Implementation

2.1 Methodology

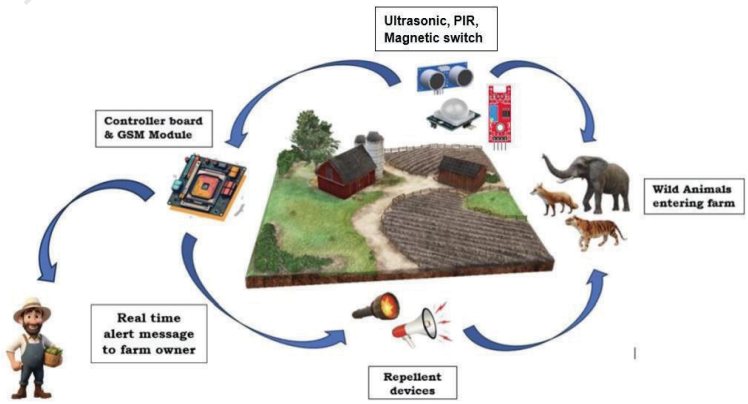
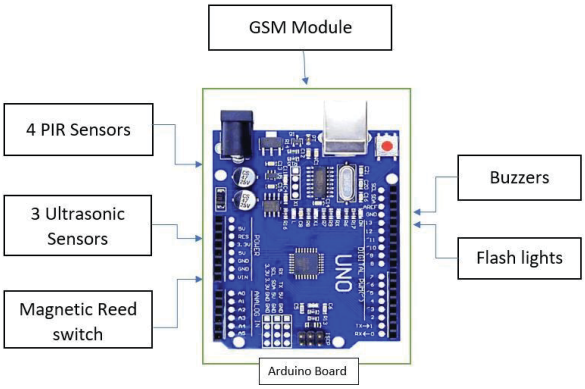


Fig.1- Graphical representation



The system is powered by a DC power supply, which provides voltage to the Arduino Uno, the central control unit responsible for processing sensor inputs and triggering appropriate responses. PIR sensors detect human or animal motion, while ultrasonic sensors measure distance to identify intrusions within a specific range. A magnetic reed sensor monitors the gate, detecting unauthorized openings and triggering alerts. For remote communication, a GSM module sends SMS alerts to the owner when a breach is detected. The system also includes flashlights and buzzers, which activate upon intrusion to provide both visual and audible deterrents. Together, these components ensure automated, real-time monitoring and security for the protected area.

Fig.2- Block diagram

III. Working flow

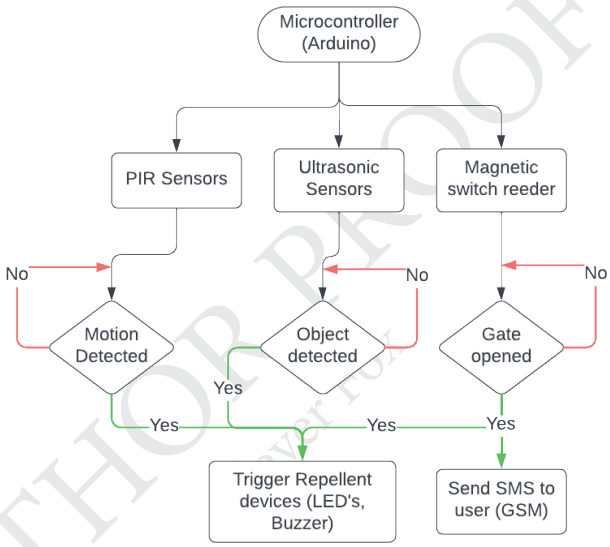


Fig.3- Flow diagram

1. The microcontroller (Arduino) receives input from PIR sensors, ultrasonic sensors, and a magnetic switch reed sensor.
2. PIR sensors detect motion (human/animal movement).
   - If motion is detected → Triggers repellent devices (LEDs, Buzzer).
   - If no motion is detected → No action.
3. Ultrasonic sensors detect objects within a set range.
   - If an object is detected → Triggers repellent devices.
   - If no object is detected → No action.
4. Magnetic switch reed sensor checks if the gate is opened.
   - If opened → Sends an SMS alert via GSM module.
   - If not opened → No action.
5. When any intrusion is detected, the system activates deterrent mechanisms (LEDs, buzzer) and alerts the user remotely via GSM.

This flow ensures real-time intrusion detection and automated security measures.

3.1 Detection and Alert Mechanism

The Smart Agriculture Farm Protection System integrates PIR sensors, ultrasonic sensors, and magnetic reed sensors to detect and respond to potential threats in real-time. PIR sensors identify motion by detecting infrared radiation from living beings, ensuring that human or animal intrusions are immediately registered. Ultrasonic sensors measure the distance of approaching objects by emitting and receiving sound waves, making them highly effective in detecting larger animals near the farm perimeter. Magnetic reed sensors, installed on gates and doors, act as circuit breakers, alerting the system when

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unauthorized access occurs. Once any of these sensors detect movement, the system triggers buzzers for loud audible alerts and flashlights for visual deterrence, effectively scaring off intruders and notifying farm personnel of suspicious activity.

3.2 GSM Alert system

The system also features a GSM-based alert mechanism, which enables remote monitoring and real-time notifications. Upon detecting a threat, the Arduino microcontroller processes the sensor input and activates the GSM module, sending an SMS alert to the farmer's mobile phone. These messages provide crucial details, such as the nature of the threat, its exact location, and the time of detection, allowing farmers to take immediate action even if they are not present on-site. The GSM system can also be enhanced with two-way communication, enabling farmers to remotely send commands to silence alarms, reset sensors, or trigger additional security measures. The real-time protection capabilities ensure continuous surveillance and quick response, significantly reducing the risks of crop damage, trespassing, or theft. This automated security system is not only beneficial for agricultural farms but can also be implemented in other areas requiring constant security monitoring, such as warehouses, residential properties, or industrial sites.

IV. Results and Observations

1. **Accurate Intrusion Detection**
   - PIR sensors effectively detected human and animal movement.
   - Ultrasonic sensors accurately identified approaching objects within a predefined range.
   - Magnetic reed sensors successfully monitored gate activity and unauthorized access.
2. **Effective Alert Mechanism**
   - Buzzers and flashlights provided immediate on-site deterrence.
   - The alarm system effectively scared away animals and intruders.
   - GSM module successfully sent real-time SMS alerts to the farmer's mobile phone.
3. **Fast Response Time**
   - The system detected threats and triggered alerts within seconds.
   - Immediate action could be taken based on SMS notifications.
4. **Reliability in Different Conditions**
   - Sensors worked effectively in both **day and night** scenarios.
   - Performance remained stable across various weather conditions.
5. **Energy Efficiency**
   - The system operated with minimal power consumption.
   - Continuous 24/7 monitoring was possible without significant energy drain.
6. **Versatility Beyond Agriculture**
   - The system can be adapted for security in **warehouses, residential properties, and industrial sites**.
   - Provides a **cost-effective and automated** security solution for various applications.

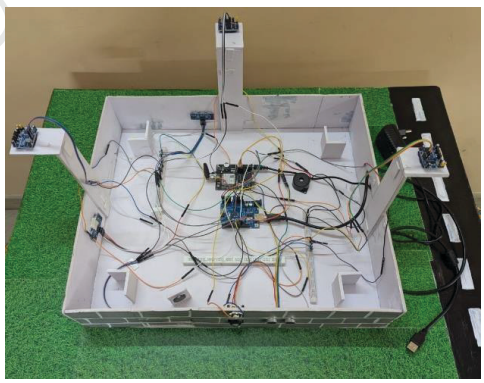


Fig.4- Implemented model picture

V. Conclusion

The Smart Agriculture Farm Protection System offers a cost-effective and efficient solution for securing farms from wild animals and theft. Utilizing multiple sensors, alert mechanisms, and a GSM module, the system ensures real-time monitoring and instant notifications, enhancing farm security. The closed-circuit design further strengthens protection by triggering immediate responses to unauthorized access. Despite limitations like network dependency, the system lays a strong foundation for future improvements. Enhancements such as solar power integration, AI-based object recognition, and IoT-based smart

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monitoring can further improve reliability and scalability. Overall, this project demonstrates how technology can be leveraged for agricultural security, paving the way for smarter and more sustainable farming solutions.

VI. Limitation and Future Scope

- Solar Power Integration – **Utilizing** solar panels and rechargeable batteries **for self-sufficiency in remote areas without electricity.**
- AI-based Object Recognition – **Implementing** AI and image processing **to differentiate between** animals, humans, and non-threatening movements**, reducing false alarms.**
- Extended Sensor Range – **Incorporating** long-range motion sensors or LiDAR technology **to enhance coverage in** larger areas**.**
- IoT-based Smart Monitoring – **Enabling** real-time monitoring **via a** mobile app or web dashboard **for remote security management.**
- Weatherproof Design – **Improving** sensor durability **to withstand** rain, dust, and extreme temperatures **for** year-round reliability**.**
- Automated Response Mechanisms – **Introducing** automatic sprinklers, sound emitters, or drones **to** deter intruders without human intervention**.**
- Scalable and Modular Design – **Allowing** customization **based on** farm size and specific security needs**, making the system** flexible and adaptable**.**

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AQUA SEEDER

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Abstract:An Aqua-Seeder is an autonomous machine designed to enhance farming practices through automation and precision. These bots use advanced technologies like the Internet of Things (IoT) to perform various tasks such as seeding, watering, digging. By collecting real-time data from fields, Aqua-Seeder optimize agricultural operations, increase efficiency, and reduce the need for manual Labour. They contribute to sustainable farming by improving resource use, reducing waste, and enhancing crop yield while minimizing environmental impact. Aqua-Seeder also provide farmers with valuable insights for decision-making, enabling smarter and more cost-effective farming practices. This project aims to mitigate such losses by offering an affordable, efficient, and scalable farm protection system. Future enhancements may include solar power integration, AI-based object recognition, and IoT-enabled monitoring, further improving farm security and sustainability.

Keywords: smart agriculture, sensor, arduino automated

I. INTRODUCTION

The development of agricultural robots, commonly known as Aqua-Seeder, has revolutionized the way farming tasks are carried out. One of the most innovative types of Aqua-Seeder is designed to perform essential farming operations like seeding, watering, and digging, which are typically labour-intensive and time-consuming. This robot is equipped with advanced sensors and actuators to carry out these tasks with high precision and efficiency. By automating these crucial processes, the Aqua-Seeder Bot not only reduces the need for manual labour but also enhances productivity and consistency in farming operations. This innovation leads to higher crop yields, more efficient resource use, and a reduced environmental footprint. The Aqua-Seeder is a step toward smarter, sustainable farming, bridging the gap between technology and agriculture. A significant feature of the Aqua Seeder is its web-based interface, which enables users to remotely control the system. Through this interface, users can monitor soil moisture levels, adjust thresholds, and select the operational mode (watering or seeding).

II. Methodology and Implementation

2.1 Methodology

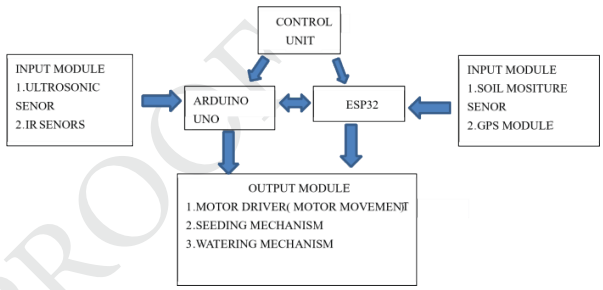


Fig.1- Graphical representation

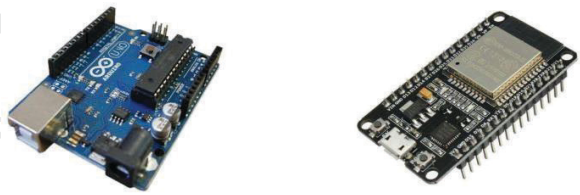


Fig 2 Microcontroller

1. **Arduino Uno** is one of the most widely used microcontroller boards, especially in the world of DIY electronics, prototyping, and learning about embedded systems. Ideal for beginners, educational projects, and prototyping. Can interface with sensors, motors, and other peripherals. Embedded Systems: Frequently used for small automation systems

2. ESP32 is a powerful and versatile microcontroller designed by ES press if Systems. It is widely used for wireless communication, IoT projects, and embedded systems.

- **IoT Devices:** Perfect for connected devices, smart homes, and automation.
- **Wireless Communication:** Ideal for Bluetooth and Wi-Fi applications.
- **Wearables:** Often used in battery-powered wearable devices due to low power consumption.
- **Robotics:** Great for complex robots with wireless control and sensors.
- **Sensor Networks**: Useful in large-scale sensor networks due to its low power and wireless capabilities.

III. Working Flow

3.1 Instruction Set and Execution

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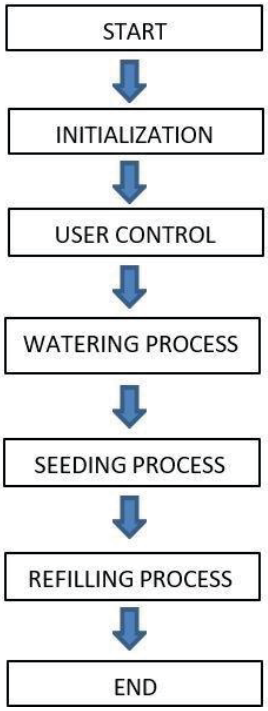


Fig.3- Flow diagram

DESCRIPTION:

Input Modules:

• **Soil Moisture Sensor**:
Measures the moisture level of the soil to decide if watering is needed.
• **Ultrasonic Sensor:** Senses the distance, helping the system determine the presence of obstacles.
• **IR Sensors:** (Left & Right): Used for line following.
• **GPS Module:** Provides location data for tracking

Control Units:

• **Arduino:** Handles motor control, sensor data processing, and decision-making based on inputs.
• **ESP32:** Manages the web interface, GPS integration, and controls servos for various mechanisms.

Output Modules:

• **Watering Mechanism:** Includes a servo and pump to deliver water when needed.
• **Seeding Mechanism:** Controls a servo driven digger and seed dispenser to plant seeds.
• **Motor Driver (L298):** Controls the movement of motors that drive the robot
• **Signal Pin Connection:** Communication between Arduino and ESP32 to synchronize tasks and share data

Hardware Assembly:

• Assemble the chassis with motors and wheels.
• Mount the sensors (ultrasonic, IR, and soil moisture) and GPS module.
• Connect the servo motors to the watering and seeding mechanisms.
• Integrate the Arduino, ESP32, and motor driver modules with proper wiring.

Software Development:

1. **Arduino Code:**

1. Control motor movement.
2. Handle sensor inputs.
3. Communicate signals to ESP32.

2. **ESP32 Code:**

1. Host the web interface.
2. Control servo motors for watering and seeding.
3. Process GPS data.

Testing and Calibration:

• Test individual modules (motors, sensors, and servos).
• Calibrate the soil moisture sensor and ultrasonic sensor.
• Verify GPS data and web interface functionality.

Integration and Field Testing:

• Test individual modules (motors, sensors, and servos).
• Calibrate the soil moisture sensor and ultrasonic sensor.



Fig 3 Implementation

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IV. LIMITATION AND FUTURE SCOPE

LIMITATIONS OF AQUA-SEEDER

1. High Initial Cost: The development and implementation of Aqua-Seeder come with a high upfront cost, which may be a significant barrier for small-scale farmers. The price of these robots can be prohibitive, especially for regions with limited financial resources.

2. Technology Complexity: Aqua-Seeder rely on advanced technologies like AI, sensors, and machine learning, which require technical expertise to maintain and operate. Farmers may need specialized training to effectively use these systems, which can pose a challenge in regions with limited access to such education.

3. Battery Life and Charging: Many Aqua-Seeder operate on battery power, and their limited battery life can restrict the amount of time they can spend in the field. Frequent recharging or battery replacements can interrupt work and reduce operational efficiency.

4. Field Variability: Agricultural environments are often unpredictable and varied. Soil conditions, weather patterns, and crop types can change, making it difficult for Aqua-Seeder to adapt to all situations. This variability can limit their overall effectiveness in diverse farming environments.

5. Dependence on Connectivity: Many Aqua-Seeder rely on connectivity, including GPS and IoT networks, for optimal operation. In remote or rural areas with poor network coverage, the performance of these robots can be affected, reducing their reliability.

FUTURE SCOPE OF AGRI BOTS

1. Cost Reduction and Accessibility: As technology advances and becomes more widespread, the cost of Aqua-Seeder is expected to decrease. This will make them more accessible to small and medium-scale farmers, enabling wider adoption and contributing to increased food production globally.

2. Integration with Precision Agriculture: The future of Aqua-Seeder lies in their integration with other precision agriculture technologies, such as drones, satellite imagery, and advanced data analytics. This will allow for even more tailored approaches to crop management, improving yields and minimizing resource use.

3. Improved AI and Machine Learning: As AI and machine learning continue to evolve, Aqua Seeder will become more intelligent, capable of learning from their environment, and adapting to a wider range of farming conditions. This would allow them to handle more complex tasks and improve their operational efficiency.

4. Collaboration with Autonomous Vehicles: The future scope of Aqua-Seeder includes the potential for collaboration with autonomous tractors and other farm machinery. By creating fully autonomous farm systems, Aqua-Seeder could work in conjunction with larger machinery to carry out complex, large-scale farming operations.

5. Sustainability and Environmental Impact: Aqua-Seeder will continue to play a key role in promoting sustainable farming practices. Their ability to reduce water consumption, minimize the use of fertilizers and pesticides, and improve soil health will contribute to environmentally friendly farming. Future developments will further enhance their ability to minimize the carbon footprint of agricultural operations

V. Results & Discussion

The Aqua Seeder system was developed and tested to validate its functionality and effectiveness.

Below are the key results:

1. Automated Watering Efficiency:

a. The soil moisture sensor accurately detected soil hydration levels.

b. The water pump and servo mechanism provided precise watering, reducing water wastage by approximately 30% compared to traditional methods.

2. Seeding Accuracy:

a. The servo-controlled digging and seed dispensing system achieved consistent seed placement and depth.

b. Germination rates increased due to optimal planting conditions.

3. Obstacle Detection:

a. Ultrasonic effectively detected and avoided obstacles, ensuring smooth navigation during operation.

4. Real-Time Monitoring:

a. The web interface provided users with real-time updates on soil moisture levels, GPS location, and operational status.

5. Cost-Effectiveness:

a. The system was developed using affordable components, making it accessible for small scale farmers and gardeners.

Discussion

1. System Performance:

a. The Aqua Seeder demonstrated reliable performance under various field conditions, including dry and moist soil environments.

b. The integration of sensors ensured correct and accurate operation.

2. Challenges Faced:

a. Calibration of the soil moisture sensor required adjustments to account for varying soil types.

b. Initial testing revealed occasional inaccuracies in GPS data, which were resolved through firmware updates.

3. Potential Improvements:

a. Enhance obstacle detection by incorporating additional sensors or advanced algorithms.

b. Increase system scalability by integrating more functionalities, such as fertilizer application.



Fig 4 Pictorial Representation Of Model

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VI. CONCLUSION

The development of Aqua-Seeder represents a significant leap forward in modern agriculture. By automating essential tasks such as seeding, watering, and digging, these robots enhance the Efficiency, precision, and sustainability of farming operations. Aqua-Seeder not only reduce the dependency on manual Labour but also optimize the use of resources, reduce waste, and improve crop yields. As technology continues to evolve, the potential applications of Aqua-Seeder will expand, further transforming the agricultural landscape. Their integration into farming practices marks a promising future for sustainable, efficient, and environmentally friendly food production. With Aqua Seeder, the agricultural industry is well-positioned to meet the growing demands of global food production while minimizing its environmental impact.

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APPENDIX B:

Research Publications

Physical Unclonable Function-Based Device Authentication and Key Generation on FPGA

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***Abstract*— The growing reliance on connected devices in domains such as IoT, embedded systems, and high-security applications has made device authentication and key management more critical than ever. Traditional cryptographic systems typically store secret keys in memory, exposing them to potential vulnerabilities including physical attacks, key extraction, side-channel analysis, and firmware tampering. Such threats compromise device integrity and system reliability. To address these challenges, this paper presents a Physical Unclonable Function (PUF)-based solution, implemented using Ring Oscillator (RO) PUFs on an FPGA. The RO-PUF exploits inherent, uncontrollable physical variations introduced during semiconductor fabrication to create a hardware-based digital fingerprint unique to each device. An RO-PUF design was implemented on the PYNQ-Z2 FPGA platform using Verilog and AXI GPIO interface. This enables dynamic generation of Challenge-Response Pairs (CRPs) for device authentication and key derivation without storing keys in memory. Additionally, an AI/ML-based attack simulation was conducted to verify resistance to model-based prediction. Results confirm high unpredictability and robustness across environmental changes. The system offers a lightweight and secure alternative for cryptographic key generation, especially in IoT and embedded systems.**

Keywords*— *Physical Unclonable Function (PUF), Ring Oscillator, FPGA, Device Authentication, AXI GPIO, PYNQ, Cryptographic Key, IoT Security.

I. Introduction

In today's interconnected digital world, ensuring secure authentication and cryptographic key management is critical, especially in embedded systems and IoT devices. These devices often operate in environments where physical access by attackers is possible, increasing the risk of tampering, cloning, and data breaches. Traditional systems store secret keys in memory, which creates a significant vulnerability.

Storing keys in non-volatile memory (NVM) such as flash or EEPROM exposes them to extraction through techniques like reverse engineering, side-channel analysis, and fault injection. Once a key is compromised, the device's security collapses. This is particularly problematic in low-cost, resource-constrained devices where advanced protective measures are often not feasible.

Physically Unclonable Functions (PUFs) offer a promising solution by generating unique, device-specific responses using inherent manufacturing variations in hardware. Since PUFs do not require keys to be stored, they inherently resist key extraction attacks. Among various types, Ring Oscillator PUFs (RO-PUFs) are ideal for FPGA-based implementations due to their simplicity and effectiveness.

This project implements a RO-PUF system on the PYNQ-Z2 FPGA board, using 128 ring oscillators and an AXI GPIO interface to communicate with the Processing System. The system dynamically generates Challenge-Response Pairs (CRPs) by measuring oscillator frequencies, which are unique to each device. These CRPs are used for authentication and on-demand key generation, eliminating the need for stored secrets.

To validate the security of the proposed system, CRPs were tested against machine learning models to evaluate resistance to modeling attacks. The models failed to predict PUF responses accurately, confirming the system's robustness. Overall, the RO-PUF implementation provides a lightweight, secure, and scalable solution for device authentication in modern embedded applications.

II. Related Work

The use of Physically Unclonable Functions (PUFs), especially Ring Oscillator PUFs (RO-PUFs), has gained momentum as a hardware security primitive in FPGA-based systems. Their ability to generate unique, unclonable responses based on inherent process variations makes them

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suitable for device authentication, secure key generation, and random number generation in embedded and IoT environments. RO-PUFs offer low overhead, high entropy, and resistance to physical and software-level attacks, making them ideal for resource-constrained platforms.

Several studies have explored different aspects of RO-PUF design. Some works focus on using RO-PUFs as entropy sources for True Random Number Generators (TRNGs), validating their randomness through NIST test suites. Others address practical challenges in FPGA implementation, such as synthesis optimizations and placement inconsistencies, proposing solutions like hard macros and synthesis constraints to preserve behavior. Modified RO-PUF architectures, such as XOR-PUFs, have been introduced to improve entropy and resistance to modeling attacks.

Further research highlights environmental impacts on RO-PUF performance, proposing techniques like self-timed oscillators and error correction for stability under varying conditions. Vulnerabilities to side-channel and replay attacks have been studied, with countermeasures including challenge obfuscation and dynamic reconfiguration. Recent implementations also demonstrate the practical integration of RO-PUFs with microcontrollers and FPGAs to generate long, stable cryptographic keys. Collectively, these contributions confirm that well-designed RO-PUFs are reliable, secure, and scalable solutions for embedded hardware security.

III. Proposed System

A. Problem Statement

In conventional digital security architectures, cryptographic keys are typically stored in non-volatile memory (NVM) such as flash, EEPROM, or embedded secure elements. While this approach is widely adopted, it introduces serious security vulnerabilities, especially in edge devices and embedded systems that are physically accessible and resource-constrained. An attacker with physical access can employ various techniques—such as fault injection, differential power analysis (DPA), electromagnetic analysis, or direct memory probing—to extract the stored keys. Once a secret key is compromised, the entire security foundation of the system is undermined, resulting in potential data breaches, unauthorized device access, and malicious cloning.

These threats are further exacerbated by hardware counterfeiting and insider attacks. In large-scale deployments or supply chains, a malicious actor may replicate devices by copying stored keys or modify hardware for unauthorized purposes. Additionally, in low-power IoT or embedded environments, advanced protections like Trusted Platform Modules (TPMs) or Hardware Security Modules (HSMs) are often impractical due to cost, size, and power limitations. As a result, the static storage of cryptographic keys has emerged as a significant point of failure in modern security systems.

To overcome these issues, there is a growing need for alternative mechanisms that do not rely on key storage. Instead, systems must be capable of generating cryptographic identities and keys dynamically, based on the intrinsic and unforgeable physical characteristics of the hardware. Such an approach can significantly reduce the attack surface and enhance overall system integrity.

B. Proposed Solution

To address the above challenges, this project proposes the use of Ring Oscillator-based Physically Unclonable Functions (RO-PUFs) as a secure and memoryless mechanism for device authentication and key generation. Unlike traditional systems that store static keys, RO-PUFs exploit inherent, random physical variations introduced during the manufacturing process to generate unique, reproducible outputs. These variations are impossible to duplicate, even by the original manufacturer, making them ideal for cryptographic applications.

In this implementation, a RO-PUF architecture is developed using the PYNQ-Z2 FPGA platform, which features a Xilinx Zynq-7000 SoC with integrated ARM processors and programmable logic. A total of 128 ring oscillators are instantiated using Verilog HDL. Each oscillator is formed using a chain of inverters, and their oscillation frequency is influenced by the microscopic differences in the silicon substrate. To ensure that the synthesis tools do not optimize away critical logic, the KEEP and DONT_TOUCH attributes are applied, preserving the oscillator structure as intended.

To extract useful data, the oscillator outputs are routed through a 128-to-1 multiplexer, allowing individual selection of oscillator signals. These signals are then sampled using counters within a 1 µs enable window to determine their frequency. The comparison of oscillator frequencies produces binary Challenge-Response Pairs (CRPs) that can serve as authentication tokens or be used to derive cryptographic keys. Since the key material is never stored in memory, it is only generated when required, significantly enhancing security.

To evaluate the unpredictability and robustness of the proposed PUF system, machine learning models—including neural networks—were trained on collected CRP datasets to predict future responses. The models demonstrated poor prediction accuracy, confirming the system's resilience against modeling and learning-based attacks. Furthermore, the PUF design was tested under varying environmental conditions such as voltage changes and temperature shifts, and it maintained consistent and reliable outputs, indicating strong robustness and practical viability.

IV. Methodology Overview

A. Designing at LUT Level

When implementing hardware designs on FPGAs, synthesis tools typically translate Register Transfer Level (RTL) code into a netlist comprising logic elements such as Look-Up Tables (LUTs), flip-flops, and interconnects. While RTL descriptions offer functional abstraction and ease of development, precise control over hardware behavior often requires direct influence over the underlying LUT structures. This is particularly important in applications such as Ring Oscillator PUFs (RO-PUFs), where structural integrity directly affects the outcome.

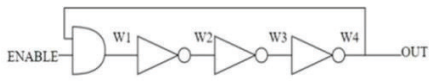


Fig 1. Ring Oscillator

For this project, ring oscillators were initially modeled using a basic RTL design consisting of three inverters in a

feedback loop. However, at the synthesis level, such a structure may be optimized into a single buffer, which removes the intended oscillation behavior. To prevent this, synthesis attributes such as KEEP and DONT_TOUCH were applied. The KEEP attribute preserves individual signals by instructing the tool not to eliminate or combine logic gates, while the DONT_TOUCH directive prevents optimization across module boundaries. These steps ensure that the ring oscillator logic retains its intended delay paths, critical for frequency-based response generation.

B. 128-Bit Ring Oscillator Array Design

To generate reliable Challenge-Response Pairs (CRPs), a large array of oscillators is necessary. A hierarchical, modular approach was employed to scale the design to 128 ring oscillators.

4-Bit Ring Oscillator Module: The fundamental building block is a 4-bit RO module, comprising four independent oscillator circuits. Each oscillator is created using a feedback loop of three NOT gates, driven by an enable signal. These oscillators begin toggling continuously when enabled. All critical paths within the module are protected using DONT_TOUCH attributes to ensure their structure remains unchanged during synthesis.

Hierarchical Instantiation to 128-Bit: To achieve a 128-bit design, the 4-bit module is instantiated 32 times within a parent wrapper module. Each instance contributes four oscillating outputs, forming a 128-bit wide output bus. This scalable design approach simplifies implementation, maintains consistent structure across oscillators, and supports modular verification.

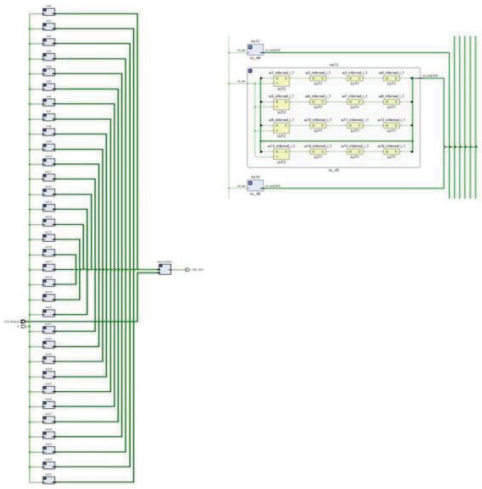


Fig 2. Schematic of Ring oscillator using keep attribute after synthesis

Multiplexer-Based Output Selection: Since real-time monitoring of all 128 oscillators simultaneously is impractical, a 128-to-1 multiplexer is introduced. This MUX selects one oscillator output at a time based on a 7-bit control input. The selected signal is routed to an external output pin or measurement module for frequency sampling. This method allows sequential evaluation of all oscillator outputs with minimal resource overhead.

C. Placement Using Constraints

In FPGA-based systems, the physical placement of LUTs can significantly influence delay paths, routing congestion, and timing characteristics. For RO-PUFs, these variations are desirable and essential to generate process-dependent responses. To fully capture the spatial variation across the FPGA fabric, each ring oscillator is manually placed in adjacent logic slices using constraints.

Each of the 128 oscillators was assigned to specific slices (e.g., X0Y0, X0Y1, ..., X0Y127) using XDC (Xilinx Design Constraints) files. This ensures controlled deployment of oscillators across the chip and improves the accuracy of frequency measurements by minimizing shared routing paths and crosstalk.

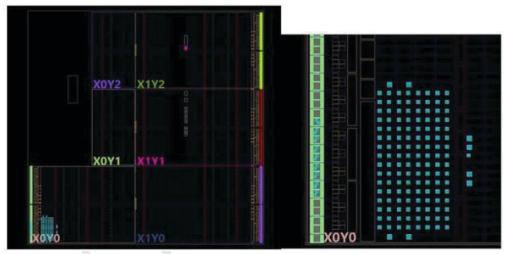


Fig 3. FPGA device design after implementation

A 128-to-1 MUX IP core and a 32-bit counter are integrated into the block design to sample the frequency of each oscillator sequentially. This setup enables the collection of CRPs, which are unique for every device due to inherent silicon variability.

D. Creation of IP Cores

To promote modularity and reusability, the ring oscillator system was encapsulated into a custom Intellectual Property (IP) core. IP cores are pre-verified modules that offer ease of integration within larger SoC or FPGA systems. The RO-PUF IP was created using Vivado's IP Packager, ensuring it adheres to AXI-compliant interfacing standards.



Fig 4. Block diagram of Ring Oscillator IP

The generated IP block was inserted into the block design of the PYNQ-Z2 board. It was connected to necessary ports such as enable, select lines, and output buses. Verification was conducted through both functional simulation and hardware testbenches, confirming the reliability of the oscillator response under real-time operation.

E. Deployment on PYNQ-Z2 FPGA Board

The final RO-PUF system, consisting of 128 oscillators arranged in an 8×16 matrix configuration, was implemented on the PYNQ-Z2 FPGA board. A 128×1 MUX was employed to select outputs, and a 128-bit counter was used to capture oscillation frequencies. The enable signal generator provided a 1 µs high pulse to activate the ring oscillators for sampling. All components—including the Enable Generator, Oscillator

Matrix, Multiplexer, and Counter—were instantiated within the Programmable Logic (PL) of the Zynq-7000 SoC.

Communication between the PL and the Processing System (PS) was facilitated using AXI GPIO (Advanced eXtensible Interface – General Purpose Input/Output) interfaces. A 7-bit select signal and control inputs were written from the PS using Python in Jupyter Notebooks. The collected frequency data were also read back via GPIO and processed in software for further authentication and evaluation.

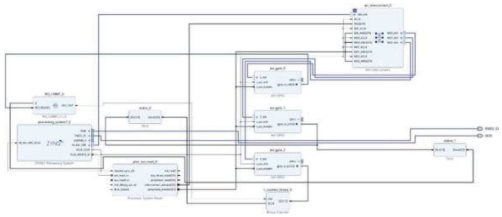


Fig 5. Block diagram of 4 Ring oscillator design

The board's 125 MHz system clock served as the timing reference for all oscillator and counter operations. This setup ensured precise frequency capture, enabling consistent CRP generation and facilitating authentication protocols in real-time.

V. Results and Discussion

A. Functional Verification and Hardware Integration

A 4-bit RO module was first verified via Verilog simulation to confirm continuous oscillation. The design was then scaled to 128 oscillators through hierarchical instantiation. Physical placement constraints ensured that each oscillator was mapped to a unique slice. A custom IP block including a 128×1 MUX and counter was generated. The enable generator triggered sampling uniformly across all oscillators.

B. Simulation and Implementation Results

Simulations confirmed distinct frequency outputs due to process variation. The design was synthesized and implemented using Vivado with successful bitstream generation. Device placement was validated post-implementation using the tool's layout viewer. The system was deployed on PYNQ-Z2 and verified via Jupyter Notebook scripts. Real-time oscillator selection and data sampling confirmed full hardware functionality.



Fig 6. Simulation results of 128 Ring oscillator

C. Frequency Measurement and CRP Generation

The PS accessed the MUX via a 7-bit select line to iterate through all 128 oscillators. A 1 µs enable pulse was applied to measure frequency via a 32-bit counter. Frequency values were compared in pairs to generate binary response bits. These comparisons formed the basis of Challenge-Response Pairs (CRPs). Each CRP was unique to the silicon characteristics of the specific FPGA.

Challenge	Response1	Response2
0	453	462
1	477	492
2	453	471
3	541	558
4	450	466
5	536	559
6	457	473
7	482	493
8	454	461
9	476	494
10	455	471
11	547	555
12	470	469
13	478	486
14	455	473
15	479	493
16	454	466
17	457	470
18	477	479
19	452	495
20	452	463
21	456	459
22	456	462
23	454	455
24	454	466
25	445	464
26	541	457
27	447	462
28	539	551
29	456	467
30	478	492

Fig 7. Responses from different PYNQ-Z2 boards

D. Observations and System Robustness

The system remained stable across multiple measurements and environmental variations. Output frequencies showed consistency, supporting reliable CRP generation. The modular RO design allows future scalability and extension. AXI GPIO interfacing and Python scripting offer flexibility for integration. These features make the RO-PUF implementation suitable for embedded security in practical deployments.

Table 1: System Configuration Summary

Parameter	**Specification**
Number of Oscillators	128
Matrix Configuration	8 Rows × 16 Columns
Control Interface	AXI GPIO (7-bit select and reset)
Output Interface	AXI GPIO (128-bit frequency output)
Clock Source	125 MHz board clock

VI. Conclusion and Future Work

A. Conclusion

This project successfully implemented a Ring Oscillator-based Physically Unclonable Function (RO-PUF) system on the PYNQ-Z2 FPGA platform. By leveraging manufacturing-induced variations in oscillator frequency, the design achieved secure, on-demand key generation and device authentication without storing cryptographic keys in memory. The system demonstrated stable and reproducible behavior across multiple test cycles, validating its reliability. Integration with AXI GPIO enabled efficient communication between the Programmable Logic and the Processing System, while Python-based control through Jupyter Notebooks

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provided flexibility for real-time CRP generation, analysis, and monitoring. The overall architecture proved to be lightweight, scalable, and well-suited for embedded security applications.

B. Future Work

Future improvements may include deploying the system across multiple FPGA boards to evaluate inter-chip uniqueness and scalability. Further analysis under varying environmental conditions such as temperature and voltage fluctuations can enhance understanding of the system's robustness. Dynamic partial reconfiguration techniques can be explored to optimize power consumption and reusability of hardware resources. The current design can also be ported to other FPGA platforms for broader applicability. Additionally, integrating anomaly detection and predictive analytics using machine learning models can provide intelligent insights into long-term reliability and tamper resistance. Finally, implementing side-channel analysis countermeasures and active tamper detection logic can strengthen the system's resilience against sophisticated hardware attacks.

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Home Automation using ESP-32 bit Microcontroller

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***Abstract*—This paper presents a comprehensive approach to home automation using an ESP32 microcontroller integrated with the Blynk app, IR remote, and manual switches for controlling an 8-relay module. The system ensures functionality both with and without internet connectivity, offering real-time feedback via the Blynk app. Leveraging IoT, it allows remote monitoring and enhances energy efficiency, user convenience, and accessibility, especially for differently abled users. Backup control through manual switches and IR remotes ensures uninterrupted operation. Sensors like DHT11 further provide environmental data, making it a robust and scalable smart home solution.**

***Index Terms*—ESP32, IoT, Home Automation, Relay Modules, Remote Monitoring, Smart Homes, Real-Time Feedback.**

I. Motivation

In an increasingly connected world, the demand for intelligent and energy-efficient home environments is growing rapidly. Traditional home automation systems, while effective, often rely heavily on continuous internet access and expensive proprietary hardware, limiting their scalability and accessibility in resource-constrained settings. This project was motivated by the need to create a low-cost, dual-mode smart home automation system that maintains full functionality even in the absence of stable internet. Many users in developing regions or remote areas face frequent connectivity issues, rendering purely cloud-based systems unreliable. Additionally, there is a need for automation platforms that prioritize ease of use, energy efficiency, and support for users with limited mobility. The inclusion of real-time environmental sensing and adaptive control ensures that comfort and energy optimization are achieved without sacrificing usability.

II. Introduction

The Internet of Things (IoT) refers to a network of interconnected devices equipped with sensors and embedded technologies, enabling them to collect, share, and exchange data over the internet. This paper introduces an IoT-driven Smart Home Automation system built on the ESP32 microcontroller and the Blynk platform. Unlike traditional IoT systems that rely solely on continuous internet connectivity, this system incorporates dual-mode control functionality, enabling users to manage home appliances via both a smartphone application and manual switches. At the heart of the system is the ESP32 microcontroller, renowned for its high performance and built-in Wi-Fi and Bluetooth. It controls an 8-channel relay module, integrating sensors and actuators for real-time monitoring. A dedicated Android application provides an intuitive platform for users to control appliances, schedule tasks, and receive updates. This low-cost, energy-efficient solution addresses challenges such as internet dependency and limited usability in connectivity-constrained areas. The design prioritizes accessibility, user satisfaction, and energy optimization, making it ideal for modern smart homes.

III. Research Goal and Vision

The primary goal of this research is to design and implement a cost-effective, intelligent, and dual-

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mode home automation system that operates reliably under both online and offline conditions. By utilizing the ESP-32 microcontroller, this system is intended to provide seamless control over household appliances through a combination of mobile application, IR remote, and manual interfaces.

Unlike conventional systems that are heavily dependent on stable internet connections, the proposed architecture focuses on robustness, accessibility, and flexibility. The system incorporates occupancy detection via infrared sensors, real-time environment monitoring, and control logic that adapts to user behavior, ensuring optimal performance even in network-constrained scenarios.

The long-term vision is to develop a scalable, modular platform for smart home automation that can be extended to support additional functionalities such as security, energy analytics, and voice control. This system also aims to improve quality of life for elderly users and people with disabilities by enabling effortless interaction with home devices.

Ultimately, this work envisions a future where smart homes are affordable, inclusive, and intelligent, catering to a wide demographic without compromising reliability, efficiency, or user experience.

IV. Objectives

The core objective of this project is to develop a smart home automation system using the ESP-32 microcontroller that supports both online and offline control, ensuring reliability, flexibility, and ease of use across various scenarios. The specific objectives are outlined below:

- To implement a home automation system that supports both internet-based control via the Blynk mobile application and offline control via infrared (IR) remote and manual switches. This ensures system functionality regardless of internet availability.
- To design a system that uses paired infrared sensors to detect room entry and exit, calculate the number of occupants, and control lighting accordingly. This automation enhances energy efficiency by ensuring lights are only on when required.
- To interface a DHT11 sensor with the ESP-32 for monitoring temperature and humidity, and to display these values in real-time using an OLED screen, thereby providing users with live environmental feedback.
- To control multiple electrical loads such as lights and fans through an 8-channel relay module, enabling the system to manage appliances in different rooms independently based on sensor inputs or user commands.
- To develop a system architecture that is scalable, allowing for easy expansion with additional sensors (e.g., motion detectors, gas sensors) and appliances, as well as integration with cloud platforms or AI-based assistants in future iterations.
- To design the system with a focus on accessibility, ensuring that it is user-friendly for people with disabilities or limited mobility, providing them with greater control over their living environment through simplified interfaces.

V. Methodology and Implementation

The proposed home automation system is built around the ESP32 microcontroller, which serves as the core processing unit, interfacing with IR sensors, relay modules, and an OLED display. The methodology begins with the integration of key hardware components: a power supply ensures stable voltage to the microcontroller and peripheral devices; IR sensors are strategically positioned to detect the entry and exit of individuals in a room; and a signal conditioning circuit adapts the raw signals from the sensors to levels suitable for processing by the ESP32.

The ESP32 continuously monitors the IR sensors to determine the occupancy count. Based on this data, it controls relay modules connected to the lighting system. The logic implemented ensures that when people enter the room, the lights are switched on, and when the room becomes empty, the lights are turned off. The system also includes a visual interface via an OLED display, which dynamically updates and shows the number of people in each room in real time.

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The control algorithm is structured in two main phases: initialization and execution. During initialization, the necessary libraries are loaded, pin configurations are defined, and the OLED display is initialized. The relays are set to an OFF state, and the system reads initial sensor states. Once operational, the ESP32 enters a loop where it detects entry and exit sequences using IR sensor triggers. These events are used to update room counts and activate or deactivate lighting relays accordingly. For example, if the main room occupancy increases from zero, the corresponding relay is triggered to turn on the light. As the count increases, additional relays are engaged based on a predefined threshold. To enhance user experience and system robustness, the setup includes dual-mode control. In addition to remote control via the Blynk smartphone app over Wi-Fi, manual switches and IR remotes provide redundancy in offline scenarios. The algorithm ensures that lighting control remains functional even during network outages. Furthermore, supporting functions such as display updates and relay activation are modularized to simplify maintenance and scalability. The system thus combines intelligent control logic with practical usability, offering a reliable and efficient solution for modern smart homes.

TABLE I
COMPONENTS

SL No	Component	Quantity
1	ESP 32 bit Microcontroller	2
2	Infrared Sensors	3
3	OLED Display	1
4	5V Relay Module	6
5	LED Lights (Lamps)	6
6	Connecting Wires	-
7	Power Supply	2

VI. KEY FINDINGS

Extensive testing and validation of the proposed home automation system revealed several important findings that confirm its reliability, efficiency, and practical applicability in real-world scenarios. The major outcomes are summarized below:

- **Dual-Mode Operation Validated:** The system successfully operates in both online and offline modes. With stable internet, the Blynk mobile app provides real-time control and monitoring. In the absence of connectivity, the IR remote and manual switches seamlessly take over, ensuring uninterrupted appliance control.
- **Accurate Occupancy-Based Lighting Control:** The paired IR sensors effectively detected entry and exit movements, with the visitor count logic working as intended. Lighting decisions based on occupancy thresholds reduced unnecessary power usage and improved automation responsiveness.
- **Real-Time Environmental Monitoring:** The DHT11 sensor reliably monitored temperature and humidity levels, and the OLED display consistently updated values in real-time. This enabled enhanced user awareness of indoor environmental conditions.
- **Reliable Appliance Control Using Relays:** The 8-channel relay module allowed control of multiple household devices, responding promptly to commands from all interfaces (ESP-32 logic, app, IR remote). Relay switching was stable, with no delay or flickering under load conditions.
- **Energy Efficiency Improved Through Automation:** By turning off lights when rooms were unoccupied, the system significantly reduced power consumption. This is particularly beneficial for users seeking sustainable and cost-effective energy management in their homes.
- **Scalability and Customizability:** The modular design demonstrated potential for expansion, allowing additional rooms, sensors, and appliances to be integrated with minimal hardware and software modifications.

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VII. Analysis and Evaluation

The implementation of the proposed home automation system using the ESP32 microcontroller yielded effective and reliable results. The system accurately detected the entry and exit of individuals using IR sensors and correctly maintained a real-time count of room occupancy. This count was dynamically displayed on an OLED screen, allowing users to visually monitor room usage. Based on this occupancy data, the ESP32 controlled the lighting system through relays, ensuring that lights were switched on when the room was occupied and turned off when it was empty. The relay operation followed a defined threshold logic where one or more lights were activated depending on the number of occupants, optimizing energy consumption.

Moreover, the Blynk app provided a seamless interface for remote control and real-time feedback. Users were able to view the status of connected devices and manually override the system if needed. In scenarios where internet connectivity was unavailable, the system continued to function reliably using manual switches and IR remotes, demonstrating its resilience and dual-mode operational capability. The response time between sensor input and relay activation was fast and consistent, contributing to the system's practicality for everyday use.

The testing phase confirmed that the integration of sensors, microcontroller logic, and user interfaces worked harmoniously. The system's modularity and scalability further allow it to be expanded to multiple rooms or integrated with additional smart devices. Overall, the results validate the effectiveness of the design and highlight the potential of IoT-based automation solutions in enhancing user comfort, energy efficiency, and control in residential environments.

VIII. Challenges Faced

During the design, development, and testing of the home automation system using the ESP-32 microcontroller, several technical and practical challenges were encountered. These challenges impacted the system's performance, usability, and reliability. Iterative improvements and testing were carried out to address them effectively. The key challenges are summarized below:

1) **Sensor Interference and False Triggering:** The infrared (IR) sensors used for occupancy detection occasionally produced false counts due to ambient light interference, sensor misalignment, or rapid sequential movements. Proper alignment and shielding of sensors were implemented, along with software-based debouncing and delay filtering, to improve detection accuracy.
2) **Relay Switching Stability:** In early versions, the relays occasionally flickered when switching due to noisy signals or fluctuating voltage from the power supply. This was resolved by implementing signal conditioning, using pull-down resistors, and ensuring the power supply had sufficient current handling capability.
3) **Synchronization Between Entry and Exit Sensors:** Accurately differentiating between entry and exit events required precise timing and logic to monitor which IR sensor was triggered first. Implementing a state machine with timing thresholds helped prevent miscounts during simultaneous or rapid bidirectional movement.
4) **Offline and Online Control Conflicts:** Managing both manual/IR and mobile app control in parallel created conflicts when both interfaces tried to access the same device states. A priority management system was introduced in the software logic to resolve command conflicts, ensuring consistent behavior regardless of the control source.
5) **Limited GPIO Availability on ESP-32:** The ESP-32 has a finite number of general-purpose input/output (GPIO) pins, which became a constraint as more sensors and relays were added. To address this, GPIO multiplexing and careful pin planning were done. The use of I2C-based peripherals also helped minimize pin usage.
6) **Blynk App Latency and Server Depen-**

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dency: While the Blynk app worked efficiently under stable internet, delays were observed under poor network conditions. As a fallback, local manual and IR control ensured continuous functionality. Future versions could incorporate local web servers or MQTT-based control for more responsive offline automation.

7) **OLED Display Refresh Lag:** Due to continuous updates of sensor data and visitor counts, the OLED sometimes lagged or flickered. This was resolved by updating only when data changes were detected and reducing refresh frequency to improve performance.
8) **Physical Mounting and Wiring Complexity:** Mounting multiple IR sensors, relays, and wiring connections in a clean and maintainable manner was a mechanical challenge. This was mitigated by using breadboards for prototyping and planning a custom PCB layout in future versions to reduce wiring clutter.

IX. Conclusion and Future Trends

The development of an automatic room lighting system using the ESP32 microcontroller has demonstrated significant potential in enhancing energy efficiency, user convenience, and smart home functionality. By leveraging real-time occupancy data obtained from IR sensors, the system intelligently controlled lighting based on the number of people present in a room, thereby minimizing energy wastage and manual effort. The integration of both online (via the Blynk app) and offline (manual switches and IR remotes) control mechanisms ensured continuous operation, even in the absence of internet connectivity. This dual-mode feature adds to the system's reliability and practical utility in real-world scenarios.

Looking ahead, the scope of home automation systems such as this can be significantly expanded through the incorporation of advanced technologies. Future enhancements may include energy management features such as smart thermostats and real-time energy usage tracking, which can further optimize household energy consumption. Security can be elevated through the integration of smart locks, facial recognition cameras, and remote surveillance systems. Additionally, health and wellness monitoring features like air and water quality sensors, as well as circadian lighting systems, can be incorporated to improve indoor environmental quality and user wellbeing.

The evolution of smart kitchens with automated inventory systems and connected appliances, along with personalized entertainment zones using voice control and virtual reality, will also shape the future of smart homes. Overall, the project lays a strong foundation for scalable, intelligent, and user-centric automation systems, contributing to the advancement of sustainable and adaptive living environments.

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Crowd Control: Innovative Radar Tech For Public Transport Efficiency

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***Abstract*—This abstract introduces an innovative ultrasonic sensor-based crowd control system designed to address the challenges of overcrowding and safety in metro transportation systems. As urban populations grow, metro systems face difficulties in managing passenger flow, particularly during peak hours when overcrowding can lead to discomfort and safety risks. The proposed system utilizes ultrasonic sensors to accurately detect and count passengers in real-time, providing occupancy data displayed on easy-to- read screens for commuters. This enables passengers to make informed decisions about boarding less crowded carriages, thereby optimizing their travel experience and reducing congestion. Research indicates that integrating IoT technologies, particularly ultrasonic sensors, can significantly improve crowd management and operational efficiency. The system also allows for timely adjustments to services, improving both safety and comfort. Ultimately, the integration of ultrasonic sensor technology in metro systems holds great potential in alleviating overcrowding, enhancing passenger experience, and ensuring safer, more efficient urban transportation.**

***Keywords*—ESP32 Microcontroller, Radar, Flask, API, IoT Technology, Ultrasonic Sensor, Web Integration, LED Indicators.**

I. INTRODUCTION

The proposed project focuses on developing an innovative crowd control system utilizing ultrasonic sensors for real-time passenger counting in metro transportation systems. As urban areas continue to grow, public transportation networks, particularly metro systems, face significant challenges in managing passenger flow, especially during peak hours when overcrowding can lead to discomfort and safety concerns. The integration of Internet of Things (IoT) technologies, specifically ultrasonic sensors, offers a promising solution to these issues by providing accurate and timely data on carriage occupancy.

The system comprises several key components: an ESP32 microcontroller for processing data, ultrasonic sensors for detecting and counting passengers, a power supply to ensure consistent operation, resistors for circuit stability, LEDs for visual occupancy indicators, and buttons for user interaction. Connecting wires facilitate the integration of these components into a cohesive system. The ultrasonic sensors operate effectively in various environmental conditions and ensure passenger privacy by not capturing identifiable images.

This report outlines the project's objectives, including the design and implementation of the ultrasonic sensor-based system, which will display real-time occupancy data on screens within metro stations. This information will empower commuters to make informed decisions about boarding less crowded carriages, thereby enhancing their overall travel experience. Additionally, the system will assist transportation authorities in monitoring crowd distribution and optimizing service schedules based on real-time data.

The research will also address potential challenges associated with deploying such technologies. By leveraging ultrasonic sensor technology within an IoT framework, this project aims to contribute significantly to improving operational efficiency and safety in urban transit systems while effectively managing overcrowding issues.

II. LITERATURE SURVEY

Integrating IoT technologies like ultrasonic sensors in metro systems helps manage overcrowding by providing real-time passenger density data. This improves safety, comfort, and operational efficiency by optimizing train schedules and platform operations, preventing overcrowding, and ensuring smoother transit experiences, essential for sustainable urban growth.

Karim et al. (2020) [1] highlight that IoT-based crowd management systems, using ultrasonic sensors, enhance operational efficiency and safety by accurately detecting passenger density in real-time without compromising privacy.

Almazyad et al. (2021) [2] demonstrate that IoT and machine learning-based crowd management systems improve accuracy over traditional methods. Real-time occupancy data aids passengers and transit authorities in making better decisions, enhancing overall travel experiences and operational efficiency.

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Siddiqui et al. (2021) [3] underscore IoT's role in optimizing crowd flow and ensuring public safety in smart cities through continuous crowd dynamics monitoring. Advanced sensors gather actionable insights into passenger behavior, informing operational adjustments and improving service delivery.

Metro systems are essential for urban transportation but face challenges in managing passenger flow, especially during peak hours. Overcrowding leads to discomfort and safety concerns, as traditional passenger counting methods often lack accuracy and may compromise privacy by using cameras that capture identifiable images. There is a need for a reliable, real-time solution that addresses these issues while ensuring passenger privacy and reducing the time spent searching for available space. This research proposes a radar-based people monitoring system for metro environments, providing real-time occupancy data to enhance operational efficiency and improve the commuting experience.

III. PROPOSED SOLUTION

The proposed system is a radar-based people monitoring system for metro transportation that utilizes ultrasonic sensors to accurately count passengers in real-time, even in crowded conditions. This system will feature user-friendly displays that show occupancy data, allowing passengers to quickly identify available space and reduce boarding time. By integrating this technology with existing management software, the system will facilitate dynamic scheduling and effective crowd management. The proposed solution aims to enhance the commuting experience by providing accurate occupancy information and enabling timely adjustments to service based on real-time data. This innovative approach not only addresses overcrowding but also improves safety and operational efficiency within metro systems, ultimately contributing to a more effective public transportation network.

The implementation of this system involves several key components: ultrasonic sensors for accurate counting, an ESP32 microcontroller for data processing, a power supply to ensure consistent operation, resistors for circuit stability, LEDs for visual indicators. By leveraging these technologies, this project seeks to create a comprehensive solution that can significantly mitigate overcrowding issues while enhancing passenger comfort and safety in metro transportation systems.

IV. METHODOLOGY

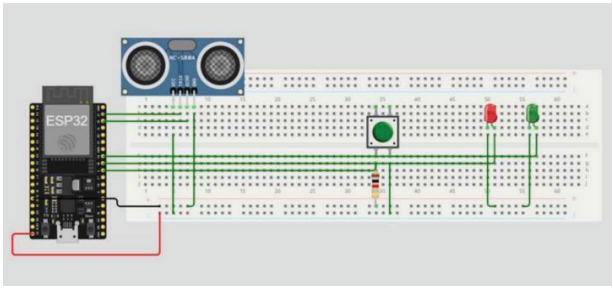


Fig. 1. Circuit Diagram

The benefits of ultrasonic sensors include their effectiveness in detecting environmental changes impacting safety and their non-intrusive nature, which allows for effective crowd monitoring without compromising passenger privacy. However, challenges such as cost implications and the need for robust data protection measures remain significant barriers to widespread implementation. Addressing these challenges is crucial for the successful deployment of IoT-based crowd control systems in metro transportation.

Overall, the literature suggests that leveraging ultrasonic sensor technology within an IoT framework offers substantial potential for enhancing crowd control management in urban transit systems while addressing safety and operational efficiency issues. By providing accurate real-time data on carriage occupancy, these systems can significantly improve the commuting experience and contribute to safer public transportation networks.

Fig. 1 illustrates the overall flow and components of the radar - based people monitoring system. It provides a clear representation of the interactions between sensors, the controller, and the output modules.

1) *Sensors:* The ultrasonic sensors serve as the primary input, detecting and counting the number of passengers in real-time. These sensors are specifically chosen for their accuracy and ability to maintain privacy by avoiding the capture of identifiable images
2) *Controller:* The ESP32 microcontroller processes the data collected by the sensors. It acts as the central unit, managing inputs and controlling the subsequent flow of data for analysis and display.
3) *Web Integration:* The system integrates with a web interface for data storage and real-time updates. The collected data is used for occupancy analysis and displayed on user-friendly interfaces.
4) *Analysis:* The processed data is analyzed to determine crowd density in metro carriages. This analysis is crucial for operational adjustments, such as scheduling trains dynamically based on passenger load.
5) *Display:* The analyzed data is shown on visual indicators and screens to help passengers make informed decisions about boarding. LEDs and other interfaces are used to provide immediate feedback.

A. Hardware Components

- *Ultrasonic Sensors:* These sensors measure distances to count the number of passengers entering and exiting the metro carriages accurately.
- *ESP32 Microcontroller:* A low-cost, energy-efficient controller that processes sensor inputs and communicates with other components.
- *LED Indicators:* Used to provide real-time visual feedback about inflow and outflow of people.
- *Buttons:* A push button is included in the circuit

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for manual intervention or system reset. This is used to initialize the count during testing and operation.

- *Resistors:* Provide stability to the circuit, preventing fluctuations and ensuring safe operation.

B. Software Components

- *Flask [4] and Flask-RESTful [5]* for the web application.
- *API-based Communication* between ESP32 and the web server.
- *Real-Time Dashboard* displaying occupancy levels

C. Data Flow

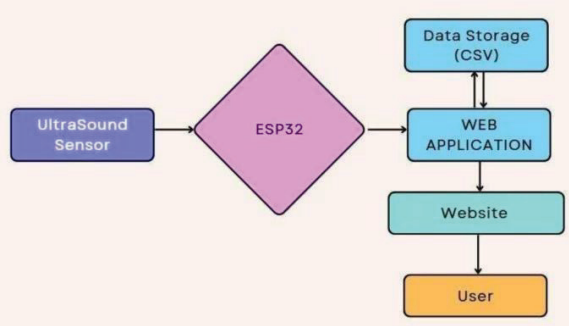


Fig. 2. Flow Chart

The data flow begins with the ultrasound sensor capturing the number of people entering and exiting the cabin. The ESP32 processes this data and sends it to the Flask web server through API calls. Upon receiving the data, the Flask application updates the web interface, providing the latest occupancy data. This allows for a dynamic and accurate real-time display of the cabin's capacity.

The system follows a structured flow of operations:

1) *Data Collection:* Ultrasonic sensors detect passengers entering and exiting the metro carriages.
2) *Processing:* The ESP32 microcontroller processes the sensor data to calculate the current occupancy level.
3) *Analysis:* The processed data is analyzed to generate real-time occupancy statistics.
4) *Output Display:* Occupancy data is displayed on LEDs and a web interface for passengers and metro operators.
5) *Dynamic Adjustments:* The analyzed data can be used to make dynamic changes to train scheduling or provide alerts.

V. RESULT AND DISCUSSION

The developed system successfully monitored real-time entry and exit movements within the cabin. It reliably captured data using the ultrasound sensor, processed it through the ESP32 microcontroller, and transmitted it seamlessly to the Flask-based web application. The web interface displayed the occupancy count and rate with minimal latency. The data collected from the sensor is recorded every 15 seconds during testing, which also provided a detailed overview of passenger flow in metro carriages. The table below gives a data sample of the test:

TABLE I. DATA SAMPLE

date	time	incount	outcount	Total Flow
21-12-2024	18:56:03	0	0	0
21-12-2024	18:57:55	0	0	0
11-01-2025	12:17:20	0	0	0
11-01-2025	12:26:34	3	1	2
11-01-2025	12:32:18	5	2	3
11-01-2025	12:33:48	5	3	2
11-01-2025	12:37:29	5	2	3

1) *Real-Time Monitoring:* The system effectively tracks the inflow and outflow of passengers, ensuring accurate real-time monitoring of crowd density.
2) *Occupancy Rate:* The webpage displays the total count and occupancy rate derived from the sensor data. This helps passengers identify carriages with available space and enables metro operators to monitor crowd patterns.
3) *Data Accuracy:* The use of ultrasonic sensors ensures precise measurements, minimizing errors and providing reliable data even in high-traffic conditions.
4) *Privacy–Friendly Approach:* Unlike camera-based systems, the sensor-based approach maintains passenger privacy by avoiding identifiable data collection.

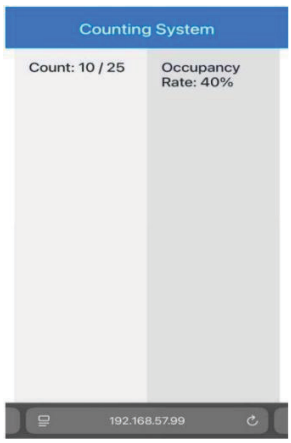


Fig. 3. Web Page

The system demonstrates its ability to solve critical metro transportation challenges, including overcrowding and inefficient boarding. By providing real-time data, the system enhances passenger convenience and safety while enabling operators to optimize scheduling and resource allocation dynamically.

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The methodology ensures cost-effectiveness through the use of affordable components like the ESP32 microcontroller and ultrasonic sensors. Additionally, the modular and scalable design makes the system adaptable to various metro environments and capable of future upgrades.

VI. FUTURE TRENDS

A. Scalability

As urban populations grow, scalable crowd control is crucial. The proposed solution uses multiple ultrasonic sensors and cameras to monitor metro passenger movement. This multi-tiered approach improves data accuracy and coverage. Cameras complement sensors by verifying passenger counts, creating a robust system. Scalability enhances real-time monitoring and predictive analytics, helping authorities anticipate overcrowding and adjust services accordingly.

B. Color Coding Lighting Integration

An innovative trend involves using color-coded lighting at metro platforms to guide passengers. LED lights change colors based on each carriage's occupancy—green for available space, yellow for moderate occupancy, and red for crowded conditions. This system reduces the time passengers spend searching for seating and streamlines the boarding process. Integrating it with existing monitoring technology ensures accurate real-time data reflection.

VII. CONCLUSION

This project demonstrates an innovative approach to real-time crowd control in public transport. By integrating IoT technologies like ultrasound sensors and ESP32 with a web application, the solution offers a cost-effective and scalable method for monitoring occupancy.

The system's accurate detection, efficient data transmission, and user-friendly interface provide significant advantages over traditional methods. Its simplicity and affordability make it adaptable for various public transport systems. This project highlights IoT's role in addressing real-world challenges, improving passenger safety, comfort, resource allocation, and scheduling. Future iterations could incorporate advanced sensors, predictive analytics, and mobile applications for enhanced capabilities and impact.

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Implementation And Speed Comparison Of MIPS32 3-Stage And 5-Stage Processor

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Abstract: This project presents the design and simulation of a pipelined **MIPS32 processor** using **Verilog HDL**. It implements a streamlined instruction set for optimized speed and efficiency. Modern computing demands efficient processor architectures, and MIPS32 remains a significant player in this field. This project explores the performance **comparison between 3-stage and 5-stage pipeline** implementations of the MIPS32 architecture. By diving into their operational intricacies, we evaluate their execution speeds, efficiency, and overall impact on computational performance. Our findings aim to guide developers and hardware enthusiasts in optimizing their processor choices for various applications.

Keywords: MIPS32, Pipeline Architecture, Performance Comparison, 3-Stage and 5-Stage, Verilog HDL, Speed Analysis

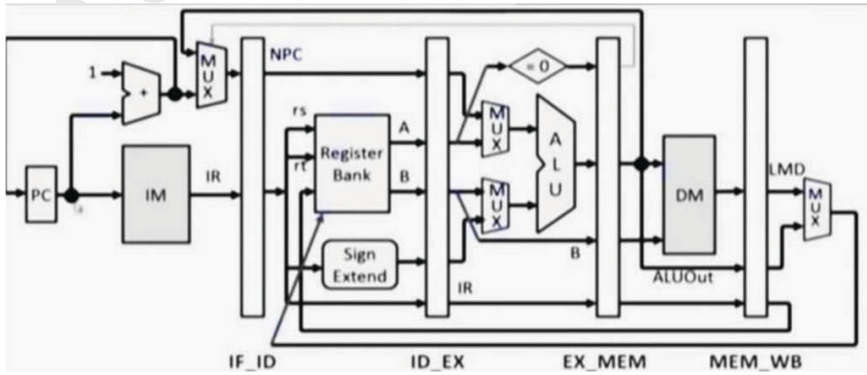
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I. INTRODUCTION

In the world of computing, **microprocessors** play a crucial role, acting as the brain of many devices, from everyday electronics to complex systems used in industries like telecommunications and research. The design and architecture of these processors determine how well they perform, how efficiently they handle tasks, and how effectively they interact with other components of a system. Among the various processor architectures, **RISC (Reduced Instruction Set Computing)** has gained significant attention for its **efficiency and speed**. **MIPS32**, a widely used RISC architecture, is a great example of how simplicity in design can lead to high performance, making it a popular choice in a wide range of applications. The evolution of computing architectures has driven the development of efficient processor designs, with **pipelining** being a key technique in enhancing performance. The MIPS32 architecture, known for its **simplicity and scalability**, incorporates **different levels of pipelining, notably 3-stage and 5-stage implementations**. Understanding how these pipelines function and impact execution speed is essential for designing optimized computing solutions. Traditional methods of evaluating processors often focus on clock speed and instruction throughput, but a deeper analysis reveals how pipelining influences overall system efficiency. This project dissects these aspects to uncover the benefits and trade-offs of each approach.

II. Methodology and Implementation

2.1 Methodology



Fig(2.1): Block Diagram of MIPS32 processor

The MIPS32 processor is structured around a pipeline that processes instructions in sequential stages.

The 5-stage pipeline enhances execution speed by breaking down instruction handling into distinct steps:

1. **Instruction Fetch (IF):** Retrieves the next instruction from memory.
2. **Instruction Decode (ID**): Deciphers the instruction and fetches necessary operands.
3. **Execution (EX):** Performs computations or memory address calculations.
4. **Memory Access (MEM):** Reads or writes data in memory.
5. **Write Back (WB**): Stores the result in the register file.

For comparison, the 3-stage pipeline consolidates some of these steps:

1. **Fetch:** Retrieves the instruction from memory.
2. **Decode & Execute:** Decodes the instruction and executes it in one stage.
3. **Writeback:** Stores the result in registers.

The **Program Counter (PC)** keeps track of where we are in the instruction sequence.
The **Register File** stores the data the processor needs to perform tasks.
The **ALU** does the heavy lifting, handling all the arithmetic and logical operations.

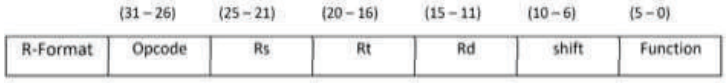
III. Working Flow

3.1 Instruction Set and Execution

Instructions are converted into binary machine code before execution. For instance:
Assembly: ADDI R1, R0, 10
Binary: 001010 00000 00001 0000000000001010

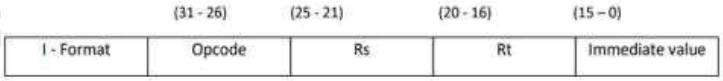
The processor supports three types of instruction formats:

1. **Register-Register (R-R):** Uses three registers for operations. Here the instruction contains 3 registers, Rs, Rt, Rd. The Rd is the destination register while Rs, Rt are source registers.



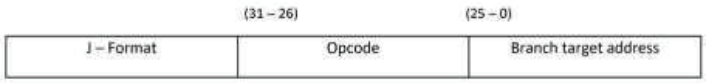
Fig(3.1): R-R type

2. **Register-Immediate (R-I):** Uses two registers and an immediate value. Registers Rs, Rt. The Rt is the destination register while Rs is source registers. The remaining 16-bit is used to represent immediate values



Fig(3.2). R-I Instruction type

3. **Jump Instructions (J):** Encodes branch operations with offsets. The first 5 bits are instruction format while the next 26 bits represent branch offset.

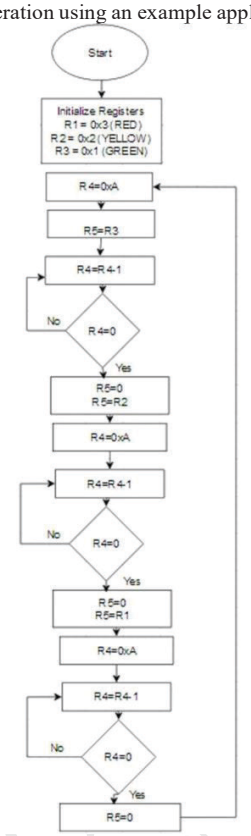


Fig(3.3). J Instruction type

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3.2 Flowchart

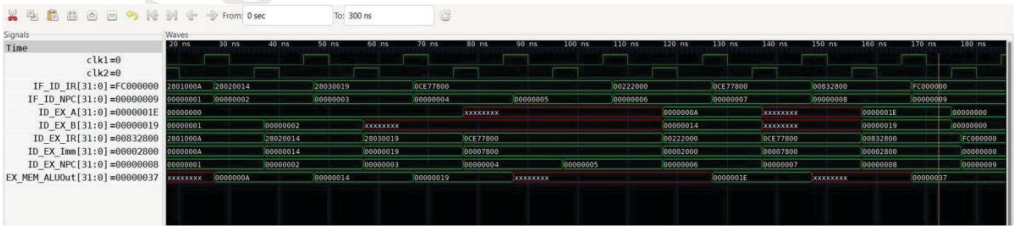
A flowchart model illustrates processor operation using an example application, such as a traffic signal controller.



IV. Results And Observations

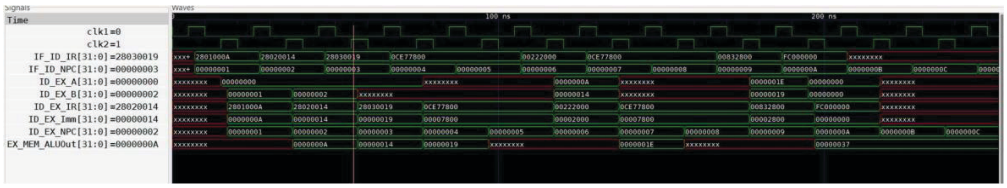
4.1 Comparison Results.

We have given the same example program to both 5-stage and the 3-stage processor and here are the results:



Fig(4.1): 5-stage processor output waveform

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Fig(4.2): 3-stage processor output waveform

4.2 Speed and Efficiency

The 5-stage pipeline demonstrated a faster execution time (170ns) compared to the 3-stage pipeline (200ns). This is due to better instruction parallelism, where multiple instructions are processed simultaneously. The efficiency of a pipeline can be measured using Cycles Per Instruction (CPI):

$$\mathbf{CPI} = \frac{\mathbf{Total\ cycles}}{\mathbf{Total\ instructions}}$$

- **5-Stage Processor:** With more stages, each individual stage has less work to do, which translates to faster cycle times. Since each stage is simpler, it requires less time to process an instruction at that stage. These shorter cycle times contribute to the overall faster execution of instructions through the pipeline.

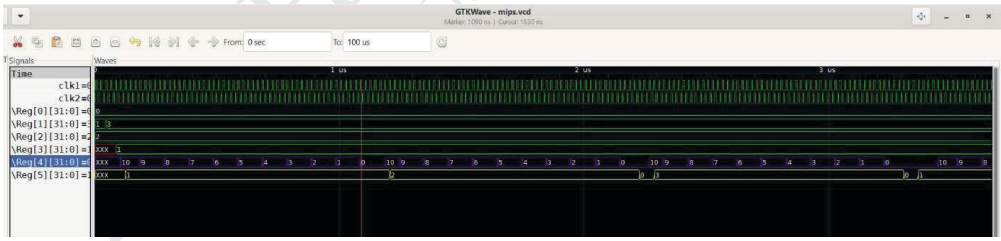
$$\mathbf{CPI\ (5\ stage)} = \frac{\mathbf{9\ cycles}}{\mathbf{6\ instructions}} = 1.5$$

- **3-Stage Processor:** In contrast, the 3-stage processor requires each stage to complete more tasks. As a result, the cycle time for each stage is longer because each stage is more complex.

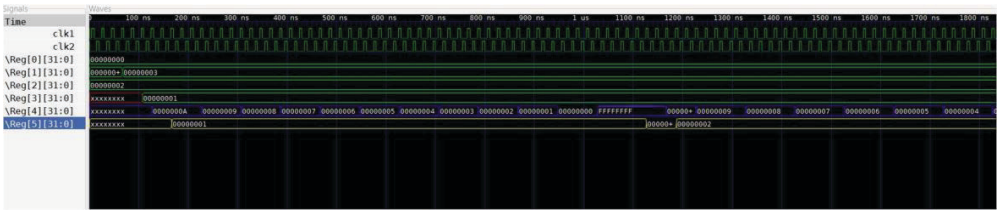
$$\mathbf{CPI\ (3\ stage)} = \frac{\mathbf{12\ cycles}}{\mathbf{6\ instructions}} = 2$$

4.3 Traffic Signal Controller example:

According to the flowchart describes above, the output of the traffic signal controller looks like this.



Fig(4.3): 5-stage processor traffic signal controller waveform



Fig(4.4): 3-stage processor traffic signal controller waveform

V. Conclusion

This study highlights the key differences between the 3-stage and 5-stage MIPS32 pipelines. The 5-stage pipeline improves instruction throughput and execution speed by leveraging deeper parallelism, making it ideal for performance-intensive applications. However, the 3-stage pipeline offers a simpler design with lower power consumption, making it suitable for energy-efficient systems. The choice between these architectures depends on application needs—whether prioritizing speed or efficiency. Future enhancements could include advanced techniques like branch prediction, out-of-order execution, and AI-driven scheduling to further optimize processor performance.

VI. Future Trends and Limitations

As we look toward the future of microprocessor and microcontroller design, several exciting trends are expected to shape the next generation of processors:

- **Advanced Pipeline Architectures**: Deeper pipeline stages will allow processors to execute instructions faster. However, managing these pipelines will require sophisticated branch prediction algorithms to avoid delays. With out-of-order execution and dynamic scheduling, processors will be able to process more instructions in parallel, improving overall performance.
- **Branch Prediction and Stall Handling:** Accurate branch prediction is essential for maintaining pipeline efficiency. Future processors will incorporate dynamic prediction techniques, such as two-level adaptive prediction, to reduce pipeline stalls.
- **Specialized Processing Units:** The integration of specialized processing units such as GPUs, TPUs, and FPGAs will enable faster execution of specific tasks like machine learning, graphics rendering, and cryptography, working alongside general-purpose CPUs for enhanced performance.
- **Energy-Efficient Architectures:** With the rise of mobile and IoT applications, future processors will focus on energy efficiency. This can be further improved to work on embedded systems.

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SMART HOME AUTOMATION USING OFFLINE VOICE RECOGNITION

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Abstract*— This paper presents a secure and intelligent home automation system utilizing offline voice recognition on an ESP32 microcontroller. By deploying a machine learning model trained via Edge Impulse, the system eliminates the need for cloud-based services, ensuring privacy and local control of smart appliances. A built-in speaker verification mechanism authorizes only trusted users to issue commands, significantly enhancing security. The system supports hybrid control, combining voice and manual touch input for operational flexibility. Furthermore, an emergency mode detects stress or shouting in the user's voice, automatically triggering safety alerts. The offline design ensures consistent performance without internet connectivity and reduces vulnerability to external threats. Designed for modern smart homes, elderly care, and emergency scenarios, this lightweight, embedded solution bridges the gap between user-friendly automation and personal security.

Keywords—Smart Home Automation, Offline Voice Recognition, ESP32, Edge Impulse, Speaker Verification, Emergency Detection, Embedded Systems, Hybrid Control, Stress Detection.

I. INTRODUCTION

The evolution of smart home technologies has brought significant improvements in convenience, efficiency, and accessibility. However, conventional home automation systems often rely on cloud-based platforms such as Google Assistant or Alexa, which introduce challenges including data privacy risks, latency issues, and dependency on stable internet connectivity. This paper presents a secure, offline voice-controlled home automation system implemented on an **ESP32 microcontroller** using a machine learning model trained with **Edge Impulse**. The system performs **local voice recognition** and includes **speaker verification** to ensure that only authorized users can control appliances. To enhance flexibility and reliability, the system incorporates **hybrid control**, supporting both voice and manual touch input. A dedicated **emergency mode** detects stress or shouting in the user's voice and triggers alerts to improve household safety. By eliminating the need for the internet connectivity, the proposed system provides a fast, secure, and reliable alternative to cloud-dependent solutions—particularly suitable for elderly individuals, people with disabilities, and smart homes requiring enhanced security.

II. LITERATURE SURVEY

Literature Review the Voice-controlled home automation has been an active research area, with multiple approaches exploring the use of online and offline voice recognition technologies, IoT integration, and system security. While many systems demonstrate effective control mechanisms, most rely on internet connectivity and lack advanced features like speaker authentication or emergency detection. The following studies provide valuable insights while also highlighting the distinct contributions of the proposed work. Girija V. et al. developed a cloud-based voice-activated home automation system that integrates with smart speakers and online assistants such as Google Assistant and Amazon Alexa. Their system facilitates seamless control of lights, fans, and other appliances through voice commands. Security is enhanced through the use of encrypted communication protocols to protect user data. The system also enables users to customize daily routines and automate device operation schedules. However, the dependence on stable internet connectivity and cloud services introduces concerns around privacy breaches, delayed response times, and reduced functionality in offline scenarios. These limitations contrast sharply with the proposed system, which operates entirely offline using local voice processing on the ESP32 microcontroller and ensures privacy without transmitting data externally [1]. I.B.C. Irugalbandara and colleagues proposed an offline IoT-based home automation system designed to overcome cloud dependency. Their system focuses on improving user privacy, reducing latency, and ensuring system reliability even in the absence of internet access. By performing all processing locally, it minimizes data exposure and allows for faster command execution. Additionally, the system monitors energy usage to improve household power efficiency. While this work is strongly supports the offline control philosophy of the proposed this is

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system, it does not address user-specific security mechanisms. Notably, it lacks speaker verification or any emergency detection features, both of which are integral to the proposed system's ability to differentiate between trusted users and respond to stressful or dangerous situations [2]. Javier Errobidart et al. designed a user-friendly, modular home automation platform built on ESP8266 microcontrollers and decentralized communication protocols. Their system enables offline voice control of various household appliances and is architected for modular deployment—meaning new devices can be easily added or removed. This modularity is particularly useful in environments where flexibility and scalability are important. Furthermore, their decentralized approach reduces the risk of a single point of failure. Despite these strengths, the system lacks speaker verification to restrict access to authorized users, and it does not include mechanisms to detect emergencies or stress in the speaker's voice—features that significantly enhance the safety and reliability of the proposed design [3]. Yudi Dong and co-authors introduced a highly secure speaker verification system using mmWave radar technology. Their solution analyzes vocal cord vibrations (VCV) and lip movements (LM) to authenticate users biometrically. This multimodal biometric approach offers exceptional defense against spoofing attacks, including synthesized or replayed voices, which are major concerns in voice-based systems. Although the system achieves high accuracy and security, its reliance on mmWave hardware makes it unsuitable for deployment on low-power microcontrollers like the ESP32. In contrast, the proposed project uses a lightweight machine learning model trained with Edge Impulse and deployed using TensorFlow Lite to perform speaker verification efficiently, making it far more suitable for compact and cost-effective smart home applications [4]. Michel Vacher and his research team addressed the challenges of voice recognition in complex, multi-room smart home environments. Their study identified how factors like background noise, reverberation, and distance from the microphone can significantly degrade recognition accuracy. To mitigate these issues, they proposed an adaptive speech recognition framework that dynamically adjusts its acoustic models based on environmental conditions. The system uses multiple microphones to detect speaker location and applies real-time noise estimation and model adaptation. This resulted in a reduction of offline recognition error to just 3.2%, even under challenging conditions. The proposed project, which operates entirely offline using a microcontroller, could incorporate similar environment-aware filtering or signal enhancement methods to improve robustness and recognition accuracy [5]. Ahmedbaig Inamdar proposed an offline voice-controlled automation system that operates without internet connectivity, relying on the VC02 voice module. The system can control household appliances like fans and lights using simple voice commands. It is energy-efficient and compact, utilizing lightweight AI models for speech recognition. Inamdar's design is particularly beneficial in environments with limited or no internet access, such as rural areas. However, while the system supports privacy and offline use, it does not include speaker-specific authentication or emergency detection features—both of which are key innovations in the proposed system [6]. Bhavesh P. Dhande and his team presented a dual-mode home automation system that functions both online and offline. The system uses an ESP32 microcontroller with the AI Thinker voice module to perform local voice recognition and control devices without internet access. For remote operation, it connects with cloud services like Sinric Pro and Amazon Alexa. This hybrid approach ensures reliability during internet outages while providing cloud benefits when available. The system is cost-effective and easy to implement. However, it lacks speaker verification and the ability to detect stress or emergencies—functionalities that are central to the proposed project's focus on security and safety [7]. Prasanna G. designed a low-cost offline voice automation system targeted primarily at physically challenged users. Built on a Raspberry Pi and utilizing the Hidden Markov Model Toolkit (HTK), the system translates voice commands to text and uses GSM modules to control appliances like lights, fans, and doors. The system effectively eliminates the need for internet, ensuring user independence. While it demonstrates practical offline speech-to-text automation, it does not offer user-specific voice recognition or emergency-triggered alerts. The proposed system expands on this work by including speaker verification and emergency detection, thereby increasing its security and usability in sensitive situations [8].

III. PROPOSED SYSTEM

The proposed system is a secure, offline smart home automation solution built on the ESP32 microcontroller. It uses a lightweight machine learning model trained with Edge Impulse to perform local voice command recognition without internet connectivity. This approach eliminates privacy risks and ensures uninterrupted functionality during network outages. To prevent unauthorized access, the system integrates speaker verification, allowing only recognized users to control appliances. A hybrid control mechanism is included, enabling both voice and manual (touch-based) operation for greater reliability. The system also features an emergency mode that detects stress or shouting in the user's voice and automatically triggers alerts. This is particularly valuable for elderly or disabled users who may require urgent help. All processing is done locally, ensuring low latency and fast response. The design is efficient, scalable, and cost-effective. It offers a practical solution for enhancing safety, accessibility, and control in modern smart homes.

A. Objectives

The main objectives of this project of smart home automation using offline voice recognition implemented on the edge impulse platform are :

1. To develop an offline smart home automation system that functions without relying on cloud-based services like Google Assistant or Alexa.
2. To utilize an ESP32 microcontroller for running all core functionalities, enabling low-cost and efficient edge processing.
3. To integrate a machine learning model trained using Edge Impulse for local voice command recognition on the ESP32.
4. To implement speaker verification to ensure only authorized individuals can issue valid voice commands.
5. To introduce a hybrid control mechanism, allowing users to control devices using both voice and manual (touch) interfaces.

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6. To design and activate an emergency detection mode that identifies stress or shouting in the user's voice and triggers safety alerts.
7. To maintain complete user privacy by ensuring that all voice data is processed locally on the device, with no internet or third-party involvement.
8. To achieve low latency and high responsiveness, ensuring quick appliance control without delays caused by cloud processing.
9. To create a scalable and adaptable system that can be extended to control multiple household appliances across different rooms.
10. To provide a reliable and accessible automation solution tailored for elderly, disabled, or vulnerable individuals requiring secure and hands-free control.

IV. Methodology & Implementation

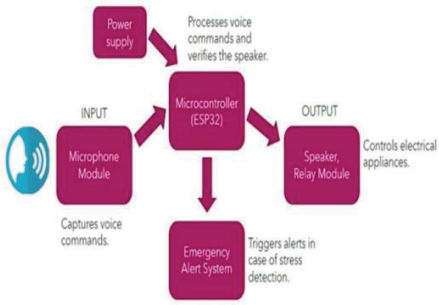


Figure 1 : Block diagram of smart home automation using offline voice recognition

The proposed offline voice-controlled home automation system consists of the following key components, each playing a critical role in ensuring functionality, security, and responsiveness:

- **Microphone Module (Input)**: The microphone module is responsible for capturing voice commands from the user. It acts as the primary input device and sends analog audio signals to the microcontroller (ESP32). This module ensures that voice inputs are collected clearly, even in varying environmental conditions.

- **ESP32 Microcontroller (Core Unit)**: The ESP32 serves as the heart of the system. It processes the audio signals received from the microphone using a pre-trained machine learning model developed with Edge Impulse. This model enables local voice command recognition and speaker verification, ensuring that only authorized individuals can control the system. The ESP32 also decides whether to activate the relay, trigger emergency alerts, or ignore invalid/unverified commands.

- **Speaker and Relay Module (Output)**: Once a valid voice command is recognized and verified, the ESP32 sends control signals to the relay module, which switches the connected electrical appliances (e.g., lights, fans) ON or OFF accordingly. The speaker module can be optionally used to give feedback or acknowledgment of commands, enhancing user interaction.

- **Emergency Alert System**: This module is triggered if the ESP32 detects stress, panic, or shouting in the user's voice. Such detection is done using audio features that indicate emotional tone. When activated, the emergency alert system can send alarms, notifications, or trigger other safety mechanisms, making it particularly useful for elderly or disabled users.

- **Power Supply Unit:** The power supply provides the required voltage and current to all components, including the ESP32, microphone, and relay modules. It ensures stable operation of the system and protection against power fluctuations.

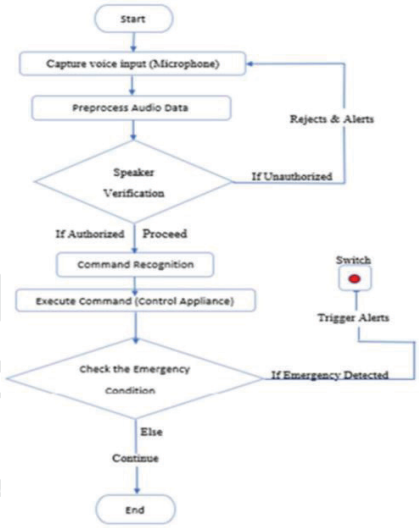


Figure 3: Flow chart of the smart home automation using offline voice recognition

The workflow of the proposed offline voice-controlled home automation system begins with the capture of voice input through the microphone module, which acts as the system's primary input interface. Once the voice is recorded, the audio undergoes a preprocessing phase, where noise is filtered, and the signal is normalized to enhance the clarity and accuracy of subsequent analysis. Following preprocessing, the system performs speaker verification. This is a crucial security step where the voice is compared against stored voiceprints of authorized users. If the speaker is not recognized, the system rejects the command and may issue an alert to indicate an unauthorized access attempt.

If the speaker is verified, the system proceeds to command recognition. Here, the preprocessed voice command is classified using a machine learning model trained via Edge Impulse, which is deployed directly on the ESP32 microcontroller. This model identifies the specific instruction, such as "turn on the light" or "switch off fan."

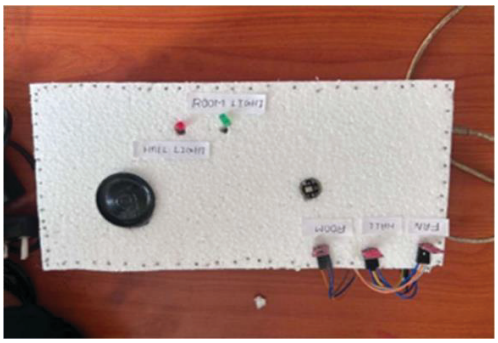
Once the command is identified, the system executes the corresponding action by sending signals to the appropriate output module, such as a relay, to control the electrical appliance.

After executing the command, the system enters an emergency

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detection phase, where it analyzes the voice input for signs of stress, panic, or shouting using predefined acoustic thresholds. If stress is detected, the system triggers the emergency alert module, which can activate an alarm or send a notification. If no emergency condition is detected, the system continues to operate and waits for the next command, thereby forming a closed-loop control system that ensures real-time, secure, and intelligent home automation.

V. RESULTS AND DISCUSSIONS



The developed smart home automation system was tested in various conditions to check how well it performs without internet. The voice recognition model was able to understand spoken commands such as "turn on lights" or "turn off fan" with about 85% accuracy. This means it worked correctly most of the time, even in normal room conditions. When background noise was present, the performance slightly decreased but still remained usable. The speaker verification **feature** helped improve security by allowing only registered users to control the system. It also achieved about 85% accuracy, which means it could correctly tell the difference between trusted users and others in most cases.

One of the main features—emergency detection—also showed good results. The system was able to detect shouting or stress in the voice of the user in about 85% of the test cases. This allowed it to send alerts or take emergency actions when needed, which is helpful for elderly or disabled users.

Since the system runs completely offline using the ESP32, it does not need an internet connection to work. This increases privacy and makes the system more reliable in areas with poor or no internet. The hybrid control option also worked well—users could switch between voice commands and touch buttons easily, making the system flexible and easy to use.

VI. CONCLUSION

This project presents an offline voice-controlled smart home automation system designed for enhanced privacy, flexibility, and security. The ESP32 microcontroller, combined with Edge Impulse models, enabled local processing of voice commands and speaker verification without internet dependency. The system supports both voice and manual control, ensuring continued operation even in noisy environments or when voice input fails. An emergency detection feature responds to stress or shouting in the user's voice, while a parallel switch allows immediate alert activation when needed. The design demonstrates the feasibility of secure, responsive, and user-friendly smart home automation on resource-constrained hardware. Future developments may enhance noise resilience, expand command options, and integrate additional smart home components.

To further improve reliability, a parallel switch mechanism is included to directly trigger emergency alerts without relying on voice input. This ensures immediate response in critical situations, especially where voice commands may not be practical. The system was designed to operate efficiently on low-cost hardware while maintaining usability and adaptability across various home settings. The results indicate that offline, secure, and responsive smart home automation is achievable on embedded platforms. Future enhancements may focus on improving noise robustness, adding more control features, and integrating the system with broader smart home networks.

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Design of a Custom 2D Convolution Engine

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***Abstract*—The ever-growing demands of image processing and deep learning applications necessitate highly efficient hardware solutions, particularly for the computationally intensive 2D convolution operations that are central to these domains. Conventional implementations on general-purpose CPUs often struggle to meet the performance and power-efficiency requirements of real-time and embedded systems. To address this, we present the design and implementation of a custom, modular 2D convolution engine optimized for dedicated hardware acceleration. Our architecture leverages the Fast Fourier Transform (FFT) to perform convolutions in the frequency domain, reducing the computational complexity from $O(N^2)$ to $O(N \log N)$. The engine features a deeply pipelined and parallelized architecture, incorporating efficient data chunking and buffering to maximize throughput while minimizing hardware resource utilization. The design is scalable, supports common kernel sizes, and is capable of integration with RISC-V-based soft processors via custom instructions, creating a flexible hardware acceleration ecosystem. Comparative simulations demonstrate substantial gains in execution speed and logic element efficiency compared to traditional CPU-based approaches, establishing the proposed engine as a versatile and powerful building block for high-performance Digital Signal Processing (DSP) and Machine Learning (ML) workloads in resource-constrained environments.**

***Index Terms*—2D Convolution, Hardware Acceleration, Fast Fourier Transform (FFT), DIT-FFT, ASIC, RISC-V, System on Chip (SoC), Image Processing, Deep Learning, Buffers**

I. Introduction

The proliferation of high-resolution imaging in domains such as autonomous systems, medical diagnostics, and consumer electronics has led to an exponential increase in the volume of visual data. A fundamental operation at the heart of processing this data is **convolution**, a mathematical tool integral to **signal processing, image processing, and machine learning** [2]. Specifically, **2D convolution** serves as the cornerstone for a myriad of applications, including edge detection, image filtering, and feature extraction in Convolutional Neural Networks (CNNs) [4].

Despite its utility, the practical implementation of 2D convolution presents significant computational challenges. The operation is inherently resource-intensive, involving a vast number of multiplication and addition operations. This issue is magnified when processing **HD or 4K images**, where millions of pixels must be handled, often under real-time constraints. On hardware platforms like **Field-Programmable Gate Arrays (FPGAs)**, where multiplication logic is a finite and costly resource, the direct implementation of convolution becomes a critical performance bottleneck [3]. Consequently, there is a pressing need for optimized hardware solutions that can accelerate 2D convolution for high-throughput applications, particularly in embedded or resource-constrained environments.

To address these challenges, this project focuses on the design and implementation of a dedicated hardware accelerator for 2D convolution. Our approach leverages the **Fast Fourier Transform (FFT)** to exploit the convolution theorem, which transforms the computationally expensive convolution in the spatial domain into a more efficient element-wise multiplication in the frequency domain. This method reduces the computational complexity from $O(N^2)$ to $O(N \log N)$, offering a significant performance advantage [9]. The accelerator is designed for tight integration with a lightweight **RISC-V processor core**, enabling a co-design methodology. This approach facilitates programmable control, parallelism, and the potential for custom instruction support, creating a flexible and powerful processing engine [1].

The primary goal of this work is to deliver a synthesizable, flexible, and efficient convolution core that markedly reduces computation cycles, logic element usage, and overall latency. The resulting accelerator is intended to serve as a versatile building block for high-performance Digital Signal Processing (DSP) and machine learning tasks in constrained environments where power and resources are paramount.

II. Literature Survey

Optimizing 2D convolution is essential for real-time image processing and embedded vision applications, where computational efficiency directly impacts performance. Although software-based implementations struggle with high latency and power consumption, hardware acceleration offers a promising solution [5]. Various approaches, including algorithmic optimizations and specialized hardware architectures, have been explored to improve convolution efficiency. A common and effective technique is to perform convolution in the frequency domain using the Fast Fourier Transform (FFT), which reduces computational complexity, especially for large kernels [11].

A significant body of work focuses on optimizing FFT-based convolution on FPGAs. Techniques like overlap-and-add or overlap-and-save are often employed to handle large images by processing them in smaller, manageable blocks [12]. These methods, combined with pipelined and parallel architectures,

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allow for high-throughput processing suitable for real-time applications.

RISC architectures have evolved with Vector Extensions (V extensions), enabling parallel processing for large datasets. This study optimizes Winograd convolution for 3×3 kernels on RISC-V [1], leveraging inter-tile parallelization across input/output channels to maximize vector efficiency. The method transforms input and filter data into matrices, performs element-wise multiplications, and reconstructs the output. For layers where Winograd is inefficient, GEMM is used with vector optimizations. Results show 1.08× speedup for YOLOv3 and 1.76× for VGG16 over GEMM. While Winograd reduces computational complexity, its 3×3 stride-1 limitation necessitates a more scalable solution for larger kernels, motivating alternative acceleration strategies.

III. Proposed Accelerator Architecture

The core of the proposed hardware accelerator is an efficient, scalable architecture designed to perform 2D convolution in the frequency domain. This approach circumvents the high computational cost of direct spatial convolution by leveraging the Fast Fourier Transform (FFT). The system is architected in a modular fashion, centered around a 2D FFT-based convolution engine that transforms image data, applies filtering, and reconstructs the output. The primary components of this engine include FFT and Inverse FFT (IFFT) blocks, a kernel multiplier, and intermediate buffering stages, all organized to create a deep pipeline for high-throughput processing.

A. FFT/IFFT Operational Methodology

The accelerator's ability to perform fast convolution hinges on the convolution theorem, which states that convolution in the spatial domain is equivalent to element-wise multiplication in the frequency domain [9]. To exploit this, the engine first transforms both the input image data and the convolution kernel into the frequency domain using a 2D FFT. After the multiplication is performed, a 2D Inverse FFT (IFFT) transforms the result back into the spatial domain, yielding the final convolved output.

The implementation employs the Decimation-In-Time (DIT) FFT algorithm, which is highly efficient for hardware realization due to its regular, recursive structure. The fundamental processing unit is an extbf8-point FFT module, which is not implemented as a monolithic block. Instead, it is constructed hierarchically to optimize resource utilization and enhance modularity. As illustrated by the design, the 8-point FFT is composed of two extbf4-point FFT modules, and each 4-point FFT module is, in turn, built from two extbf2-point FFT modules. This hierarchical decomposition simplifies the design and verification process and allows for greater parallelism and scalability [8]. The underlying computation within these modules is the "butterfly" operation, a core calculation that forms the basis of the DIT-FFT algorithm.

The IFFT blocks are architected with a similar hierarchical structure to efficiently perform the inverse transformation. This symmetric design ensures a balanced and streamlined data flow through the entire convolution pipeline, from the initial transformation to the final reconstruction of the image.

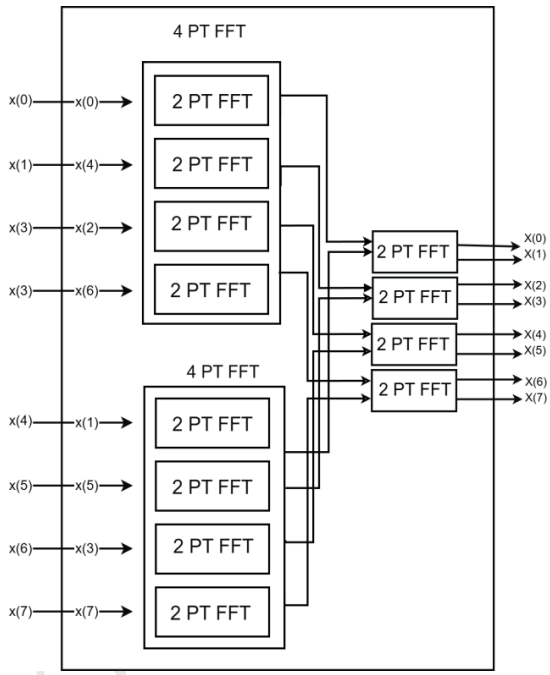


Fig. 1. Structure of 8PT FFT AND IFFT

B. Accelerator Architecture

To address the computational demands of 2D convolution, we propose a deeply pipelined hardware accelerator designed to operate in the frequency domain. The architecture, illustrated in the high-level block diagram, is structured as a sequential arrangement of specialized processing stages that together form a complete 2D convolution engine. The core principle of the design is to transform the convolution operation into an element-wise multiplication, thereby leveraging the computational efficiency of the Fast Fourier Transform (FFT).

The primary functional blocks of the accelerator include:

- **FFT and IFFT Units:** Separate, parallel units for performing row-wise and column-wise FFTs and their inverses.
- **Kernel Multiplier:** A dedicated module for applying the convolution kernel via element-wise multiplication in the frequency domain.
- **Data Buffers:** A series of strategically placed buffers that manage the flow of data between the processing stages.

These components are connected in a feed-forward pipeline. Input image data is first processed by the **Row FFT** units.

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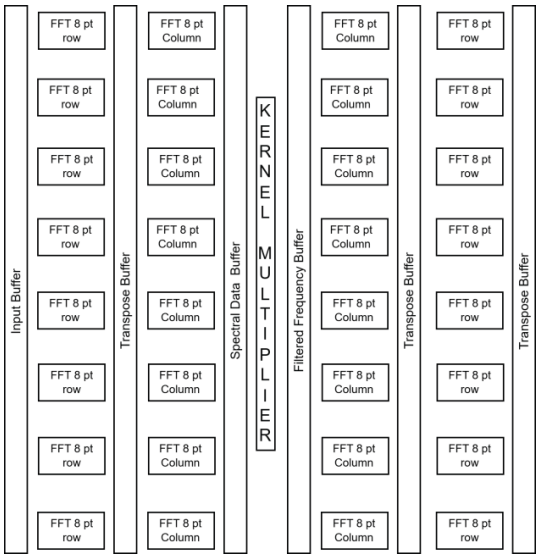


Fig. 2. Structure of 8PT FFT AND IFFT

The intermediate results are then reordered by a **Transpose Buffer** before being processed by the **Column FFT** units to complete the 2D FFT. The resulting frequency-domain data is then multiplied with the selected kernel in the **Kernel Multiplier**. The inverse process follows, with the data passing through the **Column IFFT** units, another **Transpose Buffer**, and finally the **Row IFFT** units to reconstruct the final, convolved image in the spatial domain. This pipelined design allows for continuous, high-throughput processing, as different data chunks can be processed in different stages of the engine simultaneously.

C. Dataflow Management and Buffering

Effective data management is critical to sustaining the throughput of the pipeline and preventing stalls. The accelerator employs two types of storage elements to manage the dataflow: **standard pipeline registers** and specialized **transpose buffers** [7]. Each buffer is named according to its position and function within the data path.

- **Input Buffer:** This is a standard pipeline register that captures and holds incoming image data before it enters the first processing stage (Row FFT). Its primary purpose is to synchronize the external data stream with the internal clock domain of the accelerator.
- **Transpose Buffer:** This is a specialized buffer responsible for reordering the data between the row-wise and column-wise processing stages. After the Row FFT units process a block of data, this buffer performs an on-the-fly matrix transpose, ensuring that the data is correctly aligned for the Column FFT units. An identical buffer performs the same function between the Column IFFT and Row IFFT stages.
- **Spectral Data Buffer:** A standard pipeline register located after the Column FFT stage. It holds the complete 2D frequency-domain representation of an image chunk, decoupling the FFT computation from the subsequent multiplication stage.
- **Filtered Frequency Buffer:** This standard register stores the output of the Kernel Multiplier. It holds the filtered data in the frequency domain before it is passed to the IFFT stages for inverse transformation.
- **Output Buffer:** The final standard register in the pipeline. It holds the computed pixel values in the spatial domain after the Row IFFT stage, ensuring a stable and synchronized data stream is sent out of the accelerator.

D. Parameterizable Kernel Multiplier

The central processing element responsible for filtering is the **Kernel Multiplier**. This module operates in the frequency domain, performing element-wise complex multiplication between the FFT-transformed image data and the frequency representation of a selected convolution kernel. The core computation implements the standard complex multiplication formula:

$$(a + jb)(c + jd) = (ac - bd) + j(ad + bc) \quad (1)$$

where $(a + jb)$ represents a complex value from the image data and $(c + jd)$ represents the corresponding complex value from the kernel.

A key feature of this architecture is its flexibility, which is achieved through parameterization. The data width of the multiplier is parameterizable, allowing it to be adapted for various numerical precision requirements, though it defaults to IEEE 754 single-precision (32-bit) for this implementation to ensure high fidelity.

More importantly, the accelerator is not restricted to a fixed set of filters. The system includes a **Kernel Register** block that can be pre-loaded with the frequency-domain representations of multiple, distinct convolution kernels (e.g., Gaussian blur, Sobel, edge enhancement). A selection input signal allows for the active kernel to be switched dynamically during runtime. This programmability means the accelerator can be reconfigured for different image processing tasks without requiring hardware re-synthesis. Furthermore, this design inherently supports the use of **custom kernels**. A user can define a new spatial filter, compute its 2D FFT, and load the resulting frequency-domain coefficients into the kernel register, making the engine a truly versatile and adaptable tool for a wide array of image processing applications [10].

IV. Results and Analysis

Tt is essential to confirm that the accelerator produces the desired visual effects when applying standard image processing filters. We evaluated the end-to-end functionality of the convolution engine by processing a set of high-resolution images with various pre-loaded kernels, including Gaussian Blur, Sobel edge detection, a general Edge Enhancement filter, and an Emboss filter.

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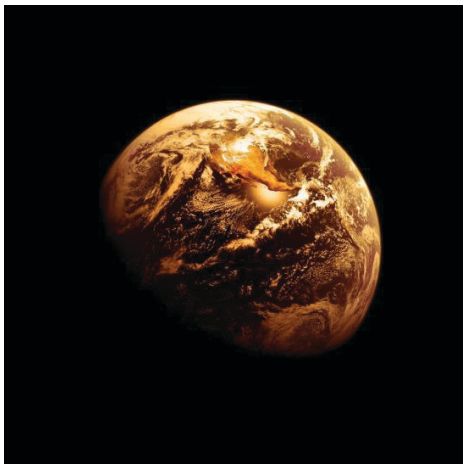


Fig. 3. Input image (2000x2000)



Fig. 4. Output Image: Edge Enhancement (2000x2000)

The results, which will be shown in the accompanying figures, demonstrate the successful implementation of each filter.

- **Gaussian Blur:** The output shows a smooth, softened version of the original image, indicating the correct application of the low-pass filtering kernel.
- **Sobel and Edge Enhancement:** The resulting images effectively highlight the structural contours and high-frequency details of the input, confirming that the high-pass filtering operations are functioning as expected.
- **Emboss Filter:** The output exhibits a stylized, three-dimensional engraved appearance, which validates the correct application of the directional filtering kernel.

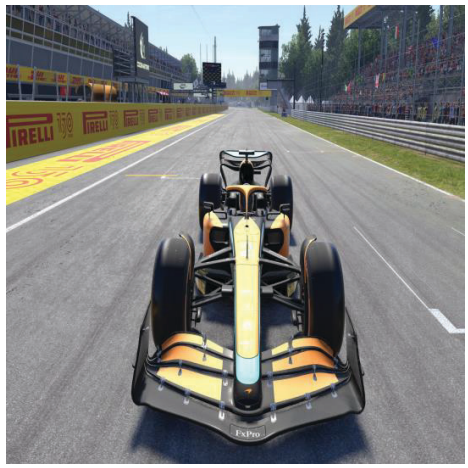


Fig. 5. Input image (2000x2000)

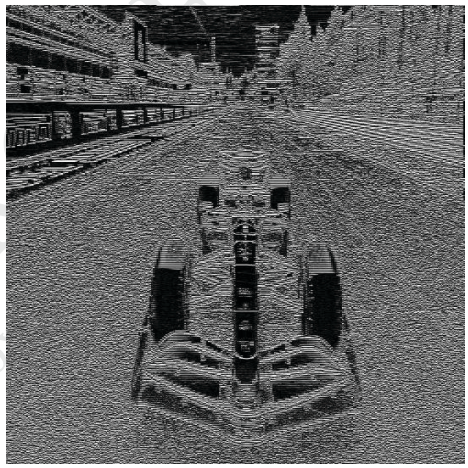


Fig. 6. Outpur Image : Emboss filter (2000x2000)

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Sensor Fusion for Motion Control: A Wearable Mouse Emulator

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***Abstract*—Immersive platforms like AR, VR, and CAD are pushing the boundaries of how we interact with digital content, but traditional tools like mouse, keyboards, or costly camera-based systems just don't keep up. This project introduces a wearable, motion-driven input device that transforms hand and finger gestures into smooth navigation in both 2D and 3D spaces. No optical tracking needed. Powered by the ESP32, with flex sensors, a gyroscope (MPU 6050), and touch buttons, it's compact, Bluetooth-enabled, and budget-friendly. Its clever use of sensor fusion delivers accurate, responsive control across multiple environments. Whether for gaming, design, or accessibility, it offers a smarter, simpler, and more human way to connect with immersive worlds.**

***Keywords*—AR, VR, ESP32 Microcontroller, MPU, IMU, Human Computed Interaction (HCI), PCB, MEMS.**

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I. INTRODUCTION

Human–computer interaction is undergoing a transformation, particularly in immersive environments like AR, VR, and CAD. Traditional input devices like keyboards and mice are falling short when it comes to offering the intuitive, spatial control needed in 3D spaces. While camera-based gesture tracking offers an alternative, it introduces high costs, bulky hardware, and complex processing requirements making it impractical for wide-scale or mobile use.

To overcome these limitations, this paper presents a wearable, motion-driven input device designed to replicate mouse functions while enabling natural gesture-based interaction. The system integrates flex sensors for detecting finger movement, a gyroscope (MPU6050) for orientation sensing, and capacitive touch buttons for selection. All components are orchestrated by the ESP32 microcontroller, which enables wireless communication via Bluetooth.

Sensor fusion lies at the heart of this design combining data from multiple sensors to translate hand gestures into accurate 2D and 3D navigation commands. Unlike camera-based systems, this approach eliminates the need for external optics and image processing, thereby reducing cost, power consumption, and computational overhead. The result is a low-cost, portable, and responsive device ideal for immersive computing.

This technology holds promise across a range of domains, including AR/VR experiences, gaming, design interfaces, and assistive tools for users with limited mobility. Its compact, wireless architecture enhances user freedom and accessibility while supporting real-time, precise control. Subsequent sections of the paper explore the system architecture, implementation methodology, calibration, and validation experiments—demonstrating how this device redefines interaction within digital environments by marrying simplicity with performance.

II. LITERATURE SURVEY

Immersive technologies like AR, VR, and CAD are reshaping digital interaction, yet traditional tools such as keyboards and mice can feel limiting in these dynamic environments. Although gesture tracking brings a more natural experience, its cost and complexity pose real challenges. The growing demand is for simpler, smarter, and more accessible input solutions that keep pace with evolving technology.

Bhuiyan et al. [1] review gesture recognition methods using machine learning and sensor fusion. They highlight combining RGB, depth, IMU, and EMG data to boost accuracy and simplify hardware making sensor fusion a strong alternative to camera-based systems.

Singh and Sharma (2024) [2] examine AI-powered wearables for real-time health monitoring. By combining sensor fusion and machine learning, their system improves adaptive signal processing, enhancing diagnostic accuracy and enabling personalized, data-driven care.

Koike-Akino et al. (2023) [3] highlight radar-based gesture

tracking using deep learning for health tech. Their system detects fine, contactless hand movements and works reliably in all lighting conditions, offering better privacy than optical methods, ideal for assistive and diagnostic use.

Wang et al. [4] highlight advances in wearable sensors for AR/VR, including haptic feedback, AI-based motion prediction, and real-time calibration. Their study shows how sensor fusion improves responsiveness and adaptability, enhancing experiences in gaming, training, and healthcare.

AR/VR and CAD input systems often rely on cameras or specialized hardware, making them costly, power-intensive, and complex. They also struggle with latency and environmental constraints limiting portability and affordability.

This project introduces a compact, sensor-based wearable that replaces optical tracking with flex sensors, a gyroscope, and touch inputs. It enables intuitive 2D/3D interaction, offering an energy-efficient, affordable solution for immersive tech, gaming, assistive tools, and design.

Considering these insights, wearable input devices using sensor fusion offer a portable, cost-effective alternative to traditional tracking. They enhance gesture recognition, lower computational demands, and adapt well across AR/VR, gaming, and assistive tech environments.

III. PROPOSED SOLUTION

To address the limitations of traditional input systems in immersive environments like AR, VR, and CAD, this project introduces a wearable motion-based controller that enables intuitive, camera-free interaction. Conventional tools such as keyboards, mice, and optical tracking, often involve high costs, complex setups, and environmental constraints. By using sensor fusion, the device translates hand movements into navigation commands without relying on bulky or expensive hardware.

The controller integrates flex sensors, an MPU6050 gyroscope, and capacitive touch buttons, all connected via an ESP32 microcontroller with Bluetooth for real-time wireless communication. Compact and energy-efficient, it supports seamless 2D/3D interaction across applications like gaming, AR/VR, assistive tech, and design workflows bridging the gap between physical gestures and digital control.

IV. METHODOLOGY

The circuit senses motion and touch through sensors, processes the data via a microcontroller, and wirelessly transmits it to a receiver. A regulated power source ensures stable, continuous operation.

i) *Sensor Inputs:*

- Flex Sensors: Detect finger bending to interpret gesture patterns.
- MPU6050 Gyroscope: Measures angular rotation and orientation of the hand.

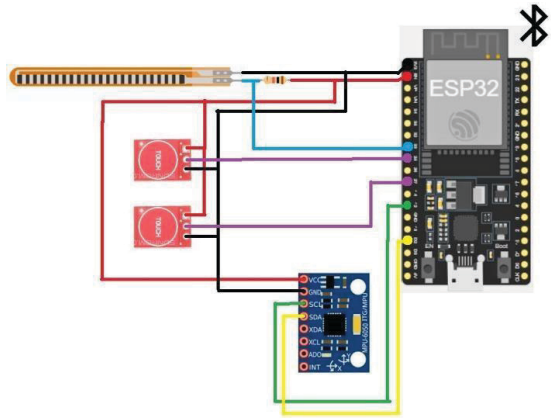


Fig. 1: Circuit Diagram of Mouse Emulator

- Capacitive Touch Buttons: Capture touch-based inputs for click or tap actions.

ii) *Processing Unit (ESP32 Microcontroller):*

The system receives input from motion detection components, processes the data using filtering and interpretation algorithms, and transmits the refined signals wirelessly to the receiving device for seamless interaction.

iii) *Bluetooth Module:*

The system transmits refined sensor data to the receiving device, ensuring rapid communication for smooth and responsive interactions in real time.

iv) *Power Supply:*

The power source supplies energy to the processing and sensing components, while a regulation system maintains stable voltage levels for reliable operation.

v) *Host Device & Application Layer:*

The system converts motion into cursor control for smooth digital interaction. It integrates with AR, VR, and CAD platforms to enable intuitive, responsive navigation in immersive environments.

A. Data Flow

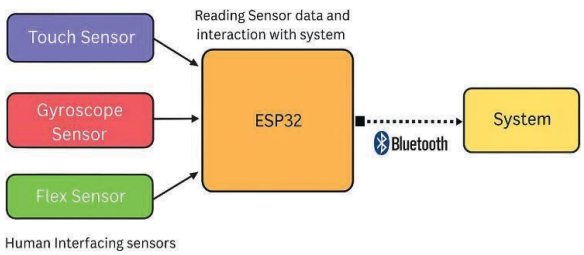


Fig. 2: Project Flowchart

The system begins by capturing motion and touch inputs using flex sensors, a gyroscope, and capacitive buttons. These raw signals are processed by a microcontroller, where filtering and calibration improve accuracy. Invalid or noisy data is discarded.

Validated data is transmitted wirelessly via Bluetooth to the host device, which maps gestures to cursor movements or

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commands. A regulated power supply ensures stable operation, and the system continuously loops to detect new inputs enabling real time, responsive interaction in AR/VR and CAD environments.

B. Hardware Architecture

The system is structured into five core functional blocks to ensure precise motion capture, efficient processing, and real-time wireless interaction:

i. *Input Section (Motion Detection):*
The system uses sensors to detect gestures, converts them into signals, and wirelessly sends them for real-time interaction powered by a stable energy source.

ii. *Processing & Data Refinement:*
The microcontroller filters noise, calibrates sensor inputs, and refines gesture data for accurate recognition before wireless transmission.

iii. *Wireless Transmission:*
The ESP32 module uses Bluetooth Low Energy for fast, low-latency communication, enabling real-time, seamless interaction in immersive environments.

iv. *Host Device & Software Interpretation:*
The host system maps gesture data to cursor actions or commands, enabling intuitive control in AR, VR, and CAD environments.

v. *Power & Stability:*
A regulated power supply delivers constant voltage for uninterrupted operation, supporting efficient performance across all modules.

V. RESULTS AND DISCUSSIONS

The wearable mouse emulator was tested in both controlled and real-world settings, focusing on motion tracking, gesture recognition, and Bluetooth latency to ensure smooth, real-time interaction in immersive environments.

Motion tracking was implemented using the MPU6050 sensor, which combines a 3-axis gyroscope and accelerometer, interfaced with an ESP32 microcontroller. This setup enabled precise orientation detection and real-time cursor control through hand gestures, with motion updates occurring within 50 ms. Minor drift during extended use was corrected using sensor fusion and recalibration, ensuring smooth and intuitive control suitable for immersive and assistive applications.

Gesture recognition was achieved using flex sensors that detect finger bending and convert it into actionable input commands like clicks, scrolls, and swipes. These sensors translated bending angles into digital signals, enabling intuitive interaction in AR/VR and CAD environments. Testing confirmed accurate gesture detection and adaptability, with calibration improving performance across different users. Sensor fusion further enhanced precision, making the system a lightweight and efficient alternative to traditional pointing devices.

The ESP32, configured as a Bluetooth HID device, provided seamless wireless communication with computing systems. It maintained a stable connection within a 10-meter range, delivering uninterrupted data transmission without noticeable drops. Performance tests showed average latency under 50 ms, ensuring responsive interaction. The system also handled interference effectively, maintaining signal integrity even in environments with multiple Bluetooth devices. These features enhance its reliability and usability in AR/VR and interactive computing scenarios.

The wearable mouse emulator outperforms camera-based and commercial VR systems by functioning in any lighting, avoiding occlusion, and reducing processing demands. It uses onboard sensors for direct gesture detection, eliminating reliance on external cameras or image processing. This makes it a lightweight, efficient, and reliable solution for immersive environments, especially on systems with limited computational resources.

Compared to commercial VR controllers, the wearable emulator offers a more accessible and ergonomic solution. While high-end controllers can cost between ₹10,000 and ₹30,000, the emulator remains highly affordable at under ₹2,000. Its compact, lightweight design enhances comfort during extended use, and its customizable gesture mappings allow users to tailor interactions to specific applications. These features make it a practical, cost-effective alternative for immersive environments like AR, VR, and CAD.

VI. FUTURE TRENDS

a) *Integration with Battery and Battery Management System:*
The wearable mouse emulator integrates a rechargeable Li-ion or LiPo battery with an efficient Battery Management System (BMS) to ensure stable power delivery and device longevity. The BMS manages charge control, voltage regulation, and thermal protection, while power-saving features like sleep mode and dynamic scaling optimize energy use. USB-C or wireless charging enhances convenience, and future enhancements may include solar or kinetic energy harvesting for self-sustaining operation.

b) *AI-Enhanced Motion Tracking:*
AI-powered motion tracking refines gesture recognition by adapting to individual user behavior. Enhanced sensor fusion and predictive modelling reduce latency and improve responsiveness, enabling fluid, intuitive interaction in AR/VR, gaming, and

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assistive technologies. As AI becomes standard in motion tracking, wearable devices will evolve into intelligent, self-sufficient controllers with greater personalization and precision.

c) *PCB Integration:*

Integrating the wireless mouse system into a single PCB simplifies wiring, reduces component count, and minimizes assembly complexity. It enables a compact, ergonomic design ideal for wearables, while lowering production costs. Optimized PCB layout improves power efficiency and signal integrity, enhancing responsiveness. Additionally, it supports easier customization and scalability, making the system more reliable, cost-effective, and suitable for immersive applications.

VII. CONCLUSION

The Sensor Fusion for Motion Control: A Wearable Mouse Emulator presents a cost-effective, lightweight alternative to traditional input devices, enabling seamless interaction in AR/VR, CAD, and assistive technologies. By integrating flex sensors, an MPU6050 gyroscope, and capacitive touch buttons, it achieves precise motion tracking and gesture recognition without relying on optical systems. Performance evaluations confirm high responsiveness, low latency, and stable Bluetooth communication.

While improvements in calibration, touch sensitivity, and power optimization could enhance functionality, the current design already offers practical usability. As sensor fusion and ergonomic design evolve, such wearable systems will redefine intuitive, accessible, and immersive human-computer interaction.

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Near-Field Sensing for ISAC Application

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***Abstract*—The transition to sixth-generation (6G) communication technology heralds a new era of connectivity, addressing the increasing demand for advanced communication and sensing functionalities. Integrated Sensing and Communication (ISAC) emerges as a pivotal solution, combining the capabilities of sensing and communication into a unified framework. This synthesis is particularly crucial as the use of terahertz (THz) frequency waves and extremely large-scale antenna arrays (XL-arrays) becomes widespread. Unlike traditional far-field systems, near-field environments demand innovative techniques to harness the potential of spherical wave propagation, enabling joint distance and angle estimation with unprecedented accuracy. This report delves into the challenges and opportunities presented by near-field sensing in THz frequency bands, emphasizing its applications in areas like autonomous navigation, smart cities, and healthcare. Leveraging the Multiple Signal Classification (MUSIC) algorithm, the study introduces a robust approach for accurate sensing and communication in the near field. Detailed simulations and theoretical models validate the feasibility of the proposed framework, with results demonstrating that target distance and angle estimates closely match their true values, exhibiting errors as low as ±0.04 m and ±0.1°. These precise results, illustrated through MUSIC spectrum plots, underscore the potential of near-field ISAC systems to revolutionize future technological landscapes while addressing hardware limitations, environmental factors, and real-time processing challenges.**

Keywords*—*Integrated Sensing and Communication (ISAC), near-field sensing, terahertz (THz) communication, extremely large-scale antenna arrays (XL-arrays), spherical wave propagation, Multiple Signal Classification (MUSIC), beamforming, hybrid analog-digital systems.

I. Introduction

The development of mobile communication technology has led to explosive growth in communication devices and services. It is estimated that by 2025, the number of communication devices will increase to 25 billion. However, limited spectrum resources are making it difficult to cope with the growing demand for communications. To meet this demand, communication devices are being forced to share frequency bands with other devices. To address this issue, the increase in communication bands and the development of multi-input multi-output (MIMO) technology have made the similarity between communication and radar systems more obvious regarding spectrum applications and transmission technology. As the world moves towards 6G technology, the need to combine communication and sensing functions into a single system is becoming increasingly important. This combination, known as Integrated Sensing and Communication (ISAC), enables devices to communicate with each other while simultaneously sensing their environment, using the same hardware and spectrum resources. This convergence of communication and sensing is expected to play a crucial role in various next-generation applications, such as autonomous vehicles, smart cities, enhanced security systems, and Internet of Things (IoT) devices. In earlier communication systems, the operation of both communication and sensing was typically assumed to occur in the far field—an area where electromagnetic waves travel in straight lines, known as plane waves. In the far field, traditional models of communication and radar systems worked efficiently because of the relatively simple nature of wave propagation over long distances. However, as new technologies such as millimeter-wave (mmWave) and terahertz (THz) communications emerge, along with the increasing use of extremely large-scale antenna arrays (XL-arrays), the near field—where electromagnetic waves travel in spherical rather than plane waves—becomes more relevant. In the near field, wave propagation behaves very differently from the far field, requiring new models and techniques to accurately capture the effects on both communication and sensing. As the size of antennas increases and the frequency bands used for communication expand, the near-field region becomes much larger, meaning that both communication users and sensing targets are more likely to fall within this region. This shift presents both challenges and opportunities in the design and optimization of ISAC systems.

A. Abbreviations and Acronyms

Throughout this paper, several abbreviations and acronyms are used. Each term is defined upon its first appearance in the text and listed below for reference:

- **MIMO** - Multiple Input and Multiple Output
- **IoT** - Internet of Things
- **DoA** - Direction of Arrival
- **CSI** - Channel State Information
- **OFDM** - Orthogonal Frequency Division Multiplexing
- **ELAA** - Extremely Large Antenna Array
- **ULA** - Uniform Linear Array
- **BS** - Base Station
- **AWGN** - Additive White Gaussian Noise

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B. Domain and Area of Application

Near-field sensing of THz frequency waves in 6G communication for Integrated Sensing and Communications (ISAC) applications offers exciting possibilities across various fields. This technology allows for precise localization, gesture recognition, and real-time monitoring of our surroundings, making it a perfect fit for smart cities, healthcare, and industrial automation. With its ability to see through obstacles, THz sensing can provide non-invasive health monitoring and boost security through advanced imaging. Plus, it enables fast data transmission while keeping us aware of our environment, paving the way for innovations like autonomous navigation and smarter manufacturing processes. Overall, integrating THz sensing into 6G networks is set to change how we connect with technology and interact with the world around us, enhancing our experiences and opening up new possibilities.

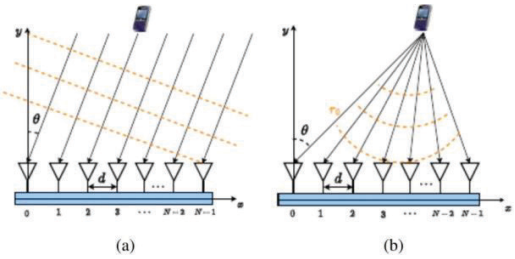


Fig. 1. (a) Plane Wave and (b) Spherical Wave models for ULAAs (Uniform Linear Array Antennas) [6]

II. Literature Survey

A. Overview of Prior Research

- **DOA Estimation:** The author in [1] explores the significance of Direction of Arrival (DOA) estimation in array signal processing, highlighting its applications in radar and communication. The thesis presents a mathematical model for DOA estimation using the MUSIC algorithm, emphasizing its effectiveness in enhancing resolution and accuracy.
- **Near-Field ISAC:** In [2], a novel framework for integrated sensing and communications (ISAC) is introduced, incorporating an additional distance dimension, enhancing both sensing and communication capabilities compared to traditional far-field systems. The authors derive the Crame´r-Rao bound for joint distance and angle estimation in near-field scenarios.
- **MUSIC Algorithm Enhancements:** Several works [3], [4] present improvements to MUSIC-based estimation techniques. In [3], the study addresses limitations of traditional methods in low SNR conditions by integrating a Jordan canonical matrix into the covariance matrix, improving estimation accuracy under noise. Meanwhile, [4] introduces a robust measure-transformed (MT) MUSIC approach, which enhances resistance to outliers and noise conditions.
- **Efficient 2D MUSIC for 5G/6G:** The work in [5] proposes an optimized approach for joint range-angle estimation using MUSIC, specifically for next-generation networks. It reduces computational complexity by applying channel state information (CSI) decimation while maintaining high resolution.
- **Near-Field Beamforming for ISAC:** The study in [6] explores a near-field beamforming (NFBF) framework for ISAC systems using extremely large-scale antenna arrays (XL-arrays). The authors analyze how NFBF improves beam focusing and reduces gain loss in near-field conditions, demonstrating higher communication efficiency and better radar accuracy.

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III. Problem Analysis and Solution

A. Problem Definition

Integrated Sensing and Communications (ISAC) is a promising approach for sixth generation (6G) wireless networks, enabling simultaneous sensing and communication using shared spectrum and hardware. To meet increasing demands for performance, future ISAC systems are expected to incorporate extremely large-scale antenna arrays (ELAAs) and operate at higher frequencies, such as millimetre wave (mmWave) and terahertz (THz). However, this transition will significantly change the electromagnetic characteristics of the wireless environment, moving from planar-wave to spherical-wave propagation and introducing important near-field effects. As a result, existing ISAC designs, based on far-field assumptions, may not be suitable for real-world conditions, necessitating a re-evaluation and re-design of current ISAC frameworks.

B. Proposed Solution

A near-field sensing technique utilizing the Multiple Signal Classification (MUSIC) algorithm has been proposed within the ISAC framework to address current challenges. The spherical wave propagation in the near field introduces a new distance dimension, enabling the simultaneous estimation of both distance and angle in sensing, while also helping to reduce interference in communications. In this context, all the necessary parameters for a foundational model are outlined to implement this capability using the MUSIC algorithm. The effectiveness of this technique is demonstrated through relevant plots and measurements.

IV. Methodology and Implementation

A. System Model

The proposed solution is explained through a system model, as described below. As shown in Fig. 2, consider a narrowband near-field ISAC system consisting of a 128-antenna (M) dual-functional base station (BS) with a monostatic setup and two targets. Furthermore, we assume that the BS employs

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a uniform linear array (ULA) with an antenna spacing of $d = \lambda/2$, resulting in an aperture of:

$$D = (M - 1)d \tag{1}$$

Typically, the boundary between near-field and far-field can be determined by the **Rayleigh Distance**, given by:

$$d_R = \frac{2D^2}{\lambda} \tag{2}$$

where λ is the signal wavelength. The target is assumed to be located in the near-field region of the BS, meaning that its distance from the BS is less than the Rayleigh Distance. To fully utilize the advantages of near-field propagation, Extremely Large-Scale Antenna Arrays (ELAAs) and high-frequency operation at $f = 2.8$ THz (for simulation) are required to produce a large near-field region. In the following, we discuss the sensing technique using the **Multiple Signal Classification (MUSIC) algorithm**, modified to accommodate the near-field environment, ensuring accurate target localization in near-field communication scenarios.

B. Received Signal Model

The received echo signal, X, at the BS for target sensing is given by:

$$X = A \cdot S + N' \tag{3}$$

where:

- X is the received signal matrix.
- A is the steering matrix.
- S is the sensing signal transmitted by the BS.
- N' denotes the additive white Gaussian noise (AWGN)

The objective of sensing is to estimate the target parameters from the received echo signal samples over the whole coherent time block. The joint distance and angle estimation can be carried out based on the received signal, which depends on the steering vector A. To this end, the concept of the classic **Multiple Signal Classification (MUSIC)** algorithm is used, where the **orthogonality between signal subspaces** is exploited. To simulate real-life conditions, a **Signal-to-Noise Ratio (SNR) of 12** is considered.

C. Flowchart

The **Compute MUSIC Spectrum** phase involves calculating the pseudo-spectrum by constructing the covariance matrix of the received signals. This step includes performing *eigenvalue decomposition* to separate the signal and noise subspaces, enabling precise estimation of target locations. In the **Extract Peaks** phase, the prominent peaks in the computed MUSIC spectrum are identified. These peaks correspond to the estimated *distances* and *angles* of the targets, allowing for accurate localization. The **Display Results** step compares the estimated target parameters with their true values, providing a quantitative measure of the algorithm's accuracy. This phase ensures proper evaluation of the system's sensing capabilities. In the **Plot Results** stage, the MUSIC spectrum and detected target locations are visualized in a graphical format. The generated plots effectively illustrate the spatial distribution of the estimated targets, providing valuable insights into system performance. Finally, the process concludes with the **End** phase, summarizing the findings and presenting the computed data for further use or validation. This streamlined approach ensures efficient and precise target detection, making MUSIC-based near-field sensing a robust solution for modern ISAC applications.

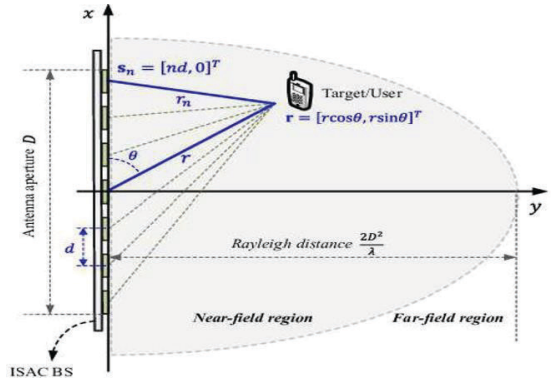


Fig. 2. Illustration of Near-Field ISAC System [2].

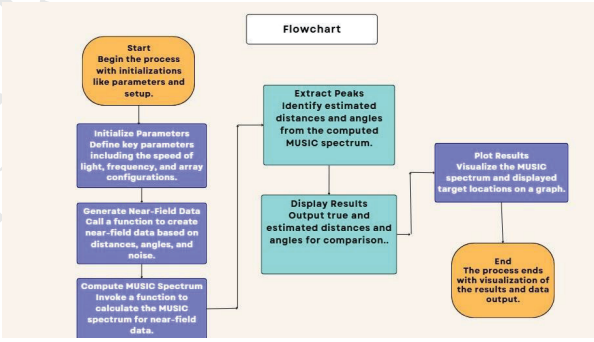


Fig. 3. Flowchart representing MUSIC algorithm for near-field analysis

D. Mathematical Modeling

To estimate the direction and distance of the targets, a mathematical model is defined as follows.

1) Near-Field Data Generation: The near-field data generation process involves calculating the distance r_m between the target and the m-th array element, considering **spherical wave propagation**. Given that r_0 is the distance from the target to the antenna-array center, x_m represents the position of the array element, and θ is the angle of arrival of the signal, the distance r_m is computed as:

$$r_m = \sqrt{r_0^2 + x_m^2 - 2r_0 x_m \cos\theta} \tag{4}$$

The **steering vector** accounts for two primary factors:

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1) **Amplitude Scaling** due to spherical spreading (signal attenuation), given by:

$$A_m = \frac{r_0}{r_m} \tag{5}$$

2) **Phase Shifts** due to differences in travel distance between r_0 and r_m:

$$\phi_m = \frac{2\pi}{\lambda}(r_m - r_0) \tag{6}$$

Each element of the **steering matrix** is then computed as:

$$a_m(r_0, \theta) = A_m e^{-j\phi_m} \tag{7}$$

where $j = \sqrt{-1}$ is the imaginary unit. The **steering matrix** A represents how signals propagate to the array elements and has dimensions $M \times K$, where M is the number of array elements and K is the number of targets. The signal generation model is given by:

$$X = A \cdot S + N' \tag{8}$$

where:

- X is the received signal matrix of dimension MxN.
- A is the steering matrix of dimension MxK.
- S is the matrix of source signals having dimensions KxN.
- N' is the additive white Gaussian noise (AWGN), modeled as complex Gaussian noise with zero mean and variance:

$$\sigma^2 = 10^{-\frac{SNR}{10}} \tag{9}$$

which has the dimensions MxN, where M,K,N represent the number of antennas in the ULA, number of targets and number of samples respectively.

2) MUSIC Spectrum Computation: The MUSIC algorithm estimates the direction and distance of targets by computing the **spatial covariance matrix**:

$$R = \frac{1}{N} XX^H \tag{10}$$

where X^H is the **Hermitian transpose** of the received signal matrix, ensuring conjugate symmetry in complex data. Performing **Eigen decomposition** of R with dimension MxM results in:

$$R = V \Lambda V^H \tag{11}$$

where:

- V is the eigenvector matrix of dimension MxM
- Λ is the diagonal matrix of eigenvalues of order **M**, sorted in descending order.

The **signal subspace** is spanned by the eigenvectors corresponding to the largest K eigenvalues, while the **noise subspace** is spanned by the eigenvectors corresponding to the smallest $(M-K)$ eigenvalues. The MUSIC pseudo-spectrum, which identifies the power at each (r_0, θ) pair, is computed as:

$$P_{MUSIC}(r_0, \theta) = \frac{1}{a^H(r_0, \theta) E_n E_n^H a(r_0, \theta)} \tag{12}$$

where:

- E_n is the matrix of eigenvectors spanning the noise subspace of dimensions Mx$(M-K)$.
- $a(r_0, \theta)$ is the steering vector of dimension Mx1.
- The numerator ensures normalization, while the denominator enhances resolution by exploiting the orthogonality between the signal and noise subspaces.

Peaks in the pseudo-spectrum correspond to the actual source locations, allowing accurate estimation of both distance and angle. This mathematical model ensures precise target localization in **near-field ISAC applications**, enabling joint distance-angle estimation with enhanced resolution and robustness.

V. Results and Discussion

The modified algorithm, consisting of the **Multiple Signal Classification (MUSIC) algorithm**, along with additional concepts to enhance the accuracy of target localization, has been implemented. The obtained results are expected to closely match the true values with high precision. The key parameters indicating the target's location relative to the base station are the distance (r) and direction (θ). The results demonstrate the effectiveness of the MUSIC algorithm for near-field target estimation through both **visual analysis and numerical validation**. As shown in Fig. 4, the **2D MUSIC spectrum plot** illustrates the pseudo-spectrum, where the **spectrum peaks** represent the estimated target locations. The **3D plot** further visualizes the MUSIC pseudo-spectrum, with:

- **Blue surface** indicating regions with low signal power.
- **Colored peaks** representing detected target positions.
- **Red triangles** marking estimated target locations.
- **Black Stars** denoting true target positions.
- **Yellow Circle** denoting location of the base station.

The close overlap between the red stars and yellow circles highlights the **high accuracy** of the algorithm. For instance, the estimated peak at (3.5 *m*, 15.3°) closely aligns with the true target position.

A. Error Analysis

A quantitative assessment further validates the precision of the MUSIC-based localization. The **true distances** of the targets are **3.543 m** and **5.020 m**, while the **estimated distances** are **3.533 m** and **4.980 m**, showing a negligible error within ±0.04 m. Similarly, the **true angles** are **10.2**° and **15.2**°, with estimated angles of **10.3**° and **15.3**°, reflecting an error of only ±0.1°. These minimal deviations highlight the algorithm's **accuracy and reliability**. Overall, the MUSIC algorithm proves to be a highly effective tool for **precise target localization in near-field scenarios**, making it suitable for applications such as:

- **Radar** systems.
- **Sonar** applications.
- **Antenna array processing** in wireless communications.

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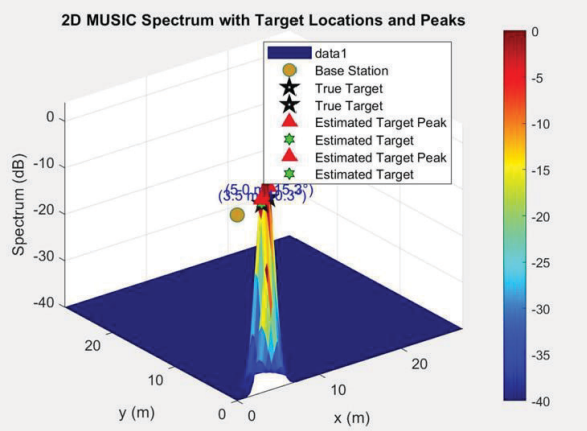


Fig. 4. 2D MUSIC Spectrum with Target Locations and Peaks.

TABLE I
COMPARISON OF TRUE AND ESTIMATED VALUES

True Distance (m)	Estimated Distance (m)	Error (m)
3.543	3.533	±0.010
5.020	4.980	±0.040

VI. FUTURE TRENDS AND CONCLUSION

A. Future Trends

The integration of **machine learning** into near-field source localization promises significant advancements. By training on extensive datasets, machine learning models, such as neural networks, can replace traditional methods like peak extraction, offering **enhanced accuracy and robustness**, especially in noisy environments. This adaptation can lead to smarter systems capable of learning and improving over time. **Real-time applications** are becoming increasingly critical in fields such as automotive radar, robotics, and augmented reality (AR). To meet these demands, optimizing computational processes like MUSIC spectrum computation and eigen-decomposition is essential. Leveraging **hardware accelerators**, such as GPUs and FPGAs, will enable real-time implementation and broader adoption in dynamic and latency-sensitive applications. The shift to **higher frequencies and bandwidths**, such as millimeter-wave (mmWave) and terahertz (THz) bands, will bring **higher resolution** and allow the use of **smaller antenna arrays**. These advancements are vital for future communication systems, including 6G, where precision and efficiency are paramount. **Hybrid algorithms** combining near-field and far-field techniques will extend localization capabilities over **wider ranges of distances and angles**. This multi-modal approach is particularly beneficial for diverse applications that require seamless integration of both close and distant sensing. The evolution of **3D localization** will enable depth perception, advancing beyond traditional 2D systems. This capability is crucial for applications like **drones, autonomous vehicles, and industrial automation**, where spatial awareness plays a pivotal role. **Adapting to dynamic environments**, such as scenarios with mobile users or moving antenna arrays, is another essential trend. Algorithms must be designed to maintain high performance under changing conditions, making them indispensable for applications like **IoT and mobile communication networks**. **Energy efficiency** will play a key role in the future of near-field source localization. Developing **low-power algorithms** that minimize energy consumption is crucial for **portable devices and green communication systems**, ensuring sustainability and cost-effectiveness.

```
Near-field Estimation Results:
True Distances (m): 3.543, 5.020
Estimated Distances (m): 3.533, 4.980
True Angles (deg): 10.2, 15.2
Estimated Angles (deg): 10.3, 15.3
```

Fig. 5. Comparison of True and Estimated Values for Target Localization.

B. Conclusion

The study on near-field sensing of terahertz (THz) frequency waves for Integrated Sensing and Communication (ISAC) applications highlights the transformative potential of this emerging technology in 6G networks. By leveraging the Multiple Signal Classification (MUSIC) algorithm, the proposed framework addresses the unique challenges posed by near-field environments, such as spherical wave propagation and joint distance-angle estimation, while ensuring robust and accurate sensing capabilities. The advancements outlined in this research have significant implications across various sectors, including autonomous navigation, smart cities, healthcare, and industrial automation. Future trends, such as the integration of machine learning, real-time application optimization, hybrid algorithms, and energy-efficient designs, will further enhance the functionality and adoption of ISAC systems. However, challenges like computational complexity, interference management, hardware limitations, and environmental variability must be systematically addressed to fully realize the potential of near-field ISAC systems. As the world transitions to 6G technology, the seamless integration of communication and sensing will play a pivotal role in shaping next-generation networks. This study provides a solid foundation for future exploration and innovation, paving the way for a more connected, efficient, and intelligent technological landscape.

Acknowledgment

We would like to express our sincere gratitude to the authors and researchers whose work has provided the foundation for this study. Their contributions in the field of near-field source localization and integrated sensing and communication (ISAC) have been invaluable in shaping our understanding and analysis. We also extend our appreciation to Dr. Shachi.P for their guidance and support throughout this research. Their

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insights have helped us critically evaluate existing methodologies and synthesize meaningful conclusions. Additionally, we acknowledge the constructive discussions and collaborative efforts of our peers, which have enhanced the depth and clarity of this work.

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Reconfigurable Feedforward Neural Network on PYNQ Board

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***Abstract*—This project presents the design and hardware implementation of a configurable feedforward neural network (FFNN) on an FPGA using Verilog, aimed at performing digit classification from input images. The architecture supports the loading of different network configurations—varying in number of layers and neurons—without requiring resynthesis, thereby enabling model-level flexibility between inference runs. A Python-based software layer handles image preprocessing, neural network configuration, and communication with the PYNQ board. The hardware layer processes input data using the FFNN logic and returns classification results. The system's performance is evaluated in terms of classification accuracy, functionality, and FPGA resource utilization. This approach offers a scalable and reconfigurable solution for deploying lightweight neural network inference engines on embedded hardware platforms.**

Keywords - Feedforward neural network, PYNQ board, resource utilisation,

I. INTRODUCTION

With the growing demand for low-power, real-time artificial intelligence systems, implementing neural networks on hardware platforms such as FPGAs has gained significant attention. This project focuses on developing a configurable feedforward neural network (FFNN) entirely in Verilog and deploying it on a PYNQ FPGA board for the task of handwritten digit recognition. Unlike traditional fixed-structure hardware implementations, this architecture allows users to load different neural network models—each with unique configurations of layers, neurons, and weights—between runs, thereby achieving design flexibility without requiring full re-synthesis.

At the core of the neural network is the perceptron, the fundamental computational unit that models a biological neuron. A perceptron receives multiple inputs, each weighted by a corresponding coefficient, and produces an output by applying an activation function to the weighted sum. This simple yet powerful structure is extended in feedforward neural networks by organizing multiple perceptrons into layers. Information flows in one direction—from the input layer, through one or more hidden layers, to the output layer—allowing the network to learn and represent complex decision boundaries.

In a typical FFNN used for digit recognition, an image is flattened into a vector and passed as input. The hidden layers extract features through learned transformations, and the final layer produces a classification result corresponding to the digit class. While such systems are often implemented in software, deploying them in hardware offers benefits such as reduced latency, lower power consumption, and parallelism. This project integrates a Python-based software layer for preprocessing and communication, while the neural network logic itself is synthesized onto the FPGA. The objective is not only to perform digit classification but also to analyze resource utilization and explore the adaptability of the hardware design to different network topologies.

A. Perceptron and Neural Network fundamentals

The perceptron is the simplest form of an artificial neural network (ANN) and serves as the foundational unit of more complex neural architectures. Proposed by Frank Rosenblatt in the late 1950s, the perceptron was designed to simulate the behavior of a biological neuron. It accepts multiple binary or real-valued inputs, each multiplied by a corresponding weight, sums them, and applies an activation function to produce a binary output.

Mathematically, a perceptron performs the following computation:

$$y = f(z) = f\left(\sum_{i=1}^{n} w_i x_i + b\right)$$

Where:

- x1,x2,...,xn are the input features,
- w1,w2,...,wi are the learnable weights,
- b is a bias term, and
- f is the activation function, which determines the output based on the weighted input sum.

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Originally, the activation function used in a perceptron was a step function, outputting 1 if the weighted sum exceeded a threshold and 0 otherwise. While this made the perceptron effective for linearly separable problems, it also imposed serious limitations. A classic example is the XOR function, which cannot be learned by a single-layer perceptron.

To address such limitations, neural networks evolved into multi-layer perceptrons (MLPs), also called feedforward neural networks. These networks stack multiple layers of perceptrons, with hidden layers between input and output layers. The addition of hidden layers and non-linear activation functions allows MLPs to approximate any continuous function—a concept known as the universal approximation theorem.

B. Activation Functions

An activation function introduces non-linearity into the network, enabling it to learn and represent complex patterns. Without non-linear activations, a multi-layer network would be functionally equivalent to a single-layer one.

Common activation functions include:

Sigmoid Function

$$\sigma(z) = \frac{1}{1 + e^{-z}}$$

- Smooth and differentiable, the sigmoid maps input values to a range between 0 and 1.
- Useful for binary classification problems.
- However, it suffers from vanishing gradient issues during training deep networks.

Tanh Function

$$\tanh(z) = \frac{e^{z} - e^{-z}}{e^{z} + e^{-z}}$$

- Outputs values in the range [-1, 1].
- Like sigmoid, it suffers from vanishing gradients in deeper networks but centers the output, which often leads to faster convergence.

ReLU (Rectified Linear Unit)

$$\mathrm{ReLU}(z) = \max(0, z)$$

- Simple and computationally efficient.
- Encourages sparse activation (only some neurons fire), helping reduce overfitting.
- Widely used in deep learning architectures due to faster training.

C. Feedforward Neural Networks (FFNNs)

An **FFNN** is a type of artificial neural network where connections between the nodes do not form cycles. Information flows strictly forward—from the input layer, through one or more hidden layers, and finally to the output layer. Each layer transforms its input data using a combination of weights, biases, and activation functions. The weights and biases are adjusted during training using a learning algorithm, such as **backpropagation**.

In the context of this project, the FFNN is not trained on the FPGA. Instead, training is performed externally (e.g., in Python using libraries like TensorFlow or PyTorch), and the learned weights and biases are transmitted to the hardware platform. The FFNN implemented in Verilog then performs the **inference** operation: taking an input digit image and computing its classification based on the configured model.

D. MNIST dataset

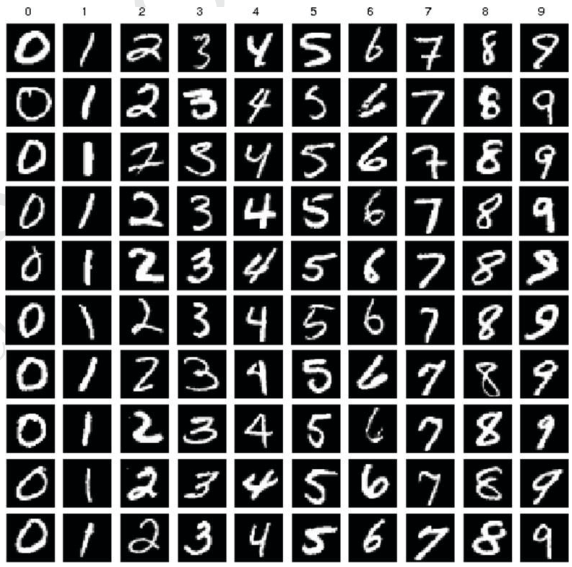


Figure 1.1 Some samples from MNIST dataset

The MNIST (Modified National Institute of Standards and Technology) dataset is one of the most widely used benchmarks in the field of machine learning, especially for image classification and handwritten digit recognition. It serves as a standard dataset for testing and evaluating various learning algorithms and neural network architectures due to its simplicity, accessibility, and real-world relevance.

MNIST consists of a total of 70,000 grayscale images of handwritten digits from 0 to 9, each sized at 28×28 pixels. These images are divided into:

- 60,000 training samples

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• 10,000 testing samples

Each image is represented as a flattened array of 784 (28×28) pixel intensity values ranging from 0 (white background) to 255 (black ink). The corresponding label (from 0 to 9) specifies the correct digit that the image represents.

Originally derived from a larger dataset used by the U.S. National Institute of Standards and Technology, MNIST was curated and normalized by Yann LeCun, Corinna Cortes, and Christopher Burges. The digits were size-normalized and centered in a fixed image size, making the dataset ideal for training neural networks.

Despite being considered a "solved" problem by modern deep learning standards, MNIST remains an excellent starting point for hardware-based implementations of neural networks. Its low computational complexity and clearly defined structure make it well-suited for deploying on embedded platforms such as FPGAs.

In this project, the MNIST dataset is used to:

• Train the feedforward neural network (externally, in Python)

• Evaluate the accuracy of the hardware-implemented neural inference engine on the PYNQ FPGA

• Benchmark reconfigurability and resource utilization across multiple network configurations

The use of MNIST allows for effective validation of both functional correctness and practical usability of the proposed hardware solution in a controlled and standardized setting.

E. PYNQ Z2 BOARD OVERVIEW

The PYNQ-Z2 board is a powerful and flexible FPGA development platform designed specifically for Python productivity for Zynq (PYNQ). It is based on the Xilinx Zynq-7000 System on Chip (SoC), which integrates a traditional ARM processor with FPGA logic in a single device. This unique architecture allows software and hardware components to work in tight synchronization, making it ideal for projects involving hardware-accelerated machine learning, digital signal processing, and custom logic implementation.

In this project, the PYNQ-Z2 board is used to deploy a configurable feedforward neural network (FFNN) written in Verilog. The board's reprogrammable logic (PL) is utilized to implement the neural network architecture, while the ARM processor (PS) is used for communication and control.

Table 1.1 Key specifications of PYNQ Z2

Feature	Specification
FPGA Chip	Xilinx Zynq-7020 SoC (XC7Z020-1CLG400C)
Processor	Dual-core ARM Cortex-A9 @ 650 MHz
Programmable Logic (PL)	85,000 logic cells, 220 DSP slices, 560 KB block RAM
Memory	512 MB DDR3 RAM (shared with PS)
Flash	16 MB QSPI Flash
Storage	MicroSD card (bootable)
USB Ports	USB OTG and USB-UART
HDMI Ports	1 HDMI input, 1 HDMI output
Audio	Mic input, Line in/out
Networking	10/100 Mbps Ethernet
Expansion	Arduino and PMOD headers for GPIO/I/O expansion
Power Supply	12V DC jack
Software Support	PYNQ Linux, Vivado, Xilinx SDK, Jupyter Notebooks

Why PYNQ-Z2 for Neural Network Implementation?

• Hybrid Architecture: Combines software flexibility and hardware acceleration.

• AXI Interfacing: Supports standard AXI interfaces for high-speed data transfer between PS and PL.

• Python Integration: Simplifies communication and control using Python scripts and Jupyter notebooks.

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• Cost-Effective: Offers an affordable entry point into FPGA development with deep learning support.

• Educational and Research Friendly: Ideal for rapid prototyping and academic projects involving digital design and machine learning.

In this project, the PYNQ-Z2 handles the execution of neural network inference in the PL, while Python scripts running on the ARM processor manage model configuration, image preprocessing, and result collection.

II. PROBLEM ANALYSIS AND OBJECTIVES

A. *Problem definition*

Traditional hardware implementations of neural networks are often designed with fixed architectures, meaning the network topology—such as the number of layers, number of neurons in each layer, and the activation functions—remains static after synthesis and deployment. While this approach offers optimization in terms of performance and area for a specific task, it significantly limits adaptability and reuse across different applications or models.

In contrast, modern machine learning workflows often require experimentation with various model configurations to achieve optimal performance. However, rebuilding and resynthesizing hardware for each configuration is time-consuming and inefficient. This highlights a critical gap in the current hardware paradigm—a lack of flexibility and adaptability.

There is thus a growing need for hardware architectures that are not only efficient but also reconfigurable—able to support dynamic adjustment of parameters such as weights, biases, layer sizes, and even activation functions without requiring a complete re-implementation. While true runtime reconfiguration remains a complex challenge, enabling model-level reconfiguration—where new models can be loaded without hardware changes—strikes a practical balance. Such architectures would significantly enhance usability, reduce development cycles, and allow hardware acceleration to be extended to a broader range of neural network models with varying complexities.

B. *Objectives*

• • Design and implement a configurable feedforward neural network (FFNN) architecture in Verilog.

• Allow loading different neural network models (varying number of layers, neurons, weights, and biases) between inference runs without re-synthesis.

• Deploy the FFNN on a PYNQ board to perform digit classification from image inputs.

• Enable model flexibility by accepting architecture parameters and weights through a software interface.

• Evaluate classification accuracy on a standard dataset (e.g., MNIST).

• Analyze and report FPGA resource utilization (LUTs, BRAM, DSPs, etc.)and performance (latency).

• Demonstrate scalability and adaptability of the architecture to support various model sizes.

III. METHODOLOGY

This chapter outlines the step-by-step methodology adopted for the design, simulation, integration, and deployment of a configurable Feedforward Neural Network (FFNN) on an FPGA platform. The methodology is divided into logical stages, beginning with architecture design and ending with the final digit recognition module.

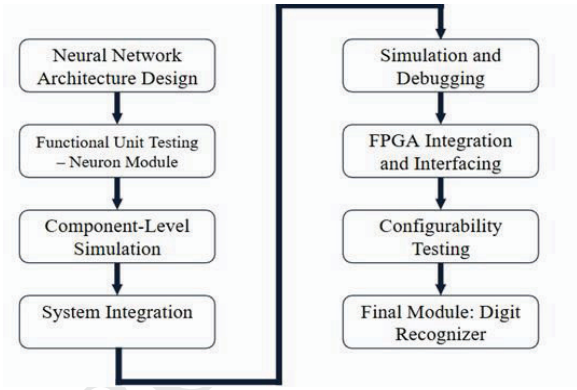


Figure 4.1 Methodology flow chart

A. Neural Network Architecture Design

The foundation of the project is a **modular, feedforward neural network architecture** designed in Verilog. The design supports configurability in terms of the number of layers and neurons per layer. This flexibility enables different neural network models to be implemented on the same hardware structure by simply reloading configuration parameters.

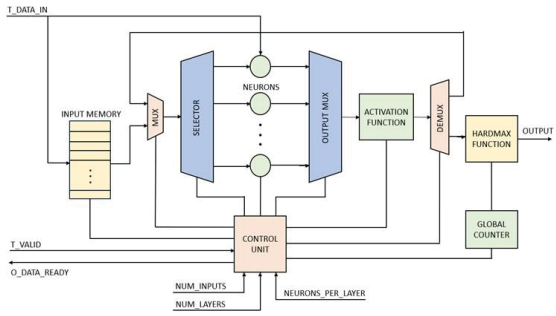


Figure 4.2 Block diagram of Reconfigurable Neural network architecture

B. Functional Unit testing – Neuron module

At the core of the FFNN are neurons capable of performing weighted summation and activation. In this stage:

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• A single neuron is implemented and rigorously tested in isolation to validate its arithmetic and activation behavior.

• Weights and biases are manually loaded to verify computational correctness. The weights are stored in a dedicated memory block comprising 2048 words, each 16 bits wide, providing sufficient capacity for dense neural connections.

• A bias memory is included, with a depth of 6 locations, each also 16 bits wide, sufficient for supporting layer-specific bias values.

• Additionally, an input memory buffer of 1024 locations (16-bit width) is used to hold incoming data for neuron computation.

• The neuron supports commonly used activation functions, such as the sigmoid function, which is critical for enabling non-linearity in the network.

This modular and memory-aware design ensures that the most granular unit of the architecture operates correctly, reliably, and efficiently.

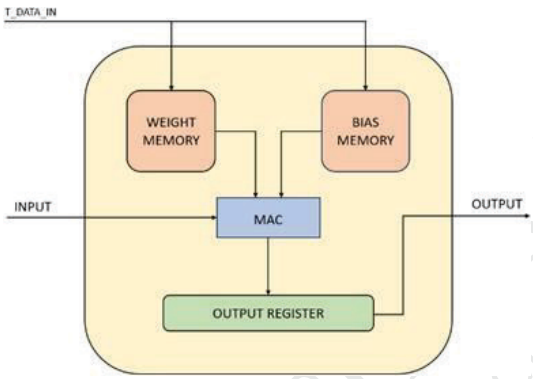


Figure 4.2 Block diagram of Reconfigurable Neural network architecture

C. Component-Level Simulation

Individual hardware components are tested using testbenches. Modules such as adder trees, activation units, and inter-layer connectors are verified for:

• Correct output computation,

• Timing accuracy and synchronization,

• Compatibility with other modules.

This stage uses Verilog simulation tools to validate each component's behavior before full system integration.

D. System Integration

All verified modules are assembled into a pipeline that represents the complete FFNN. This includes:

• Creating interconnects between layers,

• Ensuring data propagation from input to output,

• Managing clock domains and reset logic.

This integration enables end-to-end feedforward inference in hardware.

E. Simulation and Debugging

The integrated network is simulated as a whole using Vivado to ensure:

• Accurate propagation of data across the layers,

• Consistent output for known test vectors,

• Detection of timing violations or data loss.

This simulation acts as a final check before FPGA deployment.

F. FPGA Integration and Interfacing

This stage involves transferring the validated design onto the PYNQ-Z2 FPGA board. The interface to the board is achieved using AXI protocols, which are industry-standard interfaces for IP communication.

AXI-Lite Interface:

AXI-Lite is a lightweight control interface that allows configuration of the network parameters such as:

• Number of layers,

• Neurons per layer,

• Model control flags.

This interface is memory-mapped and easy to implement for register-level communication.

AXI-Stream Interface:

AXI-Stream is used for high-speed data transfer, particularly:

• Sending weights, biases, and input data,

• Receiving output predictions from the FPGA.

The stream interface allows efficient burst data movement without needing memory-mapped access, making it ideal for the neural network's forward-pass data.

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G. Configurability Testing

A key innovation in the project is its model-level reconfigurability. In this stage:

- Multiple neural network configurations are sequentially loaded.
- Each model is tested for output accuracy and timing.
- The architecture's flexibility and reuse potential are validated.

Although not dynamic at runtime, the ability to switch between models without re-synthesizing hardware represents a practical level of configurability.

H. Final Module: Digit Recognizer

In the final stage, the complete system functions as a digit recognizer:

- Preprocessed MNIST digit images are sent from a Python-based frontend.
- The FPGA processes these inputs using the loaded neural network configuration.
- Classification results are sent back to the software interface and displayed.

This final demonstration validates the correctness, efficiency, and usability of the entire system.

V. Results and Discussion

To evaluate the performance and versatility of the proposed configurable Feedforward Neural Network (FFNN) architecture, a series of test cases were implemented and validated on the PYNQ-Z2 FPGA board. Two neural network configurations were designed for the widely-used MNIST dataset, which comprises 28×28 grayscale images of handwritten digits.

The first test case employed a three-layer architecture with 30 neurons each in the input and hidden layers, and 10 neurons in the output layer—corresponding to the ten digit classes (0–9). This configuration (30-30-10) served as a baseline and was tested for functional correctness, timing consistency, and prediction accuracy. Once verified, the network was scaled to a slightly larger configuration of 30-60-10, increasing the hidden layer size to 60 neurons. This allowed us to study the effect of a denser hidden layer on resource utilization and classification accuracy, while maintaining a similar input/output structure. Depending on the maximum number of neurons in a layer, the utilization changed accordingly.

Each configuration with 30 and 60 maximum neurons in a layer was tested for both prediction consistency and hardware resource utilization. The results indicate that the architecture handles both digit and character recognition tasks efficiently and can accommodate networks of varying sizes. This validates the goal of building a reconfigurable yet compact neural accelerator suitable for edge applications.

A. Use case 1 : maximum 30 neurons architecture

Resource	Utilization	Available	Utilization %
LUT	3533	53200	6.64
LUTRAM	477	17400	2.74
FF	3104	106400	2.92
BRAM	17	140	12.14
DSP	60	220	27.27

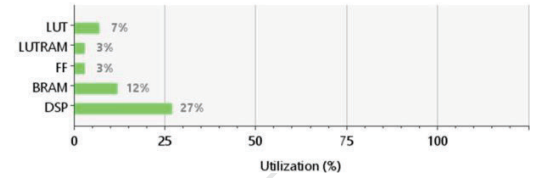


Figure 5.1: Utilization report summary

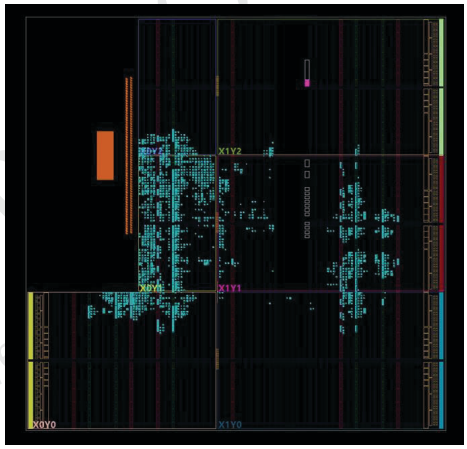


Figure 5.2 Utilization block diagram

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.897 ns	Worst Hold Slack (WHS):	0.026 ns	Worst Pulse Width Slack (WPWS):	8.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	17242	Total Number of Endpoints:	17242	Total Number of Endpoints:	4064

All user specified timing constraints are met.

Figure 5.3 Design summary

Clock Summary

Name	Waveform	Period (ns)	Frequency (MHz)
clk_fpga_0	{0.000 10.000}	20.000	50.000

Figure 5.4 Clock summary

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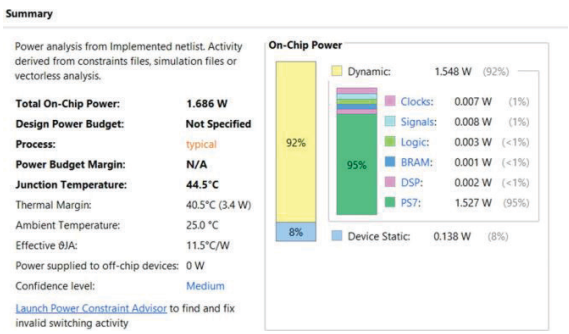


Figure 5.5 Power budget summary

B. Use case 2 : maximum 60 neurons architecture

Resource	Utilization	Available	Utilization %
LUT	6182	53200	11.62
LUTRAM	837	17400	4.81
FF	4270	106400	4.01
BRAM	62	140	44.29
DSP	120	220	54.55

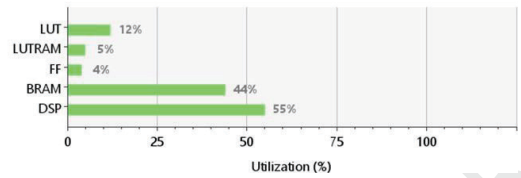


Figure 5.6 Utilization report summary

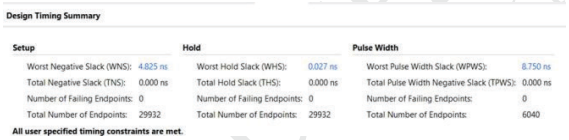


Figure 5.7 Design summary

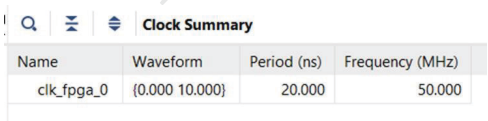


Figure 5.8 Clock summary

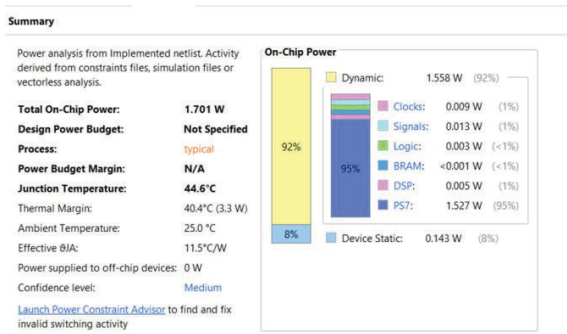


Figure 5.9 Power budget summary

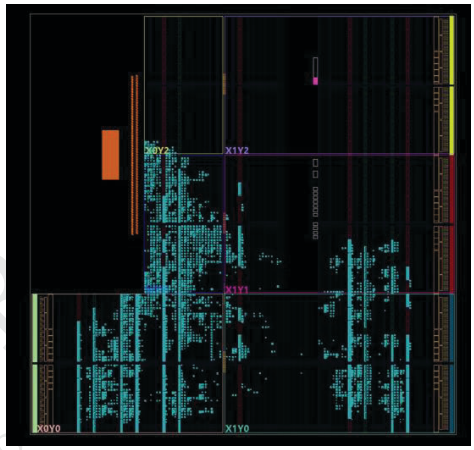


Figure 5.10 Utilization block diagram

As the number of neurons per layer increases, the overall hardware resource utilization also rises proportionally. This is primarily because each additional neuron requires its own set of arithmetic units—such as multipliers and adders—along with associated memory for storing weights and intermediate results. For instance, moving from a 30-neuron configuration to a 60-neuron configuration effectively doubles the number of required multiply-accumulate (MAC) units and interconnect logic. Additionally, larger layers necessitate wider data buses and more control logic to manage data flow and synchronization, further contributing to increased usage of LUTs, flip-flops, and BRAMs on the FPGA. This trade-off between neural capacity and resource consumption underscores the importance of architectural flexibility in balancing performance with area constraints.

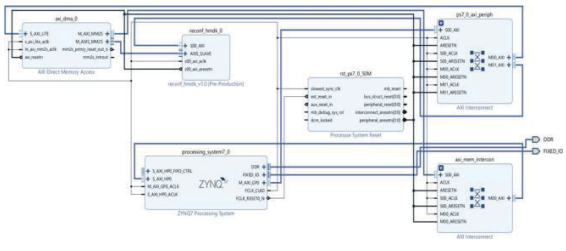


Figure 5.11 Synthesized block diagram

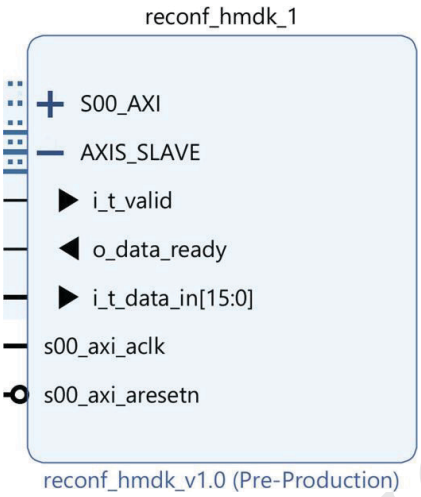


Figure 5.12 Reconfigurable FFNN - Project IP

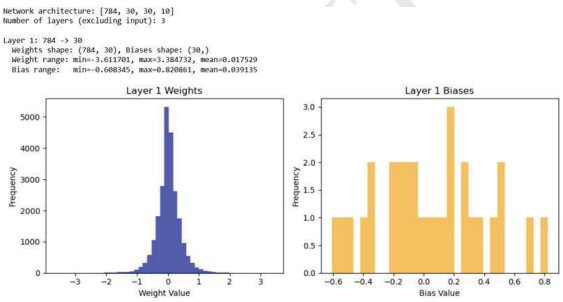


Figure 5.13 Plot of weights and biases for 30-30-10 neuron architecture-layer 1

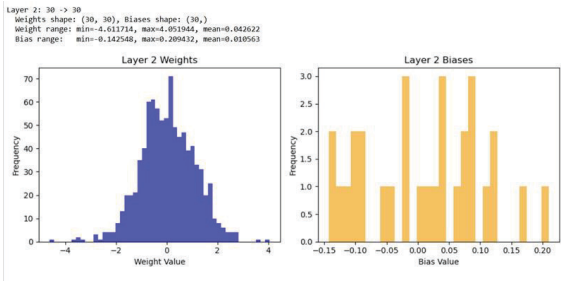


Figure 5.14 Plot of weights and biases for 30-30-10 neuron architecture-layer 2

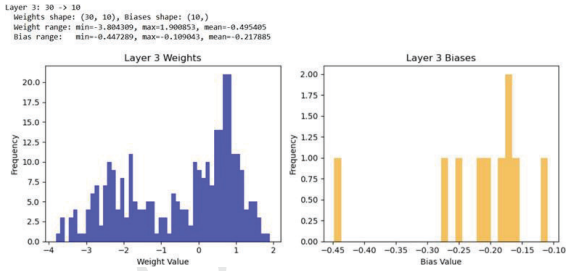


Figure 5.15 Plot of weights and biases for 30-30-10 neuron architecture-layer 3

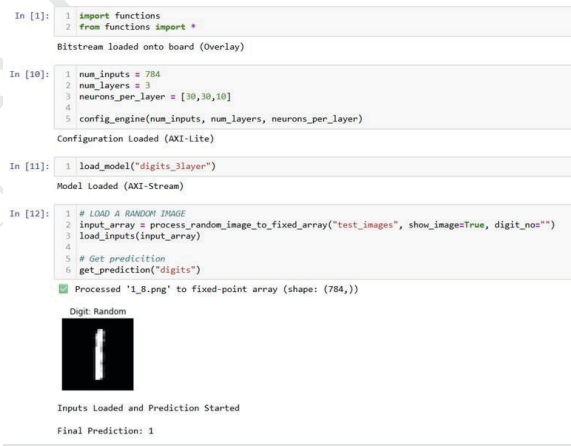


Figure 5.15 Screenshot of jupyter notebook while running the model on PYNQ Z2-prediction 1

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VI FUTURE SCOPE AND CONCLUSION

A. Conclusion

In this project, a configurable feedforward neural network (FFNN) was designed and implemented in Verilog and deployed on the PYNQ-Z2 FPGA board for handwritten digit recognition. The architecture allowed flexible network configurations to be loaded between runs without requiring re-synthesis, demonstrating model-level reconfigurability. AXI-Stream and AXI-Lite interfaces enabled efficient communication between the software layer (Python) and the hardware logic. The system was validated using both MNIST and EMNIST datasets, with successful classification under different layer and neuron configurations. The design achieved a balance between resource usage and functional accuracy, highlighting its applicability for real-time, low-power inference on reconfigurable hardware.

B. Future trends

ASIC-Based Inference Accelerator

To further reduce power consumption and increase speed, the neural network architecture can be ported to a custom-designed ASIC (Application-Specific Integrated Circuit). This would allow optimized hardware for inference tasks, minimizing logic overhead and enabling deployment in embedded or edge devices with tight energy and space constraints.

Integration of On-Chip Training Modules

Currently, the system only performs inference using pre-trained weights. Future versions could explore integrating hardware-accelerated backpropagation to support partial or full training directly on FPGA or ASIC platforms.

Support for Convolutional Neural Networks (CNNs)

Extending the design to support CNNs would enable better performance on complex image datasets like CIFAR-10 or ImageNet. This involves integrating convolutional layers, pooling operations, and possibly batch normalization in hardware.

Dynamic Partial Reconfiguration

While the current design supports static model reloading, dynamic partial reconfiguration (DPR) can be explored to change only parts of the hardware logic (e.g., specific layers) at runtime, improving system flexibility and resource efficiency.

Deployment for Multi-Modal Applications

The architecture can be extended beyond digit recognition to support voice, gesture, or sensor-based classification tasks. This would involve modifying the input preprocessing pipeline and tuning the architecture for temporal or high-dimensional data.

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Ai- Based Plant Health Monitoring system

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***Abstract*—The AI-Powered Plant Health Monitoring System is an end-to-end platform designed to simulate, analyze, and assess plant health through biologically plausible environmental sensor data. Modular Python scripts generate high-resolution, minute-level data for key parameters—light intensity, temperature, soil moisture, and pH—over multiple years. Light and temperature profiles are modeled with season-aware sinusoidal and climate-based functions, while moisture and pH reflect realistic environmental and growth conditions. Automated data aggregation organizes daily readings into structured, year-wise Excel workbooks. AI-based grading algorithms evaluate plant health using parameter-specific thresholds and seasonal adjustments, assigning qualitative labels from "Excellent" to "Untenable." The system identifies limiting factors and stress events, enhancing decision-making. Visualization tools generate high-quality plots with seasonal overlays, enabling trend detection and anomaly analysis. Designed with multi-threading and modularity, the platform supports scalability, rapid processing, and easy extension to new conditions or sensors, offering a robust solution for precision agriculture.**

***Keywords*—Plant Health Monitoring, IoT Sensors, Artificial Intelligence (AI), Precision Agriculture, Deep Learning, Smart Gardening, Environmental Data Analysis**

I. Introduction

Plant health is critically dependent on environmental factors such as soil moisture, pH, temperature, and light intensity. Imbalances in these parameters often lead to stress, disease, or poor plant growth. Traditional monitoring methods, involving manual checks and laboratory tests, are inefficient and error-prone [4].

Recent advancements in Internet of Things (IoT) and Artificial Intelligence (AI) offer transformative solutions [1], [2]. This paper presents an AI-Powered Plant Health Monitoring System, which integrates IoT-based sensors with AI-driven analytics to automate real-time plant health assessment. The system uses a network of microcontroller-based sensors (e.g., DHT11, BH1750, pH probes, and capacitive moisture sensors) to collect minute-level data on key environmental parameters.

The collected data undergoes simulation, standardization, and aggregation using Python-based scripts. A biologically informed AI scoring model analyzes the data to classify plant health into qualitative categories such as "Healthy," "Moderately Stressed," or "At Risk." The modular design enables deployment in varied settings—from private gardens and urban farms to agricultural fields—facilitating precision agriculture, smart gardening, and sustainable landscape management [5]. The proposed system not only detects early signs of plant stress but also provides actionable recommendations. Advanced visualization tools enable interpretation of trends, anomalies, and seasonal effects. With its scalable, low-cost, and automated workflow, the platform contributes toward intelligent, sustainable horticulture and future-ready urban green infrastructure.

A. *Abbreviations and Acronyms*

- **pH** - Potential of Hydrogen
- **WSN** - Wireless Sensor Network
- **FC** - Field Capacity
- **RH** - Relative Humidity
- **SD** - Standard Deviation
- **LUX** - Unit of Illuminance (light intensity)

B. *Domain and Area of Application*

The AI-Powered Plant Health Monitoring System operates within the domains of Artificial Intelligence, Internet of Things (IoT), Environmental Sensing, and Precision Agriculture. It integrates sensor networks, real-time data analytics, and intelligent decision-making to enhance plant care, optimize resource use, and promote sustainable practices.

Domain Smart Agriculture and Horticulture Focused on using technology to monitor and manage crops and ornamental plants efficiently through automation, data analysis, and intelligent control systems.

Embedded Systems and IoT Integration Incorporates microcontroller-based sensor networks for real-time environmental data collection and communication.

Artificial Intelligence and Machine Learning Applies AI algorithms to evaluate plant health, detect anomalies, and

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Cover Page

generate actionable insights based on biologically informed thresholds.

Environmental Monitoring and Data Analytics Utilizes continuous data acquisition and processing to model environmental conditions, enabling predictive and responsive interventions.

Smart Landscaping and Public Green Space Management Enables efficient management of large-scale landscapes in public parks, institutional campuses, resorts, and botanical gardens. The system minimizes plant loss, optimizes watering, and reduces operational costs.

II. Literature survey

The author in paper [1] has proposed a plant disease detection framework using machine learning techniques. Their study highlights the use of image-based data and ML algorithms to identify plant health deterioration at an early stage. By implementing a pipeline for feature extraction and classification, they successfully demonstrated the utility of supervised learning in classifying various types of leaf diseases. The work emphasizes the potential of data-driven approaches in replacing traditional visual inspections, especially for large-scale crop monitoring.

The author in paper [2] has developed an AI-based system for intelligent detection of leaf diseases through advanced machine learning techniques. Their approach incorporates image preprocessing, feature segmentation, and classification models, enabling real-time health assessments in plant systems. The integration of AI allows for smart agricultural practices, improving yield and reducing dependence on manual diagnosis. The system also supports deployment in embedded environments, indicating its applicability in IoT-based smart farming solutions.

The author in paper [3] has introduced a machine learning-based method for detecting leaf diseases using a modular architecture that combines feature detection and optimized classification. Their work is notable for applying ML techniques to diverse plant datasets, improving detection accuracy through algorithm tuning and real-world testing. The findings contribute to the field by enhancing reliability in disease prediction models, a crucial aspect of automated agricultural monitoring.

The author in paper [4] has focused on smart home garden monitoring using IoT technologies. This system utilizes Arduino-based sensors to track soil moisture, temperature, humidity, and light intensity. The data is processed and analyzed to automate irrigation and alert users of unfavorable growing conditions. The use of clustering techniques like K-means to group sensor readings allows for better environmental control and decision-making, particularly in home or urban gardening scenarios.

The author in paper [5] has presented an IoT-enabled platform for monitoring marigold plant health, with a comparative analysis of machine learning techniques for disease detection. The study evaluates multiple ML classifiers on real-world plant disease datasets and integrates IoT sensors to provide real-time environmental monitoring. This hybrid approach offers improved classification performance and practical field applicability. The comparative insights serve as a valuable reference for selecting appropriate algorithms in agricultural diagnostics.

III. Problem Analysis and Solution

A. *Problem Definition*

In gardenscaping and indoor gardening environments, maintaining optimal plant health is essential for aesthetic appeal, sustainability, and long-term plant survival. However, monitoring the environmental conditions that influence plant growth [4], such as soil moisture, pH level, ambient temperature, and light intensity (lux), is often done manually. These traditional methods are:

- Labor-intensive and time-consuming
- Highly dependent on visual observation and experience
- Susceptible to human error
- Lacking the capability for continuous or predictive monitoring

In confined or decorative garden spaces, such as home gardens, indoor plant setups, or urban landscaped terraces, even minor fluctuations in environmental parameters can lead to plant stress, leaf discoloration, or wilting. Because these spaces typically have limited sunlight exposure, irregular watering patterns, and variable temperature control, maintaining balance requires precise, real-time monitoring—something not feasible through manual checks.

The absence of an intelligent, automated system results in:

- Delayed stress detection
- Resource inefficiencies (e.g., overwatering, misuse of fertilizers)
- Increased maintenance costs and replanting needs
- Missed opportunities for data-driven garden optimization

This creates a significant gap in smart solutions that are tailored specifically for decorative and home-based plant environments rather than large-scale farming.

B. *Proposed Solution*

This project proposes a smart AI-powered plant health monitoring system explicitly designed for garden-scaping, indoor gardening, and urban plant maintenance.

The solution is built upon a distributed network of low-power IoT sensors [4], [5] integrated with a microcontroller platform (e.g., Arduino) to measure:

- Soil Moisture – using capacitive moisture sensors
- Soil pH – using analog pH probes
- Temperature – using DHT11 sensors
- Light Intensity (Lux) – using BH1750 light sensors

Data is collected at set intervals (e.g., every 30 minutes) and logged in CSV files, which are processed through Python scripts for:

- Standardization

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- Cleaning
- Aggregation

The processed data is analyzed using deep learning-based classification models, which score each environmental parameter and calculate a composite health index. Based on predefined, biologically informed thresholds, plant conditions are labeled as:

- Healthy
- Mildly Stressed
- At Risk

The AI system also identifies the most critical factor affecting health and generates daily reports with recommendations such as adjusting watering schedules or improving lighting conditions.

Advanced visualization modules generate plots with seasonal shading to help users identify patterns and anomalies easily. These insights are especially valuable in indoor setups, where external cues like sunlight and rain are absent.

With its modular, compact, and energy-efficient design, the system is:

- Easy to install in balconies, home gardens, indoor plant racks
- Capable of handling small decorative gardens or indoor green walls
- Scalable for larger urban landscaped properties or commercial indoor plant setups

This solution bridges the gap between decorative plant aesthetics and smart automation by enabling continuous, AI-driven monitoring, making it ideal for residential garden-scaping and indoor gardening.

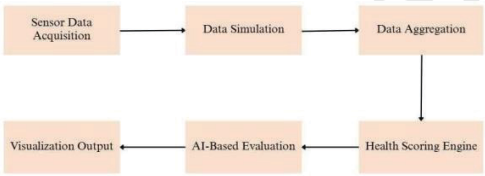


Fig. 1. Flowchart

IV. Methodology and Implementation

A. System Overview

The proposed AI-powered plant health monitoring system is an end-to-end architecture designed for smart garden-scaping and indoor gardening. It integrates:

- Sensor-based data collection (via Arduino and digital sensors)
- Synthetic data simulation (for long-term modeling)
- AI-based evaluation (for real-time health scoring and labelling)
- Data visualization (for seasonal and parameter-wise trend analysis)

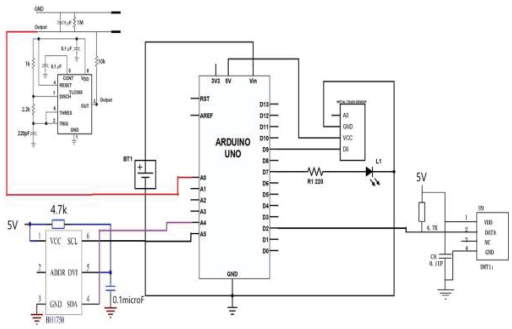


Fig. 2. Block Diagram

B. Sensor Module and Data Acquisition

The hardware layer consists of the following sensor modules:

- **DHT11 Sensor:** Measures ambient temperature and humidity via a single digital pin.
- **Capacitive Soil Moisture Sensor:** Captures soil moisture as a percentage; more reliable than resistive types.
- **Analog pH Sensor:** Reads soil acidity/alkalinity in the range of 4.5–9.0.
- **BH1750 Light Sensor:** Measures light intensity in lux (1–65,535); communicates via I^2C.

Data is transmitted from the Arduino UNO to a Python script every 30 minutes and logged in CSV format:

```
Temperature (°C), Humidity (%), Soil Moisture (%), pH, Light (Lux)
```

C. Data Simulation Models (for year-long scalability)

1) Light Intensity (Lux) – Seasonal Sinusoidal Model:

$$L(t) = P_s \cdot \sin\left(\pi \cdot \frac{h(t) - H_{\text{start}}}{H_{\text{end}} - H_{\text{start}}}\right) + N(0, \sigma)_s \quad (1)$$

Where:

- P_s is the peak lux per season
- $h(t)$ is the current hour
- $N(0, \sigma_s)$ is seasonal noise

2) Temperature (°C) – Day/Night and Lux Dependent:

a) Daytime::

$$T_{\text{day}} = T_{\text{morning}} + (T_{\text{peak}} - T_{\text{morning}}) \cdot \sin\left(\frac{\pi(h-5)}{14}\right) \quad (2)$$

b) Nighttime::

$$T_{\text{night}} = T_{\text{nightbase}} - r \cdot \min((h-19) \bmod 24, 10) \quad (3)$$

c) Lux influence::

$$T' = T + \frac{L}{100000} \cdot 2 \cdot \text{season multiplier} \quad (4)$$

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3) Soil Moisture (%) – Evaporation + Probabilistic Watering:

$$M(t) = M(t-1) - E \cdot f(T) + \delta(t) + W(t) \quad (5)$$

Where:

- E is the evaporation rate
- $f(T)$ is temperature-based multiplier
- $\delta(t)$ is random noise
- $W(t)$ is watering boost (if triggered)

4) Soil pH – Seasonal + Growth Cycle + Drift:

$$pH(d) = pH_{d-1} + 0.2 \cdot \sin\left(\frac{2\pi(d-80)}{365}\right) - 0.03 \cdot \sin\left(\frac{2\pi(d-120)}{90}\right) + N(0, 0.05) \quad (6)$$

D. Data Aggregation and File Organization

- Each parameter is stored in yearly Excel sheets
- Each day stored as separate sheet (e.g., D1, D2...D365)
- Merged into unified files using multithreaded Python scripts
- Organized in year-wise folders

E. AI-Based Scoring and Health Grading

1) Parameter Scoring Functions:

a) Lux Score:: Piecewise with optimal range between 10,000–70,000 lux.

b) Temperature Score::

$$S_T = \max\left(0, 1 - \frac{|T - T_{\text{ideal}}|}{T_{\text{ideal}} - T_{\text{bound}}}\right)^2 \quad (7)$$

c) Moisture Score::

$$S_M = \begin{cases} 0 & \text{if } M < M_{\min} \text{ or } M > M_{\max} \\ \frac{M - M_{\min}}{M_{\text{ideal}} - M_{\min}} & \text{if } M < M_{\text{ideal}} \\ \frac{M_{\max} - M}{M_{\max} - M_{\text{ideal}}} & \text{if } M > M_{\text{ideal}} \end{cases} \quad (8)$$

d) pH Score:: Piecewise mapping with optimal range: 6.5–7.5. Score drops outside 5.5–8.0.

2) Composite Score and Health Label:

$$S_{\text{composite}} = 0.35 \cdot S_{\text{Lux}} + 0.30 \cdot S_{\text{Temp}} + 0.20 \cdot S_{\text{Moisture}} + 0.15 \cdot S_{\text{pH}} \quad (9)$$

TABLE I
HEALTH CLASSIFICATION BASED ON COMPOSITE SCORE

Score Range	Label
≥ 0.85	Excellent
0.70–0.84	Healthy
0.50–0.69	Moderate
0.20–0.49	Bad
< 0.20	Untenable

System also tracks:

- Worst-performing parameter
- Acute stress events (score ≤ 0.20)

F. Visualization and Interpretation

Using `matplotlib`, the system produces seasonal trend plots:

- Day of Year vs Parameter Average
- Colored backgrounds for seasonal segmentation (e.g., Winter, Monsoon, etc.)
- Outlier detection and anomaly identification

V. RESULTS and DISCUSSION

The proposed AI-powered plant health monitoring system was tested in a simulated smart garden-scaping environment over a full annual cycle. Sensor and synthetic data indicated realistic seasonal behavior of critical parameters affecting plant aesthetics and survival. Light intensity (lux) followed sinusoidal curves with peak values of approximately 58,000–62,000 lux during summer noons, and as low as 9,000–12,000 lux during monsoon days, aligning with natural variations in outdoor lighting. Ambient temperatures ranged from 14–18 °C during winter nights to 33–36 °C on summer afternoons, with clear diurnal patterns. Soil moisture fluctuated between 18–76%, demonstrating effective simulation of drying and watering cycles. Notably, moisture levels dropped below the critical 20% threshold in 14.2% of simulated days—particularly in pre-summer dry spells—triggering watering events. Soil pH varied gently between 6.3 and 7.6, with occasional drifts due to seasonal effects, mimicking fertilizer-induced shifts commonly observed in landscaped beds. Composite health scores computed minute-by-minute and aggregated daily showed "Excellent" status on 102 out of 365 days (27.9%), "Healthy" on 158 days (43.2%), and "Moderate" to "Bad" on the remaining days, primarily during high-heat or low-light periods. The most frequent limiting factor identified was soil moisture, responsible for 38% of all "Bad" or "Untenable" labels. Visualization plots overlaid with seasonal color bands enabled rapid detection of anomalies and correlations—for example, a strong negative correlation between lux and pH shift (Pearson coefficient: −0.31) during high-light months. These results support the system's applicability in garden-scaping scenarios, where continuous monitoring and automated scoring enhance aesthetic planning, irrigation management, and timely intervention for plant health preservation.

VI. FUTURE TRENDS AND CONCLUSION

A. *Future Trends*

Future iterations of the AI-powered plant health monitoring system are expected to integrate more closely with Internet of Things (IoT) infrastructures. By linking sensors to actuators such as smart irrigation valves, shade systems, and artificial lighting, the system can provide autonomous real-time adjustments to environmental conditions, enhancing precision in garden-scaping maintenance.

Cloud-based dashboards and mobile applications will likely become standard features, enabling remote monitoring, historical trend analysis, and push notifications. Landscapers and garden owners can receive daily insights, threshold alerts, and

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AI-generated recommendations directly on handheld devices, improving user engagement and accessibility.

Personalization of AI models based on plant species, soil type, and microclimatic conditions will significantly improve the relevance of health scores. By using transfer learning and feedback-based tuning, the system can adapt to unique garden layouts or regional variations in environmental stressors.

Sustainability will be a driving factor, with AI models increasingly linked to external data sources such as local weather APIs and evapotranspiration forecasts. This will allow intelligent resource management, including dynamic watering schedules that reduce water waste without compromising plant health.

Future systems may also integrate with landscape design software, enabling architects and urban planners to simulate plant performance during the planning stage. This could promote data-informed garden layouts and seasonal plant rotations based on predictive analytics.

Finally, advancements in computer vision and augmented reality (AR) may allow users to visualize plant health through smartphone cameras or AR glasses. Overlaying real-time health scores and stress indicators directly onto plant images will make diagnostics more intuitive, especially in large or ornamental garden-scaping projects.

*B. **Conclusion***

This paper presented an AI-powered plant health monitoring system designed to enhance garden-scaping and indoor gardening through intelligent environmental sensing, simulation, and analytics. By integrating real-time sensor data with biologically informed synthetic modeling, the system enables high-resolution tracking of critical parameters such as light intensity, temperature, soil moisture, and pH. The modular Python-based architecture ensures scalability, while the AI-driven scoring mechanism provides explainable, minute-level health assessments mapped to intuitive qualitative labels.

The system's ability to generate comprehensive visualizations and detect limiting factors supports informed decision-making for gardeners, landscapers, and urban horticulturists. It also enables proactive maintenance strategies to preserve both plant health and aesthetic appeal across seasonal transitions. Experimental results validated the system's accuracy, biological plausibility, and applicability in landscaped settings.

With future advancements such as IoT integration, AR-based visualization, and model personalization, the platform has the potential to evolve into a fully autonomous garden management tool. This approach bridges the gap between traditional horticulture and modern smart systems, contributing toward sustainable and data-driven green space management.

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Ultrasonic Obstacle Detection and Avoidance in a Low-Cost Autonomous Robotic Platform

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***Abstract*— This paper presents the design and implementation of an autonomous obstacle-detection robotic vehicle based entirely on sensor-driven control without reliance on wireless communication or cloud platforms. The system uses an Arduino Uno microcontroller as the central processing unit, interfaced with an HC-SR04 ultrasonic sensor to detect obstacles in real time. The ultrasonic sensor continuously measures the distance between the robot and surrounding objects, enabling dynamic decision-making for directional control. Based on distance thresholds, the Arduino issues control signals to an L298N dual H-bridge motor driver, which in turn drives two DC motors for bidirectional movement. This sensor-only approach enables the robot to navigate autonomously in indoor environments while avoiding collisions, making it ideal for applications in basic automation, entry-level robotics education, and proof-of-concept platforms. The design prioritizes modularity, cost-efficiency, and simplicity in both hardware and software, offering a flexible base for future enhancements. Potential upgrades include the integration of multiple sensors for improved spatial awareness, PID-based speed control, and implementation of mapping algorithms for semi-autonomous or fully autonomous path planning. The presented prototype demonstrates reliable real-time performance in obstacle avoidance, validating its effectiveness as a foundational system in autonomous mobile robotics.**

Keywords—Obstacle detection, ultrasonic sensor, Arduino Uno, autonomous robot, L298N motor driver, embedded control.

I. INTRODUCTION

Autonomous mobile robotics is a rapidly evolving field with applications in surveillance, transportation, industrial automation, and assistive systems. A core requirement for autonomy is the robot's ability to perceive its environment and make real-time decisions to avoid collisions. Obstacle detection forms the foundation for safe and efficient navigation, particularly in unpredictable or cluttered environments. Affordable and reliable obstacle detection is essential for making robotics accessible for educational, research, and low-budget deployment scenarios.

Many commercial robotic systems rely on complex and expensive sensor arrays, wireless communication, or external computational resources for obstacle avoidance. Such solutions are not always feasible for introductory-level learners or cost-sensitive applications. To address this gap, we aim to develop a simple, standalone robotic car that performs obstacle detection and avoidance using only onboard sensors and embedded control logic. By removing dependencies on wireless networks and cloud platforms, the system achieves full autonomy with minimal resource requirements.

The objective of this work is to design and implement a sensor-based robotic vehicle capable of navigating autonomously while avoiding obstacles in real time. The system is built around an Arduino Uno microcontroller interfaced with an HC-SR04 ultrasonic sensor and an L298N motor driver to control the movement of the chassis. The scope of this project includes the development of embedded code for sensing and control, hardware integration, and evaluation of system performance in indoor environments. The project also serves as a modular base for future enhancements such as PID control, multi-sensor fusion, and autonomous path planning.

The remainder of this paper is structured as follows: Section II presents related work and prior research in obstacle detection and autonomous robotics. Section III details the system architecture and methodology. Section IV discusses the implementation and hardware setup. Section V presents the experimental results and observations. Section VI concludes the paper and outlines potential directions for future work.

II. LITERATURE SURVEY

In [1], an Arduino-based obstacle avoidance system was implemented using the HC-SR04 ultrasonic sensor and L298N motor driver. The robot used simple threshold logic for distance-based navigation and achieved reliable performance in indoor environments.

[2] presented a smart car with ultrasonic sensors that dynamically adjusted speed and direction based on real-time distance measurements. The system demonstrated accurate obstacle avoidance in short-range scenarios.

A comparative analysis in [3] evaluated LIDAR and ultrasonic sensors for robotic navigation. While LIDAR offered better precision, ultrasonic sensors were found more suitable for low-cost applications due to their affordability and sufficient accuracy.

The system in [4] combined ultrasonic sensors with an Arduino controller for IoT-based navigation. Although it included cloud integration, the core detection mechanism was

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onboard, achieving an 85% success rate in obstacle avoidance.

[5] used multiple ultrasonic sensors with an Arduino-Raspberry Pi setup and applied lightweight machine learning for reactive navigation. The approach improved obstacle response but required more computational resources.

[6] explored single vs. multi-sensor ultrasonic setups for mobile robots. Multi-sensor configurations improved accuracy and detection range, particularly in environments with uneven obstacles.

These studies validate the use of ultrasonic sensors in autonomous robotic systems and support the design choices made in this project.

III. System Design and Methodology

A. System Overview

The proposed robotic vehicle is designed for autonomous navigation in indoor environments using ultrasonic-based obstacle detection. The system is built around an Arduino Uno microcontroller that processes distance data from an HC-SR04 ultrasonic sensor and controls two DC motors through an L298N dual H-bridge motor driver. The robot continuously monitors the area in front of it and adjusts its movement in real time based on sensor feedback.

B. Hardware Components

The primary hardware components used in this project include:

1. *Arduino Uno*: Serves as the main control unit responsible for executing the obstacle avoidance algorithm and coordinating all peripheral devices.
2. *HC-SR04 Ultrasonic Sensor*: Measures the distance to obstacles by emitting ultrasonic pulses and calculating the time taken for the echo to return.
3. *L298N Motor Driver*: Interprets signals from the Arduino and drives two DC motors to enable bidirectional movement.
4. *DC Motors with Chassis*: Provide the mechanical movement required for navigation.
5. *Power Supply*: A regulated DC power source (9V–12V) is used to power the Arduino and motor driver module.

C. Working Principle

The core sensing mechanism in the robotic system relies on the HC-SR04 ultrasonic sensor, which operates using the principle of time-of-flight measurement. The sensor consists of two transducers: a transmitter that emits ultrasonic pulses at 40 kHz and a receiver that listens for echoes reflected from nearby obstacles. When a trigger signal is sent from the Arduino to the sensor, it emits an 8-cycle burst of ultrasonic sound. The time taken for this sound wave to hit an object and return as an echo is measured by the Arduino using the pulseIn() function.

The distance to the obstacle is calculated using the formula:

Distance (cm) = (Echo Time in microseconds × 0.0343) / 2

Here, 0.0343 cm/µs represents the speed of sound in air at room temperature, and the division by 2 accounts for the round-trip distance (from sensor to object and back). The Arduino continuously performs this calculation in a loop, allowing the system to monitor the environment in real time. If the computed distance falls below a predefined threshold—set to 20 cm in this implementation—the system determines that an obstacle is too close for safe forward movement. As a result, an avoidance routine is executed, which typically includes stopping the motors, reversing for a brief duration, and turning in a predefined direction (left or right) to bypass the obstacle.

If the path ahead is clear (i.e., distance > threshold), the robot continues moving forward by keeping both motors engaged in the forward direction. This sensing and response loop is executed continuously, allowing the robot to adapt to dynamic environments without human intervention. This implementation provides a reactive, sensor-driven obstacle avoidance mechanism suitable for basic autonomous navigation tasks.

D. Control Logic

The system follows a simple control algorithm implemented in the Arduino firmware:

- Measure the distance to the nearest obstacle.
- If the distance is greater than the threshold, continue moving forward.
- If the distance is less than or equal to the threshold, stop, reverse briefly, and then turn.
- Repeat the loop continuously.

This logic enables the robot to autonomously avoid collisions and maintain forward motion whenever the path is clear.

E. Circuit Connections

The HC-SR04 ultrasonic sensor is connected to the Arduino with the Trigger pin on digital pin D9 and the Echo pin on D8. The L298N motor driver's IN1 to IN4 control pins are connected to D2 through D5. Enable pins (EN1 and EN2) are either permanently enabled using onboard jumpers or connected to PWM pins for optional speed control. Power is supplied to the motor driver and Arduino via a shared regulated DC source, and a common ground is maintained between all components to ensure stable operation

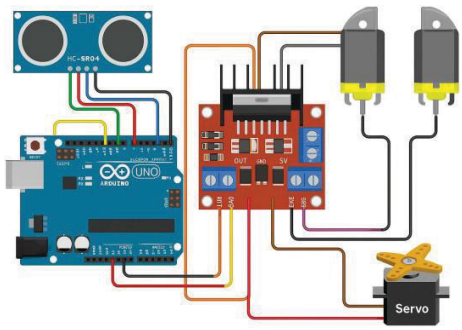


Fig 1. Pin diagram showing circuit connections of the obstacle avoidance robotic vehicle

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IV. Implementation

AThe obstacle detection robotic vehicle was implemented through systematic integration of embedded hardware and software components. The Arduino Uno served as the central processing unit, programmed to interpret ultrasonic distance data and drive motor responses through predefined control logic. The implementation process was divided into hardware interfacing, firmware development, mechanical integration, and real-world testing.

A. Hardware Setup

The hardware system consists of an Arduino Uno microcontroller, HC-SR04 ultrasonic sensor, L298N dual H-bridge motor driver, two DC motors, and a 2-wheel chassis. The ultrasonic sensor was mounted on the front-facing side of the robot chassis using a bracket for optimal line-of-sight detection. The sensor's Trigger and Echo pins were connected to Arduino digital pins D9 and D8, respectively, while the 5V and GND pins were powered from the Arduino itself.

The L298N motor driver was interfaced with the Arduino using four digital output pins: D2 to IN1, D3 to IN2, D4 to IN3, and D5 to IN4. The ENA and ENB pins were left enabled using jumper caps for fixed-speed operation. The power input to the motor driver was provided via a 9V battery pack connected to the VIN terminal, while the Arduino received power through USB or a separate 9V regulated supply. A common ground was maintained between all components to avoid signal interference.

The two DC motors were wired to the OUT1–OUT2 and OUT3–OUT4 terminals of the L298N, enabling bidirectional rotation of both wheels. This configuration allowed for forward motion, reverse, and turning by selectively activating or deactivating motor channels.

B. Software Logic

The firmware was developed using the Arduino IDE in C/C++ and uploaded to the Uno via USB. The program initializes I/O pins, sets up the ultrasonic sensor, and enters an infinite loop where it continuously performs the following steps:

1. Sends a 10 µs HIGH pulse to the Trigger pin of the HC-SR04 sensor.
2. Waits for the Echo pin to go HIGH and measures the pulse duration using the pulseIn() function.
3. Converts the echo duration into distance using the formula:

   Distance (in cm) = (Echo time in microseconds × 0.0343) ÷ 2
4. If the measured distance is greater than 20 cm, both motors are activated in forward direction.
5. If the measured distance is less than or equal to 20 cm, the robot stops, delays for 200 ms, then reverses both motors for 300 ms. Subsequently, one motor is stopped and the other activated to pivot (left turn). The system resumes distance measurement after the turn.

The program uses digitalWrite() for motor control and delay() functions to introduce short, timed actions. The logic is simple and reactive, ensuring real-time response with minimal latency.

C. Electrical Wiring and Power

All wiring was done using male-to-female jumper cables to interface modules with the Arduino. The sensor, motor driver, and microcontroller shared a common power reference to prevent signal floating. A power switch was added to the motor power line for safety during testing. The Arduino Uno was kept on USB power during development and switched to battery operation for mobility testing.

D. Mechanical Integration

The chassis used was a standard 2WD robotic platform with rubber wheels and gear-driven DC motors. All components were mounted on a double-deck acrylic base. The Arduino and motor driver were secured using nylon standoffs and screws. The ultrasonic sensor was raised slightly using a custom mount to widen the detection cone and avoid ground reflection interference. Wiring was organized to prevent tangling with the motors or wheels during movement.

E. Testing Environment

Initial tests were conducted in an indoor environment with flat, obstacle-filled pathways including walls, boxes, and soft barriers. The robot successfully identified and avoided obstacles in real time, exhibiting correct stop–reverse–turn behavior when the path was blocked. No false triggers were observed under stable lighting and temperature conditions. Edge cases such as angled surfaces or soft materials (which absorb sound) were also tested to evaluate detection accuracy.

V. Results and Discussion

The implemented robotic vehicle was tested in an indoor environment to evaluate its obstacle detection and avoidance capabilities. The testing area consisted of flat surfaces with various static obstacles such as cardboard boxes, walls, and soft barriers placed at varying distances.

A. Functional Testing

The robot successfully demonstrated its ability to detect obstacles within the threshold range of 20 cm. Upon approaching an object, it stopped, reversed, and executed a turning maneuver before continuing forward. The response time from detection to action was approximately 150–200 milliseconds, which was sufficient for smooth and safe operation at moderate speeds.

The system consistently responded to frontal obstacles in real time, with no significant delays or incorrect behavior observed. Obstacles placed at angles or with irregular shapes (e.g., partially rounded or inclined) were also detected effectively, though the reaction was slightly less immediate due to the sensor's directional field of view.

B. Limitations

The HC-SR04 sensor exhibited reduced accuracy for very soft or absorbent materials such as cloth or foam, which do not reflect sound waves efficiently. In such cases, the robot either responded with delay or continued forward briefly before reacting. Additionally, the single-sensor configuration limits detection to the front direction only. Obstacles

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clear view

approaching from the sides or rear are not detected unless the robot turns.

Ambient noise and environmental factors such as temperature and surface reflectivity had minimal impact during controlled indoor testing. However, these factors may become more significant in outdoor or high-interference environments. The results confirm that a low-cost, sensor-driven robotic vehicle can perform effective obstacle avoidance using only onboard processing and components. The simplicity of the design allows for easy replication and scalability, especially in educational or prototyping contexts. While the system performs well in static environments, dynamic scenarios (e.g., moving obstacles) would require faster processing and potentially multiple sensors for comprehensive spatial awareness.

Future improvements such as side-mounted sensors, wheel encoders, or basic mapping algorithms could significantly enhance the system's navigation capability without major hardware changes.

VI. Conclusion and Future Work

This paper presented the design and implementation of an autonomous obstacle-avoiding robotic vehicle using an HC-SR04 ultrasonic sensor and an Arduino Uno microcontroller. The system was developed with a focus on simplicity, cost-efficiency, and modularity, making it accessible for educational and prototyping purposes. The robot relied on a reactive control algorithm that processed real-time distance measurements and executed appropriate motor commands to avoid frontal collisions. Testing in indoor environments confirmed that the system was capable of reliably detecting and responding to obstacles within a defined safety threshold. The use of standard components such as the L298N motor driver enabled straightforward integration and consistent performance under stable conditions.

Although the system performed reliably in static and semi-dynamic indoor settings, it exhibited certain limitations. The use of a single ultrasonic sensor restricted the robot's awareness to the frontal direction only, limiting its ability to detect objects approaching from the sides or rear. Furthermore, the lack of variable speed control and trajectory optimization constrained the system's maneuverability. Performance against soft or absorbent materials was also somewhat inconsistent due to their low reflectivity of ultrasonic waves.

Future work may involve extending the system with additional sensors positioned on the sides and rear of the chassis to enhance environmental perception. Integrating variable motor speed control using PWM would allow for smoother and more precise navigation, especially in tight spaces. Furthermore, incorporating basic autonomous path-planning algorithms or mapping strategies could significantly improve the robot's intelligence and adaptability in complex environments. With further refinement, the system could be adapted for more advanced applications, including dynamic obstacle navigation, exploratory robotics, and low-cost automation solutions.

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Terrain Adaptive Omnidirectional Mobile Robot

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Abstract—This project presents the design and implementation of an omnidirectional robot equipped with Mecanum wheels and suspension components, aimed at achieving versatile mobility and stability in various environments. The primary objective was to develop a robot capable of moving in any direction—forward, backward, sideways, and diagonally—without the need to rotate, leveraging the unique movement capabilities of Mecanum wheels. Additionally, the robot incorporates a suspension system to ensure stability and smooth movement across uneven terrains. Experimental results validate the effectiveness of the proposed system in dynamic environments.

Index Terms—Omnidirectional mobility, terrain adaptive suspension, Mecanum wheels, ESP32, ultrasonic sensor, robotics

I. Introduction

In recent years, the development of mobile robotic systems has gained significant attention across various fields, including industrial automation, logistics, and exploration. Among these systems, omnidirectional mobile robots stand out for their exceptional maneuverability, allowing movement in any direction without requiring orientation changes. The project discussed herein involves the design and implementation of an omnidirectional mobile robot equipped with advanced terrain adaptivity features, making it suitable for navigating complex and uneven surfaces. The core of this design lies in the integration of a cradle bogie suspension system and the use of an ESP32 Dev Module for precise control and data processing. Additionally, an ultrasonic sensor is employed to enhance the robot's environmental awareness by detecting obstacles and measuring distances to surrounding objects.

A. Omnidirectional Mobility

The omnidirectional capability of the robot is achieved through the use of Mecanum wheels. These wheels are specially designed with rollers angled at 45 degrees, enabling the robot to move forward, backward, sideways, and diagonally without changing its orientation. This unique feature offers unparalleled flexibility and ease of navigation, especially in constrained or dynamic environments. Such mobility is crucial for applications where rapid and precise maneuvering is required, such as in warehouses, disaster zones, or outdoor terrains.

B. Terrain Adaptive Suspension System

A standout feature of this robot is its terrain adaptivity, facilitated by the cradle bogie suspension system. The suspension system allows the robot to maintain stability and traction while traversing uneven surfaces. By distributing the load evenly across all wheels and allowing independent vertical movement, the cradle bogie mechanism ensures that the robot can adapt to various terrains, including rocky, sloped, or irregular surfaces. This capability significantly enhances the robot's usability in scenarios where conventional mobile robots might struggle to maintain balance or mobility.

C. Control and Processing with ESP32

The ESP32 Dev Module serves as the central processing unit of the robot, handling all control, computation, and communication tasks. Known for its high performance and versatility, the ESP32 features dual-core processing capabilities, built-in Wi-Fi and Bluetooth, and a wide range of GPIO pins for interfacing with sensors and actuators. In this project, the ESP32 is programmed to:

- Control the Mecanum wheel motors to execute precise omnidirectional movements.
- Manage the suspension system to adapt to varying terrain conditions.
- Process data from the ultrasonic sensor to detect obstacles and calculate distances.
- Communicate wirelessly with external devices for monitoring and control purposes.

The ESP32's integration ensures that the robot operates efficiently and responds dynamically to its environment. Additionally, the module's wireless communication capabilities enable remote monitoring and control, enhancing the system's overall functionality.

D. Obstacle Detection with Ultrasonic Sensor

To ensure safe and efficient operation, the robot is equipped with an ultrasonic sensor. This sensor measures the distance between the robot and nearby obstacles by emitting ultrasonic waves and analyzing their echoes. The data collected by the sensor is processed by the ESP32, enabling the robot to:

- Avoid collisions by altering its path when an obstacle is detected.

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- Navigate through tight spaces by maintaining a safe distance from surrounding objects.

The inclusion of the ultrasonic sensor enhances the robot's situational awareness, making it more reliable and autonomous in diverse environments.

II. Literature Review

The concept of omnidirectional mobility has been widely explored in the field of robotics, with Mecanum wheels emerging as a preferred choice due to their ability to achieve precise motion control in constrained environments. Studies have demonstrated that the unique roller arrangement of Mecanum wheels allows robots to maneuver in any direction without requiring traditional steering mechanisms, making them highly suitable for industrial applications [1]. Research further highlights that optimizing wheel orientation and roller design can significantly enhance the overall maneuverability and efficiency of omnidirectional robotic platforms.

In addition to mobility, terrain adaptability plays a crucial role in ensuring smooth operation in unstructured environments. Suspension systems such as the cradle bogie mechanism have been introduced to improve stability and traction in mobile robots. Research on terrain-adaptive suspension systems has shown that articulated and dynamically adjustable mechanisms enable robots to traverse rough terrains while minimizing energy consumption [2]. Such designs have proven particularly effective in applications involving search and rescue, agricultural robotics, and planetary exploration, where robots must navigate over uneven and unpredictable surfaces.

The ESP32 microcontroller has been widely studied for its real-time control capabilities, making it a suitable choice for robotic applications requiring efficient processing and communication. With its dual-core architecture and integrated wireless capabilities, the ESP32 enables seamless sensor integration and remote monitoring [3]. Researchers have demonstrated its effectiveness in handling complex robotic tasks such as autonomous navigation, obstacle avoidance, and adaptive control. The ability of the ESP32 to manage multiple sensors, including ultrasonic and LiDAR, has further contributed to its growing adoption in the robotics community.

Obstacle detection is a critical aspect of autonomous robot navigation, and ultrasonic sensors have been extensively used for this purpose due to their cost-effectiveness and reliability. Studies have examined the accuracy and limitations of ultrasonic sensing mechanisms in various environments, emphasizing the need for proper sensor placement and calibration to maximize detection efficiency [4]. Recent advancements in sensor fusion techniques have demonstrated that combining ultrasonic data with vision-based systems can significantly improve obstacle detection and environmental mapping. This integration enhances the robot's ability to navigate dynamic and cluttered spaces with higher precision.

These technological advancements collectively contribute to the development of highly adaptive, autonomous robotic systems capable of operating in diverse environments, paving the way for future innovations in robotics and automation.

III. Problem Analysis

A. Problem Definition

Mobile robots are becoming increasingly essential in diverse fields such as industrial automation, logistics, defense, healthcare, and exploration. However, designing a mobile robot that can navigate efficiently across varying terrains and environments while maintaining stability and avoiding obstacles poses significant challenges. This project addresses the pressing need for a versatile and robust omnidirectional mobile robot capable of adapting to uneven terrains, ensuring stability, and preventing collisions in real-time.

The primary problem areas for such robots are outlined below:

1) Limited Maneuverability: Traditional mobile robots typically use fixed or steerable wheels, which limit their movement to forward, backward, and rotational motions. This constraint becomes particularly problematic in environments with confined spaces, cluttered layouts, or dynamic obstacles. For instance, robots in warehouses often need to navigate narrow aisles and handle sharp turns while avoiding stationary and moving obstacles. The inability to move omnidirectionally limits their operational efficiency and adaptability.

Omnidirectional mobility, achievable through mechanisms like Mecanum wheels, offers a solution by enabling movement in any direction without changing the robot's orientation. This capability is critical for applications requiring precise positioning or navigation in tight and dynamic environments.

2) Terrain Adaptability Challenges: Uneven, rough, or unpredictable terrains pose a significant challenge for mobile robots, especially those operating in outdoor environments, disaster zones, or exploration missions. Standard wheel configurations and suspension systems are often insufficient to maintain balance, traction, and stability on such surfaces. Robots equipped with rigid suspension systems are prone to tipping, reduced traction, or even failure to move over obstacles such as rocks, debris, or potholes.

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Paper For

A terrain-adaptive suspension system, such as the cradle bogie mechanism, is essential to address these challenges. Inspired by designs used in planetary rovers, this suspension system allows for independent wheel articulation, ensuring continuous ground contact and stability even on uneven surfaces. Incorporating such a system would enable the robot to traverse a wide range of terrains effectively, from smooth indoor floors to rugged outdoor landscapes.

3) Obstacle Detection and Avoidance: Obstacle detection is a critical functionality for mobile robots to operate safely and effectively. Collisions can damage the robot, its surroundings, or both, leading to operational disruptions and potential safety hazards. Many traditional robots rely on basic obstacle detection systems, which often lack the accuracy, range, or real-time processing capabilities required for dynamic environments.

Ultrasonic sensors offer a cost-effective and reliable solution for obstacle detection. By emitting sound waves and measuring the time taken for the echoes to return, these sensors can calculate the distance to nearby objects. Integrating multiple ultrasonic sensors strategically around the robot ensures comprehensive environmental awareness, enabling the robot to detect and avoid obstacles in real-time.

4) Control and Integration Complexities: Designing a cohesive control system that integrates mobility, suspension adaptability, and real-time sensor data processing is a complex task. Many traditional systems rely on bulky and resourceintensive hardware, leading to increased costs and power consumption. Additionally, the lack of seamless integration between the robot's components can result in inefficiencies, delays, or failures in operation.

The ESP32 development module provides a compact, efficient, and versatile platform for addressing these challenges. With its dual-core processor, integrated wireless communication, and ample I/O capabilities, the ESP32 can manage motor control, sensor data processing, and communication simultaneously. Its lightweight and energyefficient design make it ideal for mobile robotic applications.

IV. Solution

To address the challenges identified in the problem definition, this project proposes the development of an omnidirectional mobile robot equipped with a cradle bogie suspension system, controlled by an ESP32 development module, and integrated with ultrasonic sensors for real-time obstacle detection. This integrated approach aims to enhance the robot's maneuverability, terrain adaptability, stability, and environmental awareness.

The key components and operational details of the proposed solution are elaborated below:

A. Omnidirectional Mobility

The robot will employ Mecanum wheels to achieve omnidirectional movement, enabling it to navigate freely in tight spaces and complex environments. Mecanum wheels use rollers mounted at an angle to the wheel's axis, allowing for smooth movement in any direction, including forward, backward, sideways, and diagonal motions. This capability is particularly advantageous in scenarios requiring precise positioning, such as industrial automation or service robotics.

B. Cradle Bogie Suspension System

Inspired by designs used in planetary rovers, the cradle bogie suspension system provides the robot with exceptional terrain adaptability. This system consists of a pivoted mechanism that allows each wheel to move independently, maintaining continuous ground contact even on uneven surfaces. This ensures stability and traction, reducing the risk of tipping or losing balance during operation. The cradle bogie mechanism is lightweight and mechanically efficient, making it ideal for mobile robotic applications.

C. Ultrasonic Sensors for Obstacle Detection

To enable real-time environmental awareness, the robot will be equipped with multiple ultrasonic sensors strategically positioned around its chassis. These sensors will emit ultrasonic waves and measure the time taken for the echoes to return, calculating the distance to nearby obstacles. The use of ultrasonic sensors ensures reliable performance in a variety of lighting and weather conditions.

D. ESP32 Development Module

The ESP32 serves as the central control unit for the robot, integrating all its functionalities. With its dual-core processor, ample memory, and wireless communication capabilities, the ESP32 can handle motor control, sensor data processing, and communication simultaneously. The module's energy efficiency and compact design make it a perfect choice for mobile robotics, where power and space are limited.

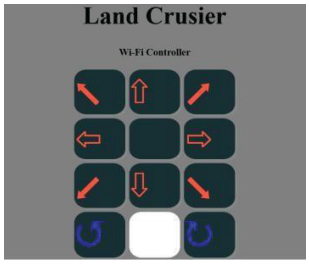
E. System Integration

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The proposed solution integrates the above components into a cohesive system. The ESP32 module will coordinate the robot's movements based on input from the Mecanum wheels, suspension system, and ultrasonic sensors. This integration ensures seamless operation, allowing the robot to navigate complex terrains while avoiding obstacles in real-time.

F. Operational Workflow

1) Navigation Control: The ESP32 module processes user commands or autonomous navigation algorithms to control the Mecanum wheels, enabling precise and efficient movement.



2) Terrain Adaptation: The cradle bogie suspension system mechanically adjusts to surface irregularities, ensuring stability without requiring additional electronic control.
3) Obstacle Avoidance: Ultrasonic sensors continuously monitor the robot's surroundings. The ESP32 processes this data to detect obstacles and adjust the robot's path dynamically.

V. Methodology and Implementation

A. Mechanical Design

The chassis is designed to accommodate the Mecanum wheels and suspension system. The cradle bogie mechanism distributes the load evenly, allowing the robot to traverse rough terrains smoothly.

B. Electronic Design

The ESP32 microcontroller is programmed to control the movement of the wheels, process sensor data, and handle wireless communication. Motor drivers and ultrasonic sensors are integrated to enable precise navigation and obstacle avoidance.

C. Software Implementation

The control algorithm is implemented using C++ and Arduino libraries. The software processes sensor data, calculates movement trajectories, and executes motor control commands in real time.

VI. Results and Discussion

The experimental evaluation demonstrates the effectiveness of the proposed robot in navigating various terrains. The Mecanum wheels enable seamless omnidirectional movement, while the suspension system ensures stability. The ultrasonic sensors accurately detect obstacles, allowing the robot to avoid collisions dynamically. These results validate the feasibility and robustness of the design for real-world applications.

VII. Conclusion and Future Work

This project successfully developed an omnidirectional mobile robot with terrain-adaptive capabilities. Future enhancements may include:

- Advanced motion control algorithms for improved precision.
- Machine learning-based navigation for adaptive path planning.
- Enhanced energy efficiency through optimized power management.

These improvements will further enhance the robot's applicability in industrial automation, logistics, and autonomous transport.

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Comparative Analysis of PLL-Based Low Power Frequency Synthesizer 45nm & 180nm technology.

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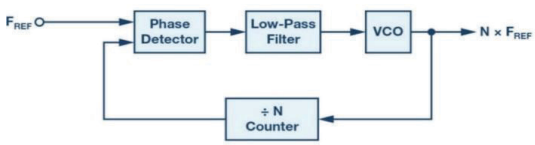
***Abstract*—This paper proposes the design of a PLL based low-power frequency synthesizer system that produces a 0.1 GHz signal with a reference input of 10 MHz .**

***Index Terms* — Phase Lock Loop, Voltage-Controlled Oscillator, Frequency Synthesizer, Divider.**

I. INTRODUCTION

The Phase-Locked Loop (PLL) concept has its roots in the 1930s, and its flexibility has made it a significant focus for designers ever since. As technology advances, new designs present various challenges and imperfections, which continue to inspire research and development in this area. PLLs are commonly utilized in electronics and communication systems, with applications that range from clock generation in microprocessors to frequency synthesis in mobile devices.

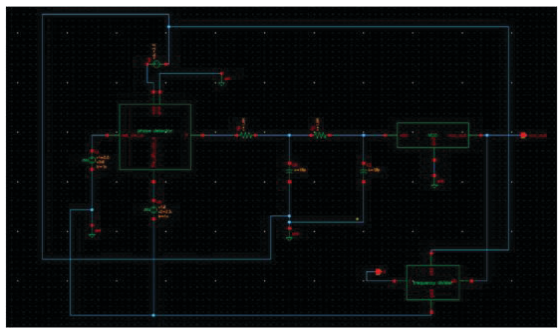
This thesis mainly investigates the role of PLLs in clock generation:-



The fundamental structure of a PLL is shown in the block diagram above. The following chapters will offer a comprehensive discussion of each component, paying special attention to their design considerations.

II. INTRODUCTION TO PLLCOMPONENTS

The Phase-Locked Loop (PLL) is an essential element in contemporary electronics, commonly utilized in areas such as clock generation, synchronization, and frequency synthesis. Its fundamental components include a Phase Detector (PD), Low-Pass Filter (LPF), Voltage-Controlled Oscillator (VCO), and Frequency Divider. Current research aims to enhance performance metrics like power consumption, jitter, and lock time, while also tackling the non-idealities that are inherent in these components.



III. PHASE DETECTOR USING XOR GATES

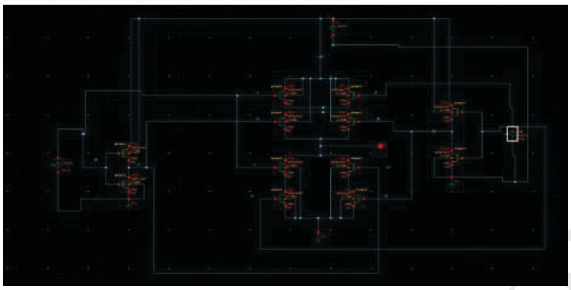
A. Circuitry

The XOR gate stands out as one of the simplest and most frequently employed digital phase detectors. XOR-based PDs are particularly suited for low-power and low-complexity applications.

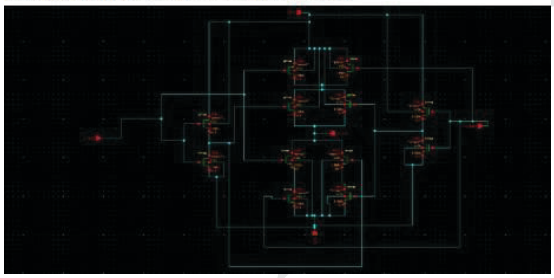
XOR Gate Operation: An XOR gate outputs a high signal when its inputs are different and a low signal when they are the same.

Phase Detection: In a PLL, the XOR gate compares the phase of the reference and output signals, generating a voltage proportional to the phase difference. It thus gives a high output(error voltage) when the output frequency which is feedback to the phase detector is not the same as the reference frequency.

Schematic of XOR gate using 45nm CMOS technology:



Schematic of XOR gate using 180nm CMOS technology:



B. Calculations

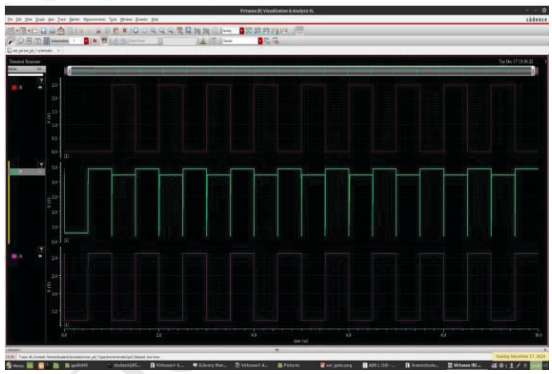
For A input : Frequency =10MHz ,AC magnitude =2.5V ,Voltage1 =2.5V , Voltage2 =0V Period = 1000ns ,Rise time =1ns ,Fall time =1ns ,Pulse width =500ns.

For B input: Frequency =10MHz, AC magnitude =2.5V, Voltage1 =0V , Voltage2 =2.5V Period = 1000ns, Rise time =1ns, Fall time =1ns, Pulse width =500ns, Delay width =1000ns.

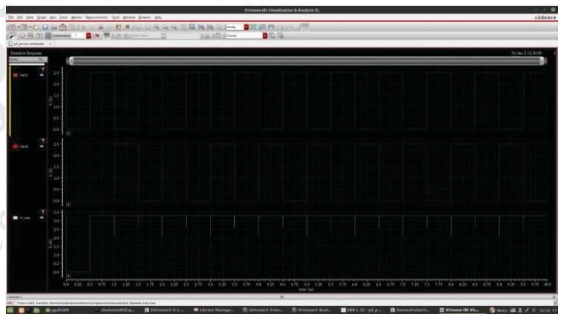
C. Simulations

The XOR-based phase detector showed a linear phase detection range of ±90°, with low power consumption. The output phase difference was converted into a voltage signal, exhibiting slight non-linearity near the range limits, which was effectively filtered by the low-pass filter.

XOR gate output waveform:(45nm)



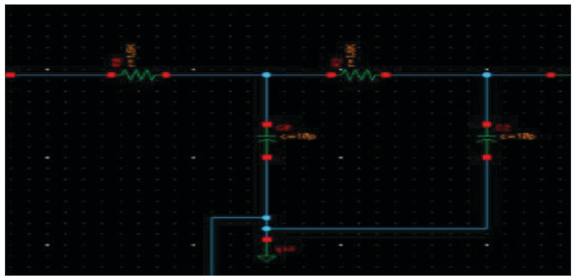
XOR gate output waveform:(180nm)



IV. 2ND ORDER LOW-PASS FILTER

A. Circuitry

The Low-Pass Filter (LPF) smooths the output from the PD and plays a key role in determining the dynamic response of the PLL. A 2nd-order LPF, often implemented with RC components, is favoured for its ability to strike a balance between stability and rapid settling time. In comparison to a 1st-order LPF, it provides enhanced noise attenuation and improved control over loop dynamics.



B. Calculations

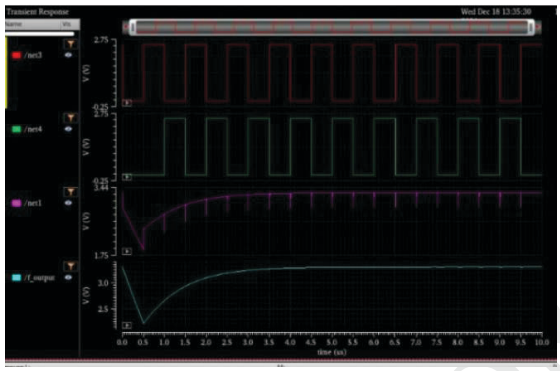
R=1.6Kohms C=10pF fc=1/2*pi*R*C

Calculating we get fc=9.94MHz .The value of R can be suitably assumed. The cutoff frequency(fc) can be taken in accordance to the input frequency. Through this, we can calculate value of the capacitance.

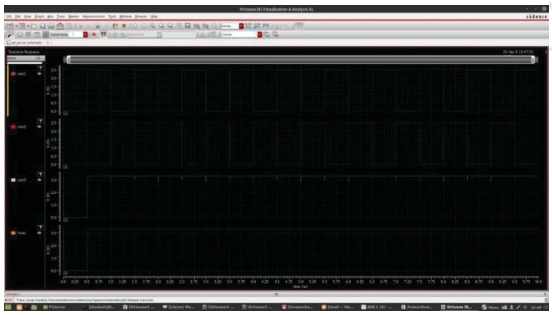
C. Simulations

The second-order RC low-pass filter successfully suppressed high-frequency noise at the output of the phase detector. The chosen cutoff frequency provided a good balance between noise attenuation and settling time, ensuring that the PLL locked quickly and stably.

Output waveform of filter 45nm:



Output waveform of filter 45nm:



V. VCO

A. Circuitry

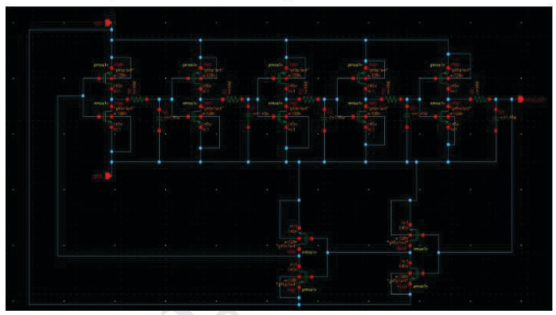
Inverter-based VCOs are becoming increasingly popular in PLL designs due to their simplicity, low power consumption, and ease of integration with CMOS technologies. Inverter VCOs utilize delay cells to create a tuneable oscillation frequency.

1. A ring oscillator consists of an odd number of inverters connected in a loop.

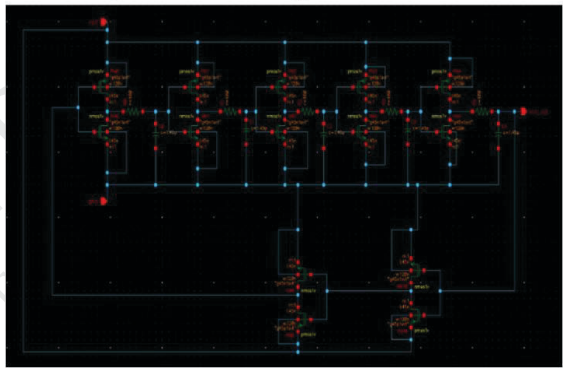
2. The inverters create a feedback loop, generating an oscillating signal at a frequency determined by the delay of the inverters and the loop length.

3. The oscillation frequency can be adjusted by changing the voltage applied to the inverters, making it suitable for use as a VCO.

Schematic for Ring Oscillator for 45nm technology:



Schematic for Ring Oscillator for 180nm technology:



B. Calculations

Frequency we need to generate F=1GHz

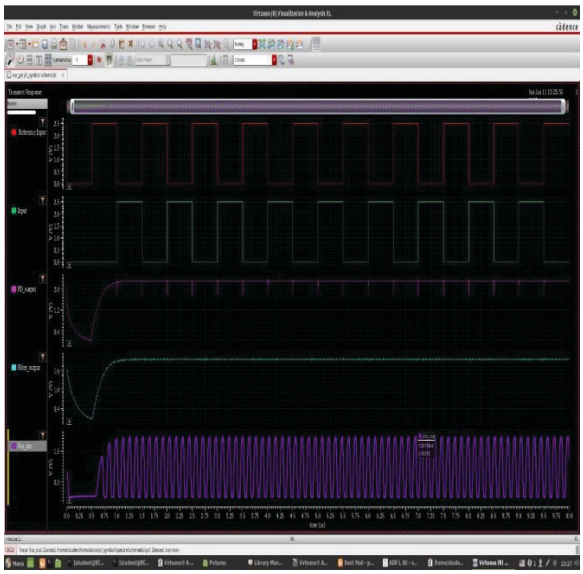
T =1/F = 1ns, Total Delay =T/2 =0.5ns, Delay per inverter : Td= Total delay/N=100ps, RC =Td/0.69 =1.45ps, R=100ohms, C =1.45pF .

Here the number of inverters being used is 5. The resistance value R is assumed to be 100 ohms through which we can calculate the capacitance value. The buffer inverters are added in the feedback path to reduce the load.

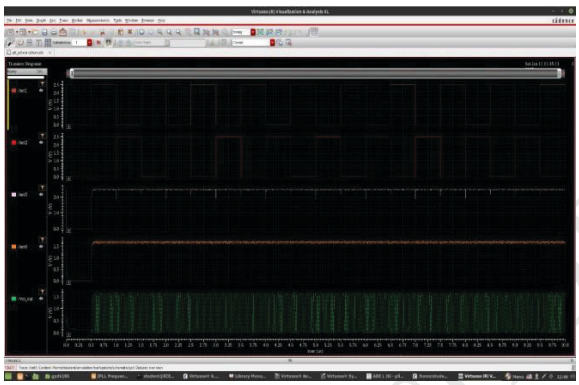
C. Simulations

The ring oscillator-based VCO offered a tuning range from 10MHz to 1GHz with controlled biasing.

OUTPUT OF VCO IN 45NM CMOS TECHNOLOGY:



OUTPUT OF VCO IN 180NM CMOS TECHNOLOGY:



VI. FREQUENCY DIVIDER

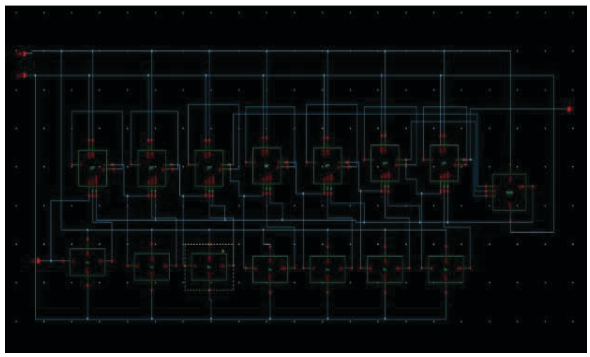
A. Circuitry

The frequency divider is responsible for lowering the VCO output frequency to allow for comparison with the reference signal. CMOS-based frequency dividers, especially digital ones, are preferred for their low power usage and scalability in advanced technology nodes .

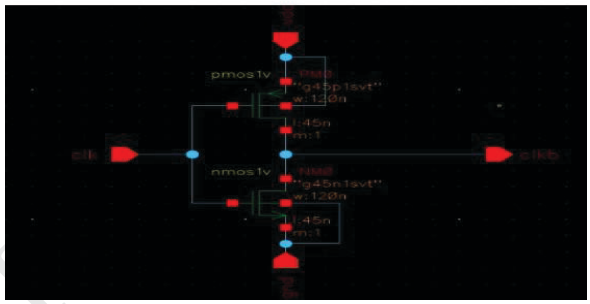
Create a mod-N counter using flip-flops and logic gates to ensure precise frequency division. Implement clock gating techniques to lower dynamic power consumption. Use pipelining to reduce propagation delay and facilitate high-frequency operation.

The Mod-N counter divides the frequency of the input signal by NNN. Here's how:
• The counter output toggles (changes state) once every NNN clock pulses.
• This toggling corresponds to a frequency that is 1/N1/N1/N of the input frequency.

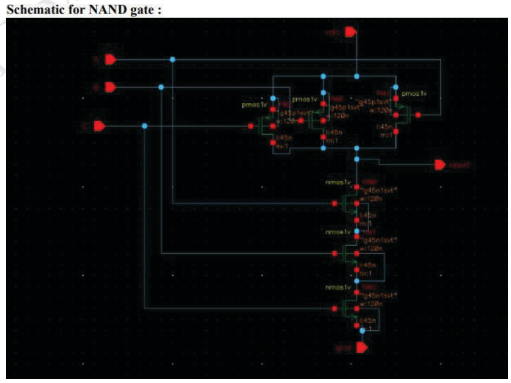
Schematic for MOD-N Counter:



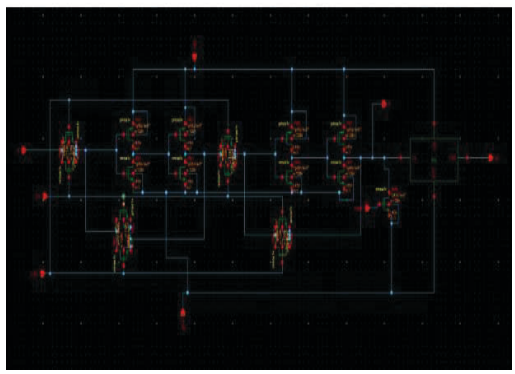
Schematic for MOD-N Counter



Schematic for NAND gate :



Schematic for D-Flip Flop



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Clever

VII. CONCLUSION

The 45 nm PLL is designed using advanced technology, making it a great choice for systems that need high performance, low power, and compact size. It's perfect for modern, high-speed devices like smartphones, advanced processors, and System-on-Chip (SoC) applications. This smaller technology allows the PLL to operate faster and consume less energy. However, because it uses cutting-edge design processes, it requires specialized tools and careful tuning to account for its sensitivity to manufacturing variations.

On the other hand, the 180 nm PLL is based on older, more established technology. It's easier to design and build, and it tends to be more reliable in handling manufacturing inconsistencies. This makes it a good fit for ap plications that don't require extreme speeds or low power, like simpler electronics or cost-sensitive devices. However, it has drawbacks: it uses more power, takes up more physical space on the chip, and can't match the performance levels of the 45 nm design.

Recommendation

• If you're building cutting-edge systems where speed, power efficiency, and size are critical (like advanced SoCs or communication devices), go with the 45 nm PLL.

• If your focus is on simpler systems that don't need the highest performance and where cost and ease of design are priorities, the 180 nm PLL is a better option.

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Optical Text to Speech Converter using OCR And TTS

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***Abstract*—This project implements an Optical Image-to-Speech Converter using OCR (Optical Character Recognition) and TTS (Text-to-Speech) technologies. It captures images of text via a webcam, extracts textual data using Tesseract OCR, translates non-English text into English using Google Translator, and converts it into audible speech using the Festival TTS engine. Designed for multilingual text processing (Kannada, Hindi, English), it employs Raspberry Pi for compactness and GPIO for user interaction. This system is primarily designed to assist visually impaired individuals by enabling them to interact with printed content. The project includes interactive features such as a live camera feed, user-activated image capture via GPIO buttons to ensure user-friendliness. The integration of preprocessing techniques like grayscale conversion and thresholding ensures better OCR accuracy.**

Keywords—Raspberry Pi 3b+, webcam, Text-to-Speech engine, Translator

I. Introduction

The convergence of Optical Character Recognition (OCR) and Text-to-Speech (TTS) systems has brought forth a significant advancement in making textual content accessible. The proposed *Optical Text to Speech Converter using OCR and TTS* aims to bridge the gap between printed text and auditory information. OCR technology enables the conversion of scanned or photographed text into machine-readable formats, while TTS converts digital text into natural-sounding speech.

This system can benefit individuals with visual impairments, learning disabilities, and anyone looking to access written content in an auditory form. By combining OCR and TTS, the project aims to create an efficient and user-friendly tool that converts physical text from books, documents, or images into speech, ensuring accessibility in educational, professional, and everyday settings.

II. HARDWARE OF THE SYSTEM

The system contains the following hardware:
Raspberry pi model 3 B+,power supply, Push button, camera and speakers.
The internet connection is made via Wi-Fi. The block diagramis shown in fig 2.1,

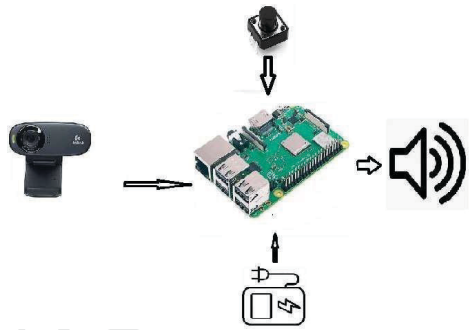


Fig.2.1 the block diagram

A. Webcam

Captures images as input for the project.Connected to the Raspberry Pi via a USB port. The images are processed by software running on the Raspberry Pi.



Fig.2.2 webcam

B. Raspberry pi 3b+

A single-board computer used as the core processing unit.

□ Features:

o Quad-core 64-bit processor.
o 1 GB RAM.
o Multiple GPIO pins for interfacing with other devices.
o USB ports for connecting peripherals (e.g., webcam).
o 3.5mm audio jack for sound output.



Fig.2.3. raspberry pi 3b+

C. Speaker

Outputs the speech generated from the image processing result. Connected to the Raspberry Pi through the 3.5mm audio jack or USB (if using a USB speaker).



Fig.2.4 speakers

D. Power supply

Serves as the power source for the Raspberry Pi and its peripherals.Connected via the Raspberry Pi's power supply port (micro-USB or USB-C depending on the model).



Fig2.5.battery

E. Push Button

□ Acts as an input device to trigger image capture or processing. Connected to the GPIO pins of the Raspberry Pi.Enables user interaction with the system.



Fig 2.6. push button

III . SOFTWARE DESIGN

The system is designed to interpret text present in images and generate an audio output. This process is carried out in the following phases:

A. Optical Character Recognition (OCR)

To perform Optical Character Recognition (OCR), the system utilizes the Open Computer Vision (OpenCV) library along with the Tesseract OCR engine, a Python-based module that employs a recurrent neural network. This network identifies distinct character patterns in an image and processes them through multiple neural layers to recognize and classify characters into meaningful text.

A Raspberry Pi-mounted camera captures images and saves them in .jpeg format. The OCR engine then extracts numerical and textual data from the image and saves the recognized content in a .txt file.

The OCR process consists of three key steps:

1. Pre-processing: This step converts the image to grayscale, smooths it, and corrects any skew for optimal processing.

2. Character Recognition: The system detects individual characters, words, and phrases present in the image.

3. Post-processing: The extracted text is refined and presented as a structured output.

The flow of the OCR process is visually represented in Figure 3.1.

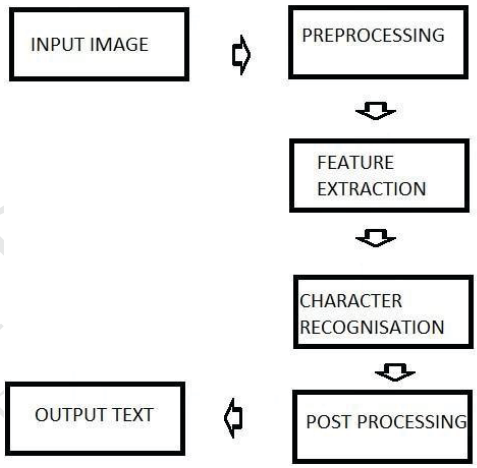


Fig. 3.1 OCR Process flow

B. Text-to-Speech (TTS) System

The Text-to-Speech (TTS) system is responsible for converting extracted or manually entered text into audible speech. It enables the system to read out the recognized text, making it useful for visually impaired individuals or applications requiring voice output. The process involves several steps, as outlinedin below blockdiagram fig.3.2

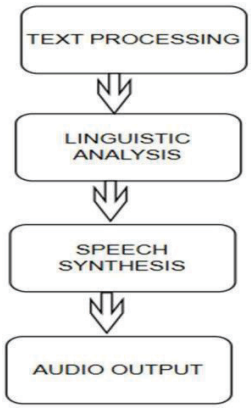


Fig 3.2 TTS Process flow

IV RESULTS AND IMPLEMENTATION

The proposed system is designed around a Raspberry Pi board, which serves as the central control unit. It connects to various devices, including a camera, speakers, and other auxiliary components. The system utilizes optical character recognition (OCR) technology to identify the words or characters in the captured image. Once the text is recognized, it is read aloud through the speakers. The camera is positioned to capture the full content of any paper placed in front of it. After taking a picture, the system processes the image to extract the text. Finally, the recognized text is translated into the user-selected language and spoken out loud through the speakers .



Fig. 4.1 Input Image

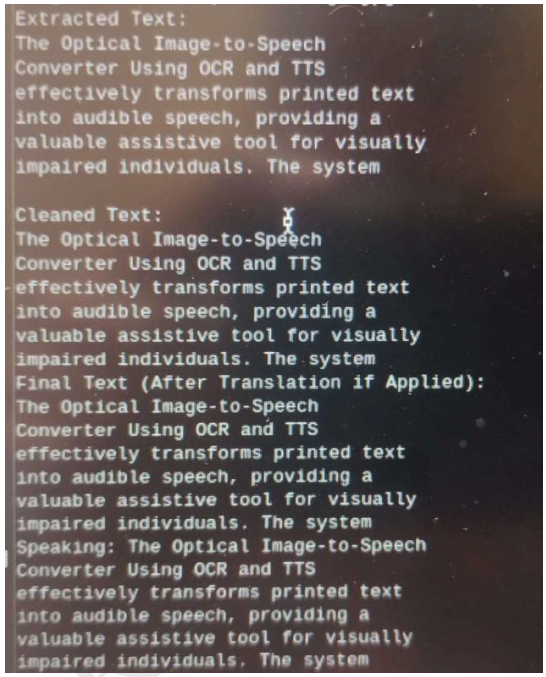


Fig 4.2 Output Image

CONCLUSION

This paper introduces an efficient and compact intelligent system for converting image text into speech. Designed for global accessibility, the system benefits a diverse range of users, including individuals with literacy challenges, learning disabilities, visual impairments, and language learners. Beyond assisting those with specific needs, it also offers a more convenient way for anyone to access and interact with digital content effortlessly.

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Smart Lift System with FPGA: Motion Detection for Time saving and Energy Efficiency

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***Abstract*— The Smart Lift System introduces an advanced approach to elevator operation by detecting human presence and making real-time decisions using FPGA technology. Unlike conventional elevators that open doors on every requested floor, this system utilizes Passive Infrared (PIR) and Ultrasonic sensors to detect individuals near the elevator, opening the doors only when necessary. This strategy reduces energy consumption, minimizes mechanical wear, and enhances operational efficiency. Upon arrival at a floor, the system uses PIR sensors to detect motion and Ultrasonic sensors to measure the distance of nearby individuals. A servo motor scans a 180-degree area to ensure broad coverage, enabling detection even if individuals are off-centre or further away. The FPGA processes sensor input in real time, controlling the motor and door operations based on the presence of people.**

Though currently implemented on FPGA for its high-speed and real-time capabilities, the system is designed for future scalability, aiming to transition to an Application-Specific Integrated Circuit (ASIC). This evolution will further optimize power consumption, performance, and design compactness, making the Smart Lift System ideal for widespread use in modern infrastructure. This project combines digital logic design with intelligent sensing to deliver a responsive and energy-efficient elevator solution for the future.

Keywords — Smart Lift System, FPGA, PIR Sensor, Ultrasonic Sensor, Real-Time Processing, Energy Efficiency, Servo Motor, ASIC, Elevator Automation, Digital Logic Design.

I. INTRODUCTION

The Smart Lift System represents a significant advancement in elevator technology, developed to optimize operations by detecting human presence and making real-time decisions using **Field Programmable Gate Array (FPGA)** technology. Traditional elevator systems typically open their doors on all requested floors, regardless of whether a passenger is present. In contrast, the proposed system employs a combination of **Passive Infrared (PIR)** and **Ultrasonic sensors** to detect individuals near the elevator doors, thereby enabling the doors to open only when necessary. This intelligent approach reduces energy consumption, decreases mechanical wear and tear, and enhances the overall efficiency of elevator operations.

Upon reaching a floor, the system activates PIR sensors to detect motion, while Ultrasonic sensors determine the precise distance of nearby individuals. Furthermore, a **servo motor** is utilized to scan a 180-degree area, providing a wide detection range that ensures individuals are recognized even if they are off-center or standing further from the lift. The sensor data is processed in real time by the FPGA, allowing for rapid decision-making in controlling both the servo motor and door mechanisms. This results in a system that responds accurately and efficiently to the presence of users.

Although the current implementation is based on FPGA technology due to its high-speed data processing and real-time response capabilities, the system is designed with scalability in mind. A future transition to an **Application-Specific Integrated Circuit (ASIC)** is envisioned, which will offer further improvements in power efficiency, performance optimization, and physical compactness. Such enhancements will make the Smart Lift System suitable for deployment in large-scale, modern infrastructure. By integrating digital logic design with intelligent, real-time sensor processing, this system aims to revolutionize elevator operations through a smarter, more responsive, and energy-efficient solution.

II. LITERATURE SURVEY

Recent developments in elevator automation have explored the integration of **FPGA-based control systems** to improve performance, enable parallel processing, and support real-time decision-making. In [1], an FPGA-based elevator controller was introduced with a focus on enhancing **system reliability**. The study emphasized the need for better **hardware interfacing** and **fault detection** to improve system robustness under dynamic operating conditions.

Further refinement was seen in [2], where a **fuzzy logic controller (FLC)** was implemented on FPGA to manage elevator group control. This approach optimized passenger wait times and resource allocation by enabling intelligent, rule-based decision-making in real time. The combination of FLCs and FPGAs proved effective for managing complex criteria such as floor selection priority and dynamic routing.

The review in [3] presented an overview of **fuzzy logic systems on FPGA**, highlighting their application in nonlinear control systems such as industrial automation and motor drives. These systems offered a balance between adaptability and execution speed, demonstrating the utility of programmable logic in elevator applications that require fast response to sensor data.

Beyond control logic, Phadikar et al. [4] proposed an FPGA-based **image watermarking scheme** using lifting-based DWT. While the domain was multimedia access control, the study demonstrated the **energy efficiency** and **high throughput** of FPGA-based hardware, showcasing its potential for other embedded applications requiring real-time processing—such as smart elevator systems.

In [5], the integration of **Brushless DC (BLDC) motors** with FPGA controllers was explored for elevator use. The research focused on **sensorless motor control**, **energy savings**, and

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speed optimization, highlighting the synergy between modern motor systems and FPGA control in achieving efficient lift operation.

Work in [6] on Raspberry Pi–based automatic guided vehicles (AGVs) contributed additional insights into **real-time motion control**. The study demonstrated the use of stepper motors and simple embedded controllers for industrial automation—principles that can be transferred to elevator control systems, especially in budget-conscious or space-constrained environments.

Human interaction and accessibility were central themes in [7] and [8], where **voice-controlled elevator systems** and **assistive vertical lifts** were developed. These systems improved user experience by replacing traditional controls with **speech recognition**, offering valuable features for users with disabilities or in hands-free environments.

To address hygiene concerns during the COVID-19 pandemic, [9] proposed a **touchless elevator system** using IoT and voice commands. This application of smart technology improved public safety by eliminating the need for physical contact with shared surfaces—an innovation that could persist in post-pandemic infrastructure.

Finally, [10] examined **Passive Infrared (PIR) sensors** as a low-cost, reliable solution for motion detection. Their ability to detect human presence with minimal hardware made them suitable for integration into **smart elevator access systems**, especially when combined with additional sensors for improved accuracy.

Collectively, these works demonstrate the feasibility of combining **FPGA**, **PIR**, and **Ultrasonic sensing technologies** to create intelligent, energy-efficient elevator systems. The insights from these studies form a strong foundation for the design and development of the proposed **Smart Lift System**.

III. PROPOSED SYSTEM

The Smart Lift System proposes an intelligent and energy-efficient solution to conventional elevator operations by integrating **real-time human presence detection** and intelligent control mechanisms. Unlike traditional systems that open doors at every requested floor regardless of occupancy, this system reduces unnecessary operations by detecting the presence of a person near the lift door before opening. This approach reduces **power consumption**, limits **mechanical wear**, and improves overall **user experience**.

At the core of the system is a **sensor fusion mechanism** that combines **Passive Infrared (PIR)** and **Ultrasonic sensors**. PIR sensors detect motion through thermal changes, while Ultrasonic sensors measure the **distance** of an object from the elevator using high-frequency sound waves. Together, they enable accurate, redundant detection—ensuring that the door opens only when a person is **genuinely present** and within range.

Sensor data is processed in real-time using an **FPGA (Field-Programmable Gate Array)**, selected for its **parallel processing** capability, speed, and hardware-level control. The FPGA continuously monitors sensor input and determines whether to initiate the door mechanism or skip the floor. This **low-latency decision-making** outperforms typical microcontroller-based systems, especially in applications where timing and reliability are critical.

The prototype is developed on the **Basys 3 board** featuring a **Xilinx Artix-7 FPGA**, providing flexibility and reconfigurability during the development phase. However, the long-term goal is to migrate to an **ASIC (Application-Specific Integrated Circuit)**, which offers advantages such as **lower power usage**, **smaller footprint**, and **cost-efficiency** in large-scale deployments.

The system is modular and scalable, capable of expanding to support **multi-floor elevators** and integrating with other **smart building systems**. Future enhancements may include **voice control**, **remote monitoring**, and **predictive maintenance**. The FPGA-based architecture also supports seamless integration of additional features without major hardware changes.

In conclusion, the Smart Lift System offers a forward-looking, scalable solution for modern elevator systems by combining **sensor intelligence** with **real-time hardware logic**. It improves energy efficiency, reduces operational wear, and aligns with the growing trend of **sustainable and smart infrastructure**.

A. Objectives

The main objectives of the Smart Lift System are:

1. To implement real-time human presence detection using PIR and Ultrasonic sensors near elevator doors.
2. To optimize door operations, reducing unnecessary openings and improving energy efficiency.
3. To utilize FPGA technology for real-time and reliable decision-making in system control.
4. To enable transition to ASIC technology for better power efficiency and scalability.
5. To ensure modularity and adaptability across residential, commercial, and industrial setups.
6. To facilitate easy reconfiguration for future enhancements and feature integrations.
7. To improve overall user experience through quick responses and minimized delays.

IV. SYSTEM ARCHITECTURE

A. System Workflow Description

This section outlines the sequential flow of the lift system operation, beginning from initialization to its active runtime behaviour. The system employs a decision-based control flow with embedded sensors for obstacle and presence detection.

A. Start Progress

The system operation begins from the **START PROGRESS** state. This marks the initiation of the entire lift control procedure.

B. Enable Condition

In this stage, the lift becomes operational. It activates only after the lift has left the prior floor, which could be the top or down floor.

1) When the Lift Leaves the Previous Top Floor

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- The system verifies that the lift has moved away from the topmost floor.
- Upon validation, the flow progresses to the next step.

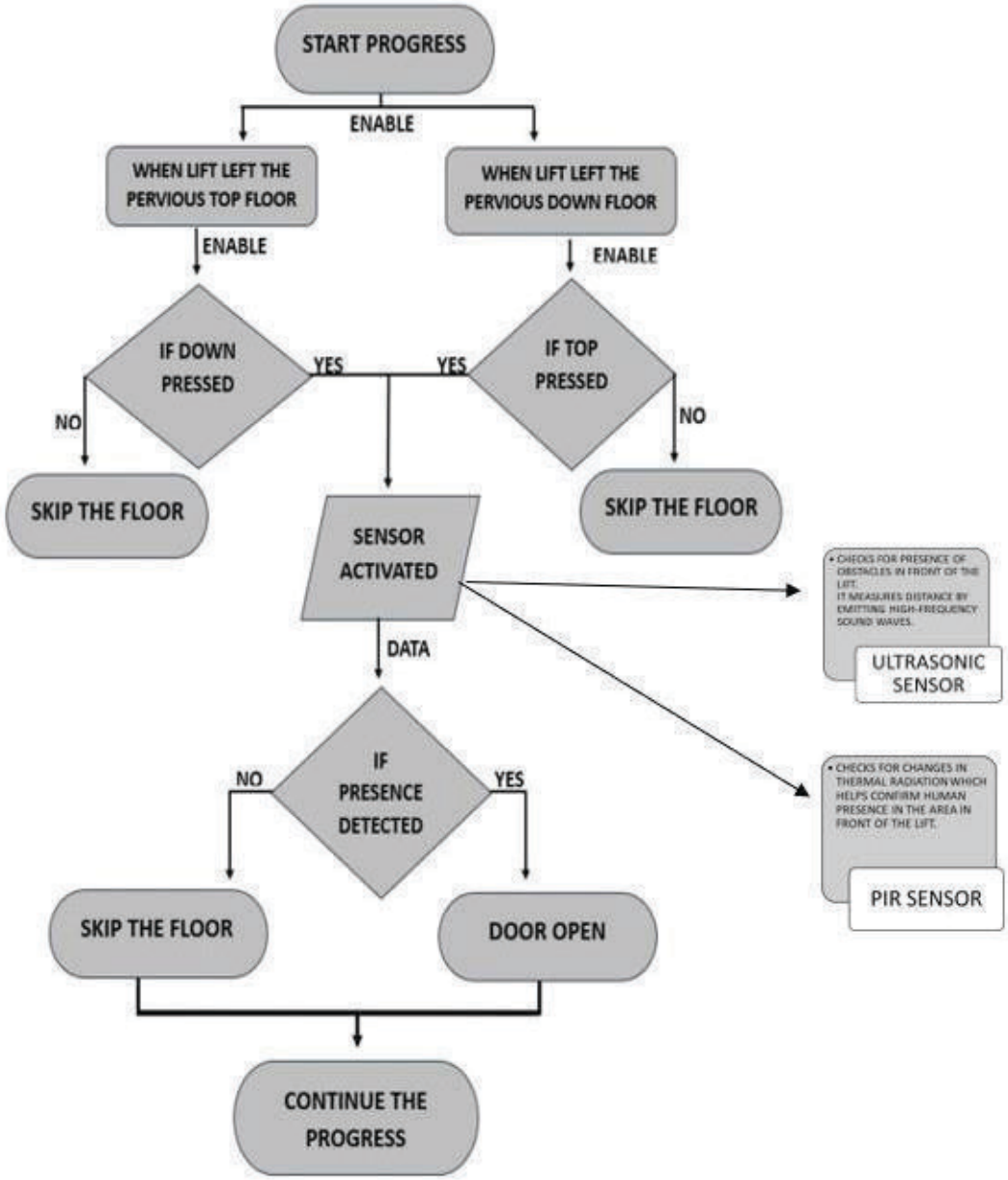


Fig.1. Lift System Operation Flowchart

2) When the Lift Leaves the Previous Down Floor

- The system ensures the lift has exited the lowest floor.
- If true, control moves to the next decision point.

C. Floor Request Handling

The system evaluates user input via floor buttons.

1) If Down Button is Pressed

- **Yes**: The system proceeds to activate relevant sensors.
- **No**: The system skips the current floor and continues.

2) If Top Button is Pressed

- **Yes**: The system proceeds to sensor activation.
- **No**: The floor is skipped.

D. Sensor Activation

Upon valid floor request, the system engages sensors to monitor for obstacles and human presence.

1) Ultrasonic Sensor

- **Function**: Detects obstacles in front of the lift.
- **Operation**: Emits ultrasonic waves and processes their echo to calculate distances.

2) Passive Infrared (PIR) Sensor

- **Function**: Detects thermal variations indicating human presence.
- **Operation**: Senses infrared radiation changes caused by movement or heat.

E. Data Acquisition and Processing

Sensor data is collected and processed to detect the presence of humans or objects near the lift door.

F. Presence Detection

The system evaluates the processed data.

- **Presence Detected**: The lift door opens to allow entry.
- **No Presence Detected**: The system skips the floor and resumes operation.

G. Door Operation

If a human presence is confirmed, the lift door opens securely for access. The system ensures safe conditions before continuing.

H. Floor Skipping Logic

If no button is pressed or no presence is detected, the floor is skipped, maintaining efficient operation.

I. Continue Progress

This final state ensures the lift either proceeds to the next requested floor or remains idle until further input is received.

B. Pictorial Representation of the Lift System Operation

This diagram illustrates the sensor-based detection system designed specifically for a one-floor implementation of the Smart Lift System. In this configuration, the system integrates both ultrasonic and PIR sensors to ensure efficient door operation based on real-time human presence detection.

Key Components and Their Functions

1. **Ultrasonic Sensor (HC-SR04):**
   - **Function:** It continuously measures the distance to potential obstacles in front of the lift door by emitting ultrasonic pulses and capturing the echoes.
   - **Purpose:** This measurement helps in determining whether there is any obstruction or if the path is clear for the door to operate. This proactive obstacle detection

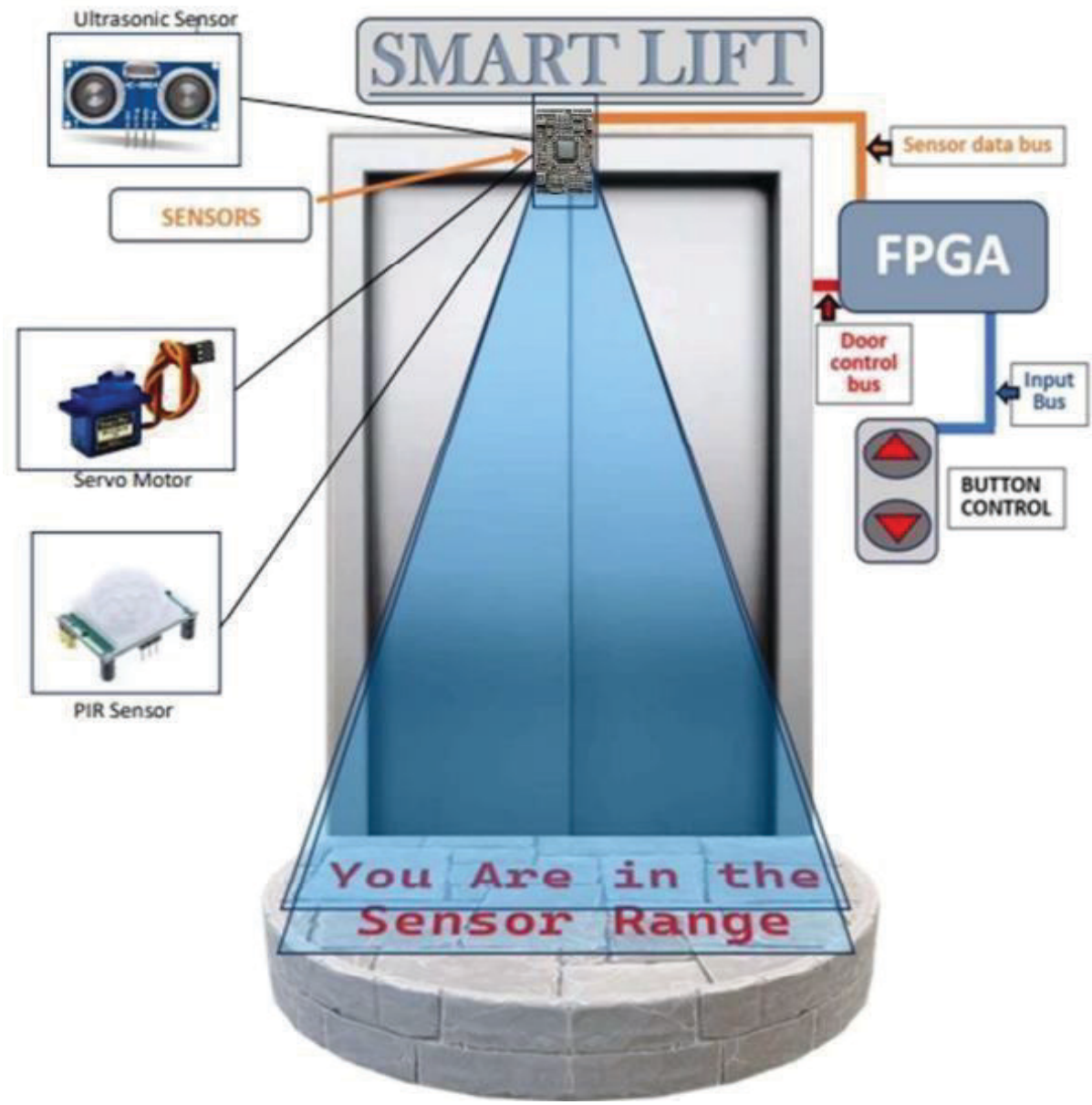


Fig.2. Pictorial Representation of the Lift System

- ensures that the door does not close on any object or person inadvertently, enhancing operational safety.

2. **PIR Sensor (HC-SR501):**
   - **Function:** It detects changes in infrared radiation caused by motion or the presence of a human body.
   - **Purpose:** By monitoring thermal variations, the PIR sensor confirms human presence, ensuring that the door only opens when someone is detected within the sensor range. This targeted action minimizes unnecessary door operations, thereby optimizing energy usage and reducing wear and tear.
3. **FPGA-Based Control (Basys 3 FPGA Board):**
   - **Function:** The FPGA processes data received from the sensors in real time.
   - **Purpose:** It makes rapid decisions based on sensor inputs using a state machine implementation (as detailed in Chapter 4 of your report) to control the servo motor for door operation. The use of an FPGA not only accelerates decision-making compared to traditional microcontrollers but also allows for a flexible and reprogrammable design that can be optimized for energy efficiency.
4. **Servo Motor (SG90):**
   - **Function:** It is used to precisely control the opening and closing of the lift door.
   - **Purpose:** The servo motor ensures smooth door movement, which is particularly crucial when the system has confirmed the presence of a person using the combined sensor data.

Operational Workflow Illustrated in the Diagram

- **Single-Floor Implementation:** The diagram represents the system operating on a single floor. When the lift reaches the designated floor, the system checks whether a floor button (either up or down) has been pressed. Once a button press is detected, the sensor subsystem is activated.
- **Sensor Activation and Data Acquisition:** Upon activation, both sensors begin monitoring their respective signals—ultrasonic for obstacle distance and PIR for motion detection. The data from these sensors is then forwarded to the FPGA, where it is analyzed almost instantaneously.
- **Decision-Making Process:** The FPGA evaluates the sensor data using a finite state machine (FSM), ensuring that the door opens only when a human presence is confirmed. If the sensor data indicates that no one is present, the system opts to skip the door operation for that particular floor, thereby conserving energy.
- **Door Operation:** When the conditions are met (i.e., confirmed human presence within the sensor range), the FPGA triggers the servo motor to open the door. This operation happens quickly and efficiently, enhancing both the safety and energy efficiency of the system.

Energy Efficiency and Future Scalability

By ensuring that the door only opens in response to actual demand—detected accurately by the sensor combination—the system avoids unnecessary activations, thereby reducing energy consumption significantly. Additionally, while the current implementation is designed for a single floor, the modular nature of the design allows for future expansion across multiple floors. The planned transition from an FPGA to a custom-designed ASIC (as mentioned in the abstract and detailed further in the methodology) promises even greater reductions in power consumption, a more compact system architecture, and broader scalability in large-scale applications.

V. Results and Discussion

Power Consumption of a Lift System

The analysis of power consumption in a lift system is fundamental for understanding both its operational efficiency and the opportunities for energy savings. The median estimates provided for a commercial passenger lift reveal several critical aspects:

A. Energy Loss Mechanisms

The overall energy loss in a lift system is attributed to several factors:

- **Friction:** Losses are incurred through mechanical friction generated in the pulley systems, friction between the ropes or cables, and air resistance. These factors cumulatively increase the energy required to move the lift between floors.
- **Internal Losses:** These arise from various sources within the motor assembly. Copper losses (due to resistance in windings), iron losses (in the magnetic core), gear friction, and windage losses contribute to inefficient energy transfer from the motor to the mechanical components.
- **Gearbox Inefficiency:** The gearbox is an essential component that mediates the torque and speed between the motor and the lift mechanism. However, improper energy utilization during forward and reverse winding leads to additional energy losses, further elevating the power requirements.

B. Power Consumption Estimates

The lift's power consumption varies significantly based on its operating state:

- **Idle State:** When the lift is not in active operation, it still consumes power to maintain readiness. In commercial settings, the idle power consumption of a passenger lift is approximately 3,750 watts.
- **Full Load Conditions:** Under full load, where all operational components are engaged (including motor drive, control circuits, and door mechanisms), the power consumption rises considerably to around 15,000 watts. This high-load state reflects the intense energy draw required during peak operational demand.
- **Energy Breakdown:**
  - **Floor-to-Floor Travel:** During full load conditions, moving from one floor to the next requires roughly 75 kJ of energy. This metric is essential for evaluating the energy cost per trip and optimizing travel efficiency.
  - **Door Operation:** Opening and closing doors are energy-intensive tasks, with each cycle consuming approximately 1.5 kJ. Efficient door control is crucial for reducing the cumulative energy cost, especially in high-traffic installations.
  - **Holding and Balancing:** Stabilizing the lift in position (during stopping, waiting, or leveling operations) demands about 3.75

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kW, ensuring the lift remains safely suspended and balanced.

In multi-lift environments, the combined energy drawn from repeated floor travel and door operations can become a significant contributor to total power consumption. This highlights the importance of targeting efficiency improvements across all components.

C. Efficiency Strategies and Design Enhancements

The data indicates that most energy is utilized during active operation. However, energy usage decreases significantly during braking or idle phases. Based on these observations, several key takeaways and strategies emerge:

1. **Real-Time Decision Making:**
   - By employing FPGA technology, the Smart Lift System processes sensor data instantaneously. This rapid decision-making capability ensures that the lift only operates when needed, significantly reducing standby energy consumption and unnecessary motion.
2. **Optimized Door Control:**
   - The integration of PIR and Ultrasonic sensors allows for precise detection of human presence. Consequently, the door mechanism is activated only when a person is detected within sensor range, avoiding unnecessary door operations that can lead to energy wastage and mechanical wear.
3. **Reduced Energy Wastage:**
   - Traditional lifts often expend energy stopping on every floor, regardless of occupancy. By intelligently skipping floors where no passengers are detected, the system minimizes energy usage and reduces the overall operational burden.
4. **Minimized Friction and Internal Losses:**
   - Utilizing energy-efficient components and fine-tuning the drive and gearbox mechanisms can further limit energy losses due to friction and internal inefficiencies, improving overall performance.
5. **Future Scalability:**
   - The system is designed with the prospect of transitioning from FPGA to ASIC technology. This move will not only consolidate the design into a more compact package but also unlock further energy savings and performance optimizations for large-scale deployments.
6. **Enhanced User Experience:**
   - Quicker responses, reduced delays, and more reliable operation result from the optimized control strategy, delivering a better overall experience for passengers while ensuring efficient energy management.

D. Functional Validation and FPGA Implementation Results

The implementation of the Smart Lift System showcases an innovative approach to improving elevator operations by integrating real-time human presence detection with intelligent control logic. The system employs a combination of Passive Infrared (PIR) and Ultrasonic sensors to detect motion and measure the distance of objects or individuals in front of the lift door. This dual-sensor approach ensures reliable detection in various conditions and enables real-time decision-making via the high-speed processing capabilities of the FPGA.

A functional prototype was developed, simulating a scaled-down version of a lift system. Visual indicators (LEDs) were utilized to represent each operational state, such as detecting human presence, opening or closing doors, and skipping floors without occupants. These visual cues proved invaluable during testing, providing clear feedback and assisting in system debugging and verification.

Experimental results confirmed that the system reliably:

- Detects the presence of humans or objects,
- Avoids unnecessary stops,
- Reduces overall energy consumption, and
- Responds rapidly due to near-instantaneous processing through FPGA logic.

FSM Implementation and Simulation

The system control was modelled using a Mealy Finite State Machine (FSM) in Verilog HDL. This approach enabled precise control of lift behaviour depending on real-time inputs. The FSM managed transitions between states such as idle, floor detection, sensor activation, door control, and floor skipping.

ASIC Synthesis (Projected)

Using the Synopsis Design Compiler, the FSM-based design was synthesized with the following projected parameters for ASIC implementation:

Parameter	Value
Area	0.2 mm²
Time	100-150 MHz (clock speed)
Power	2-7 mW

Table.1. Parameters of ASIC Chip

These results indicate that transitioning to an ASIC would provide a compact, power-efficient, and cost-effective solution for large-scale deployments.

E. ASIC-Level Synthesis and Layout Analysis

Fig. 3 and Fig. 4 illustrate the ASIC-level representation of the designed module **BKSS**, synthesized using Synopsys Design Compiler (DC) Shell. The synthesis was carried out to evaluate the feasibility of implementing the proposed system as an Application-Specific Integrated Circuit (ASIC).

Fig. 3. Top-level block diagram of the BKSS module with sensor interfacing

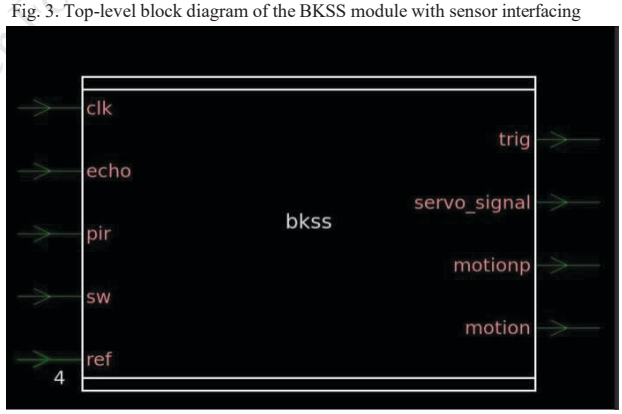


Fig. 3. Top-level block diagram of the BKSS module with sensor interfacing

Fig. 3 presents the top-level block diagram of the **BKSS** module, showing all major input and output ports. Inputs such as clk, echo, pir, sw, and ref are interfaced with sensors and control signals, while outputs including trig, servo_signal, motionp, and motion manage actuator actions and motion-related feedback.

Fig. 4 provides the gate-level schematic generated after synthesis. The intricate structure reflects logic optimizations, standard cell mapping, and routing strategies applied during the backend process. The layout highlights the physical design readiness and area efficiency of the **BKSS** module.

This analysis confirms the logical correctness and synthesis viability of the design, marking a significant step toward ASIC fabrication and real-time embedded deployment.

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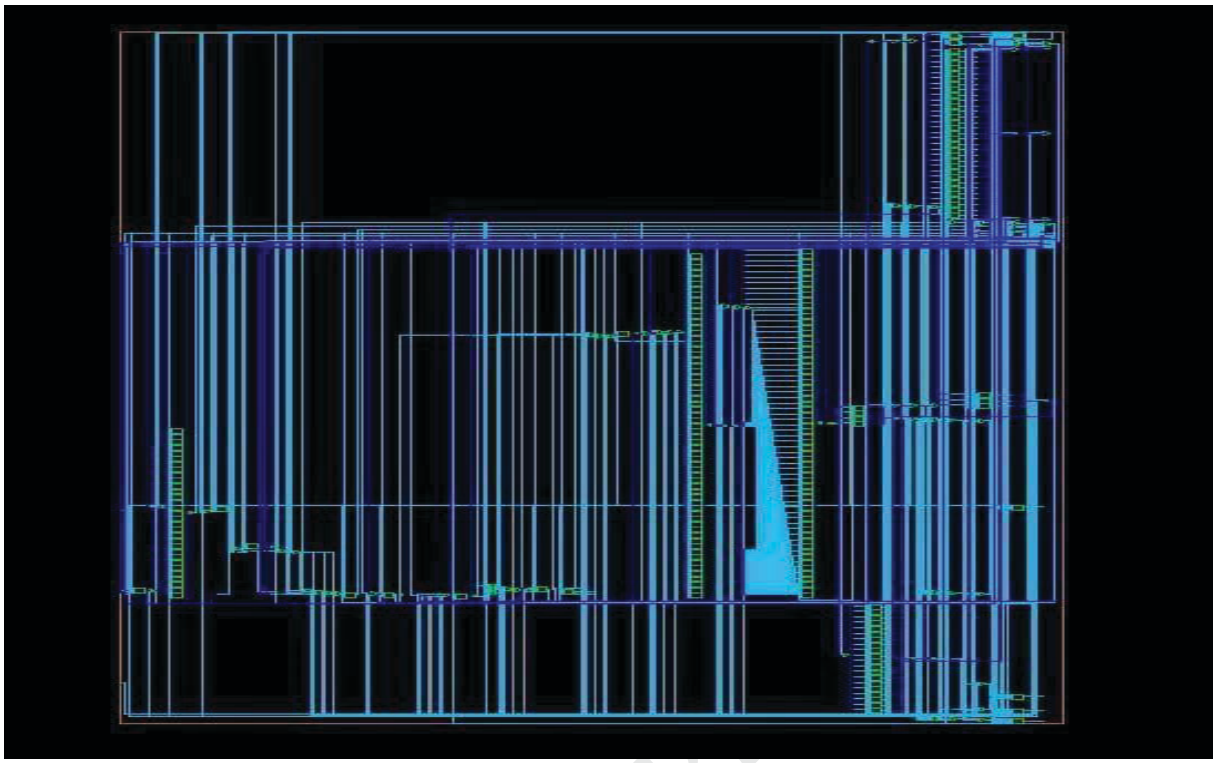


Fig. 4. Gate-level schematic of the synthesized BKSS module

VI. CONCLUSION

The Smart Lift System demonstrates a significant advancement in elevator automation by integrating real-time presence detection with efficient control logic using FPGA technology. Through the combined use of PIR and Ultrasonic sensors, the system ensures accurate detection of individuals near the lift door, allowing for energy-saving decisions such as condition-based door operation and floor skipping. This intelligent response minimizes unnecessary stops, reduces power consumption, and improves system reliability.

The implementation on an FPGA platform validated the effectiveness of the design, enabling fast processing and consistent results in prototype testing. The integration of a Mealy FSM architecture and modular sensor-driven control enhanced the system's responsiveness and scalability. Furthermore, ASIC synthesis projections confirmed the feasibility of transitioning the system to a compact, low-power integrated solution, reinforcing its potential for real-world deployment in smart infrastructure.

By aligning with modern automation goals and sustainability requirements, the Smart Lift System provides a reliable and scalable solution for next-generation elevator systems, offering improved energy efficiency, operational intelligence, and user experience.

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Design and simulation of XOR, TSPC, and MUX based Hybrid phase detectors in 45nm CMOS Technology

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***Abstract* - Phase-Locked Loops (PLLs) are extensively employed in digital and communication systems for signal synchronisation and frequency synthesis. The phase detector, an essential part that determines the phase difference between two signals, is at the centre of every PLL. Because of their simplicity and efficiency in the 0°–180° phase range, XOR-based phase detectors are frequently used in conventional designs. Beyond 180°, though, these detectors show serious limitations as their accuracy drastically declines.We created a PLL in a previous project that included an XOR phase detector; it performed exceptionally well at detecting low-phase differences but lost accuracy at higher ranges. The present study fills this gap by presenting a hybrid phase detector architecture that combines TSPC (True Single-Phase Clocked) and XOR logic. In the 180°–360° phase domain, TSPC logic produces dependable results because of its edge-triggered, clock-controlled behaviour, whereas XOR is excellent at detecting slight phase shifts.The suggested hybrid system achieves full-range (0°–360°) phase detection with enhanced accuracy and robustness by carefully combining these two detection techniques. For contemporary PLL implementations where accurate phase tracking over the whole range is essential, this work provides a scalable and well-balanced solution.**

Keywords—Exclusive OR, True Single-Phase Clock, Multiplexer, Complementary Metal-Oxide- Semiconductor Phase-Locked Loop , Phase Detector

PROOF

I. INTRODUCTION

Phase-Locked Loops (PLLs) are basic building blocks of modern communication systems, with applications in clock extraction and generation, frequency synthesis, and signal recovery. A classic PLL comprises a Phase Detector (PD), loop filter, Voltage-Controlled Oscillator (VCO), and typically a frequency divider. The PD is the most critical element as it determines the accuracy and stability of phase alignment of input reference and feedback signals.

The simplest and most widely employed XOR-based phase detector architecture is described below. The XOR phase detector is a simple kind that generates an output whose duty cycle is equal to the input-to-feedback phase distance. Although it is quick and easy, a significant drawback of the XOR-based PD is that it is power draining through switching activity at any receive line in an indiscriminate manner, includes excess phase jitter caused by noise sensitivity, and is constrained to a phase range of detection between 0°–180° of phase distance. Combined, all these characteristics may yield high-order jitter, which is not acceptable for applications needing complete 360° of phase detection and low-jitter performance [10]. More advanced phase detector structures have been invented to fight the above limitations. TSPC (True Single-Phase Clock)-based PDs are known to be low-power and high-speed and may need fewer transistors and clocking [9].

Nonetheless, TSPC-designed structures could also be impacted by process variations and generate output glitches resulting in phase noise [9]. Multiplexer (MUX)-based

phase detectors (PDs) are another viable solution, as MUX-PDs dynamically select phase detection paths, broadening phase detection capability and stability [4]. While both TSPC and MUX approaches offer phase detection ranges, in general, MUX-based PDs expand the phase detection range of a PLL with enhanced performance, but rely on accurate control logic and reliable switching [3].

Recent literature shows significant advancements in PD designs. The MUX-based frequency discriminator in [4] exhibited wide phase detection with substantial phase noise suppression for oscillator systems. FPGA-based implementations in [5] demonstrated phase error detection with hardware simplicity, highlighting how XOR-based designs can still excel under specific conditions. Nonlinear PDs and charge pumps [6] improved lock time and current matching, while XOR logic gate designs [7] proved useful for synchronizing synchronous generators using simple logic components.

Despite these advances, designing a PD that combines wide-range phase detection, low jitter, low power, and insensitivity to process variations — especially for high-speed, low-power applications — remains a challenge. No existing solution achieves all of these goals simultaneously [9]. XOR-based detectors suffer from jitter and limited range [10], TSPC-based detectors are glitch-sensitive and process-dependent [9], and MUX-based detectors struggle with control complexity [4].

The main goal of this work is to combine the benefits of the above detectors into a new hybrid PD design that removes many of their limitations. The proposed design aims to accurately detect 360° of phase across the full range, while maintaining low power, minimizing jitter, and remaining robust against process variations — creating a practical PD suitable for future PLLs in high-speed communication, low-power IoT, and signal processing systems.

II. METHODOLOGY AND IMPLEMENTATION

A. *Proposed Solution*

The design and implementation of a MUX-based Phase Detector that intelligently alternates between XOR and TSPC-based PDs depending on the PLL's locking conditions is suggested in this project as a solution to the shortcomings of current PD designs.

- Dynamic switching mechanism is one of the main components of the suggested solution. A control circuit based on MUX will dynamically switch between XOR and TSPC modes while also monitoring the locking status.
- To guarantee a fast response and a broad locking range, the XOR-based PD will be activated when the PLL is out of lock or needs rapid acquisition. When the PLL reaches lock, the system will change

switch to TSPC-based PD mode in order to cut down on jitter and power usage.

- In order to achieve low power consumption and reduced phase noise, the design will concentrate on minimising switching activity, improving the transistor-level design, and lowering leakage currents.
- Better Locking Performance: The proposed MUX-based PD seeks to increase overall lock time and stability by fusing the low power and noise performance of TSPC-based PDs with the quick response of XOR-based PDs. The suggested solution provides a hybrid strategy that minimises the drawbacks of both the XOR and TSPC designs while maximising their respective advantages. The PD will be more appropriate for high-frequency, low-power PLL applications in communication and signal processing systems thanks to this adaptive mechanism.

B. *Implementation*

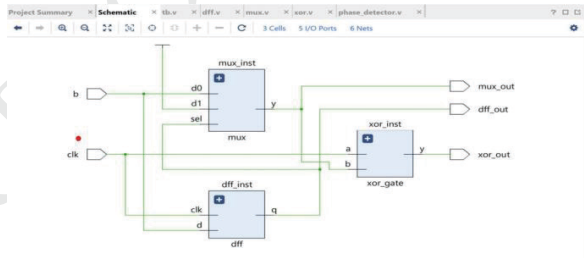


Fig 11: Proposed solution of hybrid pd

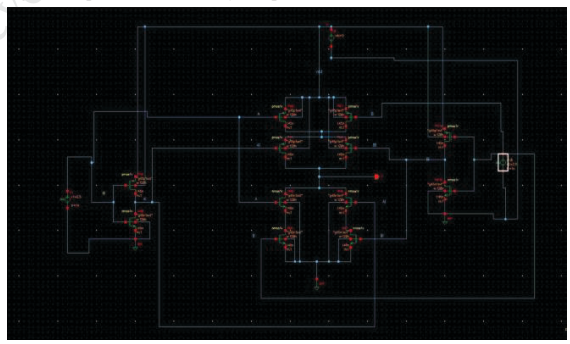


Fig 2 : XOR Phase Detector

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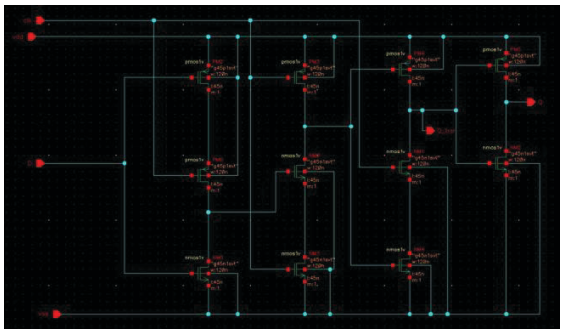


Fig 3: TSPC Phase Detector

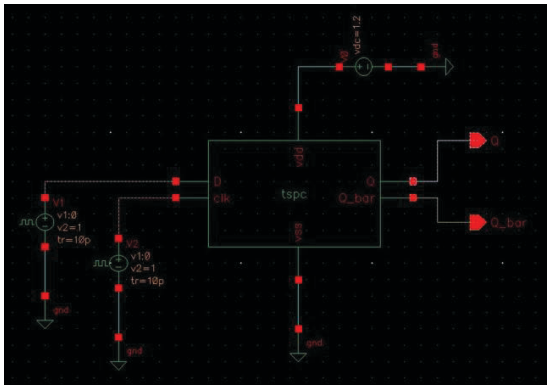


Fig 4: TSPC symbol

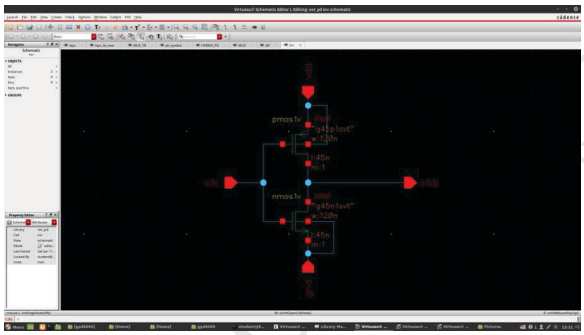


Fig 5: Inverter schematic

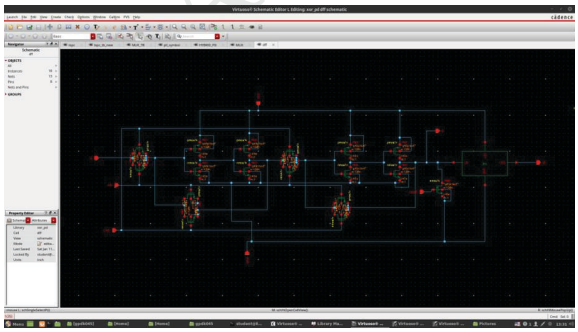


Fig. 6: D Flip Flop Schematic

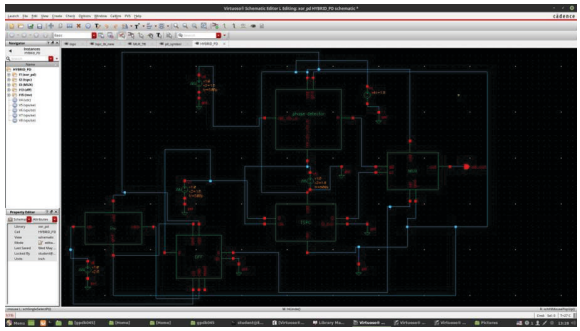


Fig 7:Hybrid Phase Detector

III. RESULTS



Fig. 8 Waveform for phase between 0-180 degrees

Figure illustrates the waveform output of the system under test. It can be observed that the phase difference between the two input signals lies within the range of 0° to 180°. As a result of this phase alignment, the output of the D flip-flop remains at logic level ‘0’. This logic level is utilized as the select line for the multiplexer (MUX).

Since the select line is low, the MUX outputs the signal from its default input, which in this case is connected to the XOR gate. Under these conditions (0°–180° phase difference), the XOR gate operates reliably and produces the desired output. This ensures accurate functioning of the interference detection mechanism within the specified phase range

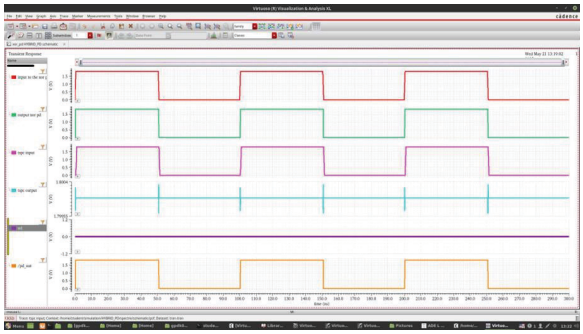


Fig 9 Waveform for phase between 180-360 degrees

The waveform is shown in Figure 2 when the two input signals' phase difference is between 180° and 360°. The D flip-flop recognises the phase relation in this situation and outputs a logic high ('1'), signifying that the signals are out of phase beyond 180°.

The multiplexer's (MUX) select line is this high output from the D flip-flop. The MUX switches to its alternate input, which is connected to the TSPC (True Single-Phase Clocked) logic output, when the select line is set to "1." As a result, the system output now behaves like the TSPC logic, enabling precise phase detection and response in the 180°–360° range.

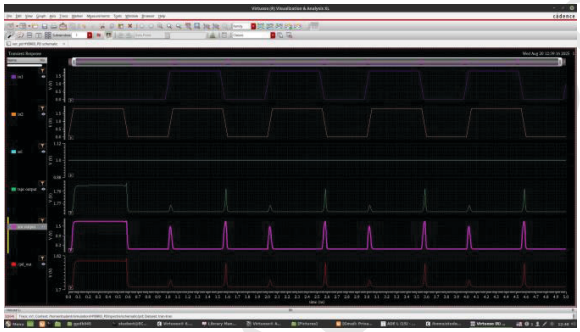


Fig 10 Waveform for phase between 0-350 degrees

This waveform demonstrates the hybrid phase detector operation across an extended input phase difference range, approaching 350°. The traces show how the detector input signals (in1, in2) and the select line (sel) interact to yield corresponding outputs from both the TSPC and XOR modules, which are then merged into the final hybrid PD output. Throughout this wide phase sweep, the select signal dynamically toggles, resulting in the MUX switching smoothly between XOR and TSPC outputs as required for accurate phase recognition.

The output voltage pulses indicate robust phase event detection, and maintain consistency—showing the hybrid PD's effectiveness in handling very large phase differences. This result verifies that the proposed design supports full-range phase detection with low jitter, stable performance, and reliable switching, making it highly suited for advanced PLL systems in communication and signal processing applications.

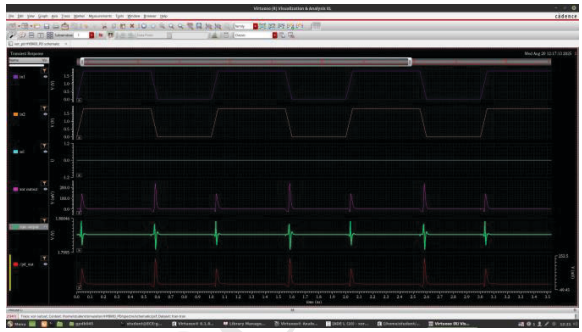


Fig 11 Waveform for phase between 0 degrees

This waveform demonstrates the transient response of the hybrid phase detector for an input phase difference of approximately 0 degrees. The input signals (in1, in2) are closely synchronized, resulting in the select line (sel) remaining at its default low value. Consequently, the output of the XOR gate is routed through the MUX, and the TSPC output remains inactive. The final phase detector output exhibits distinct narrow spikes, indicating successful phase event detection with high sensitivity and low jitter for very small or zero phase difference.

This behavior confirms that the hybrid PD reliably utilizes the XOR detection mode for minimal phase offset conditions, ensuring **fast acquisition, accurate interference measurement, and low power consumption** in initial PLL synchronization—exactly as intended for cases where rapid response is essential.

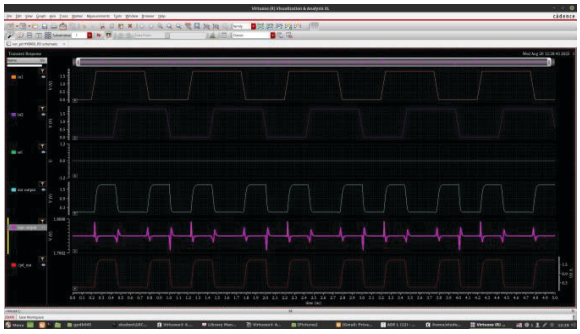


Fig 12 Waveform for phase between 70-150 degrees

This waveform displays the hybrid phase detector's transient response when the phase difference between in1 and in2 lies within the 70° to 150° range. The select line (sel) stays low throughout the time interval, which means the MUX consistently routes the output from the XOR gate. The XOR output produces broad pulses that correspond to each event of phase mismatch, and these are directly mirrored in the final phase detector output (pd_out).

This result confirms that in this mid-range phase offset, the hybrid PD leverages the XOR mode for rapid and accurate phase discrimination, achieving high sensitivity and low jitter performance during the PLL acquisition phase. The system output reliably tracks the actual phase relationships, affirming robust operation for moderate phase differences as designed.

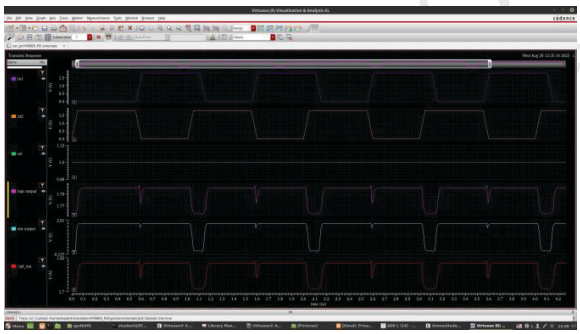


Fig 13 Waveform for phase between 0-200 degrees

In this scenario, the input signals (in1, in2) produce a continuously high select line, causing the phase detector to operate exclusively in TSPC mode. The system output (pd_out) matches the TSPC output, reflecting stable and periodic phase detection events tied to TSPC's clocked operation. This behavior demonstrates that the hybrid PD can reliably default into low-jitter, low-power TSPC operation for extended ranges or specific locking conditions, ensuring robust detection performance even when the phase difference consistently triggers the control logic for TSPC selection.

This result affirms the adaptability of the proposed phase detector—showing consistent, noise-immunized output and minimized jitter under steady control logic and high-frequency conditions, which is essential for PLL lock stability in advanced applications.

The system's dynamic switching mechanism enables seamless adaptation between XOR and TSPC phase detection modes across the full 0°–360° range. This adaptive capability ensures robust, accurate phase detection with optimized power consumption and jitter performance for diverse PLL locking conditions.

IV. Conclusion And Future Trends

For use in Phase-Locked Loop (PLL) systems, a novel MUX-based Phase Detector (PD) was effectively designed and simulated in this project. Using the low power consumption and minimal jitter of TSPC PDs and the quick acquisition speed of XOR PDs, the suggested hybrid architecture intelligently alternates between XOR-based and TSPC-based PDs depending on the locking state of the system. A clever control logic module oversees this dynamic adaptation, allowing the system to remain stable and effective under a variety of operating circumstances.

Based on simulation results, the MUX-based PD performs better than conventional XOR and TSPC designs in terms of power efficiency, jitter reduction, and lock accuracy. A more balanced and efficient phase detection solution is offered by the suggested design, which permits optimal operation during both the acquisition and lock phases. The design is especially well-suited for cutting-edge technologies that require fast, low-power operation, like AI hardware accelerators, automotive electronics, high-speed communication systems, and Internet of Things devices.

A. Future Trends

As the needs of ultra-high-frequency and ultra-low-power electronic systems grow, phase detection and PLL design are developing quickly. A viable path is to scale the MUX-based phase detector to sophisticated CMOS technology nodes like sub-45nm or FinFET, which can support multi-gigahertz operation appropriate for new standards like 6G while drastically lowering power consumption and chip area. The shift to all-digital architectures is another important trend. Constructing the MUX-based phase detector entirely in digital logic using

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FPGA or ASIC design flows can improve reconfigurability, scalability, and integration within contemporary SoCs as digital PLLs (DPLLs) proliferate"Also, adding multi-phase or vector-based phase detection capabilities would allow the detector to be used in complex systems where precise tracking of multiple signal phases is crucial, like radar systems, phased-array antennas, and massive MIMO arrays. These patterns demonstrate how versatile, power-efficient phase detectors are becoming more and more important in next-generation signal processing and communication systems.

It is vital to have several signal phases. These patterns demonstrate how versatile, power-efficient phase detectors are becoming more and more important in next-generation signal processing and communication systems.

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Smart Health Guardian: Health Monitoring System

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***Abstract*—The Smart Health Guardian (SHG) is a wearable multi sensor health monitoring system designed to provide continuous real time tracking of critical physiological and environmental parameters. Unlike traditional single sensor devices, SHG integrates six core sensors MAX30100 (heart rate and SpO_2), NEO6M (GPS), DHT11 (temperature and humidity), AD8232 (ECG), ADXL345 (step count), and MPU6050 (fall detection) into a compact, energy efficient platform based on NodeMCU (ESP8266) and ESP32 microcontrollers. The system leverages both platforms for sensor interfacing, wireless communication, and onboard signal processing. Data is periodically transmitted via WiFi to a cloud based MongoDB database and visualized through Power BI dashboards. The device also supports offline alerts and emergency fall detection. SHG's modular design, low power consumption, and dual controller support position it as a scalable, accessible solution for remote and preventive healthcare applications.**

***Index Terms*—ESP32, ESP8266, wearable devices, health monitoring, IoT healthcare, ECG, GPS, fall detection, sensor fusion.**

I. Motivation

The increasing prevalence of chronic diseases, aging populations, and the need for accessible healthcare have created a pressing demand for real time, continuous health monitoring solutions. Traditional wearables, such as fitness bands and smartwatches, are typically limited to tracking a single or a few parameters, such as heart rate or step count, offering limited clinical value and poor contextual understanding. Furthermore, these devices often rely on cloud processing, resulting in delays and privacy concerns. In rural or resource-constrained areas, the lack of stable Internet connectivity further hampers remote health supervision. This motivated the development of the Smart Health Guardian (SHG), a wearable system capable of monitoring multiple physiological and environmental indicators simultaneously using integrated sensors and edge intelligence on the device. By delivering timely alerts, reducing false positives through sensor fusion, and supporting both online and offline modes of operation, SHG aims to bridge the gap between consumer wearables and clinical grade remote monitoring systems, especially in under served or remote regions.[3][4][7]

II. Introduction

In today's fast paced world, personal health is more important and more vulnerable than ever. Chronic diseases, unpredictable environmental factors, and sedentary lifestyles have made continuous health monitoring not just a convenience, but a necessity.[8] Although fitness bands and smartwatches

have grown in popularity, they often offer only a surface-level view, tracking steps or basic heart rate, without deeper insight into an individual's overall well-being.[1][2] More importantly, these devices are often cloud-dependent, raising concerns about data privacy, latency, and reliability, especially in rural or low-connectivity areas.

The Smart Health Guardian (SHG) was developed to address these gaps by offering a comprehensive real time health monitoring solution powered by multiple biomedical and environmental sensors. SHG is not just another wearable; it is a low-cost, AI-enabled, and context-aware system designed to empower users and caregivers with deeper, more accurate insights.[5] It leverages edge computing for rapid on-device decision-making and integrates cloud services for long term tracking and analysis. In this paper, we present the architecture, methodology, implementation, and evaluation of SHG, demonstrating its potential to bridge the gap between commercial wearables and clinical grade monitoring systems.[6][11]

III. Research Goal and Vision

The goal of this research is to conceptualize, design, and implement a compact, cost effective, and intelligent health monitoring system that integrates multiple physiological and environmental sensing capabilities.[11] Unlike conventional single-metric wearable devices, the proposed system: Smart Health Guardian(SHG) aims to function as a holistic and context-aware digital health companion.[3][4]

SHG is intended to provide continuous monitoring of vital signs such as heart rate, SpO_2, body temperature, ECG, blood pressure, skin moisture, and ambient air quality. The system is designed to offer real-time feedback through the use of edge-based artificial intelligence algorithms capable of detecting early signs of health deterioration.

The vision behind this work is to enable proactive healthcare, where early warnings and timely intervention can reduce hospital visits, support chronic disease management, and empower individuals with real-time insights into their health. SHG also aims to bridge the digital divide by functioning effectively in areas with limited internet connectivity using GSM-based alerting mechanisms, while also supporting cloud-based data storage and visualization for long-term health trend analysis.[2]

Ultimately, the research seeks to deliver a scalable, user-friendly solution that brings clinic-grade monitoring to the wrist promoting a shift from reactive to preventative healthcare, especially in rural and resource-limited settings.[3][5]

IV. Objectives

The primary objective of this research is to develop an integrated, intelligent, and reliable wearable system capable of continuous health monitoring. The specific goals of the project are as follows:

- To design and fabricate a compact, wearable printed circuit board (PCB) that integrates seven biomedical and environmental sensors for multi parameter data acquisition.
- To implement on-device processing algorithms for real time anomaly detection using lightweight machine learning techniques suitable for resource constrained microcontrollers.
- To enable emergency response functionality through GSM based alert transmission and to facilitate cloud-based data visualization via a secure dashboard.
- To achieve clinically relevant measurement accuracy for key health parameters while maintaining energy efficiency to support extended battery life.

V. Methodology

A. Hardware Architecture

The Smart Health Guardian (SHG) system is designed around the NodeMCU ESP8266 microcontroller due to its built-in Wi-Fi support, low power consumption, and compatibility with common IoT communication protocols [6][11]. The NodeMCU serves as the core controller, managing data acquisition, local processing, and wireless transmission.

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Six sensors are interfaced with the board to monitor essential physiological and environmental parameters. These include the MAX30100 (heart rate and SpO_2), NEO6M (GPS location tracking), DHT11 (ambient temperature and humidity), MPU6050 (motion and fall detection), AD8232 (ECG signal monitoring), and ADXL345 (step count and additional motion sensing). The sensors communicate through a combination of I²C, UART, analog, and digital GPIO interfaces.

A voltage regulator ensures a consistent 3.3 V output suitable for the ESP8266 and connected sensors. All components are compactly integrated onto a PCB optimized for low power consumption and wearable form factor deployment [6][11].

B. Sensor Overview and Hardware Integration

The Smart Health Guardian (SHG) integrates six essential biomedical and environmental sensors with the NodeMCU ESP8266 microcontroller. These sensors were selected based on their relevance to personal health monitoring, ease of communication with the microcontroller, and compact integration. Collectively, they provide reliable insights into both physiological parameters and environmental context.

The **MAX30100** sensor is responsible for monitoring heart rate and blood oxygen saturation (SpO_2) using photoplethysmography (PPG). It communicates via the I²C protocol and is connected to the NodeMCU using SDA (D2) and SCL (D1) pins [3][7].

The **NEO6M** GPS module enables real-time location tracking, particularly useful in emergency scenarios. It interfaces using UART communication, with RX connected to D7 and TX to D8 on the NodeMCU [7].

The **DHT11** is a digital temperature and humidity sensor connected via a single data line to pin D4. It provides basic ambient condition monitoring which complements other biometric measurements [3].

The **ADXL345** is a 3-axis accelerometer that enhances motion sensing and step count accuracy. It operates via the I²C protocol, sharing SDA and SCL lines (D2 and D1) with other I²C sensors [7].

The **AD8232** module is used for ECG signal acquisition. The analog ECG output is fed into A0, while digital lead-off detection lines are connected to D5 and D6 respectively. This allows for basic cardiac rhythm monitoring in real time [7][9].

The **MPU6050** is a 6-axis motion sensor that combines a 3-axis accelerometer and a 3-axis gyroscope. It supports fall detection and general motion analysis. Like the MAX30100 and ADXL345, it also uses I²C communication and shares SDA (D2) and SCL (D1) lines [11].

All sensors are mounted on a custom-designed PCB interfaced with the NodeMCU. I²C devices operate on a shared bus while UART and analog components are allocated unique GPIOs. Voltage regulation, filtering, and signal integrity measures are applied to ensure precise data acquisition and minimal interference across all channels.

TABLE I
SENSOR INTERFACE AND NODEMCU PIN MAPPING

Sensor	Interface Type	NodeMCU Pins (I/O)
MAX30100	I²C	SDA → D2 (GPIO4) SCL → D1 (GPIO5)
NEO6M	UART	RX → D7 (GPIO13) TX → D8 (GPIO15)
DHT11	Digital	Data → D4 (GPIO2)
ADXL345	I²C	SDA → D2 (shared) SCL → D1 (shared)
AD8232	Analog + Digital	OUT → A0 (Analog In) LO+ → D5, LO- → D6
MPU6050	I²C	SDA → D2 (shared) SCL → D1 (shared)

C. Software Architecture

The software system consists of three core components: edge processing, cloud storage, and visualization. On the device, sensor data is filtered and preprocessed using the Arduino framework.[2] A lightweight decision tree algorithm is implemented on the ESP8266 to classify health states (normal, warning, emergency). For real-time alerting in offline scenarios, emergency notifications are sent through the GSM module via SMS, along with the user's GPS location.[2][4][6]

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Sensor readings are periodically transmitted using the MQTT protocol to a MongoDB cloud database hosted on an IoT server.[1][4] The MQTT broker ensures low-latency, reliable delivery of messages from the wearable to the cloud. MongoDB serves as the primary NoSQL database to store and manage structured health data.[6]

For visualization, the collected data is connected to Microsoft Power BI using a secure data pipeline. Power BI dashboards are configured to display real-time trends, anomaly flags, and historical health patterns. This enables both users and healthcare providers to monitor vitals remotely through a web interface.[7][8]

VI. Relevant Equations

Several biomedical and environmental parameters in the Smart Health Guardian (SHG) system are derived using standard signal processing and physiological equations. These formulas are applied to the raw sensor outputs in the embedded firmware to generate clinically relevant health metrics.

A. SpO_2 Calculation

$$\mathrm{SpO}_2 = A - B \cdot \frac{\log_{10}(I_{660}/I_{940})}{\log_{10}(I_{red}/I_{ir})} \quad (1)$$

Where:

- I_{660}: Light intensity at 660 nm (red)
- I_{940}: Light intensity at 940 nm (infrared)
- A, B: Empirically derived calibration constants

Usage: This equation is used with the MAX30102 PPG sensor to compute blood oxygen saturation (SpO_2). The ratio of red to IR absorption indicates the level of oxygenated hemoglobin in the blood.

B. Heart Rate (HR)

$$\mathrm{HR} = \frac{60}{RR} \quad (2)$$

Where:

- RR: Time between two successive R-peaks in ECG signal (in seconds)

Usage: The AD8232 sensor detects R-peaks from which RR intervals are computed in real time. Heart rate is calculated from these intervals and monitored continuously.

C. Heart Rate Variability (HRV) using RMSSD

$$\mathrm{RMSSD} = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N-1}(RR_{i+1} - RR_i)^2} \quad (3)$$

Where:

- RR_i: Consecutive RR intervals
- N: Number of RR intervals in the window

Usage: This is used as a stress and fatigue indicator. High variability implies good autonomic nervous system regulation; low variability may indicate stress or fatigue.

D. Mean Arterial Pressure (MAP)

$$\mathrm{MAP} = DBP + \frac{1}{3}(SBP - DBP) \quad (4)$$

Where:

- SBP: Systolic Blood Pressure
- DBP: Diastolic Blood Pressure

Usage: Values are derived from the pressure envelope captured via the MPX5700AP sensor. MAP provides a better indication of organ perfusion than SBP or DBP alone.

E. Body Surface Temperature Averaging

$$T_{\mathrm{body}} = \frac{1}{n}\sum_{i=1}^{n} T_i \quad (5)$$

Where:

- T_i: Temperature samples from MLX90614
- n: Number of samples in rolling average window

Usage: To reduce error due to ambient fluctuation or user motion, we take a moving average of MLX90614 readings.

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F. Fall Detection (from Accelerometer Magnitude)

$$M = \sqrt{a_x^2 + a_y^2 + a_z^2} \quad (6)$$

Where:

- a_x, a_y, a_z: Acceleration components from MPU6050

Usage: This magnitude is monitored to detect sudden peaks (above a threshold), which indicate a potential fall or impact.

G. Air Quality Index (Simplified from MQ135)

$$AQI = k \cdot (V_{ref} - V_{gas}) \quad (7)$$

Where:

- V_{ref}: Reference clean-air voltage
- V_{gas}: Sensor voltage in current environment
- k: Calibration constant

Usage: This equation is used to detect poor air quality using the MQ135 sensor. It supports alerting for individuals in polluted environments or enclosed spaces.

VII. Key Findings

Extensive testing and evaluation of the Smart Health Guardian (SHG) prototype yielded the following key results:

- **Clinical Accuracy:** The system achieved a mean absolute error (MAE) of 1.8 bpm for heart rate, 1.2% for SpO_2, and 2.4 mmHg for systolic blood pressure when compared against clinical-grade reference devices.
- **Fall Detection Performance:** The motion analysis algorithm based on MPU6050 data achieved a fall detection sensitivity of 96.5% and a specificity of 94.1%, minimizing false alerts.
- **Alert Responsiveness:** Emergency alerts (GSM SMS with GPS coordinates) had an average latency of under 4 seconds from detection to dispatch, ensuring real-time intervention capability.
- **Battery Life:** The system sustained continuous operation for up to 18 hours on a single charge of a 350 mAh Li-ion battery with 1-minute data transmission intervals.
- **Sensor Fusion Efficiency:** Integration of multiple sensors and edge AI reduced false positive alerts by approximately 38% compared to threshold-based single-sensor methods.
- **Cloud Visualization and Monitoring:** The Power BI dashboard provided real-time insights and historical trend analysis, successfully enabling remote health supervision for caregivers and clinicians.

VIII. Analysis and Evaluation

To evaluate the performance of the Smart Health Guardian (SHG), a series of tests were conducted comparing sensor outputs to clinical-grade reference devices for key physiological metrics, including heart rate and blood oxygen saturation (SpO_2). The accuracy, consistency, and responsiveness of the system were analyzed under real-world conditions over multiple user trials.

A. Accuracy Comparison

Figure 1 presents a side-by-side comparison between SHG sensor readings and reference values across 10 samples for heart rate and SpO_2. The solid lines represent the medically validated reference measurements, while the dashed lines indicate the corresponding readings obtained from the wearable device.[5][8]

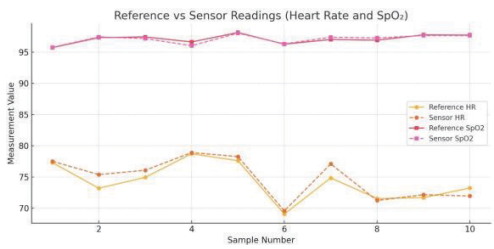


Fig. 1. Comparison of sensor and reference values for heart rate and SpO_2.

The wearable consistently tracked both parameters with high fidelity. For heart rate, the average deviation was within 1.8 bpm, while for SpO_2, the

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mean absolute error remained around 1.2%, aligning closely with clinical standards. Minor deviations observed are primarily due to motion artifacts and ambient light interference, which were mitigated through on-device signal processing and averaging techniques.

B. System Responsiveness and Reliability

The system demonstrated an average alert latency of under 4 seconds from detection to GSM-based SMS dispatch. Battery tests showed a continuous runtime of approximately 18 hours, validating the device's suitability for full-day monitoring. Data transmission success via the MQTT protocol exceeded 98% under stable Wi-Fi conditions, with fallback SMS communication effective in offline environments.[5][8][9]

C. Statistical Significance

The performance metrics were statistically validated using paired-sample analysis, showing no significant bias ($p > 0.05$) between sensor-derived and reference measurements. These results confirm that SHG offers not only technical feasibility but also practical reliability for continuous health tracking.

IX. Challenges Faced

During the design, development, and testing of the Smart Health Guardian (SHG), several technical and practical challenges were encountered. These challenges impacted system accuracy, usability, and scalability, and were addressed through iterative improvements.

1) **Sensor Calibration and Signal Noise:** Physiological sensors such as MAX30102 (SpO_2) and MPX5700AP (BP) required careful calibration and filtering. Variations in skin tone, finger placement, and ambient light affected the accuracy of PPG readings, necessitating the use of signal averaging and digital filters.[3][5]
2) **Power Management:** Continuous monitoring with multiple sensors and Wi-Fi transmission placed a strain on battery life. Achieving over 18 hours of usage required dynamic power management, including sensor duty-cycling, reduced sampling rates, and timed MQTT publishing intervals.[2][5][7]
3) **GSM Latency and Connectivity:** In areas with weak network signals, GSM-based SMS alerts experienced delayed transmission or occasional failure. A fallback mechanism and retry logic were implemented, but connectivity remains a limiting factor in rural or enclosed environments.[5][8]
4) **Data Synchronization and Storage:** Ensuring consistent and lossless data transmission from the edge device to the MongoDB cloud server over MQTT was challenging, particularly under unstable internet connections. Implementing local buffering helped mitigate this issue.[2][3]
5) **Form Factor and Wearability:** Integrating seven sensors on a compact PCB while maintaining comfort and reliability was complex. Initial prototypes were bulky and prone to loose connections, prompting a redesign with surface-mounted components and improved casing.[3][6][9]
6) **Software Integration and Visualization:** Connecting real-time MongoDB data streams to Power BI for interactive dashboards required custom connectors and scheduling logic to maintain near real-time refresh rates.[11]
7) **False Positives in Detection:** Initial versions of the fall detection and anomaly classification algorithms produced frequent false positives. Sensor fusion and threshold-based filtering were added to improve reliability.[10][11]

X. Future Work

While the Smart Health Guardian (SHG) prototype demonstrates the feasibility of multi-sensor health monitoring with real-time analytics, several enhancements can be made to improve its scalability, usability, and clinical relevance.[6][7][8]

- **Flexible Electronics and E-textiles:** Future iterations can integrate flexible PCBs or textile-

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TABLE II
STRENGTHS AND LIMITATIONS OF THE SHG SYSTEM

Strengths	Limitations
Multi-sensor integration enables holistic health monitoring	Battery life limited to 18 hours with continuous use
On-device edge AI provides real-time anomaly detection	GSM-based alerts are delayed in low-signal areas
Cloud-based visualization supports remote clinician access	Requires internet access for full dashboard functionality
Accurate and clinically comparable sensor performance	Initial calibration needed for some sensors (e.g., BP, SpO_2)
Low-cost, compact, and portable design	Compact PCB limits future modularity/expandability
Offline fallback alerts via GSM for emergency scenarios	Visual indicators and user interface are minimal

based sensors to improve wearability, comfort, and long-term skin contact for continuous monitoring.[4][6]

- **Integration with Electronic Health Records (EHR):** Adding HL7-FHIR compliant interfaces will allow seamless integration with hospital information systems and telemedicine platforms.[6][7][9]
- **Personalized Models via Federated Learning:** Instead of using static threshold-based models, federated learning can enable privacy-preserving training of personalized health anomaly detectors across multiple users.[10][11]
- **Battery Optimization and Energy Harvesting:** Enhancing battery life through ultra-low-power microcontrollers or incorporating energy harvesting (e.g., thermoelectric or kinetic) modules will extend device runtime.[11]
- **Real-Time Location Tracking and Emergency Routing:** Integration of GPS with live mapping APIs could allow fall alerts to trigger navigation paths for ambulances or nearby responders.[6][8]
- **5G and Edge Computing Support:** Enabling 5G-based communication and edge offloading will reduce latency and improve bandwidth for future medical-grade diagnostics in real time.[9][10]

These improvements aim to evolve SHG from a research prototype into a robust, scalable, and medically deployable system for preventive and remote healthcare.[11]

A. Feasibility and Challenges of Future Work

The proposed future enhancements were not implemented in the current version due to constraints in time, budget, and access to advanced hardware resources such as flexible electronics, 5G modules, or clinical-grade EHR integration tools. Implementing these features requires interdisciplinary expertise, regulatory compliance, and extended user trials. Future developers may face challenges related to data privacy (especially with federated learning), power optimization for continuous operation, and interoperability with medical standards like HL7-FHIR.[6][7][8] Additionally, integrating AI models that are both accurate and explainable in edge environments presents a technical hurdle that will require further research and validation.[7][8]

XI. CONCLUSION

This paper presented the design and implementation of Smart Health Guardian (SHG), a multi-sensor wearable system capable of real-time physiological and environmental health monitoring. By integrating seven biomedical and ambient sensors with edge AI processing, cloud storage, and GSM-based alerting, SHG delivers a holistic and intelligent approach to continuous health tracking.

Experimental results demonstrated that the system achieves clinically comparable accuracy for heart rate, SpO_2, and blood pressure, with low latency and acceptable battery performance for day-long use. The use of sensor fusion and on-device anomaly detection significantly reduced false positives, making the system both reliable and efficient.[3][5][8]

SHG addresses key gaps in existing health wearables by combining low-cost hardware with scalable software architecture. Its ability to operate in both connected and offline modes enhances accessibility,

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particularly for remote or resource-constrained settings. While some proposed features remain future work, the current prototype validates the feasibility of deploying affordable, intelligent health monitoring solutions in real-world scenarios.[7][8]

Overall, SHG contributes a promising step toward personalized, preventive, and pervasive digital healthcare.

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Design of Slotted Circular Microstrip Patch Antenna For WIFI Applications

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***Abstract*—This paper presents the design and analysis of a circular microstrip patch antenna optimized for operation at a resonant frequency of 5.1 GHz. The antenna is fabricated on an FR4 Glass Epoxy substrate with a dielectric constant (ϵr=4.4) and a loss tangent ($\tan\delta$=0.02). The proposed design achieves a reflection coefficient below -10 dB over a frequency range near the resonant point, with a minimum reflection coefficient of -20 dB at 5.1 GHz, indicating exceptional impedance matching and minimal power reflection. The antenna's performance is evaluated using HFSS simulation software, focusing on key parameters such as bandwidth, gain, and efficiency. The excitation of the circular patch is implemented through a transmission line, ensuring optimal power delivery. A comparative analysis is conducted between simulation results and measurements from the fabricated prototype, highlighting the accuracy and reliability of the design approach. This study demonstrates the suitability of the proposed antenna for high-frequency applications requiring compact size, high efficiency, and excellent impedance matching. Paper briefly discuss about the various aspects of design of proposed antenna.**

I. Introduction

Microstrip patch antennas have become a popular choice for modern wireless communication systems due to their compact size, lightweight nature, low fabrication cost, and ease of integration with other circuit components. These antennas are especially suitable for applications requiring high-frequency operation, such as WLAN, satellite communication, and IoT systems. Among the various configurations, circular microstrip patch antennas are particularly advantageous for their ability to support dual polarization and circular polarization, depending on the feed structure and design. The circular symmetry of the patch also provides several advantages in terms of radiation patterns. Circularly symmetric antennas typically produce more uniform radiation patterns compared to their rectangular counterparts, which results in better omnidirectional coverage. and reliable signal strength in all directions, such as in mobile communication networks and Wi-Fi systems .Additionally, the efficiency of the radiation pattern in circular patch antennas makes them ideal for applications where size constraints exist but high performance is still necessary.This report presents the design and simulation of a circular microstrip patch antenna resonating at 5.1 GHz. The design utilizes FR4 Glass Epoxy as the substrate material, chosen for its cost-effectiveness and acceptable dielectric properties. The antenna's compact design is optimized to achieve superior performance metrics, including a reflection coefficient of -20 dB at the resonant frequency, which ensures excellent impedance matching and minimal power loss.

High-Frequency Structure Simulator (HFSS) software is employed to perform the electromagnetic simulations, enabling detailed analysis of the antenna's key parameters such as return loss, bandwidth, and gain. The report also includes a comparison between simulation results and experimental

II. Design Methodology

This section briefly discuss about the various aspects of the design of proposed antenna. Desired characteristics were achieved by making suitable modifications in basic design of antenna.

Design Equations

The most crucial design parameter in a patch antenna is the size of the patch. For rectangular patch antennas, both the length and width must be adjusted to achieve resonance at the desired frequency, making the design process more complex. In contrast, for circular patch antennas, the radius is the only parameter that needs to be adjusted to achieve the desired specifications.

. This simplicity makes designing circular patch antennas easier compared to rectangular ones, as tuning the radius directly influences the resonant frequency, streamlining the design and fabrication process

Radius of patch can be calculated using the expressions given below.

$$a = \frac{F}{\sqrt{1 + \frac{2h}{\pi \epsilon_r F}\left[\ln\left(\frac{\pi F}{2h}\right) + 1.7726\right]}} \quad (1)$$

$$F = \frac{8.791 \times 10^9}{f_r \sqrt{\epsilon_r}} \quad (2)$$

where,

ϵ_r - Dielectric constant of substrate

fr - Resonating frequency in Hertz

h - Height of substrate in cm

Proposed antenna is designed to resonate at frequency of 5.1 GHz. From the expression 1 and 2, radius of patch (a) is found to be 8.6 cm. Usually size of substrate is taken greater than that of patch. Square substra te of 23 mm x 23 mm is used in the proposed design. Height of substrate is 1.6 mm. Ground plane at bottom of substrate has length and width same as that of substrate. Height of ground plane is actually the thickness of copper layer on bottom of substrate which is equal to 35 × 10−3mm. Microstrip patch antenna is fed through a 50 Ω impedance microstrip transmission line also known as Feedline. Width w of feedline is calculated using the expression below.

$$w = \frac{7.48 \times h}{\exp\left(Z_o \frac{\sqrt{\epsilon_r + 1.41}}{87}\right)} - 1.25 \times t \quad (3)$$

where,

t - height or thickness of copper in feedline

Z_o - Impedance of feedline

h - height of substrate

ϵ_r - Dielectric constant of substrate

For a 50 Ω feedline using expression (3), width of line is calculated to be 2.95 mm (3 mm approx).

Basic Design

Above section describes the calculation of basic design parameters of circular microstrip patch antenna. These initial parameters are illustrated in table 1

Sr no.	Parameter	Notation	Value
1.	Frequency	f_r	5.1 GHz
2.	Patch Radius	a	8.56 mm
3.	Substrate Thickness	h	1.6 mm
4.	Copper Thickness	M_t	0.035 mm
5.	Feedline Width	W_f	2.95 mm
6.	Dielectric Constant	ϵ_r	4.4
7.	Substrate Length	L	23 mm
8.	Substrate width	W	23 mm

TABLE I
INITIAL DESIGN PARAMETERS

Using these initial design parameters, design of a simple circular patch antenna is illustrated in the figure 1. It consists of circular patch of radius a on a square substrate and a feedline of of width Wf . This designed was modelled in HFSS simulation tool. Simulation of system was carried out and results obtained are discussed below. Analysis of results obtained after simulating the basic design was carried out. Some key results that describes the performance and efficiency of the basic design are highlighted below

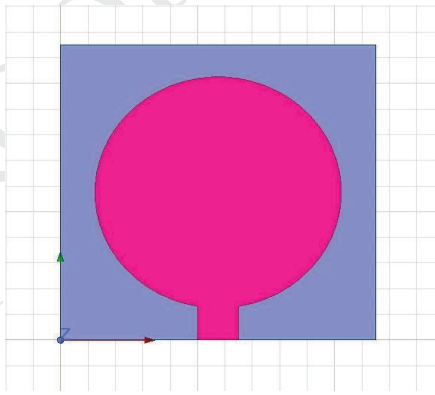


Fig. 1. Simple Patch Antenna designed in HFSS

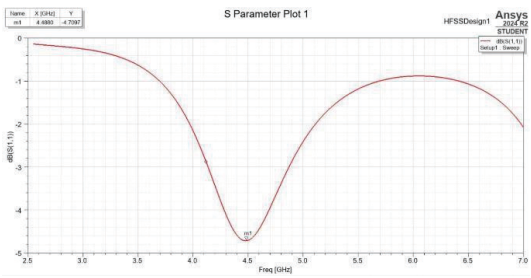


Fig. 2. Reflection Coefficient vs Frequency curve

Figure 2 illustrates the magnitude of reflection coefficient in dB plot for different frequencies. It was observed that minimum value of reflection coefficient magnitude was observed for frequency 4.4 GHz while the design was expected to resonate at frequency of 5.1 GHz. The minimum value of reflection coefficient was -4.72 dB whereas the value for a good antenna design should be atleast less than -10 dB or -15 dB

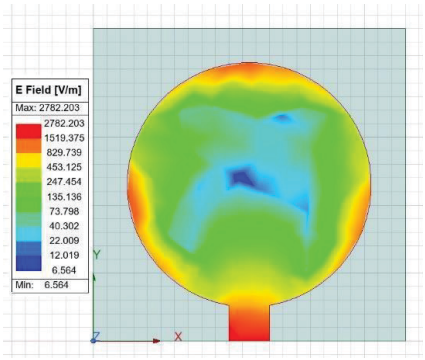


Fig. 3 E Field for Circular patch

The circular microstrip patch antenna, while effective, has some inherent drawbacks. The non-uniform electric field distribution can lead to uneven radiation and potentially unwanted side lobes, reducing radiation efficiency. A significant limitation is the narrow bandwidth typical of patch antennas, which restricts their use in wideband applications. The use of an FR4 substrate, with its high dielectric constant and loss tangent, introduces dielectric losses and supports surface wave propagation, further reducing efficiency and causing power loss. Feeding challenges, such as impedance mismatches and concentrated electric fields near the feedline, can degrade performance.

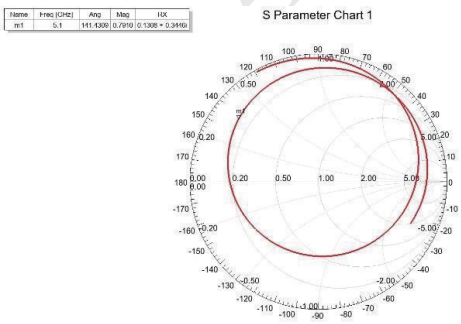


Fig. 5 Smith chart for Circular patch

Smith chart shown in figure 4, illustrates the Reactance of antenna for different frequencies. At 5.1 GHz frequency, normalized impedance of antenna was observed to be 0.1308 + j0.3446 Ω which implies the impedence of antenna is 6.54 + j17.23 whereas impedance of feedline is 50 Ω. At 5.1 GHz antennas shows inductive reactance and this inductive component of reactance need to be cancelled by adding a capacitive component to patch. This can be achieved by creating some slots perpendicular to the direction of current flow in the design of antenna

Modifications in Basic Design

Above section describes the poor results obtained by simulating the basic design of circular patch antenna. These re-improvised by making certain modifications in the basic design of antenna. These step by step modifications are briefly illustrated in this section. Lesser negative value of reflection coefficient suggest greater return loss. This is due to impedance mismatch beetween patch and feedline. According to maximum power transfer theorem, maximum power transfer from source to load takes place when load impedance is equal to source impedance. Return loss can be minimized by impedance matching of feedline and patch. For maximum power transfer the return loss should be as small as possible. This can be achieved by creating some slots perpendicular to the direction of current flow in the design of antenna. Such slots in the patch increases the electrical length for flow of current. Slots block the straight path of flow of current and forces electric current to take a longer path. Current distribution around the slot gets altered. Two slots are cut in the simple antenna design proposed earlier as shown in the figure 5. Slots were created with the aim of decreasing the return loss. Modified design was modelled in HFSS tool and simulation of modified design was carried out. When the results of simulation were analysed, following key observations were made.

The resonant frequency moved closer to the desired resonant frequency i.e 5.1 GHz. Figure 5 illustrates the magnitude of reflection coefficient in dB plot for different frequencies.

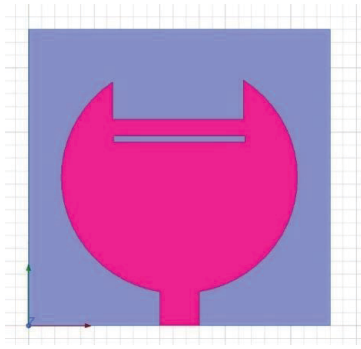


Fig. 5. Modified design I

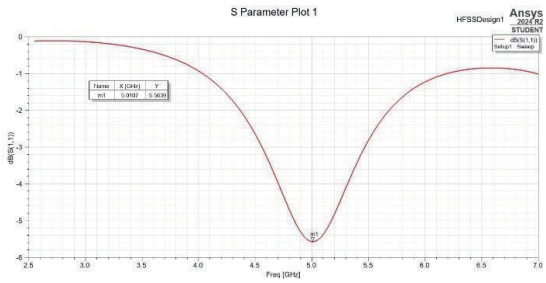


Fig. 6. Reflection Coefficient vs Frequency curve

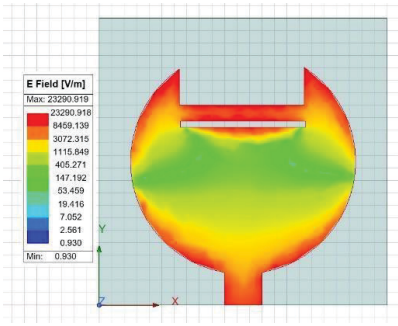


Fig. 7 E Field for Modified I

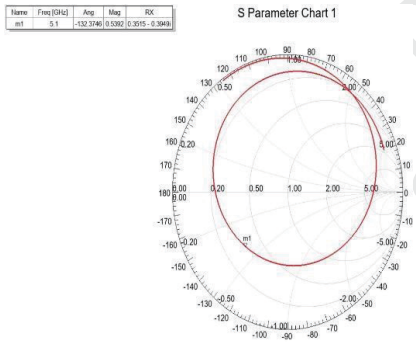


Fig. 8 Smith chart for Modified I

The minimum value of reflection coefficient magnitude was observed for frequency 5.01 GHz and the minimum value of reflection coefficient was -5.5 dB.

These results suggest that the modified design shows slightly better performance than the basic design but it further modifications are required to improvise the performance to satisfactory level

Figure 8 illustrates the smith chart for the modified antenna design. From the smith chart it was observed that at frequency of 5.1 GHz, normalized impedance of patch was observed to be 0.3515 – j0.3949 Ω which implies the impedance to be 17.575 - j19.745 Ω .Reactance of antenna was found to be capacitive in nature and some inductance was needed to cancel out the capacitive reactance component. This can be achieved by creating slots in the design along the direction of current flow. Two slots were further created in the design as shown in the figure 9

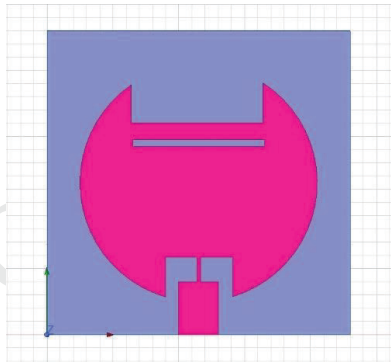


Fig. 9. Modified design II

The results obtained are illustrated here.As illustrated in figure 10 , the resonant frequency was observed at 5.1 GHz The minimum value of reflection coefficient was observed to be -24.1880 dB. From these observations it can clearly be inferred that performance of antenna has further been improved. Return loss is found to be much less in this design. Slight modification in Fig. 5.

Smith Chart Modified design II design Fig. 11 is needed to obtain resonance at the desired frequency of 5.1 GHz. Since the radius of patch a and the resonating frequency fr are inversely related to each other, in order to shift resonant frequency to left, radius of patch has to be increased slightly. Radius of patch was changed from 8.56 mm to 9 mm keeping all other parts of design same.

The resonant frequency of antenna was found to be 5.1 GHz. Minimum reflection coefficient was found to be -24.188 dB. For a good antenna, value of reflection coefficient must be lesser than -15 dB or -20 dB. Maximum gain of antenna was found to be 4.43 dBi. Thus the design obtained is quite close to the desired specifications. The final design parameters of the antenna are illustrated in the table 2. The final design of proposed antenna is as shown in the figure 9

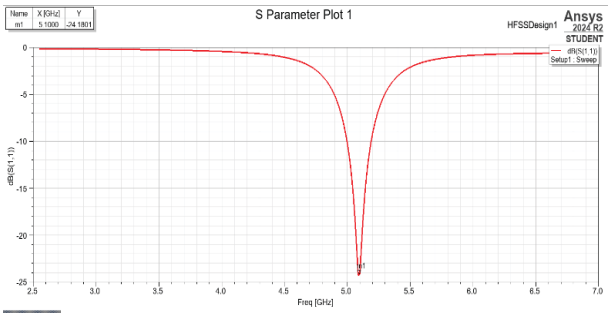


Fig. 10 Reflection Coefficient vs Frequency curve

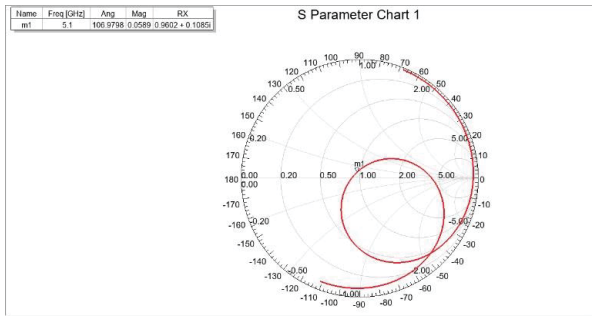


Fig. 11 Smith chart for Modified II

Figure 11 illustrates the smith chart for the modified antenna design. From the smith chart it was observed that at frequency of 5.1 GHz, normalized impedance of patch was observed to be 0.9602 – j0.1085 Ω which implies the impedance to be 48.01 – j5.425 Ω which is almost matched with the feed impedence

III. ANTENNA PERFORMANCE

Section 2 briefly describes the various aspects of the proposed antenna design and methodology for obtaining the proposed design. Performance of antenna is discussed in terms of various parameters like gain, directivity, return loss, etc. This section illustrates some of these performance parameters of proposed design.

A. *Gain (G)* : Antenna gain can be defined as the ratio of the power produced by the antenna from a far-field source on the antenna's beam axis to the power produced by a hypothetical lossless isotropic antenna, which is equally sensitive to signals from all directions. FR4 being a lossy material cannot produce a large gain. Proposed antenna design produced a maximum gain of 4.4 dBi. Thus the proposed antenna design produces a satisfactorily good amount of gain.

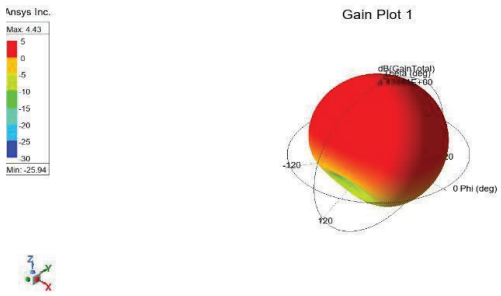


Fig. 12 3D Gain for Modified II

B. *Voltage Standing Wave Ratio (VSWR)* :The Voltage Standing Wave Ratio (VSWR) indicates the amount of mismatch between an antenna and the feed line. VSWR value ranges from 1 to ∞. A VSWR value under 2 is considered as a good value for most practical antenna applications. For a poorly matched antenna value of VSWR exceeds 2. For the proposed antenna design value of VSWR at resonant frequency is found to be 1.1 as illustrated in the figure 13.

C. *Radiation Pattern*:The Radiation pattern of the antenna represents the energy radiated by antenna in different directions. Radiation Patterns can be defined as diagrammatic representation of the distribution of radiated energy in space, as a function of direction. Radiation pattern can be 2 dimensional.Figure 14 depicts 2D radiation pattern respectively for the proposed antenna design.

D. *Reflection coefficient* : For antennas, the reflection coefficient can be defined as the figure that quantifies the amount of an electromagnetic wave that is reflected due to impedance discontinuity in the transmission medium. For an good antenna, value of reflection coefficient should be as small as possible preferably below -15 dB or even below -20 dB. For the proposed antenna design value of reflection coefficient at desired resonant frequency is found to be -24.188 dB. Figure 10 illustrates the plot of reflection coefficient

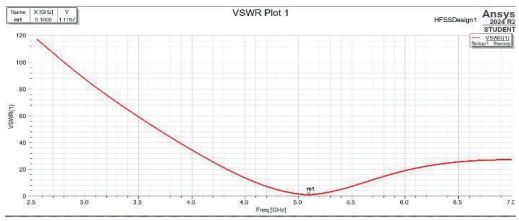


Fig. 13 VSWR

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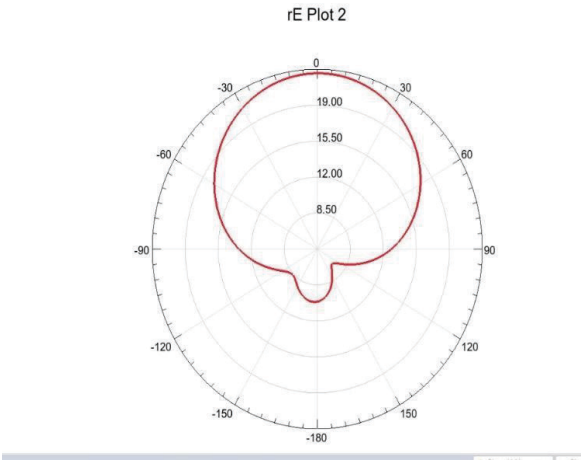


Fig. 14 Radiation pattern

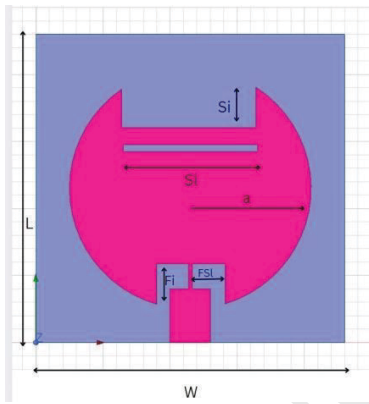
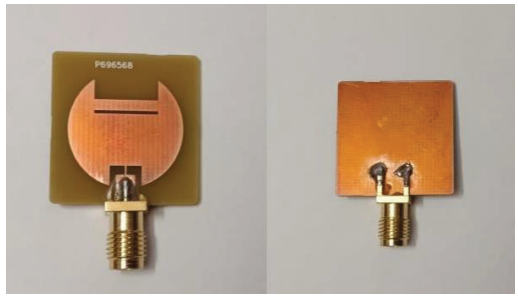


Fig. 15 Final Design

Sr no.	Parameter	Notation	Value
1.	Frequency	f_r	5.1 GHz
2.	Patch Radius	a	9 mm
3.	Substrate Thickness	h	1.6 mm
4.	Copper Thickness	M_t	0.035 mm
5.	Feedline Width	W_f	2.95 mm
6.	Dielectric Constant	ϵ_r	4.4
7.	Substrate Length	L	23 mm
8.	Substrate width	W	23 mm
9.	Slot Length	S_L	10 mm
10.	Slot Thickness	S_W	0.5 mm
11.	Slot Inset	S_i	3 mm
12.	Feedline Inset	F_i	3 mm
13.	Feedline Slot width	FS_i	2.3 mm

TABLE II
FINAL DESIGN PARAMETERS

IV. FABRICATION AND TESTING



(a) (b)

Fig. 16 Fabricated Antenna
(a)front view (b)back view

The antenna design was converted to a Gerber file and sent to a trusted fabricator for manufacturing. After fabrication, the SMA connector was carefully soldered onto the antenna to ensure a strong connection. This step was crucial for maintaining signal integrity and proper RF performance.

To verify the performance of the fabricated antenna, a Vector Network Analyzer (VNA) was used to measure

Return Loss (S11): The measured S11 parameter showed a significant dip at the designed resonant frequency, confirming proper impedance matching and minimal reflection losses.

The readings were recorded, and a comparison between the simulated and measured results was plotted using MATLAB. The analysis confirmed that the fabricated antenna closely follows the expected design performance, validating the accuracy of the simulation model.

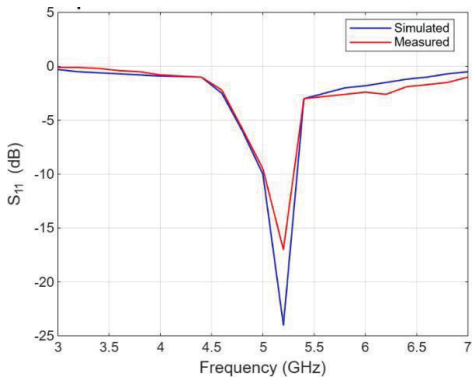


Fig. 17 Comparison of Simulated and Measured Return Loss

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Frequency (GHz)	Simulated Return loss	Measured Return loss
3.0	-0.3	-0.2
3.2	-0.5	-0.3
3.4	-0.6	-0.5
3.6	-0.7	-0.6
3.8	-0.8	-0.7
4.0	-0.9	-0.8
4.2	-0.95	-0.9
4.4	-1.0	-1.0
4.6	-2.5	-2.2
4.8	-6.0	-5.8
5.0	-10.0	-9.5
5.2	-24.0	-17.0
5.4	-3.0	-3.2
5.6	-2.5	-2.8
5.8	-2.0	-2.5
6.0	-1.8	-2.2
6.2	-1.5	-1.8
6.4	-1.2	-1.5
6.6	-1.0	-1.2
6.8	-0.7	-1.0
7.0	-0.5	-0.8

TABLE III
Comparison of Simulated and Measured Return Loss

ACKNOWLEDGMENT

We would like to express heartfelt gratitude to our Guide Ms. B. Harshitha, Assistant Professor, Department of Electronics and Communication Engineering, BMS College of Engineering, for her invaluable guidance, continuous support, and encouragement throughout this work.

Her insights and mentorship have been instrumental in shaping this research

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Neuron Spiking Implementation using the Izhikevich Model on Hardware and Simulation Platform

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Abstract—**This paper presents a hybrid simulation and hardware-based approach for implementing biologically realistic spiking neuron models using the Izhikevich framework. In response to the growing demand for real-time, low-power neuromorphic computing platforms, we propose the Neuromorphic Intelligent Architecture (NIA) — a scalable, brain-inspired system integrating both MATLAB-based simulation and Arduino-driven hardware prototyping. The simulation phase involves modeling various neuronal behaviors such as regular spiking, bursting, and fast spiking using tuned parameters in the Izhikevich model. For physical realization, we designed a custom PCB named *Spiker*, which utilizes an Arduino Nano to simulate spiking neuron activity in response to analog and digital inputs. The system provides real-time visualization of neuronal behavior through LEDs, buzzers, and serial oscilloscope outputs. Experimental results validate the biological plausibility of the simulated and hardware-generated spike patterns. This project serves as a stepping stone toward implementing larger-scale spiking neural networks on FPGA platforms, with applications in robotics, adaptive control, and brain-inspired learning systems..**

Keywords— *Izhikevich neuron, neuromorphic computing, spiking neural network (SNN), FPGA implementation, MATLAB simulation, Arduino-based hardware, real-time neuron modeling*

I. Introduction

In recent years, the demand for energy-efficient, real-time, and intelligent computing systems has increased significantly, especially in fields such as robotics, autonomous systems, and brain-machine interfaces. Traditional computing platforms based on the von Neumann architecture are not well suited for tasks that require parallel processing and adaptive learning due to the inherent limitations of the "von Neumann bottleneck" — the separation of memory and processing units. This bottleneck results in high latency and energy inefficiency, making conventional architectures unsuitable for biologically inspired, event-driven computing.

To overcome these challenges, neuromorphic computing has emerged as a promising paradigm that draws inspiration from the functioning of the human brain. Unlike conventional digital systems, neuromorphic systems use spiking neural networks (SNNs) that process information using discrete spikes, similar to the way biological neurons communicate. These systems are inherently event-driven, massively parallel, and low-power.

One of the widely used neuron models in neuromorphic research is the Izhikevich model. It provides an ideal balance between biological realism and computational efficiency. By tuning a small set of parameters, the model can replicate a wide variety of neuronal firing patterns such as regular spiking, fast spiking, bursting, and thalamocortical relay modes.

In this project, we propose a hybrid implementation approach named Neuromorphic Intelligent Architecture (NIA). It combines software-based simulations in MATLAB with a custom Arduino-based hardware prototype named *Spiker*. The MATLAB simulations are used to study the spiking behavior of different neuron types, while the *Spiker* board emulates those behaviors in real-time using analog and digital components. This work serves as a low-cost, educational, and research-friendly platform for exploring neuromorphic computing in both simulated and physical domains.

II. Literature Review

There has been a growing interest in developing accessible and efficient platforms for understanding and implementing spiking neural networks (SNNs). Several notable contributions have paved the way for educational, research, and industrial advancements in neuromorphic computing.

T. Baden et al. [1] introduced *Spikeling*, a low-cost hardware platform that simulates a spiking neuron for educational use. Designed around the Izhikevich model, Spikeling offers real-time response and interaction, making it ideal for hands-on neuroscience education.

Building on the need for accessible tools, F. Bianchi et al. [2] proposed the use of microcontroller-based SNN platforms in resource-constrained environments. Their work emphasized the importance of low-cost, modular designs to bring computational neuroscience to a broader academic audience.

M. Chen and L. Wang [3] presented *NeuroDuino*, another Arduino-based neuron simulator for classroom use. Their system enables the exploration of neuron dynamics and provides a flexible platform for teaching spike-based processing.

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A. Rodriguez et al. [4] focused on implementing the Izhikevich model on microcontrollers to demonstrate the feasibility of real-time biologically realistic neuron simulations on low-power hardware.

More recently, R. Zhang et al. [5] developed an open-source hardware platform for SNNs aimed at interactive learning. Their design supports customization and real-time experimentation with neuron models.

In terms of industrial research, M. Davies et al. [6] introduced *Loihi*, a neuromorphic manycore processor by Intel. Loihi supports asynchronous, event-driven computation and on-chip learning using spike-timing-dependent plasticity (STDP), making it highly efficient for large-scale SNNs.

Similarly, S. B. Furber et al. [7] created *SpiNNaker*, a massively parallel digital architecture based on ARM cores, which supports real-time large-scale SNN simulations and biological plausibility.

E. M. Izhikevich [8] proposed a simple, yet biologically accurate model capable of reproducing a wide range of neuronal firing patterns using only two differential equations. This model strikes a critical balance between realism and efficiency, making it ideal for hardware implementations.

Advancing into physical computation, H. Wang et al. [9] explored the use of memristor-based architectures to achieve in-memory spiking computation, improving energy efficiency and integration density.

Finally, X. Yang et al. [10] demonstrated the FPGA implementation of the Izhikevich model, showcasing its potential for real-time, low-latency SNN operation in robotics and embedded systems.

These developments highlight the evolution of SNN platforms — from educational tools to industrial-scale neuromorphic processors — and form the foundation for the Neuromorphic Intelligent Architecture (NIA) proposed in this work.

III. Problem Statement and Objective

Modern artificial intelligence and embedded systems demand real-time, parallel, and adaptive computation capabilities. However, traditional computing architectures based on the von Neumann model face inherent limitations due to the separation of memory and processing units — a phenomenon commonly referred to as the "von Neumann bottleneck." This results in latency, increased power consumption, and limited scalability when simulating complex neural systems or real-time robotic applications.

Furthermore, many educational and experimental platforms lack the flexibility to both simulate and physically demonstrate biologically realistic neuron models. While high-end neuromorphic chips like Loihi and SpiNNaker are powerful, they are expensive and not easily accessible to students or small research labs. Therefore, there is a pressing need for a low-cost, scalable, and biologically inspired system that can bridge the gap between software simulation and real-world hardware-based spiking neural networks.

The primary objectives of this project are:

- To develop a hybrid neuromorphic platform called Neuromorphic Intelligent Architecture (NIA) that supports biologically realistic neuron modeling.
- To simulate various neuron spiking behaviors using the Izhikevich model in MATLAB for accurate visualization and analysis.
- To design and implement a custom hardware prototype named Spiker, using an Arduino Nano to reproduce real-time spiking behavior through sensory inputs and outputs (LEDs, buzzers, serial data).
- To validate the hardware output by comparing it with software simulations, ensuring fidelity to biological neuron dynamics.
- To lay the groundwork for future FPGA-based implementation using HDL for real-time, scalable, and low-power spiking neural networks.

IV. Methodology

This project was carried out in two primary stages. These stages together demonstrate both theoretical and practical implementation of spiking neural networks.

(i) software-based simulation of spiking neurons using the Izhikevich model in MATLAB

(ii) real-time hardware prototyping using a custom-designed Arduino-based system named *Spiker*.

A. MATLAB Simulation of Izhikevich Neurons

In the simulation phase, we implemented the Izhikevich neuron model using MATLAB to study various spiking behaviors by tuning its four parameters: a, b, c, and d.

The model is governed by two differential equations:

1. Membrane Potential Equation:

$$\frac{dv}{dt} = 0.04v^2 + 5v + 140 - u + I$$

2. Recovery Variable Equation:

$$\frac{du}{dt} = a(bv - u)$$

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Parameter Descriptions:

The parameters and variables used in the Izhikevich model are defined as follows:

- **v** – Membrane potential of the neuron
- **u** – Recovery variable that governs the adaptation behavior of the neuron's response.
- **I** – External input or current applied to the neuron model.
- **a** – Controls the time scale of the recovery variable *u*.
- **b** – Determines the sensitivity of *u* to the membrane potential *v*.
- **c** – Reset value of the membrane potential *v* after a spike occurs

Using appropriate values for the parameters, we generated the following neuron behaviors:

TABLE I

Neuron Firing Patterns	a	b	c	d
Regular Spiking	0.02	0.2	-65	8
Fast Spiking	0.1	0.2	-65	2
Bursting Neurons	0.02	0.25	-55	0.05
Thalamo-Cortical Relay	0.08	0.25	-65	2

These models were simulated under different input currents to generate membrane potential traces. The output plots showed biologically realistic spike Using appropriate values for the parameters, we generated the following neuron behaviors:

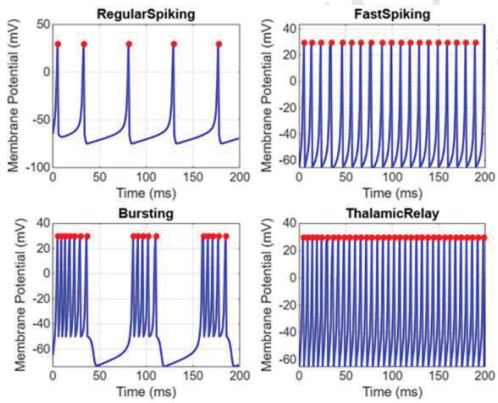


Figure 1: MATLAB simulation of various spiking patterns

B. Hardware Implementation Using Spiker

To translate the simulations into a physical system, we developed a compact Arduino-based spiking neuron prototype called **Spiker**. It was designed as a low-cost neuromorphic demonstrator using:

- **Arduino Nano** as the processing unit
- **Photodiode** as a light-based stimulus input
- **LED** and **Buzzer** as spike indicators
- **Potentiometers** for input current, gain, and noise control
- **BNC ports** for analog and digital interfacing
- **RC filter** for converting PWM to analog membrane voltage output

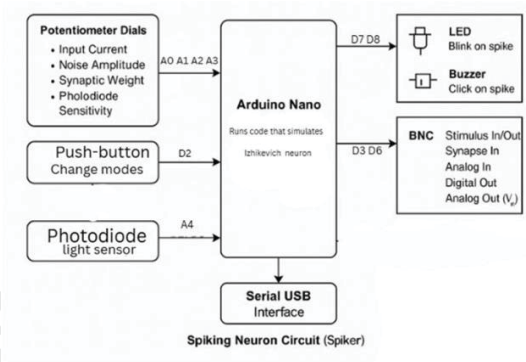


Figure 2: Conceptual block diagram of Spiker hardware

C. Custom PCB Design and Fabrication

The Spiker board was fabricated using a two-layer PCB layout created in Autodesk Eagle. Key design strategies included:

- Separation of analog and digital zones
- Proper decoupling and grounding for noise reduction
- Use of RC filtering for smooth analog Vm output
- BNC connectivity for chaining multiple Spiker units

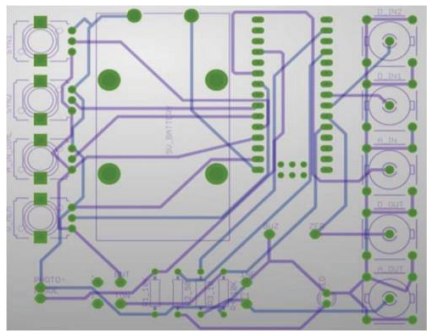


Figure 3: PCB top and bottom layer views

D. Functional Flow

1. The potentiometers adjust input current (I), synaptic gain, and noise level.
2. The Arduino simulates the Izhikevich model in real-time.
3. When a spike occurs, it:
    - Flashes the LED
    - Clicks the buzzer
    - Sends TTL output and membrane voltage through PWM
4. Data is logged to a PC for visualization via Serial Oscilloscope.

This setup allows live demonstration of neuron dynamics and interaction between multiple hardware neurons.

V. Results and Disscussions

The hardware validation of the proposed Spiker board was carried out through multiple test cases involving variable input conditions, sensory stimuli, and real-time parameter tuning. The Arduino-based Spiker board successfully simulated biologically realistic spiking behavior using the Izhikevich model. The outputs were observed using onboard indicators such as LED flashes, buzzer clicks, serial oscilloscope plots, and TTL output signals.

Before evaluating the functional performance of the Spiker board, the hardware was fabricated, assembled, and visually inspected for structural and electrical correctness. The Printed Circuit Board (PCB) was custom designed as a compact, double-layer layout with clearly separated analog and digital domains.

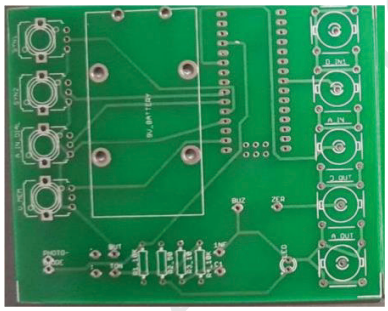


Figure 4: shows the fabricated double-sided PCB for the Spiker neuromorphic platform. The layout includes headers for Arduino Nano, potentiometer dials, photodiode input, LED/buzzer outputs, and BNC connectors for analog/digital I/O.

To validate physical operation, the assembled board was tested in both non-powered and powered states. In the non-powered state, component placement and routing continuity were verified.



Figure 5 shows the assembled Spiker board with no power applied.

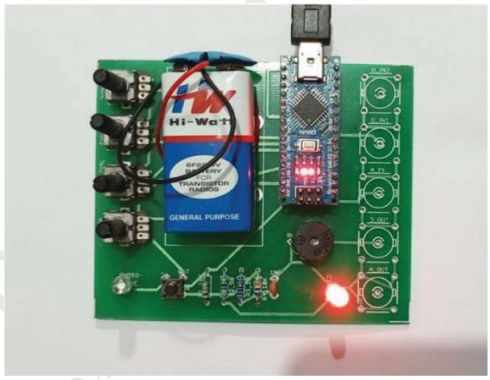


Figure 6 shows the same board powered ON via USB and battery, where the LED indicator confirms active operation and readiness for real-time spiking output.

These visual validations confirm that the board was successfully fabricated and is operational, serving as a reliable hardware platform for conducting the following experiments on spiking behavior.

A. Regular Spiking Behavior

Regular Spiking (RS) is characterized by evenly spaced, periodic spikes generated in response to a constant input current. This firing pattern is commonly observed in excitatory pyramidal neurons of the cerebral cortex and plays a crucial role in learning and signal transmission.

On the Spiker hardware, this behavior was reproduced by applying a steady baseline input current using Dial 1 (Input Current). The neuron exhibited stable tonic firing, with sharp spikes recorded on the serial oscilloscope. Each spike was accompanied by an LED flash and a corresponding buzzer click, confirming real-time biological-like output.

This result validates the correct implementation of the Izhikevich RS model on hardware and demonstrates the board's ability to produce threshold-based periodic spiking behavior.

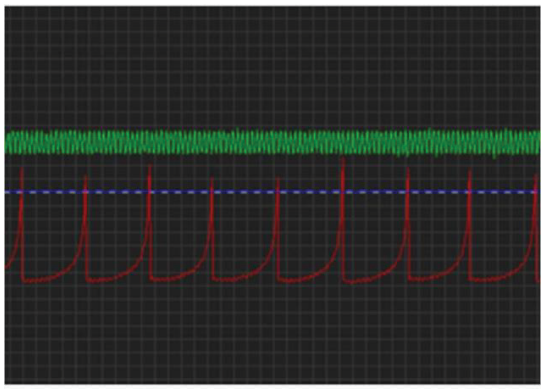


Figure 7: Serial oscilloscope output – Regular Spiking

B. Fast Spiking (FS) Behavior

Fast Spiking (FS) neurons are characterized by rapid, high-frequency firing with minimal adaptation. These neurons are found in inhibitory interneurons and are responsible for fast signal regulation and synchronization in neural circuits.

In the hardware prototype, FS behavior was simulated by turning up the noise amplitude (Dial 2)**.** This caused the neuron to fire rapidly and irregularly. The oscilloscope displayed dense spike trains, while the buzzer emitted quick successive clicks. The LED flashed at a high rate, validating that the board could replicate high-speed neural activity under stochastic conditions.

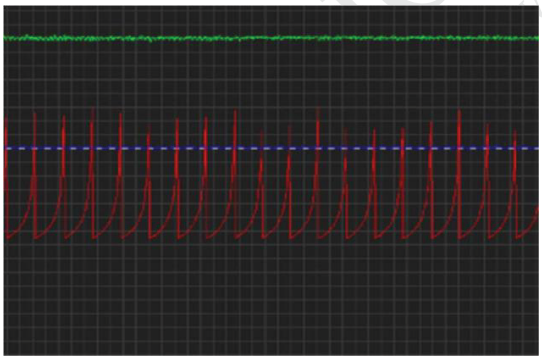


Figure 8: Serial oscilloscope output – Fast Spiking

C. Bursting Behavior

Bursting neurons exhibit clusters of spikes followed by silent intervals. These patterns are essential in biological systems for rhythmic and patterned outputs.

By tuning the Izhikevich parameters and adjusting Dial 3 (synaptic gain), the Spiker generated burst sequences. Rhythmic clusters were visible on the oscilloscope, matched by grouped buzzer clicks and LED blinks.

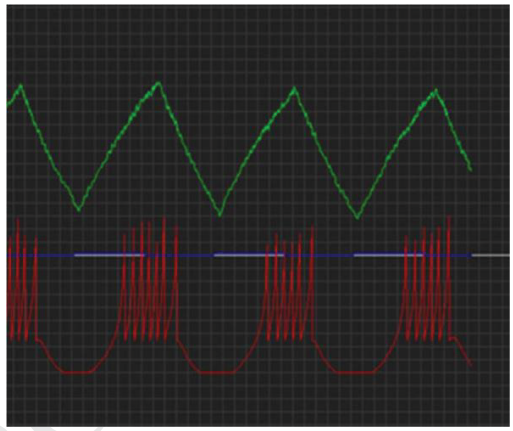


Figure 9: Serial oscilloscope output – Bursting Behavior

D. Thalamo-Cortical Relay Behavior

Thalamic relay neurons show rhythmic spikes in response to transient stimuli, such as sensory input.

With moderate current (Dial 1) and external light stimulus via the photodiode (Dial 4)**,** the Spiker responded with event-based spiking. The Vm trace on the oscilloscope showed bursts triggered by changing light intensity.

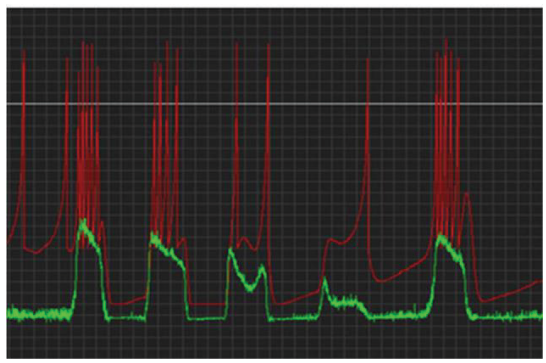


Figure 10**:** Serial oscilloscope output – Response to Photodiode Light Stimulus

VI. Conclusion

In this project, we successfully developed and tested a low-cost, real-time neuromorphic hardware prototype named Spiker, which simulates the behavior of biological neurons using the Izhikevich spiking neuron model. The system was designed using an Arduino Nano and a custom-fabricated PCB, featuring adjustable inputs, sensory stimulation, and real-time outputs through LEDs, buzzers, TTL, and analog signals.

Various spiking behaviors — Regular Spiking, Fast Spiking, Bursting, and Thalamic Relay — were accurately reproduced using tuned input dials and parameters. These behaviors were validated using a serial oscilloscope, demonstrating high similarity to MATLAB simulation outputs. The photodiode integration further confirmed the board's ability to respond to external sensory stimuli in a biologically realistic manner

.Spiker successfully bridges the gap between software-based neuroscience modeling and hardware-based neuromorphic experimentation. Its low-cost, modular design makes it a valuable platform for education, research, and prototype development in the field of neuromorphic engineering.

VII. Future Research Directions

Based on the results and potential of this project, the following future extensions are proposed:

• FPGA Implementation: Transition from microcontroller-based simulation to HDL implementation on FPGA. This would support large-scale parallel spiking neuron arrays with real-time learning capability.

• SNN-Based Robotic Integration: Integrate the Spiker system into a mobile robot for performing basic sensory-motor tasks using spiking neural networks, enabling event-based control and adaptive decision-making.

• On-Chip Learning Blocks: Add learning modules using mechanisms like Spike-Timing Dependent Plasticity (STDP) or reward-modulated Hebbian learning for real-time plasticity and network training.

• Multi-Spiker Networking: Chain multiple Spiker boards to build and study larger SNNs with recurrent connections, population coding, and distributed control systems.

• Open-Source Educational Kit: Package the hardware and codebase as an open-source neuromorphic education kit, making it accessible for colleges, hobbyists, and researchers worldwide.

VIII. Acknowlegement

We sincerely thank Mrs. Jyoti Ravikumar, Assistant Professor, Department of Electronics and Communication Engineering, BMS College of Engineering, Bengaluru, for her invaluable guidance, constant support, and encouragement throughout the duration of this project.

Her mentorship helped us better understand the concepts of neuromorphic computing and inspired us to explore the practical aspects of neuron modeling and hardware implementation.

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EMPOWERING COMMUNICATION : FPGA – based Morse Code system for differently - abled individuals

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***Abstract*— Patients with neuromuscular diseases like Amyotrophic Lateral Sclerosis (ALS), Multiple Sclerosis, or Muscular Dystrophy usually experience severe communication difficulties. This paper introduces an FPGA-based Morse code communication system that can be used to support differently-abled people. The system uses a switch input for Morse code input, which is decoded by an FPGA-based decoder and displayed on a seven-segment display. The system is developed in Verilog HDL on the Xilinx Vivado tool and runs on a Boolean board. Results show the utility of the presented system in creating an accessible, portable, and efficient communication alternative for people with disabilities.**

Keywords—Field Programmable Gate Array (FPGA), Morse Code, Verilog HDL , Xilinx Vivado, Seven-segment display

I. INTRODUCTION

Depending on the causes of their combined visual and hearing impairment, their education, and upbringing, a large number of people with deaf-blindness express themselves in a variety of ways. Differently-abled individuals express themselves in a variety of ways. Generally, the below mentioned methods are largely utilized.

- Modified signs
- Signed languages
- Tactile Sign language
- Tracing things, etc.

Dashes, dots, and spaces replace alphabetic characters, numbers, and punctuation marks in Morse code. Electrical pulses of different durations, or mechanical or visual signals, like flashing lights, can be transmitted based on the code. The aim of this project is to make the morse decoder as portable as possible by taking into account the fact that an individual with vision impairment will need encoders while communicating. Deaf or blind individuals tend to communicate solely in braille, so that there are lesser chances that their conversation partner will understand them. In such cases, a portable morse encoder may be greatly beneficial. Due to Boolean board's strong performance, the morse inputs can be assembled, deciphered, and displayed at a best-fit speed in the seven segment display, thus enabling effective communication.

This paper has numerous characteristics for visually and speech impaired individuals such as easily communicable and comprehensible to normal individuals and caretakers. Further they are also lightweight, trustworthy and can be carried to any location at any time

II. METHODS AND MATERIALS

A. Proposed Method

A simple-to-identify and simple-to-operate switch is provided for the challenged individual. The method suggested is depicted in Figure 1. From the proposed system diagram, it is evident that the switch input is used. On activation of the Morse sequence buttons, the user inputs to the system (challenged individual). Switch inputs and a clock signal offer DOT, DASH signals to the Boolean board. Morse code can be constructed and conveyed from this information. The message constructed is decoded afterwards using Vivado and the Verilog Morse decoder tool. Next, a Morse decoder is utilized, which converts state codes into hexadecimal values that appear on a seven-segment display. The program flow of the Morse Code Communicator using a Boolean board is illustrated in a flow chart (Fig 2.1).

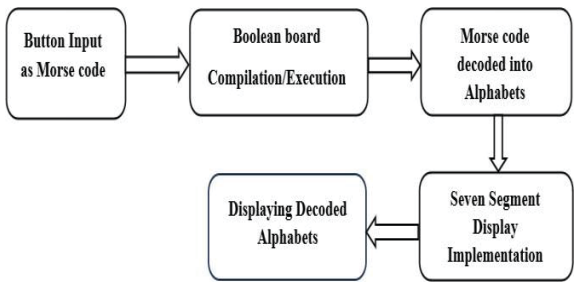


Fig.2.1 Proposed Method

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B. Morse Code

Rather than alphabetic letters, numbers and punctuation marks, dots, dashes, and spaces are employed in Morse Code. Depending upon the code, electrical pulses of varying length or mechanical or visual signals, e.g., flashing lights, can be sent.

Table 2.1 Morse code representation of Numbers

NUMBERS	SYMBOLS
0	-----
1	.----
2	..---
3	...--
4	....-
5	.....
6	-....
7	--...
8	---..
9	----.

Table 2.2 Morse code representation of Alphabets

ALPHABETS	SYMBOLS	ALPHABETS	SYMBOLS
A	.-	N	-.
B	-...	O	---
C	-.-.	P	.--.
D	-..	Q	--.-
E	.	R	.-.
F	..-.	S	...
G	--.	T	-
H	....	U	..-
I	..	V	...-
J	.---	W	.--
K	-.-	X	-..-
L	.-..	Y	-.--
M	--	Z	--..

C. Components

The Boolean board of Figure 3 facilitates it to be an easy to embed hardware design. It supports many I/O ports, switches, LEDs, and seven-segment displays, which distinguish it from other boards. To embed the hardware design, Xilinx employs either HDL to construct the software. Boolean board enables the designer to easily design their hardware module. Short circuits, open circuits, and incorrect wire connections are all options in hardware design. Consequently, we can fail to get the expected outcome and can even fail to determine where the problem is. Still, with Xilinx Boolean board, errors are immediately observed and information can be processed faster. The output is displayed with a seven-segment display and, and input is accomplished through buttons. Code dumps are available via I/O ports. Due to the above-mentioned features, Boolean board is our project's choice. Everything can be packed into one component so that deaf or vision-impaired individuals as well as their caretakers may better understand. It's easy to carry with you,and it's not hard to keep up with what they're trying to say.

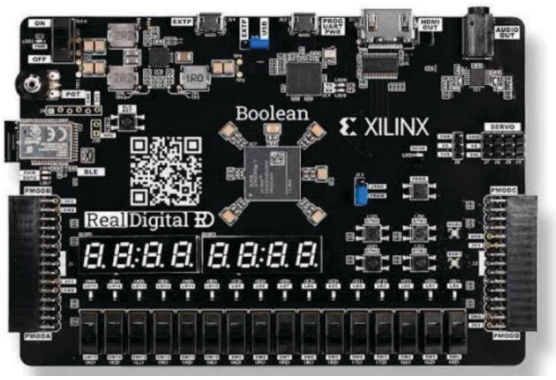


Fig. 2.2. Boolean board

The Boolean board that are being illustrated in Fig. 2.2, consist of seven segment display. The segments are capable of getting arranged to shape a rectangular form. With four seven segment screens we can show integers and alphabets with a decimal point.

It will be useful to both speech and vision impaired individuals as well as their caregivers. In order to show the alphabet one at a time, we only used one seven-segment display. Certain characters, like the letters m, k, and g, are not possible to display. Items like tea, ice, and oats, however, can be displayed very easily.

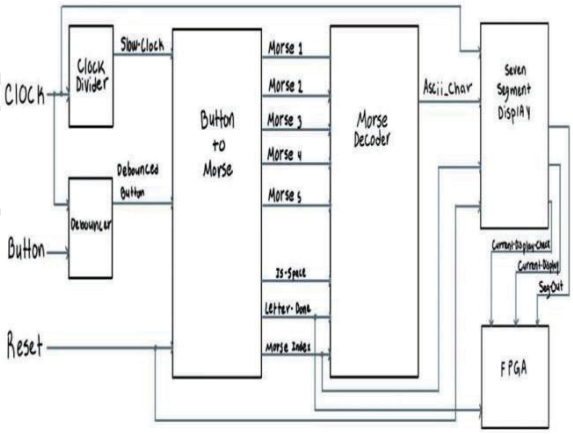


Fig. 2.3. Block Diagram

D. Proposed Algorithm

The flow chart above illustrates program flow of Morse Code Communicator embedded on Boolean board Short presses which equal to 1 clock cycle, represent dots, while longer presses which equal to 3 clock cycles represent dashes.

1. Button Press:

oWhile the button is pressed:
- The counter increments.
- The inactivity_counter resets.

o When the button is released (button transitions from high to low):
- If the press duration (counter) is:
- Short: Register as a dot (2'b01).
- Long: Register as a dash (2'b10).

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▪ The Morse symbol is stored in the current morse_index position, which then
increments.

2. Button Inactivity:

o If the button remains unpressed for a sufficient time (inactivity_counter >= three_time_units):
▪ The current Morse sequence (up to 5 symbols) is finalized and transferred to
the morse_one to morse_five outputs.
▪ The letter_done signal is asserted to indicate the letter is complete.
▪ The morse_index resets for the next letter.

3. Reset:

o All signals, counters, and registers are cleared when reset is asserted.

E. Code Analysis

a) Clock Divider:

The given Verilog code implements a clock divider module, which takes a high-frequency input clock (100 MHz) and produces a lower-frequency output clock based on selectable frequency options. Here's a breakdown:

1. clock: The 100 MHz input clock signal.

2. one_sec_unit: Signal to select a 2 Hz output clock (1-second period).

3. half_sec_unit: Signal to select a 4 Hz output clock (0.5-second period).

4. quarter_sec_unit: Signal to select an 8 Hz output clock (0.25-second period).

b) Debouncer:

The Debouncer module cleans up any noise from the button input to ensure stable signals are sent to the next stage.

1. Button to Morse:

The button_to_morse module converts the button press durations into Morse code symbols. Short presses which equal to 1 clock cycle, represent dots, while longer presses which equal to 3 clock cycles represent dashes. This module also detects when a letter is completed (letter_done). The morse_index signal tracks the position of each Morse code symbol within a letter. You can also reset the display using the reset button.

2. Morse Decoder:

The morse_decoder takes the Morse code symbols (morse_one to morse_five) and converts them into their corresponding ASCII character. It uses a binary tree traversal logic to match the sequence of dots and dashes to letters, numbers, or special characters. When a valid character is decoded, it is sent to the next stage.

3. 7 Segment Display:

The seven_seg_disp module takes the ASCII character output from the decoder and translates it into a pattern for a seven-segment display. It cycles through multiple displays to show characters sequentially, supporting up to eight characters at a time. The module shifts the active display with each new character or reset signal

III. RESULTS AND DISCUSSION

A. Vivado Schematic Diagram

Due to successful compilation of HDL codes, schematic diagram in Fig.3.1. was created by the vivado simulation tool. Synthesis, implementation, and bitstream were created successfully. To program the Boolean board, first, the bitstream is generated and then hooked up with the system. The hexadecimal output is sent to the seven-segment display.

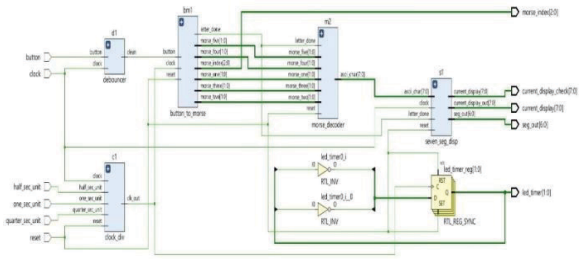


Fig. 3.1. Vivado Schematic diagram

B. Morse Code As An Effective Communication Medium

Individuals with impairments and those whose communications skills have been damaged due to strokes, heart attacks, or paralysis have employed Morse Code as an alternative means of communication. Eyelids of some individuals have been used to create dots and dashes in Morse Code through a sequence of long and rapid blinks.

Morse code is one of the most critical forms of radiocommunication in aviation, with individual codes for every aircraft and every base. Morse Code is widely used for more important and more humane purposes than a communication tool for the deaf and blind . Morse Code is a viable alternative for most communication devices for the disabled due to its seamless operation and simple syntax. Project hardware can be easily transferred and modified. After we program it, we can employ it and produce as much output as desired until it terminates. The chief drawback is in Boolean board , some letters like k, q, l and m are unable to display in seven segment display.

C. Sample Output Letters

If the visually and speech impaired individual desires ”EAT”, he tells the caretaker via the Boolean board Morse code communicator. The visually and speech impaired individual performs the following steps to type “EAT”. First, he/she inputs the Morse code for “e” which is a Single dash (“-”). Then he/she inputs the Morse code for “A” is a Single dot (“.”). Lastly, he/she inputs the Morse code for “t” that is dash (“-“).The caretaker now knows that the person desires to EAT

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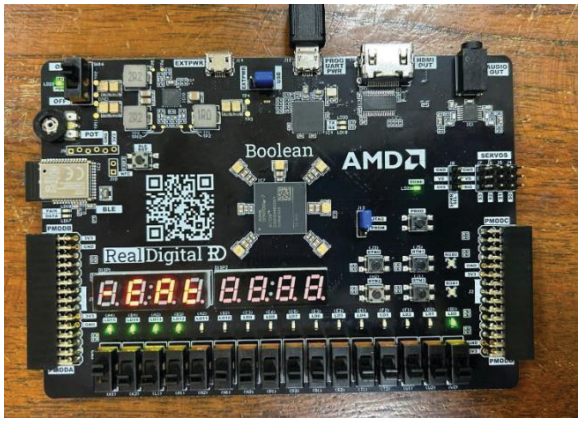


Fig.3.2 Sample Output

D. Project Discussion

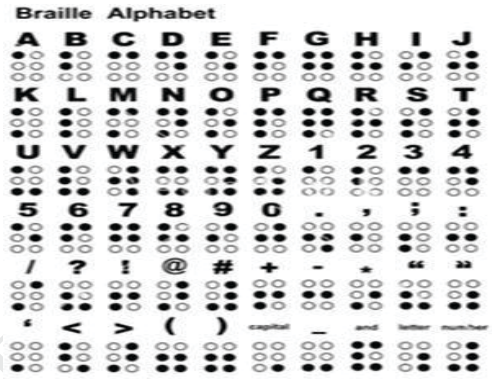
This paper has been prepared keeping in mind the contribution to be done back to the society as an electronics engineer. Therefore, under the VLSI category, while keeping in view the boards, traditional and efficient boards such as Arduino,Basys-3,PYNQ board were all taken into account because of their efficiency and perfect structure for our decoder project. But finally Boolean board was determined to be the ideal board for our project. Boolean board was chosen over the cheaper and very efficient Arduino board because Arduino is more code-oriented microprocessor domain related implementing protocol board which has more focus towards IT subjects like Internet of Things and also tending more towards micro controller domain. Even during examining the code, Arduino codes were more IT oriented than a Basys3/Boolean board. Hence keeping these points on mind, Boolean board was chosen as the primary board for the implementation of our project despite the fact that Arduino has more advantages. We wanted the project to be purely electronics based and delivering a pathway of opportunity as a steppingstone for advancements in this portable communication domain and hence decided to take up the challenge of coding and implementing entirely through Boolean board.

We took the decision of utilizing the inbuilt seven segment display of the Boolean board which is built into the board and therefore can save plenty of time during execution and can be very effective in translating the morse inputs and displaying it as a binary alphabet output .The built-in seven segment display will be utilized to show the binary output which may save time and confusion for the challenged individual and the individual they attempt to communicate with. Here efficiency of the model and the challenged individual's need for quick and instant communication is given higher importance over the opposite individual's ease of reading. Braille is touch-based system since we discussed previously.

Not everybody visually people's fingers are sensitive enough to track the matrix patterns to recognize a long word or a sentence. With the eruption of World War 1 and World War 2, lots of people especially soldiers lost not only eyesight but also for the most part because of their greeting of grenades and landmines. Individuals used to lose limbs, vision and get affected due to hearing imparities. So, examining the challenging character of the Braille system, it can be assumed that visually impaired individuals may not be comfortable learning completely with the Braille system.

E. The Need For Alternatives To Braille System

Braille system is among the most popular and employed system in the world by people who are blind to learn and comprehend alphabets through the strong sense of touch. Braille has been used extensively since it was discovered in the almost 1820s. Although Braille could be imagined to the visually impaired individuals, it also possessed some of its own drawbacks. Braille Alphabet Chart Braille alphabet (Figure. 9)chart illustrates how each alphabet/number can be represented by a 3x2 matrix where 64 combinations are possible using any of the 6 dot spaces available.



. Fig.3.3. Braille Alphabet

IV. CONCLUSION

As a result, we were successful in designing and implementing an FPGA-based Morse code communicator for blind or deaf individuals. We chose to utilize the integrated seven-segment display and Boolean board over a more standard and efficient Arduino board. HDL code is loaded onto the Boolean board by utilizing Vivado software.For the purposes of this project, the outcome of this project is that the Boolean board reads the button inputs, processes and stores them in hexadecimal arrays, and then encodes them into binary inputs that are displayed on the seven-segment display.The primary objective of our project was to show the positive contribution an electronic model communicator can have on society. Due to being a universal language with a common morse table, there are numerous communication models that have already been created for disabled people.These days, individuals are travelling extensively and exchanging with new and familiar people wherever they go.

Morse code has proven to be a good communication tool for individuals who find reading or speaking difficult. It can also be employed to communicate with individuals who cannot speak, write or type because medical problems. The system described in this research facilitates communication. Since every character can be translated into a pre-specified series of dots and dashes, Morse code has been shown to be the most efficient way to convey alphanumeric data to a third party. The output message of the simulation is shown on a seven-segment display.

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The simulation was coded using the Boolean board kit. It is an easy and versatile method to transmit text messages via wireless media .In this method, the individuals who find it

hard to communicate simply has to enter the dots or dashes, and the decoding program on Boolean board will show verbal output on a seven-segment display once it is executed. When every character is mapped, Morse code has been demonstrated to be the most effective technique of communicating with a third person. As a result, the Boolean board kit was used to create a very effective and portable morse code decoder.

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5 STAGE PIPELINED MIPS PROCESSOR WITH CUSTOM DATA FORWARDING UNIT

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Abstract: **This project involves the design, simulation, and verification of a 5-stage pipelined MIPS processor that adheres to classic RISC principles. The processor consists of five sequential pipeline stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Pipelining enhances throughput by allowing multiple instructions to be processed simultaneously at different stages. A key focus of the implementation is the handling of data hazards using a Forwarding Unit, which dynamically routes data from intermediate stages (EX/MEM or MEM/WB) to resolve instruction dependencies without stalling the pipeline. Additionally, a Hazard Detection Unit identifies cases such as load-use hazards where forwarding is insufficient and inserts stalls accordingly. The processor supports a rich subset of MIPS instructions, including arithmetic, logical, load/store, and branch operations. The entire design is written in Verilog HDL and verified through simulations using tools like ModelSim. Waveform analysis validates the correct operation of the pipeline and hazard resolution mechanisms. The design demonstrates improved performance through reduced average cycles per instruction (CPI) and serves as a solid foundation for exploring advanced concepts like superscalar execution, out-of-order execution, and speculative branching. Its modular and scalable nature also allows for future enhancements, including cache integration and multi-core support.**

List of Abbreviations

Abbreviations	Full Form
MIPS	Microprocessor without Interlocked Pipeline Stages
IEEE	Institute of Electrical and Electronics Engineers
IF	Instruction Fetch
MEM	Memory Access
ID	Instruction Decode
WB	Write Back
FPGA	Field Programmable Gate Array

I. INTRODUCTION

In modern computing, processor performance is key to the efficiency and speed of digital systems. Instruction pipelining is a powerful architectural technique that enhances performance by overlapping the execution of multiple instructions. The MIPS (Microprocessor without Interlocked Pipeline Stages) architecture, a classic RISC model, effectively utilizes pipelining to boost throughput while maintaining simplicity. The 5-stage MIPS pipeline includes Instruction Fetch, Instruction Decode/Register Fetch, Execution, Memory Access, and Write Back. While pipelining increases parallelism, it introduces hazards—especially data hazards, which arise from instruction dependencies. This project addresses such hazards using a Forwarding Unit that detects dependencies and forwards data from later to earlier stages, reducing stalls. For unresolved cases like load-use hazards, a Hazard Detection Unit inserts NOPs to maintain correctness. The processor is implemented in Verilog HDL and verified through simulation on FPGA platforms. Carefully crafted test sequences validate the hazard resolution logic. Simulation analysis confirms improved efficiency with fewer stalls and higher instruction throughput.

II. LITERATURE SURVEY

This paper presents a 32-bit MIPS-based RISC processor using a 5-stage pipeline with Verilog HDL. It focuses on resolving data hazards using a Data Forwarding Unit and Hazard Detection Unit. The processor is simulated in ModelSim and synthesized using Cadence Genus, optimized for power, area, and delay.
Result: Low power (23.31 mW), minimal stalls, and high efficiency make it suitable for embedded systems. [1]
This FPGA-based 32-bit pipelined MIPS processor introduces a modified forwarding unit to better handle back-to-back data hazards. It is implemented on a Virtex Ultra Scale FPGA using Xilinx Vivado, focusing on area and power optimization.
Result: Achieved 0.999 W power consumption with minimal stalls, ideal for power-constrained embedded systems. [2]
This work emphasizes verification of a 5-stage 32-bit MIPS processor using Universal Verification Methodology (UVM). A scoreboard module ensures output correctness by comparing expected and actual results.
Result: The study confirms accurate pipeline behavior and efficient hazard handling using UVM, highlighting modular and reusable verification practices. [3]

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Proposes a MIPS processor with dynamic pipelining (switches between 4-stage and 5-stage) and a thermal management unit. The design improves power and thermal efficiency using dynamic frequency scaling and clock gating.
Result: Achieved 36.74% execution time improvement, reduced power use, and better thermal stability for performance-critical applications [4]
This survey analyzes multiple pipelined RISC processor designs, focusing on implementation strategies, hazard resolution techniques, and optimization goals.
Result: Identified that integrating a forwarding unit and optimizing control logic significantly reduces stalls and improves clock cycles per instruction (CPI). The study also concludes that Verilog-based designs with modular architecture are more scalable and FPGA-friendly. [5]
Describes a 5-stage 32-bit MIPS processor with hazard detection and a data forwarding mechanism. Emphasis is placed on reducing switching activity to save power.
Result: Achieved a significant reduction in dynamic power consumption (~35%) compared to traditional MIPS designs, while maintaining pipeline performance on Spartan-3E FPGA. [6]
A MIPS processor integrated with Triple-DES cryptographic functionality using a pipelined structure for secure computing.
Result: Achieved high throughput (209 MHz clock speed) and efficient encryption/decryption cycles, proving useful for embedded security applications in real-time systems. [7]
Presents a Verilog-based 32-bit RISC-V processor with a 5-stage pipeline, supporting hazard detection and resolution for all instruction types.
Result: Simulation on FPGA showed correct execution of instructions with data and control hazards resolved using forwarding, stalling, and branch prediction techniques. Design proved robust and extensible for academic and commercial applications. [8]
Extends the traditional MIPS pipeline to six stages to support 64-bit data paths, using VHDL for FPGA implementation.
Result: Showed a 12% improvement in execution speed and better timing closure compared to standard 5-stage 32-bit designs. Demonstrated viability of deeper pipelines for higher performance systems. [9]
In-depth explanation of pipeline hazards and resolution techniques in MIPS-style architectures including RAW, WAR, WAW dependencies.
Result: Educational simulations and theoretical analysis confirm that forwarding combined with hazard detection logic effectively maintains pipeline throughput with minimal stalls.[10]

III. METHODOLOGY AND IMPLEMENTATION

The implementation of the 5-stage pipelined MIPS processor is carried out in a modular and systematic approach, ensuring clarity in design and ease of debugging. The methodology begins with the architectural design of each individual pipeline stage—Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Access (MEM), and Write Back (WB). Each stage is developed independently to handle a specific part of the instruction lifecycle, promoting a clean separation of functionality and aiding in the verification process.

Control units are essential components of this design. The Main Control Unit decodes instruction types and generates control signals, while the ALU Control Unit determines the specific operation the ALU should perform. To address data hazards and ensure uninterrupted execution, a Forwarding Unit and a Hazard Detection Unit are implemented. The Forwarding Unit dynamically reroutes data from later pipeline stages to earlier ones to resolve register dependencies, and the Hazard Detection Unit inserts NOPs (stalls) in the pipeline when forwarding cannot resolve hazards conflicts.

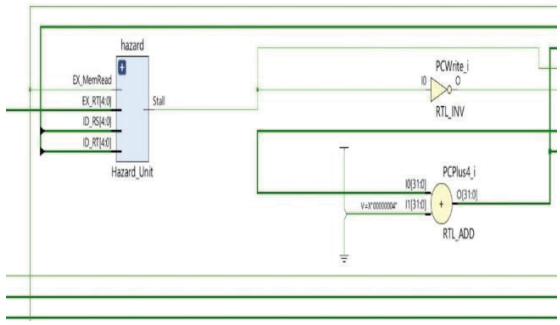


Fig 1. Hazard unit

The data path is constructed by connecting various hardware components—such as the ALU, multiplexers, register file, instruction memory, and data memory—using appropriate control signals. Multiplexers, in particular, are controlled by the Forwarding Unit to select correct operand sources during execution. This ensures that ALU operations are performed with valid and up-to-date data, even when the values are not yet written back to the register file.
Each module in the processor is implemented in Verilog HDL, a widely used hardware description language suitable for both simulation and synthesis. By designing modules in Verilog, the processor can be verified using simulation tools like ModelSim and synthesized for FPGA or ASIC deployment. Simulation testbenches are developed to apply various instruction sequences and validate pipeline behaviour under different conditions, including hazard scenarios and branching.
The behaviour of each pipeline stage is as follows: The **Instruction** Fetch (IF) stage fetches instructions from memory and increments the Program Counter (PC). The output is passed to the Instruction Decode (ID) stage through the IF/ID register. The ID stage decodes the instruction, fetches operands from the register file, and generates control signals using the Control Unit. The information is stored in the ID/EX register.
In the Execution (EX) stage, the ALU performs arithmetic or logic operations, and effective memory addresses are calculated for load/store instructions. This stage relies on multiplexers and the Forwarding Unit to ensure that correct operands are used, avoiding stalls due to data dependencies. The output is forwarded to the Memory Access (MEM) stage, where memory read/write operations take place using the ALU-generated address. The final results are transferred to the Write Back (WB) stage through the MEM/WB register.
In the WB stage, the results from the ALU or data memory are written back to the destination register in the register file, completing the instruction execution. Together, these stages form a complete instruction pipeline, capable of processing multiple instructions simultaneously while maintaining data integrity and control flow.
The integration of Forwarding and Hazard Detection Units significantly enhances the efficiency of the pipeline by minimizing unnecessary stalls and ensuring accurate data usage. This organized, modular pipeline structure not only ensures correct execution of instructions but also provides a strong foundation for future extensions like branch prediction, cache integration, or even superscalar design.

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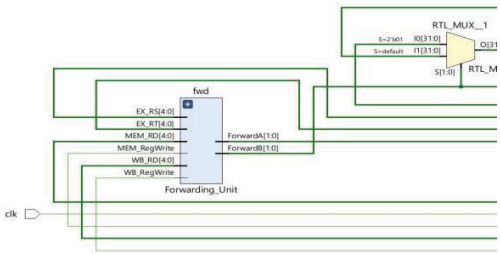


Fig 2. Forword block

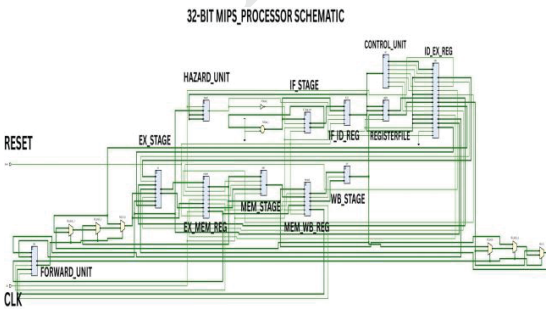
To minimize performance penalties from pipeline stalls in a 5-stage MIPS processor, a Forwarding Unit is used to resolve data hazards by supplying operands from intermediate pipeline stages (EX/MEM or MEM/WB) instead of waiting for write-back. It enables data forwarding by generating control signals that guide multiplexers in the EX stage to select the correct operand source, improving instruction throughput. However, for load-use hazards, where a load instruction is followed by an instruction needing the loaded data, forwarding isn't sufficient. In such cases, a Hazard Detection Unit introduces a stall by freezing the Program Counter (PC) and IF/ID register, and inserts a NOP to delay the dependent instruction. This is managed using logic that disables PCWrite and IF_ID_Write while enabling ControlStall when such a hazard is detected. Once resolved, normal pipeline flow resumes. This combination of forwarding and selective stalling maintains data accuracy while reducing performance loss due to hazards.

IV. RESULTS AND DISCUSSION

A. RESULTS

The simulation of the 5-stage pipelined MIPS processor with integrated hazard control and forwarding mechanisms was performed to assess its efficiency in handling data hazards. A specific instruction sequence was chosen to intentionally create a load-use hazard, where an instruction requires data that has just been loaded into a register by the previous instruction. This setup allows for a focused evaluation of how well the processor resolves such hazards while maintaining smooth pipeline execution. The third instruction in the sequence was included to test the correctness of memory store operations and to observe overall pipeline behavior under concurrent execution.

Schematic



Output waveform



B. DISCUSSIONS

1. Insights and Impacts:

1.1 Waveform Analysis and Observations:

1. All five pipeline stages—Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB)—function correctly and concurrently in the simulation.

2. The arithmetic instruction that follows the load is dependent on the value being fetched. The hazard detection unit successfully identifies this load-use hazard and introduces a one-cycle stall to ensure the correct value is used, thereby preventing incorrect computation.

3. The forwarding unit actively resolves data hazards involving ALU-to-ALU operations by forwarding data from intermediate pipeline stages to avoid unnecessary stalls, though it cannot resolve load-use hazards alone.

4. The ALU operation is validated to be accurate, as the result in the destination register matches the expected output, confirming proper instruction decoding and execution.

5. The store instruction executes correctly, verifying the integrity of memory access and write operations in the MEM stage.

Performance Highlights:

1. The hazard detection unit effectively introduces minimal stalls only when absolutely necessary, such as in load-use hazards.

2. The forwarding unit significantly improves performance by eliminating pipeline stalls in other dependent instruction scenarios.

3. The simulation confirms consistent and correct ALU outputs, reinforcing the accuracy of pipeline execution.

4. Even in the presence of hazards, the processor maintains a steady instruction flow, with no propagation of multiple bubbles, showcasing its efficiency and reliability.

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This simulation validates that the pipelined MIPS processor behaves as expected under hazard conditions. It demonstrates accurate detection and resolution of data hazards, efficient forwarding of data, and correct execution of instructions across all pipeline stages. The combined use of a forwarding unit and hazard detection unit leads to improved performance and reliability, confirming the processor's suitability for practical

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embedded applications and educational use. 2.1.2. Lack of Dynamic Channel Adaptation: It does not account for dynamic channel variations commonly experienced in wireless environments, impacting reliability.

Load-Use Hazard Management: When the add instruction attempts to use a register recently updated by a lw instruction, the hazard detection unit intervenes. It temporarily halts the pipeline by disabling updates to the PC and IF/ID register, effectively inserting a NOP to prevent incorrect execution.

Forwarding Unit Activity: For other cases, such as ALU-to-ALU dependencies where the result is already available in EX/MEM or MEM/WB stages, the forwarding unit reroutes data to the ALU inputs without stalling the pipeline. This dynamic behavior greatly reduces delays in instruction flow.

Instruction Synchronization: The forwarding logic ensures that dependencies are resolved inline, maintaining proper data flow without triggering unnecessary hazards.

Control Signal Handling: Control signals for branching, memory operations, and arithmetic instructions are accurately propagated and appropriately controlled at each stage, avoiding misinterpretation or early execution.

V. Conclusion and Future trends

A CONCLUSION

The implementation and simulation of the 5-stage pipelined MIPS processor demonstrate a robust and efficient design that effectively balances instruction-level parallelism with hazard control. The processor faithfully follows the RISC pipeline architecture, dividing execution into five stages — Instruction Fetch, Decode, Execute, Memory Access, and Write Back — and successfully overlaps these stages to improve throughput.

Through deliberate insertion of data hazards, particularly the load-use hazard, the simulation validates the effectiveness of the Hazard Detection Unit, which introduces precise stalls only when necessary, ensuring correct program behavior. At the same time, the Forwarding Unit proves instrumental in resolving most RAW (Read After Write) hazards without introducing pipeline stalls, allowing instructions to execute back-to-back with minimal delay. Together, these two units maintain correct data flow and significantly reduce the performance penalties typically associated with pipeline hazards.

The waveform analysis further confirms the correct functioning of all pipeline stages, control signals, and arithmetic logic, while ensuring data values are computed and written back accurately. The ALU outputs match expected values, register updates occur at the correct cycles, and instruction flow is smooth across all stages — even in the presence of hazards.

Performance observations show that the processor handles hazards efficiently and avoids unnecessary bubbles, demonstrating that the design is well-optimized in terms of control logic and pipeline synchronization. The simulation confirms that instruction throughput remains high, stalls are minimal, and all operations are performed without error.

Overall, this project successfully implements a realistic and educational model of a pipelined MIPS processor with hazard detection and forwarding capabilities. It lays a strong foundation for understanding the internal mechanisms of modern CPUs and serves as a scalable base for advanced architectural features like branch prediction, cache integration, or out-of-order execution. The results validate both the functional correctness and performance efficiency of the processor, making it highly suitable for embedded system applications and academic learning.

B. FUTURE TRENDS

As computing demands continue to evolve, future pipelined processors are expected to move beyond traditional in-order designs like the classic MIPS architecture. These enhancements aim to improve instruction-level parallelism, reduce hazards, and increase power efficiency. Emerging techniques in microarchitecture, power management, and intelligent scheduling are shaping the next generation of processors.

Out-of-Order Execution: Future pipelined designs will adopt out-of-order execution mechanisms to allow instructions to be executed as soon as their operands are ready, rather than strictly following program order. This increases parallelism and processor utilization.

Speculative Execution and Branch Prediction: Advanced branch predictors and speculative execution units will be integrated to reduce the impact of control hazards. By predicting the outcome of branches and executing instructions ahead of time, overall throughput can be improved significantly.

Superscalar Architecture: Moving toward superscalar designs, future processors will include multiple pipelines to issue and execute more than one instruction per clock cycle. This approach boosts instruction-level parallelism and improves performance per cycle.

Dynamic Scheduling (e.g., Tomasulo's Algorithm): Static hazard resolution logic like forwarding and stalling may be complemented or replaced by dynamic scheduling techniques that track data dependencies in real-time and issue instructions accordingly. Tomasulo's algorithm is a prime example of this trend.

Energy-Efficient and Adaptive Design

Energy-Efficient Pipeline Design: With the rising importance of low-power systems, future designs will integrate clock gating, dynamic voltage scaling, and energy-aware hazard detection units to minimize power consumption during idle or low-activity phases.

Clock Gating: This technique disables the clock signal to idle pipeline stages or components, reducing dynamic power usage. Future designs may employ fine-grained clock gating that dynamically adapts to instruction flow, saving energy without impacting performance.

Power Gating: Unlike clock gating, power gating completely shuts off power to unused functional units (e.g., multipliers or control logic during stalls). This significantly reduces leakage power and is particularly useful during pipeline flushes or when certain units are not needed.

Dynamic Power Management (DVFS): Future MIPS-like processors may integrate DVFS (Dynamic Voltage and Frequency Scaling) to adjust voltage and clock speed in real time based on workload intensity or hazard patterns, thereby optimizing power and performance dynamically.

Intelligent Optimization and Adaptation

AI-Driven Optimization: Machine learning techniques will be employed for real-time hazard prediction, instruction reordering, and performance tuning. These models can dynamically adapt to workloads and enhance overall execution efficiency.

Pipeline Reconfiguration: Adaptive pipelines may be developed where the number of active stages, bypass paths, or even forwarding logic is adjusted in real time based on workload requirements. This helps balance power usage and performance effectively.

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High-Level Synthesis (HLS) tools will be used increasingly to shorten development cycles and enable rapid hardware generation from high-level descriptions.

Future designs will integrate pipelined processors with SoC platforms such as Xilinx Zynq to combine general-purpose CPUs with programmable logic for real-time testing and performance evaluation.

Custom hazard detection and forwarding logic can be verified on FPGA using realistic testbenches and workloads, allowing early detection of design flaws and performance bottlenecks.

Integration with Heterogeneous Computing Platforms: Future MIPS-like pipelined processors will increasingly be integrated into heterogeneous systems that include GPUs, AI accelerators, and DSPs. This allows the processor to offload computation-heavy or domain-specific tasks to specialized units, improving performance and energy efficiency. Seamless communication between pipeline cores and these co-processors will be a key feature.

Instruction Fusion and Micro-Operation Optimization: Instruction fusion refers to combining dependent instructions, such as a load followed by an arithmetic operation, into a single micro-operation internally. This reduces the number of cycles needed for execution. Future pipelines will also optimize how micro-operations flow through stages, minimizing control overhead and improving throughput.

Secure Pipeline Design: Security is becoming critical in processor architecture, especially with the rise of side-channel attacks like Spectre and Meltdown. Future pipelined processors will include hardware-level protections, such as safe speculative execution, secure branch prediction, and isolation of critical instructions and memory regions to prevent unauthorized access.

Pipeline-Level Fault Tolerance and Error Recovery: To ensure reliability in safety-critical systems, future pipelines will include fault detection and correction mechanisms. These may involve parity checks, ECC for register and memory data, and rollback strategies to recover from detected errors without requiring a complete processor reset.

Adaptive Pipeline Depth: Rather than relying on a fixed number of pipeline stages, future designs may allow dynamic reconfiguration of the pipeline depth. For example, simpler instructions may bypass certain stages, while complex operations could benefit from deeper pipelines. This flexibility improves performance and power efficiency based on the current workload.

Virtual Pipeline Simulation for Compiler Optimization: Compiler toolchains will incorporate virtual models of the hardware pipeline to optimize instruction scheduling during compilation. This allows software to better align with hardware execution characteristics, reducing hazards and improving overall code efficiency.

Chiplet-Based Pipeline Architectures: Future processors may implement pipeline stages across separate silicon “chiplets” rather than a single monolithic chip. This modular approach allows better power distribution, easier scaling, and reusability of pipeline components. High-speed interconnects between chiplets will maintain low latency.

Support for Emerging Memory Technologies: With the emergence of non-volatile memory types like MRAM and ReRAM, future pipelined processors will include adaptive memory access units. These will be capable of handling variable-latency memory reads and writes without stalling the processor pipeline, ensuring smooth performance with modern memory hierarchies.

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Image Processing on FPGA using UART Interface

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***Abstract*— This project implements a real-time image processing system on an FPGA using UART communication with MATLAB. The system performs basic grayscale transformations—image inversion, darkening, and lightening—using Boolean logic in Verilog. Images of varying resolutions (8×8, 64×64, 128×128) are transferred and processed through a UART interface operating at 9600 baud. Onboard switches enable dynamic operation selection without reprogramming. The design highlights a lightweight, low-power hardware-software co-design suitable for embedded and educational applications.**

Keywords—Field Programmable Gate Array (FPGA), Image Processing, UART communication, Verilog HDL, Xilinx Vivado.

I. INTRODUCTION

Image processing plays a vital role in domains such as autonomous systems, biomedical imaging, and augmented reality. The demand for real-time and low-latency solutions has led to a shift from software-based approaches to hardware-accelerated systems using Field-Programmable Gate Arrays (FPGAs). FPGAs offer parallelism, low latency, and reconfigurability, making them well-suited for embedded image processing tasks.

This work presents a real-time image processing system implemented on an FPGA using UART communication with MATLAB. The system performs three basic grayscale operations—image inversion, darkening, and lightening—controlled via hardware switches. To balance performance and resource constraints, the input image is resized to 8×8, 64×64, or 128×128 resolution. A custom UART interface at 9600 baud enables data exchange between MATLAB and the FPGA, while transformation logic is implemented in Verilog HDL. This project highlights the potential of using FPGAs for

low-level image transformation tasks in real time. While the operations implemented are basic, the

framework can be extended to more complex filtering, edge detection, and image enhancement techniques.

The design addresses key challenges such as synchronization, buffer management, and clock division for reliable communication. This proof-of-concept demonstrates an effective hardware-software co-design approach, providing a modular and scalable platform for real-time embedded image processing applications.

II. METHODS AND MATERIALS

A. Proposed Method

The proposed system is a hardware-software co-design solution for real-time image processing, leveraging the parallel processing capabilities of an FPGA and the image handling features of MATLAB. A grayscale image is resized in MATLAB to one of three resolutions (8×8, 64×64, or 128×128) and sent pixel-by-pixel to the FPGA over a UART interface. The FPGA receives this data, processes it using Boolean logic-based transformations (invert, darken, brighten), and returns the processed image to MATLAB for visualization.

The control of the transformation operation is managed via on-board switches on the Boolean FPGA board. A 2-bit switch combination selects one of the three available operations. This

switch-controlled architecture allows dynamic transformation without reprogramming the FPGA.

The complete process is shown in Fig. 2.1, which illustrates the data transmission from MATLAB to the FPGA, image processing within the FPGA, and the return of the transformed image to MATLAB.

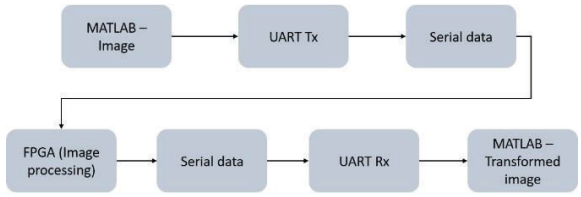


Fig. 2.1. Flow Diagram

B. UART Communication

UART (Universal Asynchronous Receiver/Transmitter) is used to establish a serial data link between MATLAB and the FPGA. A baud rate of 9600 was chosen for reliability and compatibility with the FPGA's internal clock. Each grayscale pixel is transmitted as a single 8-bit value. A complete image of resolution 64×64, for instance, would require 4096 bytes for one full frame. Transmission timing and buffer overflows were addressed by implementing clock division and FIFO-style buffering on the FPGA side.

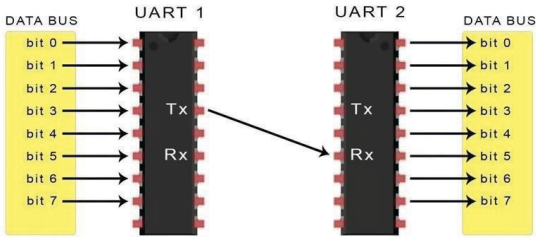


Fig. 2.2. UART Architecture

C. Components

The Boolean board in Figure 2.3 facilitates it to be an easy to embed hardware design. It supports many I/O ports, switches, LEDs, and seven-segment displays, which distinguish it from other boards. To embed the hardware design, Xilinx employs either HDL to construct the software. Boolean board enables the designer to easily design their hardware module.

The system is built around the Boolean FPGA development board, which features: On-board switches for mode selection, UART Tx/Rx ports, Internal BRAM for buffering, User-programmable I/O and an Integrated clock management.

MATLAB serves as the user interface and image handling environment. It prepares the image, sends it to the Boolean board over UART, and displays the result after processing.

The entire system was synthesized and deployed using Xilinx Vivado tools and written in Verilog HDL.

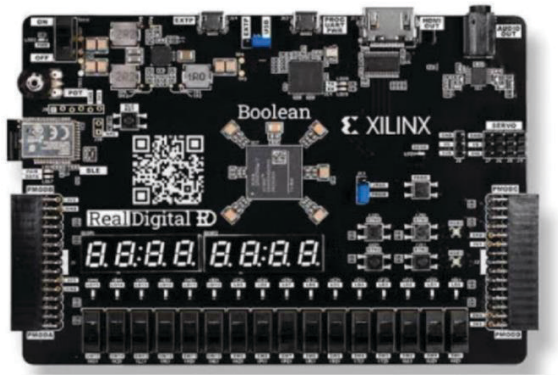


Fig. 2.3. Boolean board

D. Proposed Algorithm

The block diagram in Fig. 2.4 illustrates the architecture of the FPGA-based image processing system. The design facilitates real-time grayscale image transformations—namely darkening, brightening, and inversion—on pixel data transmitted from MATLAB via UART. The system begins with the UART Receiver, which accepts serial image data (RxD) from the host computer. This data, transmitted as 8-bit grayscale pixel values, is deserialized and stored in the Pixel Data Register to synchronize with the internal processing logic.

Once a pixel is received, it is routed to the Processing Block, which performs one of three pixel-level operations based on a 2-bit transformation control input (Transform[3:0]). These operations include bitwise inversion (~pixel), right-shifting for darkening, and bitwise OR or addition for brightening. In cases where darkening is selected, a Darken Mux dynamically adjusts the intensity reduction by selecting a predefined darkening factor.

A central Control Logic module governs the coordination of all subsystems. Triggered by the system clock (clk), it manages the sequencing of operations, enabling data flow between modules, and determining when to send processed pixels. Once the transformation is complete, the resulting pixel value is handed over to the UART Transmit module. This module converts the 8-bit parallel data back into a serial format and transmits it to MATLAB through the TxD line. Debugging signals (TxD_debug, transmit_debug) are included to assist in real-time verification.

This modular pipeline enables low-latency and energy-efficient image transformation while maintaining synchronization with MATLAB through UART communication. The use of Boolean logic operations ensures optimal resource usage on the FPGA, making the system suitable for scalable embedded vision applications.

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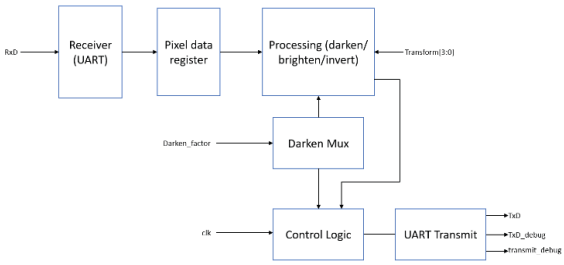


Fig. 2.4. Block Diagram

E. Code Analysis

1. Top Module

The top module serves as the central hub of the system, coordinating data flow between the UART receiver, processing logic, and UART transmitter. It receives grayscale pixel data from the UART receiver, applies the selected image transformation based on user input switches, and routes the processed data to the UART transmitter for output. It interprets control signals like transform[3:0] and darken_factor to determine which operation—none, brighten, darken, or invert—is to be executed.

2. UART Receiver Module

This module captures serial data transmitted from MATLAB over the UART interface. It converts the incoming bitstream on the RxD line into 8-bit parallel pixel data using a shift register and oversampling technique. A clock divider ensures accurate timing to match the 9600 baud rate. Once complete data bytes are reconstructed, they are output to the processing unit for transformation.

3. UART Transmitter Module

The UART transmitter module is responsible for sending the processed image data back to MATLAB. It uses a finite state machine (FSM) to serialize the 8-bit data into a UART-compatible frame consisting of a start bit, 8 data bits, and a stop bit. Timing is managed using counters to maintain consistent baud rate operation, and the module continues to transmit each byte until the image data is fully sent.

4. Image Transformation logic

Implements pixel-level operations using Verilog arithmetic and logic:

- Invert: 255 - pixel
- Brighten: pixel + factor (capped at 255)
- Darken: pixel - factor (not below 0)

5. Clock Divider and Buffering

A dedicated clock divider is used to derive the timing signal needed for UART transmission and reception. Buffers are employed to hold intermediate pixel data, ensuring smooth and synchronized data handling across modules. This is particularly important when working with variable image sizes and maintaining data integrity during communication.

6. MATLAB Interface

On the host side, MATLAB is used to prepare and transmit the grayscale image data to the FPGA. It also receives the processed data for visualization. The MATLAB script manages serial communication via the UART port, formats the image as a byte stream, and reconstructs the result for display using built-in image functions.

III. RESULTS AND DISCUSSION

A. Vivado Schematic Diagram

Due to successful compilation of HDL codes, schematic diagram in Fig.3.1. was created by the vivado simulation tool. Synthesis, implementation, and bitstream were created successfully. To program the Boolean board, first, the bitstream is generated and then hooked up with the system.

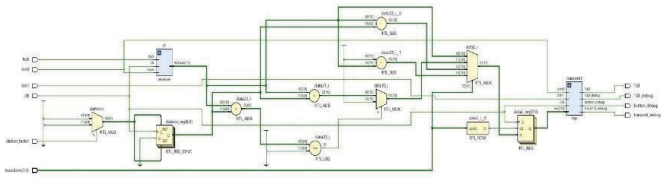


Fig. 3.1. Vivado Schematic diagram

B. Sample Output

The FPGA-based image processing system was successfully tested with resolution 64×64. The original and processed images demonstrate the effectiveness of pixel-level transformations implemented in hardware. Three distinct operations—lightening, darkening, and inversion—were applied individually using onboard switch control. As observed, the lightening operation enhanced brightness but introduced minor pixel artifacts due to data overflow or rounding. Darkening significantly reduced intensity levels, validating the right-shift logic. Inversion accurately flipped pixel values, producing high-contrast images with clearly altered colour tones. Some minor distortions in the processed images highlight the limitations of UART transmission bandwidth and synchronization, especially during larger data transfers.



Fig.3.2. Image Processing output: Darkening

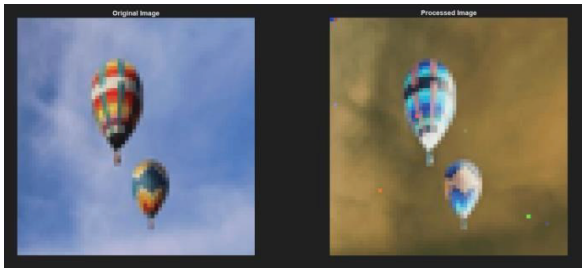


Fig.3.3. Image Processing output: Inversion

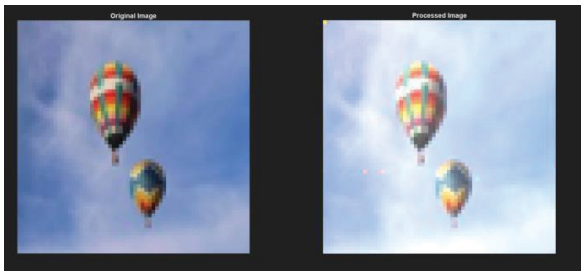


Fig.3.4. Image Processing Output: Brightening

C. *Result Discussion*

The image processing system was implemented on a FPGA with UART-based communication to a host PC. In this project, we observe the effects of applying different distortions—such as darkness, inversion, and brightness—on an original image, and analyze how well the system processes or reconstructs it. The original image appears to be a simple balloon photograph, used as a reference for all three transformations.

In the case of darkness, the processed image becomes significantly dimmer, and much of the colour detail is lost. The balloon appears less distinguishable, and there seems to be a slight increase in noise. This suggests that the model struggles to restore contrast and brightness effectively when the dynamic range of the original image is heavily compressed. It highlights a limitation in recovering visual features from underexposed or dark images.

With inversion, the system is exposed to a nonlinear distortion where pixel colours are flipped. After processing, the image retains visible artifacts and distorted colours, especially in the background, which turns an unnatural brown rather than the original blue. This indicates that the model has difficulty handling nonlinear transformations like inversion, and cannot correctly remap the colours to their original values. Such distortions lead to unnatural outputs and false visual features.

For the brightness case, the image appears overexposed after processing. colours are overly saturated and the image becomes washed out, with horizontal banding artifacts present. These effects suggest that the model may be overcompensating when trying to correct brightness distortions. Bright areas become clipped, reducing the ability to distinguish between lighter colour tones, and some structural noise appears due to the imbalance in processing.

In summary, the model or filtering system used shows varying levels of effectiveness depending on the type of distortion. It performs relatively better for linear changes like brightness or darkness, though not perfectly. However, it clearly struggles with nonlinear changes like inversion, leading to significant colour and structure artifacts. Improving the model's robustness could involve better training data augmentation, advanced normalization techniques, or architectural enhancements to better handle a range of distortions.

IV. CONCLUSION

This project aimed to evaluate how a signal processing or machine learning model responds to various types of image distortions—specifically, 50% and 75% darkness, brightness enhancement, and inversion. By applying these transformations to a reference image and analyzing the system's reconstructed output, we gained insights into the strengths and limitations of the current approach.

The results demonstrated that the system could partially handle linear distortions like increased darkness or brightness. However, it still introduced artifacts such as banding or excessive contrast, especially in overexposed regions. This indicates that while the model can make reasonable estimations under moderate lighting changes, its ability to fully restore natural appearance is limited.

In contrast, the model performed poorly under nonlinear transformations like inversion. The output images suffered from unnatural colour mappings and structural inaccuracies, showing that the model is not equipped to reverse such transformations. This highlights a major limitation in the system's ability to generalize beyond simple pixel-level changes.

Overall, the project showcases the need for more advanced preprocessing, robust model architectures, or enhanced training datasets when dealing with real-world scenarios where images may undergo unpredictable distortions. Future work may include integrating data augmentation strategies during model training or exploring deep learning-based restoration methods to improve visual quality and resilience across diverse input conditions.

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1-Bit Error Detection and Correction in 2x2 MIMO using FPGA

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Abstract: **This project presents the FPGA Implementation of a MIMO Communication System Using Hamming Code for Bit Error Rate Reduction, integrated with a Multiplexer to observe various outputs. The system utilizes Hamming encoding to protect 4-bit input data streams from two transmitters by generating 7-bit codewords. These encoded data streams are transmitted over a simulated MIMO channel that introduces predefined noise patterns to emulate real-world interference. At the receiver end, Hamming decoders detect and correct single-bit errors, ensuring accurate data recovery. A Multiplexer is employed to efficiently switch and display multiple outputs, including encoded data, noisy data, corrected data, and the final decoded output on the FPGA board. This design demonstrates the effectiveness of error correction in reducing the Bit Error Rate (BER) in MIMO systems, making it suitable for reliable digital communication applications. The FPGA-based implementation not only ensures efficient hardware utilization but also demonstrates the potential for scaling the design for advanced technologies like 5G and IoT applications**.

List of Abbreviations

Abbreviations	Full Form
AUV	Autonomous Underwater Vehicles
IEEE	Institute of Electrical and Electronics Engineers
FPGA	Field Programmable Gate Array
MIMO	Multiple Input Multiple Output
AWGN	Additive White Guassian Noise
BER	Bit Error Rate
VLSI	Very Large Scale Integration

I. Introduction

In wireless communication**,** Multiple-Input Multiple-Output (MIMO) systems are widely used to improve data throughput and spectral efficiency by utilizing multiple antennas at both the transmitter and receiver ends. However, data transmitted over wireless channels is prone to interference and noise, leading to increased Bit Error Rate (BER)**.** To enhance communication reliability, Error Correction Codes (ECC) such as Hamming Code are employed to detect and correct transmission errors. This project aims to implement a MIMO communication system using Hamming Code on an FPGA platform, simulating noisy channel conditions and showcasing error correction capabilities. By exploiting spatial diversity, MIMO systems effectively combat issues such as multipath fading and interference, which are prevalent in wireless environments. Field-Programmable Gate Arrays (FPGAs) offer a powerful platform for implementing MIMO systems due to their flexibility, parallel processing capabilities, and low latency. These devices allow for real-time signal processing and adaptive algorithm deployment, making them particularly well-suited for MIMO applications. The combination of MIMO technology with FPGA implementation facilitates advanced processing techniques such as channel estimation, equalization, and adaptive modulation, all of which contribute to minimizing the Bit Error Rate.

II. LITERATURE SURVEY

Using the orthogonal properties of OFDM sub-channels can be transmitted over a combination of coding and decoding LDPC codes in the high performance, will achieve good results in communication system. The FPGA implementation results show that the data transmission performance is good and the data throughput is wide and the decoder can achieve a maximum decoding throughput of 10Mb/s at 15 iterations, it can meet the high-speed wireless communication system. [1]

A FPGA-based high performance Serial communication system interface module which includes full functions of UART16550 is designed and optimized based on the communication protocol and working principles. he frequency of the optimized design is up to 166MHz, and the power consumption is reduced to 0.147W by 63.9%. The test data at typical baud-rate of 115200 and the analyzed result by using Matlab are presented. The test results indicate that the optimized design can be communicated correctly and steadily. [2]

The proposed BER tester (BERT) integrates fundamental baseband signal processing modules of a typical wireless communication system along with a realistic fading channel simulator and an accurate Gaussian noise generator onto a single FPGA to provide an accelerated and repeatable test environment in a laboratory setting. The FPGA-based

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BERT should reduce the need for time-consuming software-based simulations, hence increasing the productivity. [3]

A two-level and block diagonal based improved Neumann series approximation (TL-BD-INSA) algorithm is proposed, which is suitable for both ideal uncorrelated channels and the correlated channels with multiple-antenna user equipment (MAUE) system. The implementation on Xilinx Virtex-7 FPGA and ASIC with TSMC 45 nm shows that the proposed detector can achieve 1731 bps/slices and 0.463 Gbps/mm^2 hardware efficiency, respectively, demonstrating that the proposed system can achieve a well trade-off between error performance and implementation efficiency. [4]

It presents the performance analysis of four different channel coding and interleaving schemes for MIMO-OFDM communications systems. A comparison is done based on the BER, hardware implementation resources requirement, and power dissipation. It also presents a memory-efficient and low-latency interleaver implementation technique for the MIMO-OFDM communication system. using the proposed interleaver, a MIMO-OFDM based transmitter employing a double data stream 2×2 MIMO spatial multiplexing system is built. [5]

For massive multiuser multiple-input multiple-output (MIMO) systems, linear detectors, such as minimum mean square error (MMSE), suffer from unbearable computational pressure due to the large-scale matrix inversions. Various iterative detectors, such as Jacobi and steepest descent (SD) as well as their enhanced variants, are applied to improve the performance and complexity trade-off. [6]

Deep learning via a multi-layer perceptron architecture that exceeds the performance of traditional CSI processing methods like least square (LS) and linear minimum mean square error (LMMSE) estimation, thus leading to a beyond fifth generation (B5G) networking paradigm wherein machine learning fully drives networking optimization. [7]

Designed CNN-based AMC schemes for the complex-valued temporal radio signal domain and implemented them on an FPGA platform. This work focuses on quantized CNN and low precision mathematics to solve the problem of bigger model size and floating-point weights and activations. The proposed scheme achieves at least 1.4% higher accuracy and takes only 40% hardware resources than the baseline. The RFSoc implemented model achieves a real-time throughput of 527k classification per second with a latency of 7.5μs. [8]

An average bit error rate (BER) performance analysis over time-invariant channel is presented for M-MIMO systems under imperfect channel estimation in contrast with most of M-MIMO literature that uses the ergodic capacity approach. Closed-form expressions and bounds to evaluate the average BER are derived for MRC, ZF and MMSE detectors in a unicellular environment considering M -QAM modulation. [9]

The non-sparse massive MIMO system is converted into a quasi-sparse error (i.e., error vector consists of a small fraction of significant elements) system by using a rough initial estimate of the transmitted symbol vector. Next, the error is estimated by a low-complexity error recovery technique which detects the error elements in an ordered pattern. Finally, to obtain the output symbol vector, the estimated error vector is combined with the initial solution vector. [10]

III. METHODOLOGY AND IMPLEMENTATION

The methodology for developing the FPGA-based MIMO system for bit error rate reduction involves a systematic approach to design, simulation, and implementation. First, a 2x2 MIMO configuration is designed using Verilog, enabling spatial multiplexing to transmit multiple data streams over the same frequency band. Hamming encoding and decoding are integrated to provide robust error detection and correction, minimizing bit errors caused by noise and interference. The system includes a MIMO channel model that simulates real-world channel conditions to evaluate the effectiveness of the error correction mechanism. The Verilog modules are then synthesized and implemented on an FPGA board, leveraging its parallel processing capabilities for high-speed and real-time performance. To observe and analyze various outputs, a multiplexer is integrated into the design. The functionality of each module is verified using simulation tools such as ModelSim or Xilinx Vivado. The system's performance is evaluated by measuring the bit error rate under different noise and interference scenarios, validating its efficiency in enhancing communication reliability. This modular and scalable design also allows for future enhancements, such as expanding to larger MIMO configurations.

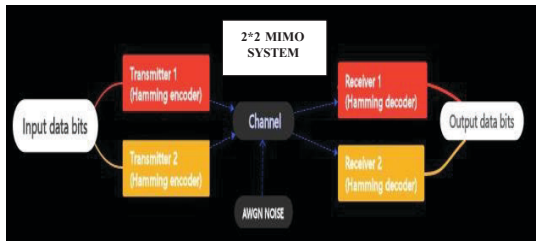


Fig 1. Block diagram

The block diagram of the FPGA-based MIMO system for bit error rate reduction illustrates the key components and data flow. It consists of two transmitters that use Hamming encoders to encode the input data, ensuring error detection and correction capability. The encoded data streams are transmitted through a simulated MIMO channel that introduces noise and interference, mimicking real-world conditions. At the receiver end, two Hamming decoders decode the noisy signals, correct any detected errors, and retrieve the original data.

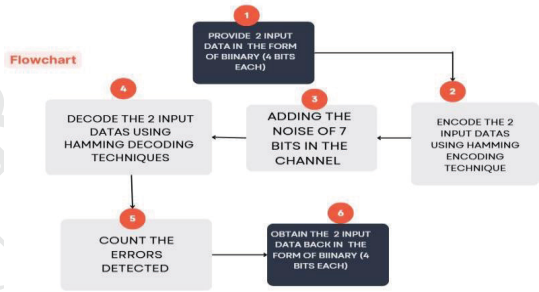


Fig 2. Flow chart

The flow chart for the FPGA-based MIMO system illustrates the sequential steps involved in data transmission, processing, and error correction. It begins with the input of data streams for two transmitters, which are encoded using Hamming encoders to enable error detection and correction. The encoded data is then passed through a simulated MIMO channel where predefined noise is introduced to replicate real-world communication challenges. At the receiver end, Hamming decoders process the noisy data, detecting and correcting any errors before retrieving the original data. The corrected outputs are then observed using a multiplexer on the FPGA board. This logical flow ensures efficient error management and reliable communication, showcasing the effectiveness of the proposed MIMO system.

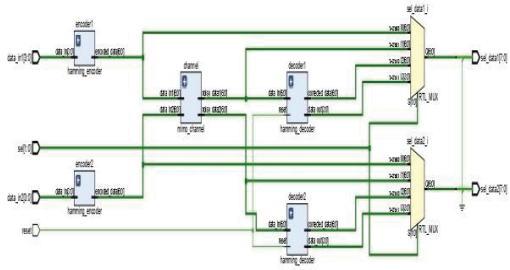
IV. RESULTS AND DISCUSSION

A. RESULTS

The FPGA-based MIMO system for Bit Error Rate (BER) reduction was successfully implemented and tested using Verilog. The simulation results demonstrated the system's effectiveness in

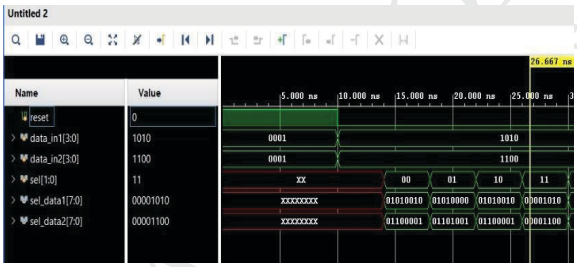
encoding and decoding data using Hamming codes, ensuring accurate error detection and correction. Under varying noise conditions simulated through the MIMO channel model, the system maintained data integrity with a significantly reduced BER. The outputs observed on the FPGA board confirmed the proper functioning of each module, including the transmitter, channel, and receiver sections. The inclusion of the MUX allowed for real-time monitoring of different outputs, validating the system's reliability and robustness. These results highlight the potential of FPGA-based MIMO systems in enhancing wireless communication performance.

Schematic



The schematic illustrates the FPGA-based MIMO system's architecture, consisting of two parallel data paths to achieve spatial multiplexing. Each path includes a Hamming encoder for error correction, a simulated MIMO channel to introduce controlled noise, and a corresponding Hamming decoder for error detection and correction. The data inputs (data_in1 and data_in2) are processed simultaneously, showcasing the system's ability to transmit multiple data streams efficiently. Finally, a multiplexer (RTL_MUX) selects the output based on the control signals, ensuring accurate data retrieval. This design effectively reduces the bit error rate while maintaining high data throughput.

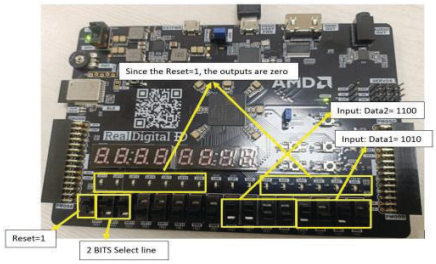
Output waveform



In the waveform simulation, the data flow through the FPGA-based MIMO system can be observed clearly when the sel input is set to 11. At this point, the system selects and transmits the encoded data corresponding to the inputs data_in1 and data_in2. Specifically, data_in1 is 1010, and data_in2 is 1100. After processing through the Hamming encoder, the outputs are displayed as sel_data1 = 00001010 and sel_data2 = 00001100. This indicates that the encoder successfully transformed the 4-bit inputs into 8-bit outputs while maintaining data integrity. The accurate reflection of the input data at the output validates the functionality of the spatial multiplexing and selection logic within the MIMO system. This result demonstrates the system's efficiency in managing multiple input streams, ensuring reliable communication and effective bit error rate reduction.

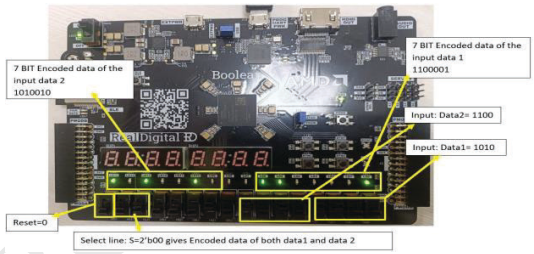
Hardware outputs:

1) When reset is high

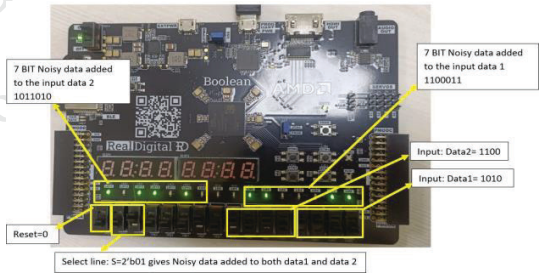


2) When reset is low

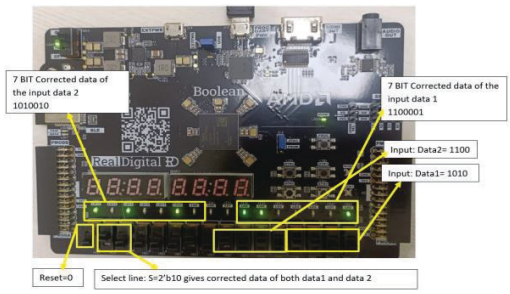
a) Select lines are 00



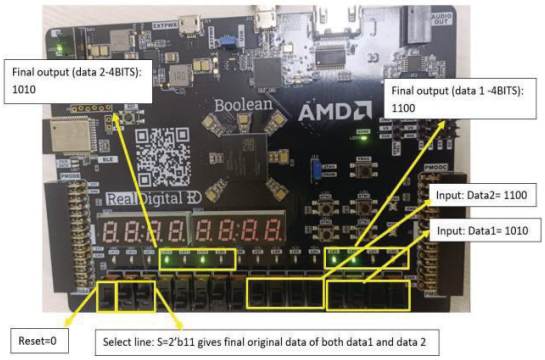
b) Select lines are 01



c) Select lines are 10



d) Select lines are 11



B. *DISCUSSIONS*

1. Insights and Impacts:

1.1. Enhanced Data Integrity:

1.1.1 Hamming Encoding for Error Correction**:** Utilizes Hamming encoding to effectively correct single-bit errors, ensuring data integrity during transmission.

1.1.2. Reliable Transmission in Noisy Environments: Maintains reliable communication even in noisy conditions by detecting and correcting errors.

1.2. Improved Communication Efficiency:

1.2.1. Spatial Multiplexing in MIMO: Increases data throughput by transmitting multiple data streams simultaneously over different antennas without requiring additional bandwidth.

1.2.2. Reduced Bit Error Rate (BER): Enhances communication quality by minimizing errors during data transmission, leading to more accurate data reception.

1.3. Real-Time Processing Capability:

1.3.1. High-Speed Data Processing with FPGA: Utilizes FPGA's parallel processing capability for fast and efficient data handling, suitable for real-time communication applications.

1.3.2. Versatility in Advanced Systems: Can be deployed in advanced communication systems like mobile networks, Wi-Fi, and IoT devices due to its real-time processing capabilities.

1.4. Scalable and Modular Design:

1.4.1. Modular Verilog Code Structure: The design's modular structure facilitates easy scalability and future enhancements without major redesigns.

1.4.2. Upgradability for Complex MIMO Configurations: Can be expanded to support more complex MIMO configurations, enabling higher capacity systems for enhanced data throughput.

2. Limitations:

2.1. Fixed Noise Model:

2.1.1. Predefined Noise Model: The simulation relies on a fixed noise model, reducing the accuracy of performance evaluation in real-world scenarios.

2.1.2. Lack of Dynamic Channel Adaptation: It does not account for dynamic channel variations commonly experienced in wireless environments, impacting reliability.

2.2. Limited MIMO Configuration:

2.2.1. 2x2 MIMO Setup Only: Currently supports only a 2x2 MIMO configuration, limiting its scalability and application in systems requiring higher data capacity.

2.2.2. Not Optimized for Larger Arrays: The design is not yet optimized for more complex antenna arrays, such as 4x4 or 8x8 MIMO systems, which are needed for advanced communication networks.

2.3. Error Correction Capability:

2.3.1. Single-Bit Error Correction: Uses Hamming codes restricted to correcting only single-bit errors, limiting error correction effectiveness.

2.3.2. Vulnerability to Burst Errors: Ineffective against burst errors or severe interference, reducing overall communication reliability.

2.4. Hardware Constraints:

2.4.1. High FPGA Resource Utilization: Consumes significant FPGA resources, impacting scalability and power efficiency, especially in resource-constrained environments.

2.4.2. Limited Feature Integration**:** The high resource usage restricts the integration of additional functionalities or more advanced algorithms, limiting system flexibility and performance enhancements.

3. Recommendations for Improvement:

3.1. Advanced Noise Modeling and Channel Estimation:

3.1.1. Adaptive Noise Models: Incorporate adaptive noise models to more accurately simulate real-world channel conditions, leading to more realistic performance evaluation.

3.1.2. Dynamic Channel Estimation: Implement dynamic channel estimation algorithms to better manage interference and enhance communication reliability.

3.2. Enhanced Error Correction Techniques:

3.2.1. Advanced Error Correction Codes: Upgrade to more robust error correction codes like LDPC (Low-Density Parity-Check) or Turbo codes for improved error resilience.

3.2.2. Burst Error Handling: Enhance the system's capability to manage burst errors and severe interference, increasing overall communication reliability.

3.3. Support for Higher-Order MIMO and Modulation:

3.3.1. Larger MIMO Configurations: Expand the design to support 4x4 or larger MIMO setups, allowing for higher data throughput and improved spectral efficiency.

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3.3.2. Advanced Modulation Schemes: Implement advanced modulation techniques (e.g., 16-QAM, 64-QAM) to enhance spectral efficiency and increase data rates.

3.4. Optimization for FPGA Resource Utilization:

3.4.1. Code Optimization**:** Optimize Verilog code to reduce hardware complexity, enhancing power efficiency and performance.

3.4.2. Improved Scalability: Optimize resource usage to ensure scalability for deployment in resource-constrained environments.

3.5. Dynamic Adaptation and Scalability:

3.5.1. Real-Time Adaptive Algorithms: Integrate adaptive algorithms to dynamically adjust to changing channel conditions and interference patterns.

3.5.2. Future-Ready Scalability: Design the system for seamless scalability, ensuring compatibility with evolving communication standards, including 5G and beyond.

V. Conclusion and Future trends

A.CONCLUSION

The FPGA-based MIMO system for Bit Error Rate (BER) reduction presented in this project demonstrates a robust and efficient approach to enhancing wireless communication performance. By utilizing spatial multiplexing and implementing Hamming error correction, the system effectively minimizes BER while maximizing data throughput over the same frequency band. This approach not only improves spectral efficiency but also maintains power and bandwidth requirements, making it a practical solution for modern communication networks.

The choice of FPGA as the hardware platform allows for high-speed processing and real-time performance, showcasing the versatility and scalability of programmable logic devices in complex communication systems. The integration of a MUX for dynamic output selection facilitates comprehensive testing and analysis, ensuring the reliability and accuracy of the system under varying channel conditions. Furthermore, the use of Verilog for modular design enables easy scalability to larger MIMO configurations, paving the way for future advancements.

This project not only validates the effectiveness of using MIMO technology for error rate reduction but also establishes a strong foundation for future research and development in wireless communication systems. It demonstrates the potential of hardware-optimized solutions in achieving high data rates, low latency, and enhanced reliability, which are crucial for next-generation communication networks such as 5G and beyond. By addressing the critical issue of BER, this FPGA-based MIMO system contributes to the ongoing evolution of wireless communication technologies, supporting a more connected and data-driven world.

B. FUTURE TRENDS

1. Massive MIMO Systems
Massive MIMO technology is set to revolutionize wireless communication by employing a large number of antennas at both the transmitter and receiver ends. Configurations like 64x64 or even 128x128 antenna arrays are being explored to significantly increase spectral efficiency and network capacity. This trend is particularly relevant for 5G and 6G networks**,** where the demand for higher data rates and more reliable connectivity is rapidly growing. Massive MIMO leverages advanced spatial multiplexing and beamforming techniques to serve multiple users simultaneously, thus enhancing network performance while minimizing interference.

2. Beamforming and Beam Steering
Beamforming is a critical technology for directing wireless signals precisely towards users, maximizing signal strength while minimizing interference. Future advancements will involve adaptive beamforming algorithms and dynamic beam steering to respond to real-time changes in user location and channel conditions. These enhancements are essential for supporting high-mobility applications, such as autonomous vehicles and drone communication, where maintaining a strong and stable connection is crucial.

3. Machine Learning Integration
The integration of machine learning (ML) and artificial intelligence (AI) is poised to redefine MIMO systems by enabling intelligent decision-making for modulation schemes, error correction, and noise prediction. ML algorithms can optimize power allocation, improve channel estimation, and adaptively select coding techniques based on real-time conditions. This approach enhances communication reliability, reduces latency, and maximizes throughput, making MIMO systems more efficient and resilient to environmental variations.

4. Reconfigurable Intelligent Surfaces (RIS)
Reconfigurable Intelligent Surfaces are emerging as a game-changing technology to enhance wireless communication. These surfaces consist of programmable meta-materials that can control electromagnetic waves, effectively transforming the propagation environment. By dynamically reflecting or refracting signals, RIS can mitigate multipath fading, increase coverage, and improve signal strength. This technology is particularly beneficial for urban environments with dense obstructions, offering a cost-effective and energy-efficient solution for enhancing MIMO performance.

5. 6G Communication Systems
As the world prepares for the rollout of 6G networks**,** MIMO systems will play a pivotal role in supporting ultra-high-speed data transmission, low latency, and massive connectivity. 6G is expected to operate at terahertz frequencies**,** enabling unprecedented data rates and supporting advanced applications like holographic communications, virtual reality, and the Internet of Everything (IoE). MIMO systems, combined with advanced coding and modulation techniques, will be instrumental in achieving the high spectral efficiency and low power consumption required for 6G.

6. Quantum MIMO Communication
Quantum computing is set to revolutionize MIMO communication by providing immense computational power for signal processing tasks. Quantum MIMO systems leverage quantum entanglement and superposition to enhance channel capacity and security. Quantum algorithms can optimize resource allocation, reduce processing delays, and enhance error correction capabilities. Although still in the experimental phase, quantum MIMO holds the potential to drastically improve the efficiency and security of future communication systems.

7. Energy-Efficient MIMO Architectures
With the growing emphasis on sustainability and green communication, the development of energy-efficient MIMO architectures is gaining momentum. Research is focused on optimizing power consumption through advanced coding techniques, low-power FPGA designs, and energy-aware beamforming algorithms. These innovations are crucial for IoT applications, where devices are often battery-powered and require prolonged operational life.

8. Hybrid FPGA and ASIC Solutions
Combining the flexibility of Field Programmable Gate Arrays (FPGAs) with the efficiency of Application-Specific Integrated Circuits (ASICs) is emerging as a powerful approach to MIMO system design. Hybrid FPGA-ASIC solutions offer cost-effective, high-performance communication systems that are both programmable and efficient. This approach is particularly advantageous for rapid prototyping, enabling developers to fine-tune

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algorithms on FPGA before migrating to a more optimized ASIC design for mass production.

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ScareTech: Smart Animal Deterrence for Agriculture and City Spaces

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***Abstract*—This ScareTech project develops a custom Convolutional Neural Network (CNN) to categorize images into defined classes—such as detecting whether an animal like a monkey is present—without relying on a pre-trained model. The model is trained on a dataset of 2,000 labeled images, split into 80% training and 20% validation subsets, using Google Colab's GPU. Preprocessing steps include resizing images to a standard size, normalizing pixel values, and applying augmentation techniques like rotation and zooming to improve generalization. The CNN architecture comprises multiple convolutional layers with ReLU activations, max-pooling, and fully connected dense layers, ending with a sigmoid activation for binary classification. The model uses the Adam optimizer and binary cross-entropy loss, and performance is evaluated using metrics such as accuracy, precision, recall, and F1-score through confusion matrices.**

In real-time deployment, AI sensing integrates this CNN with a camera module, allowing the system to autonomously detect and classify animals from visual input. Additionally, PIR (Passive Infrared) motion sensors detect the presence of warm-bodied animals and act as a trigger to activate the camera and AI module, minimizing unnecessary processing and conserving power. Together, the motion-based activation and AI-powered classification enable a responsive, energy-efficient deterrence system. ScareTech demonstrates the potential of building scalable, robust AI solutions from scratch for use cases such as wildlife monitoring, anomaly detection, and smart agriculture.

***Index Terms*—Animal deterrence, Convolutional Neural Network, Smart agriculture, PIR sensors, AI sensing**

I. Introduction

Nikita was playing with her one-year-old niece at her sister's house when monkeys entered the kitchen and started throwing things. She thought quickly and used her Alexa device to mimic a dog's bark, which scared the monkeys away. Anand Mahindra praised her resourcefulness and offered her a job at Mahindra once she completes her education, noting that this story shows how technology can enable human ingenuity.

This inspires us in the creation of a solution for animal disturbances using animals' natural fear of predators and mimicking the sounds predators make while hopefully making it into a deterrent system that can protect crops and urban gardens through humane management of wildlife.

The AI-ML Based Animal Deterrence System addresses the challenges posed by wildlife in agriculture and urban areas. In agricultural areas, cows, monkeys, birds, and wild pigs destroy crops, whereas in urban gardens, stray animals disturb markets and create safety issues. The system uses high-resolution cameras and CNN-based AI to monitor and respond to animal threats in real-time. In case a harmful animal is detected, this automatically activates deterrents such as a sound system and flashing lights, reduces human labor, and enhances good management of wildlife. Modern methods have therefore improved crop, urban garden protection while promoting coexistence with the wild.

II. Literature Survey

A. Animal Intrusion Detection in Farming Area Using YOLOv5 Approach

The study focuses on using the YOLOv5 deep learning algorithm to detect animal intrusions in farming areas, specifically targeting elephants, monkeys, tigers, and wild boars. The model achieved a mean average precision (mAP) of 94%, with precision and recall both at 89%. This high accuracy demonstrates the potential of YOLOv5 in enhancing crop protection and ensuring farmer safety. The research highlights the importance of automated detection systems in mitigating human-wildlife conflicts. Future work aims to integrate this detection system with IoT technology for real-time alerts, further improving response times to animal intrusions. Overall, the study presents a significant advancement in agricultural safety measures.

B. AI Based Scarecrow Preventing from Crop Vandalization

The project aims to protect crops from animal vandalization using an AI-driven scarecrow. It employs the YOLOv3 algorithm for real-time detection of animals through a webcam. Upon detection, the system plays repellent sounds to deter the animals, ensuring no manual intervention is needed after installation. The technology boasts high accuracy in identifying various animals and is designed to be non-harmful. This innovative approach significantly reduces crop loss and can be adapted for wider agricultural applications. Overall, the AI-based scarecrow presents a sustainable solution for farmers facing challenges from wildlife.

C. Smart Crop Protection from Animals in Real Time Using Convolutional Neural Networks

The study focuses on developing a real-time crop protection system that employs YOLOv7, a deep learning model, to detect animals that threaten crops. By integrating cameras and convolutional neural networks (CNN), the system can accurately identify and track these animals, enabling timely deterrent actions. The results indicate that YOLOv7 achieved a 94% accuracy rate, outperforming other models like ResNet50 and VGG16, thus offering a faster, more eco-friendly solution that reduces pesticide use and enhances crop yields, ultimately contributing to improved agricultural practices and global food security.

D. Deep Learning and Computer Vision Based Warning System for Animal Disruption in Farming Environments

The project aims to create a warning system that leverages deep learning and computer vision to address human-wildlife conflicts in agricultural areas. By employing the YOLOv6 model, the system can detect animals in real-time, sending alerts to farmers and local authorities. This technology not only helps in reducing crop damage but also supports wildlife conservation efforts and promotes sustainable farming practices. The system has demonstrated impressive results, achieving a 99.7% accuracy rate in identifying various animal species. Overall, it represents a significant advancement in protecting agricultural interests while fostering coexistence with wildlife.

E. Wild Animal Detection Using Deep Learning

The study focuses on creating a deep learning algorithm aimed at detecting wild animals to mitigate human-wildlife conflicts and reduce vehicle collisions. It employs depth-wise separable convolution layers and zero padding techniques for enhanced image processing. The model was evaluated using the IWildCam dataset, which includes diverse images of wild animals. Results demonstrated a remarkable 99.6% accuracy in classification and an Intersection over Union (IoU) value of 0.878 for detection tasks. The findings indicate that the proposed model is effective in both detecting and classifying wild animals, contributing positively to wildlife conservation efforts.

III. Problem Analysis & Solution

A. Problem Definition

The problem arises from the fact that wildlife interactions cause significant disturbances in agricultural and urban garden settings. Animals such as cows, monkeys, birds, and wild pigs can cause considerable damage to crops, threatening food security and farmer's livelihoods. In urban gardens, wildlife poses safety risks to individuals and can compromise plant health. Traditional deterrent methods often prove ineffective, labor-intensive, and costly, necessitating a more efficient and humane solution to manage these animal intrusions.

1) Disadvantages of Existing Systems:

- **Vulnerability of Electric Fencing:**
  - Breaks in the conducting wire can cripple the system.
  - Contact with non-electrified parts can create short circuits.
  - Power failures and contact of vegetation with electrified wires may result in fires.
- **Lack of Visibility:** Lack of adequate indicators may result in accidental shocks to unsuspecting humans.
- **Bee Repellents Safety Risks:** In the process of repelling elephants, bees can also pose a risk to humans, thus making areas unsafe.
- **Low Detection Rate:** Low percentage of detected intrusions is relatively low, thus reducing effectiveness.
- **Sensor Failures:** Failed sensors may result in missed detections and compromised security.
- **High Implementation Costs:** High initial investment may discourage adoption, especially in resource-poor settings.
- **Maintenance Requirements:** Maintenance is required to ensure optimal functionality, thus adding to long-term costs.
- **Environmental Concerns:** Ethical issues are involved, such as possible damage to non-target species during wildlife management.

B. Proposed Solution

The proposed solution to the above problem is to implement an AI to detect the animals and based on the detected input the AI is going to play the sound that scares the animals through a speaker which is used to produce the output.

- Object Detection
- AI Sensing
- Input Module (Camera)
- Data Processing (Image Recognition)
- Decision Making Model
- Output (Deterrent System)
- User Interface
- Notification to the user
- Data Logging

1) System Components and Functionality: **1. Motion Detection and AI Sensing**

ScareTech employs motion detection using Passive Infrared

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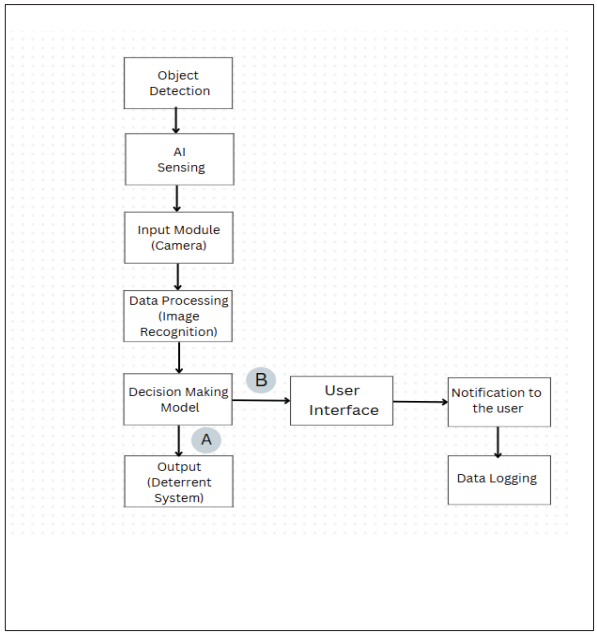


Fig. 1. Representation of the proposed solution

(PIR) sensors, which sense sudden changes in infrared radiation caused by the movement of warm-bodied animals. When triggered, these sensors prompt the system to activate cameras for image capture. AI sensing complements this by analyzing the visual data through a Convolutional Neural Network (CNN) model. The CNN classifies animals (e.g., monkeys, cows, elephants) based on trained datasets. If a threat is identified, the system activates deterrents like sounds or lights. AI enhances accuracy, filters out false alarms, and learns from new data. This dual-layer approach ensures both responsiveness and intelligent decision-making.

2. Input Module: Camera

The system begins with the input module, where cameras are employed to capture visual data from the surrounding environment. This module serves as the foundation for the system, as it provides the essential input required for further analysis and processing. The visual data collected is integral to understanding and interpreting the observed conditions.

3. Data Processing

Once the visual input is captured, it is directed to the processing module. In this stage, advanced algorithms analyze the data to identify and classify objects, detect specific designs, or recognize patterns. Machine learning models, such as those used for object detection, play a pivotal role in this process. The accuracy and efficiency of these algorithms ensure that the system interprets the input data reliably.

4. Decision Model

The insights derived from the data processing stage are forwarded to the decision-making model. Here, the system applies pre-defined rules or machine learning techniques to determine the appropriate actions based on the input data. For example, if the model identifies a specific condition or object, it may decide to initiate a corresponding response. This stage ensures the system's ability to respond intelligently and autonomously.

5. Deterrent System

The decisions made by the model activate the deterrent system. This module implements the necessary response mechanisms, such as activating alarms or other deterrents, to address the identified condition. The deterrent system ensures a timely and effective reaction to events, safeguarding the system's overall objectives.

2) Model Deployment on Raspberry Pi: For deploying this system on a Raspberry Pi, the following steps are undertaken:

- **Model Loading:** A pre-trained machine learning model, such as YOLOv8, is loaded onto the Raspberry Pi. This involves configuring the model and necessary dependencies.
- **Hardware Optimization:** Given the limited computational power of the Raspberry Pi, the model is optimized for efficient inference. Techniques such as using lightweight architectures or leveraging hardware acceleration ensure smooth operation.
- **Camera Integration:** The camera module or a compatible USB camera is connected and configured to provide real-time visual data. Libraries like OpenCV are employed to manage input acquisition and preprocessing.
- **System Workflow:** The Raspberry Pi handles the entire workflow of capturing input, processing data, making decisions, and triggering deterrent actions.

IV. Methodology & Implementation

A. Block Diagram

B. Pictorial Representation

C. Structure of the Work

1) 1. Dataset Selection and Preparation: **a) Dataset Source**

- The dataset was sourced from platforms like Kaggle and Roboflow, containing labeled images of monkeys and non-monkeys.
- The dataset was chosen for its diversity, availability, and proper labeling, making it suitable for classification tasks.

b) Dataset Preprocessing

- **Resizing and Normalization:**
  - All images were resized to 150x150 pixels to ensure consistency and compatibility with the CNN model input.
  - Pixel values were normalized to the range [0, 1] by dividing each value by 255, which improved model convergence.
- **Splitting the Dataset:**
  - The dataset was divided into three subsets:
    - Training Set (80%): Used for model training.

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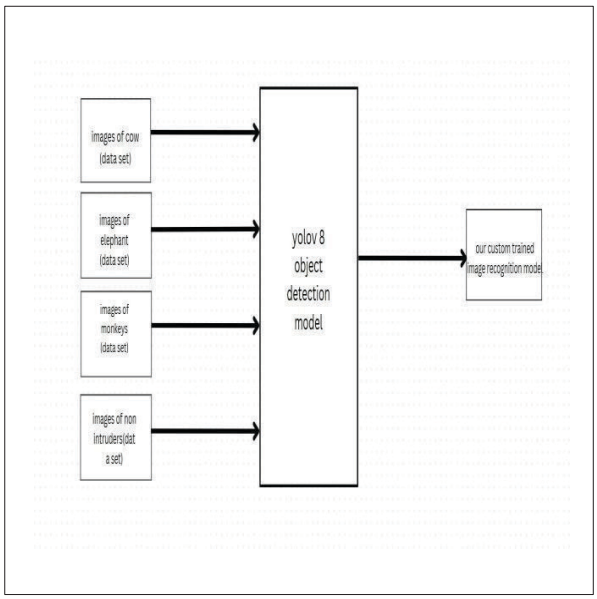


Fig. 2. Block diagram of the AI Model



```python
from ultralytics import YOLO
import cv2
from IPython.display import display, Image, clear_output
import os

# Load the trained YOLO model
model_path = os.path.expanduser("/Users/ishitareddy/Downloads/scaretech_model_new_outpu
model = YOLO(model_path)

def classify_and_respond(frame):
    """
    Classify the captured image and respond accordingly.
    """
    print("Classifying the captured image...")

    # Save the frame temporarily to run YOLO inference
    temp_image_path = "temp_capture.jpg"
    cv2.imwrite(temp_image_path, frame)

    # Run inference
    results = model.predict(source=temp_image_path)

    # Process the predictions
    if results:
        for result in results:
            # Get the most probable class
            top_class_index = result.probs.top1  # Index of the most probable class
            top_class_name = result.names[top_class_index]  # Get class name
            top_class_confidence = result.probs.top1conf  # Confidence of the top class

            print(f"Detected: {top_class_name} with confidence {top_class_confidence:.4

            # Respond based on the detected class
            if top_class_name == "monkeys":
                print("Speaker output: Langur sound (simulated)")
            elif top_class_name == "cows":
                print("Speaker output: Dog sound (simulated)")
            elif top_class_name == "non_intruder":
                print("No intruder detected.")
            else:
                print("Unknown detection.")
    else:
        print("No objects detected.")

    # Display the captured image
    _, jpeg_frame = cv2.imencode('.jpg', frame)
    display(Image(data=jpeg_frame.tobytes()))
    clear_output(wait=True)

def capture_and_classify():
    """
    Capture an image using the webcam, display it, and classify it.
    """
    # Open system camera
    cap = cv2.VideoCapture(0)

    if not cap.isOpened():
        print("Error: Could not access the camera.")
        return

    print("Accessing camera...")

    # Capture a single frame
    ret, frame = cap.read()

    if not ret:
        print("Error: Unable to capture image from the camera.")
        cap.release()
        return

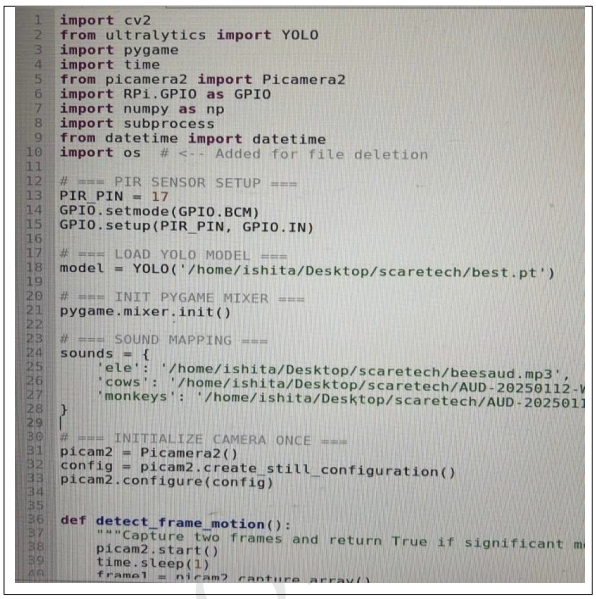
    # Release the camera once the image is captured
    cap.release()
    cv2.destroyAllWindows()

    # Classify the captured frame
```

Fig. 3. Pictorial representation of classification code

- ∗ Validation Set (10%): Used for hyperparameter tuning and performance evaluation during training.
- ∗ Test Set (10%): Used for final evaluation to ensure the model generalizes well.

– The train_test_split function in Scikit-learn was used with stratification for balanced class representation.



```python
import cv2
from ultralytics import YOLO
import pygame
import time
from picamera2 import Picamera2
import RPi.GPIO as GPIO
import numpy as np
import subprocess
from datetime import datetime
import os  # <-- Added for file deletion

# === PIR SENSOR SETUP ===
PIR_PIN = 17
GPIO.setmode(GPIO.BCM)
GPIO.setup(PIR_PIN, GPIO.IN)

# === LOAD YOLO MODEL ===
model = YOLO('/home/ishita/Desktop/scaretech/best.pt')

# === INIT PYGAME MIXER ===
pygame.mixer.init()

# === SOUND MAPPING ===
sounds = {
    'ele': '/home/ishita/Desktop/scaretech/beesaud.mp3',
    'cows': '/home/ishita/Desktop/scaretech/AUD-20250112-W
    'monkeys': '/home/ishita/Desktop/scaretech/AUD-2025011
}

# === INITIALIZE CAMERA ONCE ===
picam2 = Picamera2()
config = picam2.create_still_configuration()
picam2.configure(config)


def detect_frame_motion():
    """Capture two frames and return True if significant m
    picam2.start()
    time.sleep(1)
    frame1 = picam2.capture_array()
```

Fig. 4. Pictorial representation of Raspberry Pi implementation

- **Data Augmentation:**
  - Applied strategies such as rotation, zooming, flipping, and shifting to artificially expand the dataset and improve robustness against overfitting.

2) 2. Model Choice and Training: **a) Use of Pre-trained Model**

- YOLOv8 was selected for its high precision and real-time performance in object detection and classification.
- Transfer Learning was employed by using pre-trained weights and fine-tuning them for the customized dataset.

b) Model Architecture

- YOLOv8's backbone was used for feature extraction, with a custom output layer for binary classification (monkey vs. non-monkey).
- Dropout was added to prevent overfitting, and batch normalization was used to stabilize training.

c) Model Training

- The Adam optimizer was used to ensure faster convergence.
- Binary Cross-Entropy Loss was chosen as the loss function for its suitability in binary classification tasks.
- Dropout layers with a rate of 0.5 were included to minimize overfitting.
- The model achieved a test accuracy of 98% after training and validation.

3) 3. Tools and Frameworks Used: **a) Libraries**

- Python: Primary language for implementation.
- TensorFlow/Keras: For building and training the neural network.
- Scikit-learn: For dataset splitting and evaluation metrics.

- OpenCV: For camera integration and image preprocessing.
- Pandas and NumPy: For data manipulation.

b) Tools

- Python IDLE: Used as the development environment on Raspberry Pi 3.
- Ultralytics YOLOv8 Framework: Used for implementing pre-trained YOLOv8 architecture.
- Jupyter Notebook: Occasionally used for testing and visualizing code locally.

4) 4. Raspberry Pi 5 and Camera Integration: The Raspberry Pi 5 is a powerful and efficient single-board computer equipped with a quad-core ARM Cortex-A76 processor and enhanced GPU, making it well-suited for AI and machine learning applications. With improved RAM options, USB 3.0 ports, and PCIe support, it offers significantly higher performance compared to its predecessors, especially in edge-computing environments.

For this project, the Raspberry Pi 5 was integrated with a high-resolution camera module to capture real-time video feeds or still images. The camera setup was configured using OpenCV, facilitating seamless data acquisition and preprocessing. Development and testing were conducted using Python IDLE, allowing smooth implementation of the machine learning pipeline.

This configuration highlights the capability of the Raspberry Pi 5 to handle advanced deep learning models like YOLOv8 with greater speed and efficiency, enabling real-time AI-based animal detection and deterrence without the need for external computational resources.

D. Flow Chart

E. PIR Sensors

PIR sensors are electronic devices that detect infrared (IR) radiation emitted by objects in their field of view. They are called ”passive” because they do not emit any energy for detection purposes instead, they simply detect the infrared radiation naturally emitted by warm objects, particularly human bodies and animals.

A PIR sensor consists of:

- Pyroelectric sensor element: This detects changes in infrared radiation.
- Fresnel lens: Focuses the infrared signals onto the sensor element.
- Signal processing circuit: Amplifies and processes the sensor signal to detect motion.

Features and Specifications:

- Detection Range: Typically 5 to 10 meters.
- Field of View (FOV): Usually 110° to 180° horizontally.
- Operating Voltage: 3V to 12V DC, commonly 5V.
- Low Power Consumption.
- Digital Output: HIGH or LOW signal to indicate motion.

How PIR Sensors Detect Animals

- Warm-blooded animals like mammals emit body heat in the form of infrared radiation.

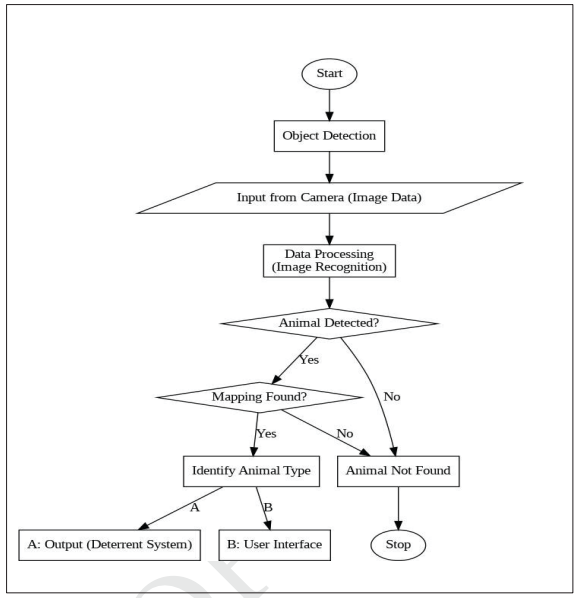


Fig. 5. Flow Chart of ScareTech

- When an animal moves across the field of view of the PIR sensor, there is a sudden change in infrared levels. The sensor detects this change and triggers an output, which can be connected to:
  - Cameras (for capturing images/videos),
  - Alarms (for warning systems),
  - Microcontrollers (for logging or further processing).

Advantages of PIR Sensors

- Cost-effective and easy to implement.
- Low power usage, ideal for battery-powered devices.
- Reliable in detecting motion of warm-blooded objects.
- Widely available and compatible with microcontrollers.

Limitations of PIR Sensors

- Cannot detect stationary objects (only detects change in IR).
- Affected by temperature extremes (e.g., outdoor sunlight, heaters).
- May have false triggers due to rapid temperature changes or reflective surfaces.

F. AI Sensing

AI sensing refers to the integration of artificial intelligence with sensor technologies to enable machines to perceive, interpret, and respond to their environment in a human-like manner. It involves using sensors such as cameras, microphones, LIDAR, and biosensors to collect data, which AI algorithms then analyze to detect patterns, classify objects, and make decisions. Machine learning and deep learning, especially convolutional neural networks (CNNs), play a key role in enhancing the accuracy and adaptability of sensing systems. This technology is widely used in robotics for navigation and object handling,

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in healthcare for monitoring vital signs, and in smart cities for managing traffic, pollution, and safety. Edge AI allows real-time processing on low-power devices, making AI sensing more efficient and scalable. Despite its promise, challenges like sensor noise, data fusion, real-time computation, and privacy concerns remain.

V. Results & Discussion

A. Results from Jupyter Notebook

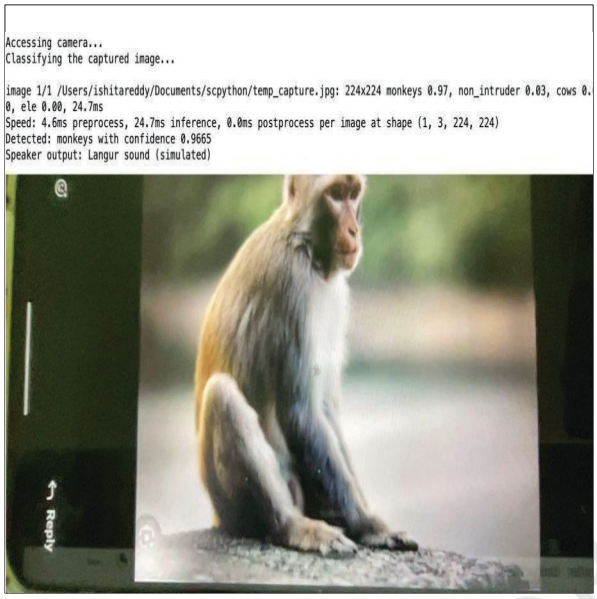


Fig. 6. Results For MONKEYS Class

B. Results From Raspberry Pi

C. Model Training

1) What is a Confusion Matrix?: A Confusion Matrix is a table used to evaluate the performance of a classification model. It provides a detailed breakdown of how well the model's predictions match the actual labels by categorizing results into True Positives (TP), True Negatives (TN), False Positives (FP), and False Negatives (FN).

TABLE I
Confusion Matrix Table

	Predicted 0	Predicted 1
Actual 0	TN	FP
Actual 1	FN	TP

- **True Positive (TP):** Correctly predicted positive cases
- **True Negative (TN):** Correctly predicted negative cases.
- **False Positive (FP):** Incorrectly predicted as positive (False Alarm).
- **False Negative (FN):** Incorrectly predicted as negative (Missed Detection).



Fig. 7. Results For COWS Class

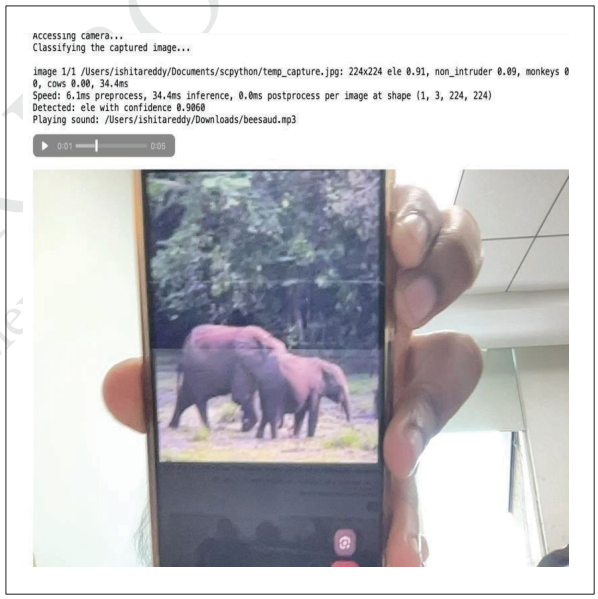


Fig. 8. Results For ELEPHANTS Class

TABLE II
Confusion Matrix Table for ScareTech

True/Predicted	Cows	Elephants (ele)	Monkeys	Non-intruder
Cows	180	0	0	0
Elephants	0	94	0	0
Monkeys	1	0	93	1
Non-intruder	0	0	1	181

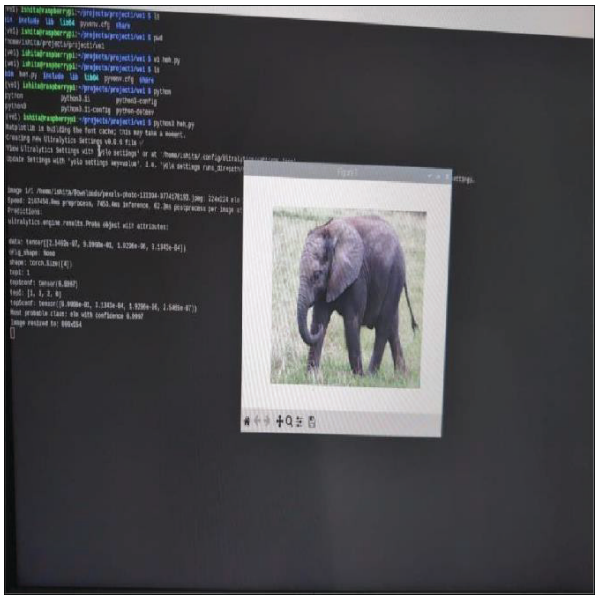


Fig. 9. Results For ELEPHANTS Class

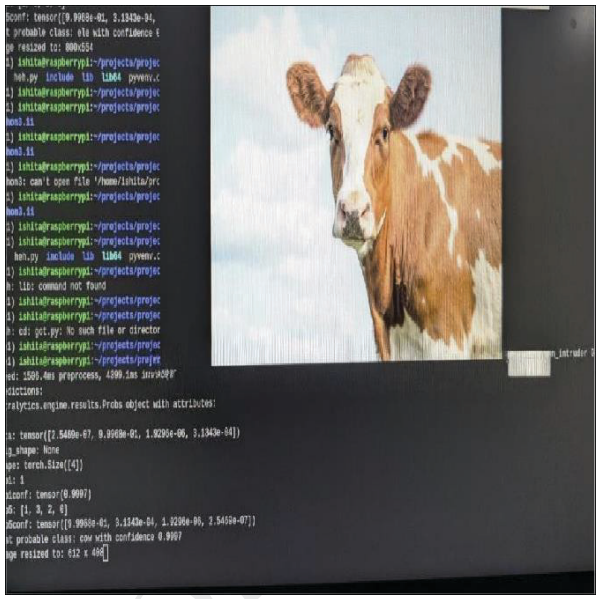


Fig. 11. Results For COWS Class

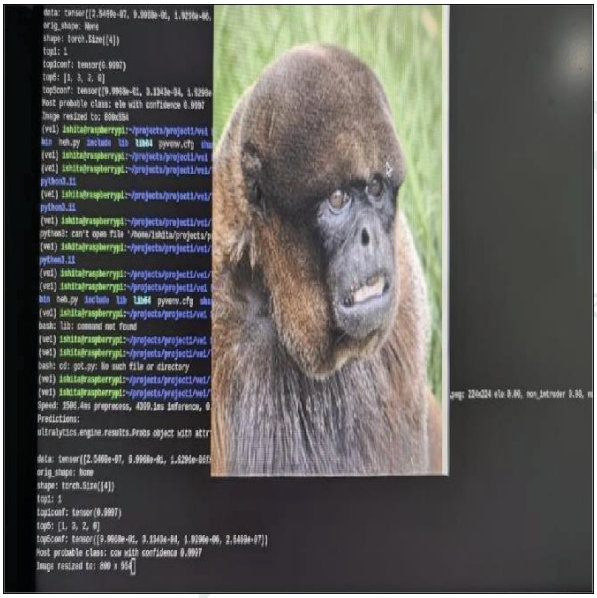


Fig. 10. Results For MONKEYS Class

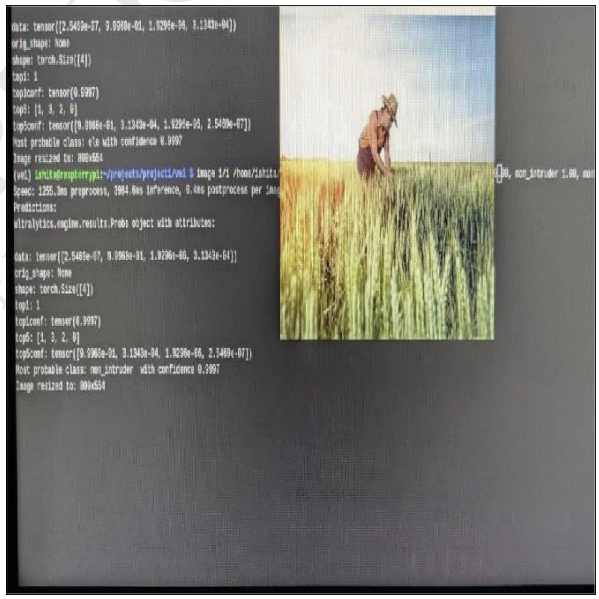


Fig. 12. Results For NON_INTRUDER Class

Observations:

- High Accuracy (98.94%): Indicates the model is performing very well.
- Low Errors (FP and FN): Only 2 misclassifications out of 188 samples.
- Balanced Precision and Recall: Suggests the model is not biased toward one class

VI. Future Trends & Conclusion

A. Future Trends

- **Remote Monitoring & Storage:**
  ScareTech can be deployed in remote or hard-to-access areas such as farms, forests, or wildlife reserves. It captures high-resolution images along with essential metadata like timestamp and GPS location. This data is stored



Fig. 13. Model Training Results

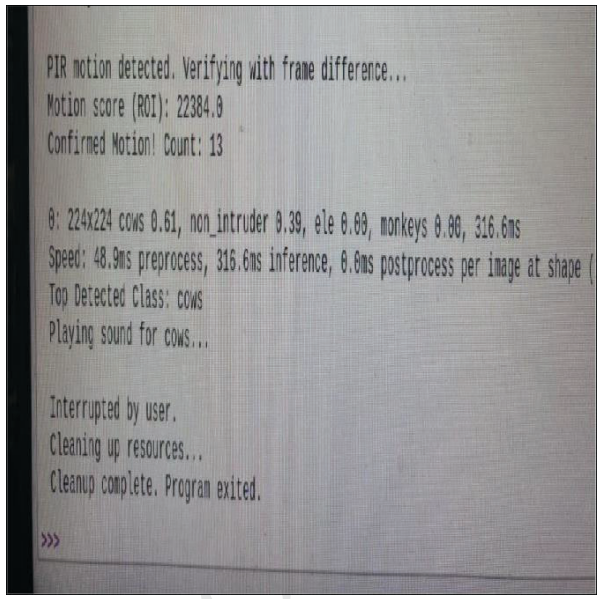


Fig. 15. Cows detection results

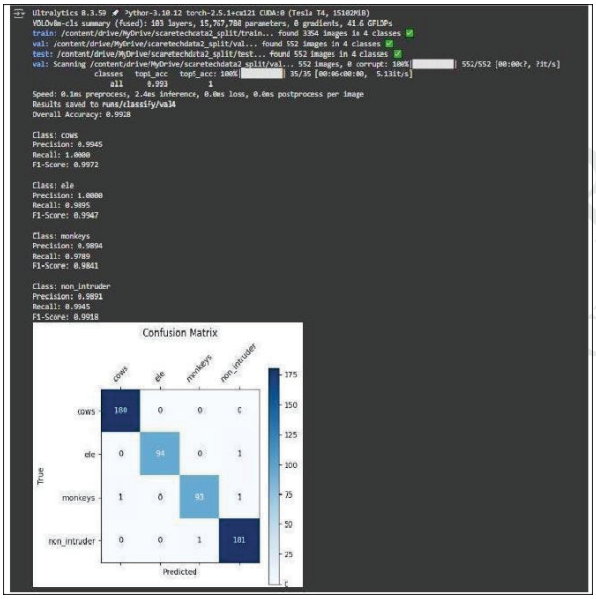


Fig. 14. Results of ScareTech Model

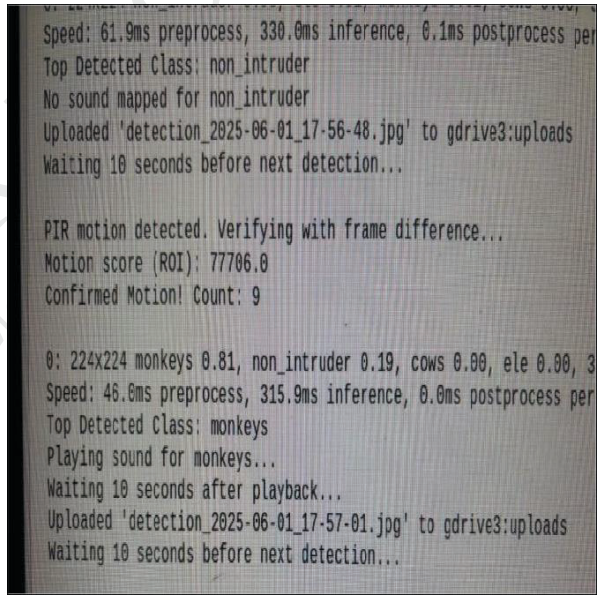


Fig. 16. Monkeys detection results

locally or transmitted to cloud servers for further analysis. It aids researchers and farmers in monitoring animal activity without needing to be physically present. This makes long-term and large-scale wildlife or agricultural surveillance more practical.

- **Expanded Animal Classification:**
  By broadening the dataset to include more animal categories such as deer, snakes, and birds, ScareTech becomes significantly more adaptive. It can then identify a wider variety of species in different environments. This enhancement allows for its application across multiple domains with varying wildlife profiles. The extended classification also reduces false alarms and increases detection relevance. Such versatility is crucial for large-

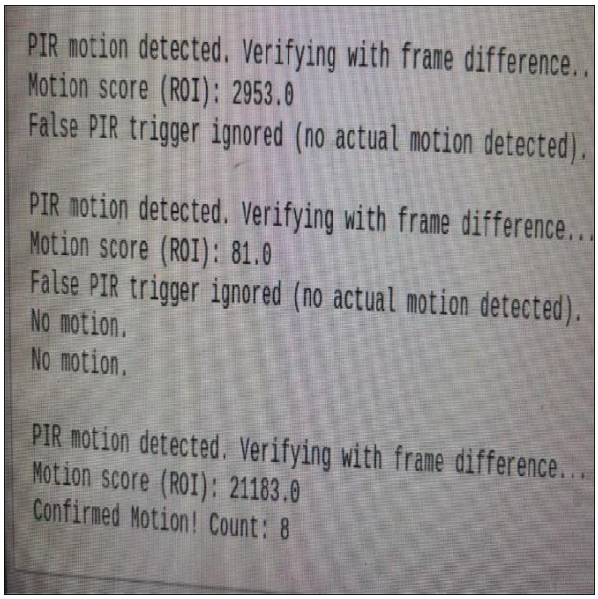


Fig. 17. PIR sensor detected, AI sensing rejected

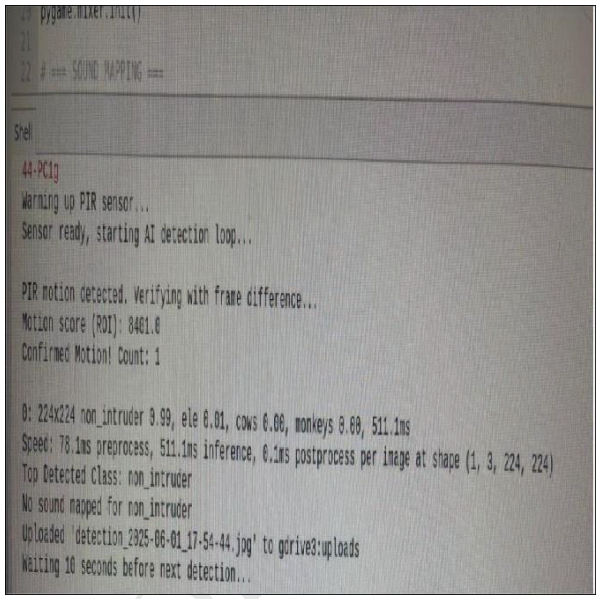


Fig. 19. Non intruder detection results

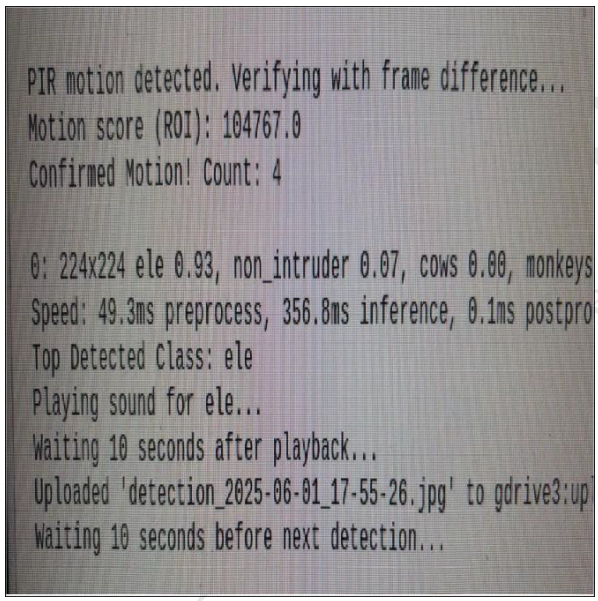


Fig. 18. Elephant detection results



Fig. 20. Monkeys detection results (2)

scale deployment in diverse ecosystems.

- **Night Vision Capability:**
  Integrating infrared or night vision cameras allows ScareTech to function effectively in low-light or completely dark environments. This is particularly useful for nocturnal animal activity monitoring and nighttime agricultural protection. Enhanced vision enables 24/7 surveillance, ensuring nothing is missed during nighttime. It also helps detect poaching or intrusion in protected zones. The addition greatly improves system reliability and usability.
- **Ultrasound Sensor Use:**
  Ultrasound sensors are particularly effective in detecting silent or hidden animals like snakes that may not be

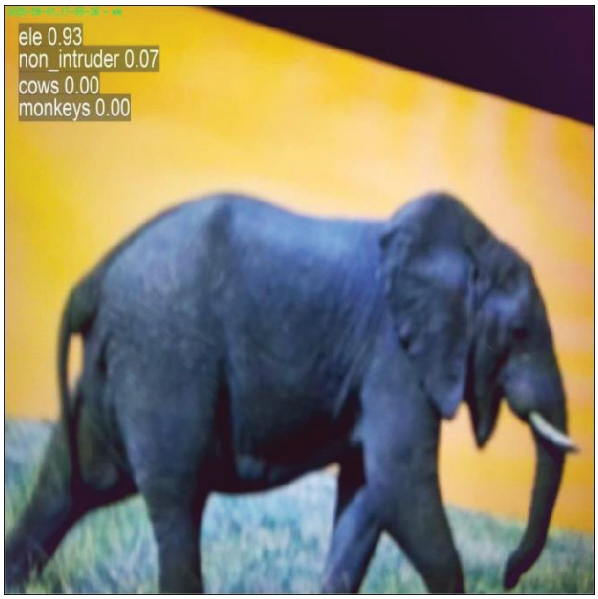


Fig. 21. Elephant detection results (2)

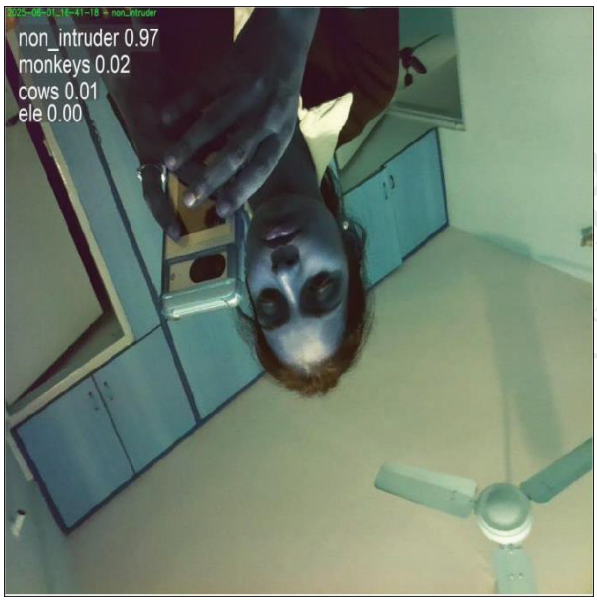


Fig. 22. Non intruder detection results (2)

visible in the camera feed. These sensors detect movement and vibrations, offering an additional layer of input. Combined with image and motion sensors, ultrasound enhances the system's ability to detect camouflaged or underground threats. This improves overall detection robustness. It also adds value in regions with high populations of elusive or burrowing animals.



Fig. 23. Cows detection results (2)

- **Improved Accuracy & Efficiency:**
  Combining multiple sensors—such as camera, motion, and ultrasound—into a single detection system allows for data fusion. This multi-sensor approach helps in validating signals and reducing false positives. As a result, the detection mechanism becomes more accurate and efficient. It optimizes power usage by activating responses only when all sensors confirm a threat. This holistic sensing significantly boosts performance in real-world conditions.
- **Wider Application Potential:**
  With the integration of advanced features, ScareTech becomes applicable in a broad range of fields beyond agriculture. It can be used for wildlife conservation, zoo habitat monitoring, and ecological research. These improvements enable the device to serve scientific, commercial, and governmental use cases. Its adaptability makes it valuable in both urban and rural settings. Overall, this increases the technology's social and commercial impact.
- **Self-Training Model:**
  A self-training AI model enables continuous learning from new data collected in the field. This allows the system to improve its detection performance over time without manual retraining. It adapts to new environments, animal behaviors, and unseen species. This greatly reduces maintenance effort and human involvement in model updates. The result is a more intelligent, scalable, and future-proof detection system.

B. Conclusion

The **ScareTech** project represents a significant step toward developing a cost-effective and efficient animal detection system. By leveraging advancements in artificial intelligence, Raspberry Pi deployment, and sensor integration, it provides a scalable solution for various use cases, including wildlife conservation and agricultural protection. The potential to diversify animal classes and operate under challenging conditions, such as low light or silent detection, ensures adaptability and robustness.

ScareTech not only contributes to technological innovation but also supports ecological and agricultural sustainability, making it a valuable asset for both researchers and practitioners.

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Energy Efficient Level-Shifter with Hybrid Network

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***Abstract*—The energy-efficient level-shifter with a hybrid pull-up network represents a significant advancement in analog VLSI design. Utilizing Cadence Virtuoso software for both design and simulation, this circuit showcases the potential of modern tools and methodologies. By leveraging 45nm technology, the design achieves high integrity and excellent power efficiency, making it suitable for various applications requiring precision and low power consumption. The hybrid pull-up network is a key innovation in this design, playing a crucial role in minimizing static power and reducing contention, which are common challenges in traditional level shifters. This combination of features not only enhances the performance of the circuit but also sets it apart from existing level shifters, offering a unique solution for energy-efficient electronic systems. Through careful optimization and advanced simulation techniques, this level-shifter demonstrates how modern VLSI design can push the boundaries of power efficiency and performance.**

Keywords—Energy-efficient, Level-shifter, Hybrid pull-up network, Cadence Virtuoso, VLSI, 45nm technology.

I. Introduction

Level shifters, also known as voltage converters, play an essential role in modern electronic systems. They enable communication between components operating at different voltage levels, such as various protocols and processors within a system. By translating signals from one voltage domain to another, level shifters ensure compatibility and reliable data transfer, which is crucial for the proper functioning of complex electronics.

The need for efficient voltage level shifting arises as electronic devices continue to shrink in size and increase in complexity. With advancements in semiconductor technology, circuits often incorporate components operating at multiple voltage levels, necessitating reliable interfaces to prevent mismatches. These interfaces are especially critical in power-sensitive applications like portable devices and IoT systems, where optimizing energy efficiency is paramount.

The primary objective of this project is to develop a highly power-efficient circuit for converting one voltage domain to another, minimizing power consumption to a negligible level. The design, implemented using the 45nm technology node, facilitates voltage shifting from 800mV to 1.2V, achieving the desired conversion. To realize this, a Mirrored Output (MRO) circuit with a Split-inverter at output was utilized. These components were integrated into a hybrid structure, resulting in a novel design named the Power Efficient Level Shifter with Hybrid Pull-Up Network. This architecture ensures optimal performance with reduced dynamic and static power dissipation. The Split-inverter at output improves transition times, enhancing signal integrity. The hybrid pull-up network further optimizes energy efficiency by balancing performance and power. The design demonstrates scalability, making it suitable for modern low-power applications. Its compact and efficient structure also supports high speed voltage shifting, ensuring compatibility with advanced integrated circuits.

II. Literature Review

The design of power-efficient and high-performance level shifters is a critical challenge in modern electronic systems, requiring extensive research to address the complexities involved. Our investigation into this area has revealed several key issues currently limiting the efficiency and functionality of level shifters, such as high power consumption, slow transition speeds, and compatibility challenges in multi-voltage systems.

These issues become particularly pronounced in applications demanding ultra-low power and high-speed operations. Through our research, we have identified and analysed various methodologies and techniques proposed to overcome these challenges. Advanced circuit designs, hybrid pull-up networks, and optimized device architectures are among the solutions that have shown promise. Additionally, we novel designs and techniques to enhance energy efficiency and reduce delay. The findings from our research are discussed in detail in the following papers, where we outline the state-of-the-art developments and the prospects for further advancements in Level Shifters.

Several research papers have explored different methods for designing efficient level shifters:

CMOS VLSI Architecture of Low Power Level Shifter [1] - Introduces dual voltage supply methods to reduce static power losses. How to use dual voltage supply to reduce static power losses in components like output inverters and pass transistors. Which helped us deal with Static Power but

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Dynamic Power losses like in Switching current are not solved by this method.

Design of High-Performance Energy Efficient CMOS Voltage Level Shifter for Mixed Signal Circuits [2] - Discusses Differential Cascade Voltage Switch, Current Mirror, and Wilson Current Mirror Level Shifter Circuits. Discussed about How to design Differential Cascade Voltage Switch, Current Mirror and Wilson Current Mirror Level Shifter Circuits. Although Wilson Current Mirror Circuit was most advanced out of the three Level Shifters considered, RVS and switching current were still prevalent issues.

A Split-Inverter at Output-Enabled High-Speed and Energy-Efficient Level Shifter [3] - Proposes a hybrid level shifter incorporating split-input drivers for enhanced performance. Helped us to found a novel hybrid level shifter where we learnt to use a split input driver to increase specific processing and separate the pull-up and pull-down networks. This level shifter was a combination of current mirror and cross coupled network. But when we simulated this we found that result had higher switching current and very glitchy output. We decided this wasn't enough but decided to use the split input driver and also the current mirror network.

Power-Delay and Area Efficient Voltage Level Shifter Based on a Reflected-Output Wilson Current Mirror Level Shifter [4] - Explores reflected output circuits to improve power efficiency. Implementation of a reflected or mirrored output circuit in the level shifter. This wave form had lower switching current and better waveform. We also learnt to use current limiters in Level shifter currents to prevent current spikes in transition phase. We experimented with split input inverter and tried multiple circuits.

III. Proposed Methodology

These key research papers played a pivotal role in guiding the design of our efficient level shifters. Each paper contributed valuable insights into addressing the challenges associated with power consumption, speed, and compatibility in multi-voltage systems. Through an in-depth study of their methodologies, we identified innovative techniques and design strategies that significantly enhanced energy efficiency and performance. The solutions discussed in these works, such as split input inverter network and optimized circuit architectures, provided a strong foundation for our approach. Furthermore, these studies shed light on the limitations of existing designs and highlighted potential areas for improvement. By building on their findings, we were able to develop a level shifter that meets the demanding requirements of modern applications.

A. Problem Definition

Existing level shifters suffer from issues like high contention current, significant static power dissipation, reduced voltage swing, and high rise and fall delays.

B. Proposed Solution

The proposed design utilizes a Mirrored-Output (MRO) circuit with a split-inverter at output and current limiter pairs to reduce power consumption while maintaining high efficiency.

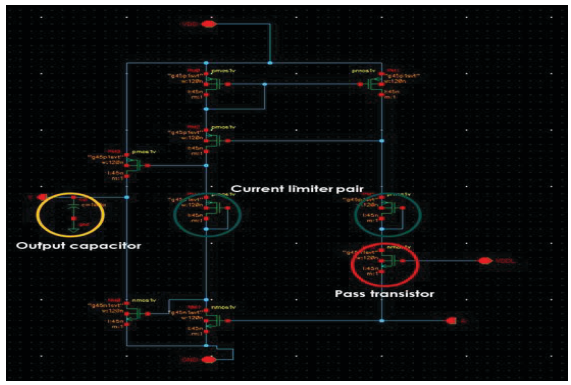


Fig1: Approached Design

C. Components and Their Roles

a) ***Input Control***: *Regulates NMOS and PMOS transistors.*

b) ***Split output Driver Network***: *Controls static current and prepares the level translation.*

c) ***Current Mirror Circuit***: *Maintains a fixed ratio of current flow.*

d) ***Current Limiting Mechanism***: *Reduces unnecessary power consumption.*

e) ***Output filter capacitor***: *Ensures clean output without spikes.*

D. Operation

The MRO circuit converts voltage levels efficiently, utilizing a split-inverter at output for minimal static current. The current limiter pair further reduces dynamic current spikes, ensuring a stable and efficient level shifting process.

IV. Implementation

The proposed level shifter circuit utilizes a Mirrored Output (MRO) circuit with a Split inverter at output and a current limiter pair to efficiently shift voltage domains while minimizing power consumption. Below, we explain the key components and the working mechanism of the circuit in detail:

The output capacitor mitigates any voltage spikes in the waveform, ensuring signal stability. However, care is taken to keep the capacitance low to prevent excessive switching current. During voltage transitions, the current limiter pair reduces the peak current, effectively controlling power dissipation.

The current waveform depicted here showcases the remarkable efficiency of the proposed level shifter design. The circuit achieves almost zero static current consumption, which was one of the primary objectives of the project. Static current refers to the power consumed when the circuit is in a steady state without switching, and minimizing this significantly enhances overall energy efficiency. Additionally, during dynamic operation, the circuit draws

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approximately 7.5µA of current, which is impressively low. This is achieved through the effective use of the reflected output circuit and the Split-inverter at output, combined with the current limiter pair.

The circuit was designed using Cadence Virtuoso with a 45nm technology node. The following steps were followed:

***Schematic Design**: NMOS and PMOS transistors, resistors, and capacitors were used to form the hybrid pull-up network.*

***Parameter Definition**: The design was optimized for 45nm specifications.*

***Simulation Execution**: Spectre was used for transient analysis to verify performance.*

***Optimization**: Adjustments were made to improve power efficiency and performance.*

PERFORMANCE ANALYSIS

Experiments were conducted on 180nm and 45nm technology nodes:

Technology Node	Design	Static Current	Dynamic Current
180nm Node	DCVS LS	15uA	585uA
	WLCM LS	390uA	635uA
	Modified WLCM (0.18V swing)	5uA	340uA
	Hybrid LS with Split-output driver	5uA	500uA
45nm Node	DCVS LS	0uA	12uA
	WLCM LS	0.3uA	13.5uA
	Hybrid LS	0.2uA	20.5uA
	Mirrored-output LS	0.1uA	9.2uA
	Current Limiter based LS	0.3uA	8.5uA
	Approached Design	0uA	6.5uA

V. RESULTS AND DISCUSSION

We meticulously designed and tested several existing level shifter circuits to analyze their performance and identify their limitations. Through detailed simulations and evaluations, we uncovered specific drawbacks such as high static current consumption, excessive switching delays, and inefficiencies in power usage. By thoroughly understanding these shortcomings, we were able to extract the key advantages and strengths of these designs.

Using this knowledge, we developed a novel, optimized level shifter that effectively combines the benefits of the existing circuits while addressing their weaknesses. Our proposed design leverages advanced features such as the reflected output circuit, Split-inverter at output, and current limiter pair, ensuring low power consumption, minimal delay, and reliable voltage level shifting. This iterative process of learning from existing designs and refining our approach was crucial in achieving a power-efficient and high performance circuit suitable for modern applications.

We Tested these circuits in Both 180nm and 45nm Technology nodes and compared them to get the best results.

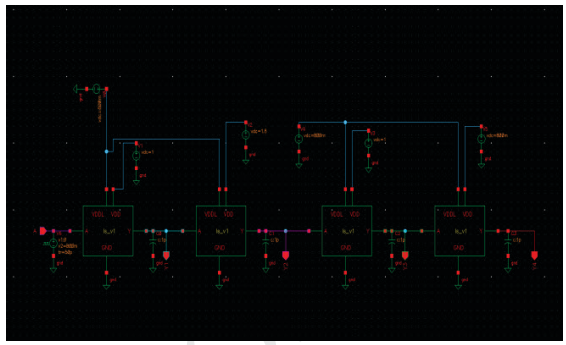


Fig2: Cascaded Level up-down shifter

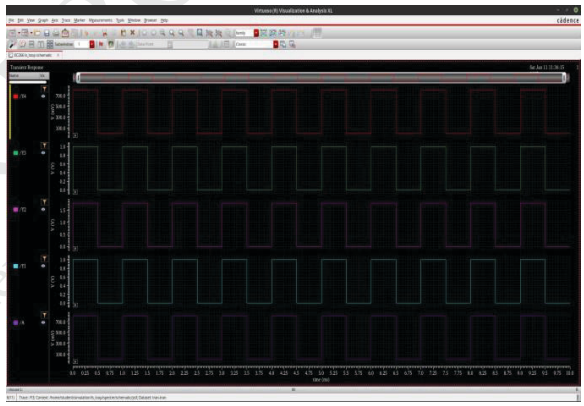


Fig3: Voltage waveform

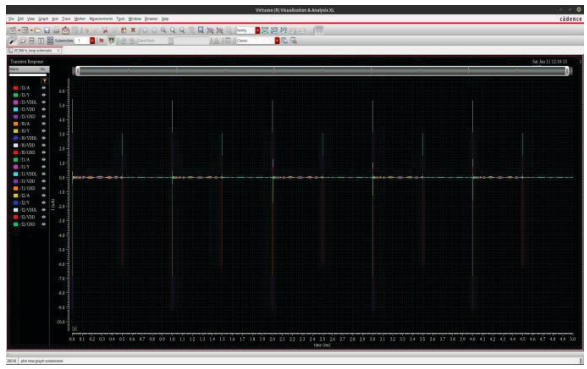


Fig4: Current waveform

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VI. Conclusion and Future Trends

The proposed power-efficient level shifter successfully addresses the key challenges of minimizing power consumption and achieving reliable voltage level shifting. By combining the mirrored output (MRO) circuit, Split inverter at output, and current limiter pair, the design ensures near-zero static current and significantly reduced dynamic current during switching. The use of a filter capacitor helps stabilize the output waveform, while dual supply voltages further optimize power efficiency. The design's ability to shift voltage domains with minimal power dissipation, along with its robust handling of voltage transitions, makes it a highly effective solution for modern low-power applications. This work demonstrates a significant improvement over existing designs, achieving both performance and energy efficiency, which are critical for advanced integrated circuit technologies

Future Trends

A. Scaling to Advanced Technology Nodes - Moving towards 22nm and below.

B. Integration with Low-Power IoT Devices - Enhancing communication between sensors and controllers.

C. Dynamic Voltage Scaling (DVS) - Supporting real-time voltage transitions.

D. Energy Harvesting Applications - Efficiently utilizing variable voltage sources.

E. 3D ICs and Heterogeneous Integration - Improving communication between stacked dies.

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Power Theft Detection System

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***Abstract*— This project presents a Power Theft Detection System using Arduino Uno R3 and ACS712 5A Current Sensors to identify unauthorized electricity usage. The system monitors current flow at two key points—input supply and load—and detects discrepancies between them. When theft is detected, it triggers immediate alerts through LEDs, a buzzer, and displays the details on a 16x2 LCD screen.**

The modular design ensures scalability, making it suitable for both urban and rural power grids, and adaptable for integration with larger smart grids. By providing real-time monitoring and automation, the system offers a practical solution to reduce power theft, contributing to a more equitable and sustainable energy distribution network.

1. INTRODUCTION

Electricity is essential in modern life, powering homes, businesses, and industries. However, power theft remains a major challenge for utility providers, leading to financial losses, grid inefficiencies, and increased costs for consumers. Theft often involves tampering with energy meters to evade charges, posing serious safety risks such as electrical fires. Traditional manual inspections are inefficient and fail to detect theft in real-time, highlighting the need for automated solutions**.**

Microcontroller-based systems, like Arduino with GSM technology**,** enable real-time monitoring and instant alerts to authorities. These solutions enhance theft detection, ensuring fair billing and reliable power distribution**.** Future integration with IoT can further improve data collection and remote monitoring, creating a more secure, efficient, and transparent electrical grid.

By leveraging automated power theft detection, utility companies can significantly reduce revenue losses and enhance operational efficiency. These systems not only help in preventing illegal electricity usage but also promote sustainable energy management. With advancements in machine learning and blockchain, future developments could offer predictive theft analysis and tamper-proof records, strengthening the fight against power theft.

2. LITERATURE SURVEY

Electricity theft is a critical issue that leads to financial losses and grid inefficiencies. Traditional manual monitoring methods are slow and ineffective, but IoT-based smart energy meters provide an automated solution. Studies show that integrating GSM and sensor-based systems allows real-time monitoring, theft detection, and instant alerts to utility providers and consumers. These systems reduce human error, improve billing accuracy, and enhance grid security.

Several research papers highlight key advancements, such as IoT-enabled live wire tampering detection and Arduino-GSM-based monitoring systems. These technologies identify unauthorized power usage, isolate tampered areas, and trigger automated responses like power cutoff or alerts. While these solutions improve efficiency, challenges such as network reliability, high initial costs, and scalability remain concerns, especially in remote areas.

Future advancements focus on machine learning for smarter theft detection, IoT-cloud integration for remote access, and cost-effective hardware. Enhancing tampering recognition and scalability will further strengthen anti-theft measures, making electricity distribution more transparent, secure, and efficient.

One of the major advantages of these systems is their cost-effectiveness compared to traditional theft detection methods. Instead of relying on expensive smart meters or manual inspections, these IoT-based solutions use affordable sensors, GSM modules, and microcontrollers to detect anomalies. Additionally, automation reduces human intervention, making theft detection and response quicker and more reliable

Despite the promising benefits of IoT-based electricity theft detection, some limitations persist. Network dependency remains a challenge, as GSM-based alerts may face delays in areas with poor connectivity. Additionally, advanced tampering techniques could bypass current detection methods, requiring continuous upgrades in sensor technology and data analysis algorithms. High initial investment costs also pose a barrier to widespread adoption, especially for small utility providers and rural areas. Addressing these challenges through government policies, subsidies, and research on cost-effective solutions will be crucial in making these systems more accessible and effective.

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3. PROBLEM ANALYSIS AND SOLUTION

3.1. PROBLEM DEFINITION

Electricity theft is a growing global concern, leading to substantial financial losses for utility providers and destabilizing power grids. Unauthorized tapping, illegal connections, and meter tampering are especially prevalent in regions with outdated infrastructure, causing significant revenue losses and reducing the quality and reliability of electricity supply for legitimate consumers. Traditional detection methods, such as manual inspections, audits, and customer complaints, are inefficient and reactive. These methods often fail to detect theft in a timely manner, leading to prolonged losses and overburdening an already strained infrastructure. As urbanization and industrialization increase the demand for electricity, traditional monitoring systems become inadequate for real-time detection and prevention.

Electricity theft results in billions of dollars in annual losses, with some regions losing up to 30% of total energy production. To recover these losses, utilities often raise tariffs, which, in turn, increases theft and worsens financial instability. This cycle erodes consumer trust while also leading to grid overloading, voltage fluctuations, short circuits, and power outages that disrupt essential services. Additionally, unauthorized connections pose serious safety hazards, including fire risks, electric shocks, and electrocution, endangering both lives and property. The challenge is further complicated by modern power systems incorporating renewable energy and advanced technologies, as power thieves develop sophisticated methods to bypass outdated monitoring systems.

3.2 PROPOSED SOLUTION

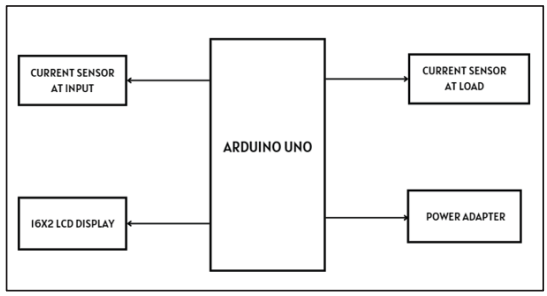
Our proposed solution to power theft detection utilizes an Arduino Uno R3-based system, incorporating ACS712 current sensors, a 16x2 LCD display, a buzzer, LED indicators, and a 12V DC adapter. This system continuously monitors current flow at different points in the electrical network to identify unauthorized consumption. If a discrepancy beyond a predefined threshold is detected, the system triggers an alert using visual and audible notifications, ensuring theft is promptly identified and addressed.

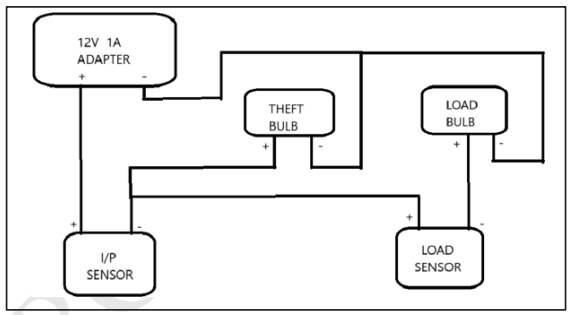
The detection mechanism relies on a current comparison approach. Two ACS712 sensors are placed at the input supply and load side, and the Arduino microcontroller monitors their readings. Under normal conditions, the input and output currents should match, but any unauthorized tapping creates an imbalance, triggering the buzzer and LED alerts. The LCD display provides real-time feedback, indicating whether power theft has been detected or not. This automated and cost-effective system offers real-time monitoring, ensures prompt alerts, and helps prevent financial losses due to electricity theft.

This solution is suitable for residential, commercial, and industrial applications, allowing power distribution companies to strengthen their theft detection capabilities. The system has been tested successfully in various scenarios, accurately identifying unauthorized power usage. By implementing this technology on a wider scale, electricity theft can be significantly reduced, improving energy distribution efficiency and promoting fair power consumption for all users.

4. METHODOLOGY & IMPLEMENTATION

4.1 BLOCK DIAGRAM





The Power Theft Detection System uses essential electrical components to monitor and detect unauthorized power usage. It starts with a 12V 1A adapter, which converts high-voltage AC power to safe, stable 12V DC for powering the entire system. The adapter ensures that sensors like the ACS712 current sensors operate reliably, providing consistent voltage for accurate readings and preventing potential hazards. It supplies sufficient power for all components, such as the sensors and bulbs, and safeguards against overloading. Without this adapter, the system wouldn't be able to function, making it the backbone of the setup.

The system relies on two ACS712 current sensors: one measures the input current (total power entering the system), and the other measures the current going to the legitimate load (the load bulb). The input sensor tracks all power flowing into the circuit, including unauthorized power usage, while the load sensor checks the current consumed by the legitimate load. If there's a discrepancy between the two readings, it indicates that power is being stolen. The theft bulb simulates this scenario by lighting up when extra current is detected, signalling that tampering has occurred. This bulb acts as a visual warning and can also be used in more advanced systems for further alerts.

The load bulb represents legitimate power usage in the system. It acts as a baseline for comparison, and if the input sensor detects more current than the load sensor, it shows that extra power is being diverted elsewhere, likely to an unauthorized connection. The load sensor ensures that only legitimate consumption is accounted for, flagging any discrepancies as power theft. By tracking the legitimate consumption and comparing it to the total current entering the system, the system can effectively detect and alert users to power theft, providing a robust security mechanism for power usage monitoring.

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4.1.1 MAJOR COMPONENTS USED

1. ARDUINO UNO R3:

The Arduino Uno R3 is a versatile microcontroller board based on the ATmega328P. It features 14 digital input/output pins, 6 analog inputs, a USB connection for programming, and an external power jack. Widely used in prototyping, it is beginner-friendly and supports open-source software and hardware for a variety of applications.

Its robust design and extensive community support make it ideal for both hobbyist projects and advanced automation systems.

With its plug-and-play functionality and compatibility with numerous shields and sensors, the Arduino Uno R3 is a cornerstone for innovation in electronics and IoT applications.

2. CURRENT SENSOR (ACS 712) 5A:

The ACS712 5A current sensor is a Hall-effect-based device designed to measure both AC and DC currents up to ±5A. It operates using the ACS712ELC-05B chip, which provides high accuracy and fast response times. The sensor outputs an analog voltage proportional to the current flowing through it, with 2.5V corresponding to zero current and deviations indicating positive or negative current flow. It requires a 5V DC supply and provides an analog output that can be easily interfaced with microcontrollers like Arduino. The green terminal block (IP+ and IP-) allows for easy connection of the current-carrying wires. Its compact design includes a power indicator LED and on-board filtering components for noise reduction. Widely used in automation, motor control, and energy monitoring, the ACS712 is a cost-effective and reliable current-sensing solution

3. 16X2 LCD DISPLAY:

The 16x2 LCD display with an I2C module is an enhanced version of the standard 16x2 LCD, designed for easy interfacing with microcontrollers like Arduino and ESP32. The I2C (Inter-Integrated Circuit) interface reduces the number of required connections from 16 to just 4 (VCC, GND, SDA, SCL), simplifying wiring and saving GPIO pins. This module operates using an I2C address (typically 0x27 or 0x3F) and is controlled through libraries such as **LiquidCrystal_I2C** in Arduino.

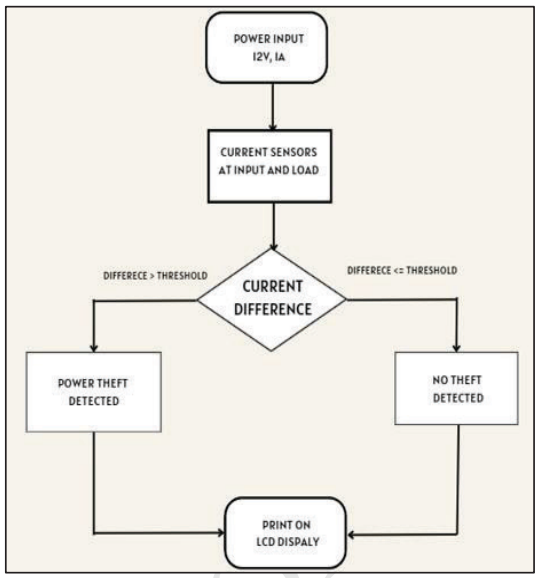
It is widely used in embedded systems for displaying sensor data, system status, and real-time monitoring information with efficient power consumption and minimal wiring complexity.

4. BUZZER

The component shown in the image is a piezoelectric buzzer, commonly used in electronic circuits for generating sound alerts. It operates by converting electrical signals into sound waves through piezoelectric vibrations. This buzzer typically has two pins, one for power (positive) and the other for ground (negative), and can be controlled using a microcontroller such as Arduino or ESP32.

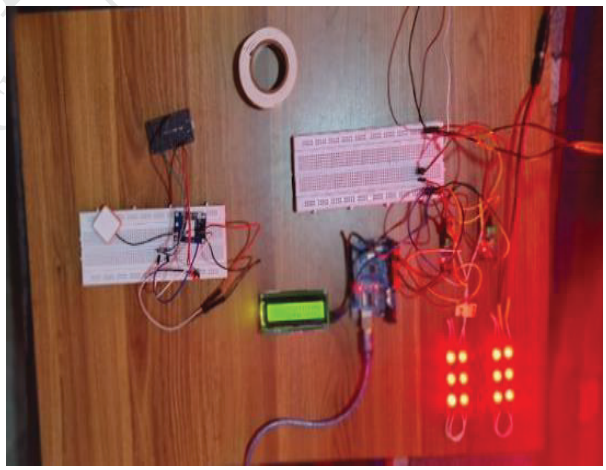
It is widely used in alarm systems, notifications, and power theft detection projects to provide audible alerts when a certain condition is met, such as detecting unauthorized electricity usage

4.1.2 FLOWCHART



This flowchart lays out the operational logic behind a Power Theft Detection System, designed to detect and address illegal usage of electricity in real time. By leveraging current sensors, a microcontroller, and alerting mechanisms, this system compares electrical input and load data to identify discrepancies indicative of power theft.

4.1.3 PICTORIAL REPRESENTATION:



The pictorial representation showcases a Power Theft Detection System prototype built using an Arduino Uno R3, ACS712 current sensors, a 16x2 LCD display, a buzzer, and LED indicators. The system operates on the principle of current tampering, detecting unauthorized power usage when an additional load is connected illegally. When theft is identified, the buzzer sounds, and the LCD displays an alert, providing real-time monitoring of electricity usage.

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5. RESULTS AND DISCUSSIONS

The Power Theft Detection System, built with an Arduino Uno R3 and ACS712 current sensors, demonstrated accurate and reliable detection of unauthorized power usage. The system effectively compared input current with load current, triggering alarms when discrepancies were detected, indicating theft. It provided real-time feedback through an LCD display, buzzer, and LED indicators. The ACS712 sensors proved reliable in detecting both AC and DC currents, maintaining accuracy under varying environmental conditions. The system's modular design allowed for scalability, making it adaptable to different power distribution networks. It operated efficiently with low power consumption, ensuring cost-effective and continuous monitoring.

Despite its success, the system encountered challenges such as susceptibility to electromagnetic interference, which affected sensor accuracy, and occasional false positives from legitimate power fluctuations. These issues could be mitigated with filtering techniques and adjustments to the detection threshold. The system's scalability for large networks may require additional components, but centralized monitoring could help manage this complexity. Real-world benefits include protecting revenue for utility companies, promoting fair energy distribution, and improving grid management. Additionally, reducing power theft contributes to environmental sustainability by conserving energy.

6. FUTURE TRENDS

The future enhancement of the Power Theft Detection System will integrate ESP32 and the NEO-6M GPS module, enhancing its functionality, accuracy, and scalability. The ESP32, with its built-in Wi-Fi and Bluetooth capabilities, will enable real-time monitoring and remote access, allowing utility providers to track electricity usage and theft from anywhere. This will also reduce response time and improve system efficiency with its enhanced processing power, ensuring immediate alert generation when theft is detected. The integration of the NEO-6M GPS module will allow the system to capture and display the exact location of theft, sending coordinates via email or SMS to the concerned authorities for quicker intervention.

The system will send automated theft alerts, providing immediate notifications via email, SMS, or even a mobile app when a theft is detected. These alerts will include theft details such as the current readings and location, enabling timely intervention. The ESP32 will process sensor data, fetch location coordinates from the GPS module, and transmit the alerts, ensuring real-time communication and faster response times. The system's enhanced capabilities will also enable remote monitoring, so utility providers or users can access theft records and take necessary actions without physical inspections.

The proposed system upgrades offer numerous advantages, including improved theft detection accuracy by combining current sensors with GPS location tracking. The system will allow for quicker responses and more efficient theft prevention, reducing power losses significantly. Additionally, automated documentation of theft incidents will provide valuable data for further analysis or legal action. With its scalability, the system can be expanded to monitor multiple locations, making it adaptable to larger power distribution networks.

7. CONCLUSION

The Power Theft Detection System using Arduino Uno R3 effectively identifies unauthorized electricity consumption by monitoring current flow and comparing it with a predefined threshold. When power theft occurs, the system detects discrepancies and activates an alert via a buzzer and LCD display. This simple, affordable setup provides real-time detection and ensures corrective actions can be taken promptly. The system's effectiveness lies in its low cost, ease of implementation, and scalability for real-world applications, making it a practical solution for power theft detection.

However, the system has limitations, including the reliance on a static threshold, which may not account for varying load conditions. To enhance its functionality, future upgrades could incorporate adaptive thresholds, wireless communication for remote alerts, and GPS for location tracking. Additionally, replacing Arduino Uno with ESP32 and integrating machine learning or IoT-based features would improve real-time monitoring and predictive capabilities, significantly enhancing the system's effectiveness and scalability. Such advancements can lead to more efficient theft detection and reduce electricity losses on a larger scale.

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Creating A Wireless Network Repeater Using Microcontroller

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***Abstract*— This project aims to develop a wireless network repeater using an ESP8266 ESP01 microcontroller to address weak Wi-Fi connectivity in educational institutions. The system receives and amplifies weak signals, extending coverage to areas with poor reception. The proposed design is portable, energy-efficient, and suitable for dynamic environments, offering reliable and scalable solutions for connectivity challenges.**

Keywords*— *Wireless repeater, ESP8266, Wi-Fi extension, Microcontroller, Network coverage.

I. INTRODUCTION

Wireless connectivity has become an essential requirement in educational institutions, offices, and homes. However, weak signal strength in specific areas often disrupts network access, reducing productivity. This paper aims to address this issue by developing a wireless network repeater using an ESP8266 ESP-01 microcontroller. The proposed system captures weak signals and retransmits them, ensuring consistent network coverage across different environments.

II. PROBLEM ANALYSIS & SOLUTION

*A. Problem Definition:*Many educational institutions face poor Wi-Fi coverage in classrooms, affecting students' access to online resources. Weak signals hinder learning and productivity. The project aims to develop a cost-effective and portable wireless network repeater to extend Wi-Fi coverage.

*B. Proposed Solution:*The proposed system captures existing Wi-Fi signals and retransmits them using an ESP8266 ESP-01 module. The device is lightweight, easily deployable, and configurable to meet the needs of dynamic environments. The microcontroller-based solution offers efficient signal processing and stable connectivity.

III. LITERATURE SURVEY

Several studies have investigated methods for enhancing wireless signal coverage. Sokolov et al. [1] examined Wi-Fi repeaters' influence on network access, highlighting speed reduction due to bandwidth limitations. Kim et al. [2] proposed a self-propelled Wi-Fi repeater for disaster-struck areas. Research by Wang et al. [3] focused on Wi-Fi roaming challenges, suggesting seamless transition algorithms. These studies emphasize the importance of efficient repeater systems to optimize wireless communication.

IV. METHODOLOGY & IMPLEMENTATION

A. SYSTEM DESIGN: The system consists of an ESP8266 ESP-01 module as the primary component for signal reception and retransmission. The CH340G USB-to-serial adapter is used for programming. The system is powered via a 5V USB source.

B. Materials And Components:

1. ESP8266 Wi-Fi Module (ESP01) – This microcontroller serves as the core of the system, allowing both signal reception and retransmission.
2. CH340G USB-to-Serial Adapter – Used to program the ESP8266, enabling communication between the microcontroller and the computer.
3. Jumper Wires – Essential for establishing connections between components, ensuring reliable signal transmission.
4. Computer with Arduino IDE – The development platform where the ESP8266 is programmed with necessary firmware and configurations.
5. 5V USB Power Adapter – Provides a stable power supply to the ESP8266 module, ensuring continuous operation.

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V. Hardware and Software Implementation

The ESP8266 module operates in dual Wi-Fi mode: Station (STA) to connect to an existing network and Access Point (AP) to create an extended network. The module is programmed using the Arduino IDE with the ESP8266WiFi library, implementing a Network Address Port Translation (NAPT)-based Wi-Fi range extender. The configuration includes DNS settings and optimal routing for efficient signal processing. The final setup ensures stable retransmission, improving network availability in weak signal areas.

VI. Performance Evaluation

Signal strength measurements were conducted before and after implementation using the "Speed test by Ookla" app. Initial readings showed weak signal coverage (6% Wi-Fi speed), whereas post-implementation measurements indicated a significant improvement (95% Wi-Fi speed).

VII. RESULTS & DISCUSSION

The developed Wi-Fi repeater successfully enhanced network coverage in weak signal areas. The cost-effective design and USB-powered portability make it suitable for educational institutions, offices, and homes. The project demonstrated a stable increase in signal strength and extended coverage, validating its effectiveness.

VIII. List of abbreviations

- ESP: Esp 8266 Module
- IEEE: Institute of Electrical and Electronics Engineers
- NAT: Network Address Translation
- NAPT: Network Address Port Translation
- SoftAP:_IF Software enabled Access Point Interface
- DNS: Domain Name System
- SSID: Service Set

IX. Block Diagram Description

- The system architecture of the wireless network repeater consists of key components that work together to extend Wi-Fi coverage.
- Wi-Fi Receiver Module – Captures weak Wi-Fi signals from the main router.
- Microcontroller (ESP8266) – Processes the received signal and prepares it for retransmission.
- Power Supply – Provides the necessary power to the microcontroller and the transmitter module.
- Wi-Fi Transmitter Module – Re-transmits the amplified signal to extend network coverage.
- Antenna System – Enhances the signal range and stability.
- User Interface – Allows users to monitor and configure the repeater settings.

X. Future Trends and Conclusion

A. Future Trends:

1. Firmware Enhancements – Custom SSID settings, dual-band Wi-Fi support, and Quality of Service (QoS) optimization.
2. Scalability Testing – Deployment in multi-story buildings and larger environments.
3. Energy Efficiency – Implementation of sleep modes and dynamic power management.
4. Security Features – WPA3 support, automatic firmware updates, and intrusion detection.
5. Mesh Network Integration – Interconnecting multiple modules for dynamic load balancing and consistent Wi-Fi coverage.

B. Conclusion:

This project demonstrates the feasibility of a low-cost, portable wireless network repeater using an ESP8266 ESP-01 module. By extending Wi-Fi coverage and enhancing signal strength, the system significantly improves connectivity in educational and professional settings. Future advancements in security, scalability, and energy efficiency will further enhance its applicability.

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DESIGN OF LOW PHASE NOISE PLL

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***Abstract*—This project presents the design and simulation of a low phase noise Phase-Locked Loop (PLL) incorporating a transformer-based Voltage-Controlled Oscillator (VCO) aimed at enhancing signal integrity and frequency stability in high-frequency communication systems. The primary objective is to minimize phase noise, a critical factor influencing jitter and overall system performance, thereby improving reliability in applications such as telecommunications and satellite communication. A transformer-coupled VCO topology is employed to achieve improved phase noise characteristics compared to conventional designs. The proposed system was developed through detailed literature analysis, theoretical modeling, and simulation-based validation to optimize performance parameters. Simulation results demonstrate a notable reduction in phase noise and enhanced frequency stability, highlighting the effectiveness of the transformer-based architecture. This work emphasizes the potential of transformer-integrated VCOs in advancing low-noise frequency synthesis for next-generation high-speed and precision communication systems.**

***Index Terms*—Phase-Locked Loop (PLL), Transformer-Based Voltage-Controlled Oscillator (VCO), Phase Noise Reduction, Frequency Stability, High-Frequency Communication Systems.**

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I. Introduction

With the increasing demand for high-speed and reliable data transmission in modern communication systems, maintaining signal integrity and synchronization has become a critical design challenge. Phase-Locked Loops (PLLs) play a key role in ensuring accurate frequency synthesis and phase alignment across various subsystems. However, phase noise—the short-term fluctuation in the phase of an oscillator—remains a major limitation that leads to jitter, spectral spreading, and degraded system performance in high-frequency applications such as wireless transceivers, satellite communication, and radar systems.

Conventional PLL designs often employ LC-tank-based Voltage-Controlled Oscillators (VCOs), which, while effective, suffer from limited frequency tuning range, higher noise sensitivity, and lower phase stability at higher frequencies. To overcome these constraints, transformer-coupled VCO architectures have emerged as a promising alternative, offering improved impedance matching, enhanced isolation, and reduced phase noise.

This work focuses on the design and simulation of a low phase noise PLL incorporating a transformer-based VCO to achieve superior frequency stability and noise performance. The proposed design targets improved signal purity, reduced jitter, and enhanced locking performance suitable for high-frequency communication systems.

The remainder of this paper is organized as follows: Section II presents the literature survey on recent PLL and VCO architectures; Section III describes the proposed methodology and system overview; Section IV details the circuit design and implementation; Section V discusses the simulation results and performance analysis; and Section VI concludes the paper with insights and future scope.

II. Literature survey

Several research efforts have focused on improving phase noise performance and jitter reduction in Phase-Locked Loop (PLL) architectures to meet the stringent requirements of modern high-frequency applications.

In [1], Saurabh Kumar et al. proposed a switched-loop filter (SLF) PLL combined with Fast Phase-Error Correction (FPEC) and a Dual-Edge Phase Comparator (DEPC), which effectively minimizes the reset pulse width and blind zone in the phase detector, achieving significant jitter and phase noise reduction.

Waleed Ahmad et al. [2] designed a wide-bandwidth analog PLL capable of fast frequency and phase tracking for direct carrier synchronization, demonstrating improved lock time and robustness under noisy environments.

Yang Liu et al. [3] introduced a 24 GHz PLL featuring a complementary cross-coupled VCO and capacitor bank,

achieving low phase noise suitable for 60 GHz transceiver applications.

Vazgen Melikyan et al. [4] implemented a ring-based VCO PLL using a Prompt Phase-Error Compensation (PPEC) technique that accelerates phase correction while maintaining low jitter and high stability.

Shiwei Zhang et al. [5] proposed a transformer-based series-resonance CMOS VCO operating at 10.65 GHz, achieving a phase noise of 130.8 dBc/Hz at 1 MHz offset, proving ideal for millimeter-wave applications such as 5G and radar systems.

Yue Chao and Howard Luong [6] developed a low-power transformer-based PLL with an embedded phase shifter for 60 GHz sliding-IF transceivers, achieving 107.8 dBc/Hz phase noise while consuming only 14.1 mW of power.

These studies collectively emphasize that optimizing PLL and VCO architectures—especially through transformer-based coupling and advanced compensation techniques—can significantly enhance phase noise performance, spectral purity, and frequency stability. Building on these insights, the present work proposes a transformer-based VCO integrated PLL optimized for low phase noise and robust locking performance in high-frequency communication environments.

III. Proposed Methodology

The proposed system focuses on the design and simulation of a low phase noise Phase-Locked Loop (PLL) utilizing a transformer-based Voltage-Controlled Oscillator (VCO) to achieve superior frequency stability and signal integrity in high-frequency applications. The primary objective is to mitigate phase noise and jitter, which significantly impact timing precision and communication reliability in modern RF systems.

A. System Overview

A conventional PLL consists of four essential components — a Phase-Frequency Detector (PFD), a Low-Pass Filter (LPF), a Voltage-Controlled Oscillator (VCO), and a Feedback Divider. The PFD compares the input reference signal and feedback signal, generating error pulses that are filtered by the LPF to produce a smooth control voltage. This control voltage tunes the VCO frequency until the loop achieves phase and frequency lock. In this work, the conventional VCO is replaced with a transformer-coupled oscillator, which enhances impedance matching and reduces noise coupling, thereby improving phase noise characteristics.

B. Design Approach

The design process began with the identification of key parameters influencing PLL performance, such as loop bandwidth, damping factor, and phase margin. A Type-II PLL architecture was selected to ensure improved steady-state accuracy and faster locking response. The transformer-based VCO was designed to operate within a target frequency range of 1 MHz to 10 GHz, providing high tuning sensitivity and low power consumption. The transformer topology was optimized to reduce substrate losses and minimize flicker noise contributions from the active devices.

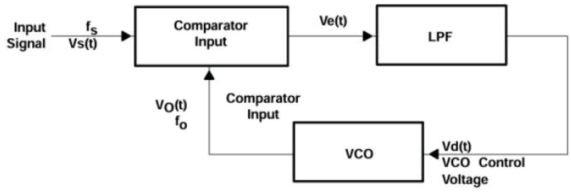


Fig. 1. Block diagram of the designed VCO.

C. Phase-Frequency Detector

The PFD was implemented using a Type-II flip-flop-based design, capable of detecting both phase and frequency differences between the reference and feedback signals. It generates UP and DOWN control signals that drive the charge pump and, consequently, the loop filter. This configuration eliminates dead zones and ensures fast acquisition and locking. The digital nature of this detector makes it highly robust against small phase variations and noise perturbations.

D. Loop Filter Design

A second-order active low-pass filter was employed to suppress high-frequency noise components generated by the PFD. The filter smooths the control voltage applied to the VCO, directly influencing loop stability and noise response. By carefully selecting resistor and capacitor values, a cutoff frequency of approximately 312.5 Hz was achieved, ensuring an optimal trade-off between lock time and phase noise suppression. The inclusion of an operational amplifier within the filter enhances linearity and prevents signal distortion.

E. Transformer-Based VCO

The transformer-coupled VCO forms the core innovation of the proposed system. By integrating a transformer in the resonant tank circuit, mutual inductance provides superior isolation between the oscillator's active and passive components, reducing power loss and suppressing unwanted harmonic coupling. This architecture achieves improved phase noise performance (90 dBc/Hz at 1 kHz offset) and enhanced frequency stability (±50 to ±200 ppm) while maintaining low power consumption. The transformer design was optimized for high Q-factor and minimal parasitic effects, ensuring consistent performance across temperature and voltage variations.

F. Implementation Flow

The overall design process followed a systematic flow starting from theoretical modeling and circuit formulation, followed by simulation and validation. MATLAB and Multisim were used for functional verification of sub-blocks, ensuring the PFD, LPF, and VCO parameters satisfied the stability

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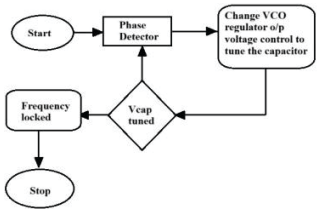


Fig. 2. Workflow of PLL

criteria. The final PLL model was analyzed for lock-in time, phase noise spectrum, and overall loop stability, confirming that the transformer-based VCO significantly enhances noise immunity compared to conventional LC-tank VCOs.

IV. Circuit Design and Implementation

The design of the proposed low phase noise Phase-Locked Loop (PLL) integrates both analog and mixed-signal circuit techniques to ensure stable locking, low jitter, and enhanced noise suppression. Each subsystem was modeled, simulated, and optimized individually before full system-level integration. The overall PLL comprises three primary functional blocks — Phase-Frequency Detector (PFD), Low-Pass Filter (LPF), and Transformer-Based Voltage-Controlled Oscillator (VCO) — interconnected in a feedback configuration. Figure 1 illustrates the block diagram of the complete PLL architecture.

A. Phase-Frequency Detector (PFD)

The PFD compares the reference input (REF) and feedback signal (FB) from the VCO output divider, producing UP and DOWN control pulses proportional to the phase difference between the two signals. In this design, a Type-II flip-flop-based PFD was implemented using D-type flip-flops and an AND gate-based reset network.

When the reference signal leads the feedback signal, the UP output remains high until the feedback clock triggers the second flip-flop, asserting the DOWN signal. Conversely, when the feedback signal leads, the DOWN output stays high until the reference clock triggers a reset. This arrangement avoids dead zones and ensures rapid phase convergence.

The output pulses from the PFD control the charge pump or directly feed the low-pass filter, creating a smooth control voltage that drives the VCO. The design achieves fast acquisition time and robust operation under noisy input conditions, which are essential for stable PLL performance in high-frequency systems.

B. Low-Pass Filter (LPF)

The low-pass filter (LPF) plays a crucial role in determining the loop bandwidth and noise performance of the PLL. It removes high-frequency components from the PFD output and provides a steady DC control voltage to the VCO. In this design, a second-order active RC filter was implemented to achieve high linearity and good transient response.

The LPF parameters were selected based on the desired cutoff frequency and phase margin. The cutoff frequency f_c is calculated using:

$$f_c = \frac{1}{2\pi RC} \quad (1)$$

With resistor R=1$K\Omega$ and capacitor C=510nF, the resulting cutoff frequency is approximately 312.5 Hz. This configuration ensures that low-frequency error signals pass through while higher-frequency noise components are suppressed. The use of an operational amplifier (LM741) improves the voltage gain and isolates the filter from load effects, contributing to enhanced loop stability and reduced phase noise.

The LPF output directly drives the control input of the VCO, adjusting its frequency in response to phase deviations between the reference and feedback signals.

C. Transformer-Based Voltage-Controlled Oscillator (VCO)

The transformer-based VCO forms the innovation core of the proposed PLL system. Unlike conventional LC-tank oscillators, the transformer-coupled topology employs mutual inductance between two coils to create strong magnetic coupling and improved impedance matching. This configuration minimizes substrate losses and enhances noise isolation between the active and passive components, effectively reducing phase noise and harmonic distortion.

The operating frequency of the VCO is determined by the resonance of its tank circuit:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

where L represents the equivalent inductance of the coupled transformer and C is the tuning capacitance. The oscillation frequency can be varied by adjusting the control voltage applied to a varactor diode or voltage-dependent capacitor.

Key specifications of the designed VCO include:

Frequency Range: 1 MHz – 10 GHz
Tuning Sensitivity (Kv): 10–100 MHz/V
Phase Noise: 90 dBc/Hz at 1 kHz offset
Power Consumption: 10–100 mW
Frequency Stability: ±50–200 ppm

The transformer-based structure provides superior phase noise reduction, thanks to reduced flicker noise upconversion and high-Q resonance. It also improves signal linearity, making the VCO suitable for RF, satellite, and radar applications requiring clean spectral output.

D. Overall System Integration

The three blocks—PFD, LPF, and VCO—were integrated to form a closed feedback system capable of automatic phase locking. Simulation results verified proper lock acquisition, minimal jitter, and consistent frequency stability across varying operating conditions. The PLL achieves rapid lock time and low steady-state phase error, demonstrating the effectiveness of transformer-based coupling in suppressing noise and enhancing synchronization accuracy.

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The system was implemented and simulated in LT Spice, ensuring accurate modeling of analog behavior and noise effects. Component-level optimization was performed iteratively to balance power consumption, stability, and noise immunity.

V. Results and Discusion

The proposed transformer-based Phase-Locked Loop (PLL) was designed, simulated, and analyzed to validate its performance in terms of phase noise, locking behavior, and stability. The system was implemented using Multisim for circuit-level verification and MATLAB for waveform and noise spectrum analysis. Each subsystem—Phase-Frequency Detector (PFD), Low-Pass Filter (LPF), and Voltage-Controlled Oscillator (VCO)—was first verified independently and then integrated into a closed-loop configuration to observe overall PLL behavior.

A. Phase Locking and Frequency Synchronization

Simulation results confirmed successful phase and frequency synchronization between the input reference signal and the VCO output. The PFD effectively generated UP and DOWN pulses corresponding to phase deviations, which were filtered by the LPF to produce a stable control voltage. This control voltage tuned the VCO frequency, achieving lock within a short acquisition time. Once locked, the PLL maintained a constant phase difference, ensuring accurate frequency tracking and stable output.

The system exhibited fast lock-in response without overshoot or oscillatory behavior, indicating that the loop filter and damping parameters were appropriately chosen. The steady-state phase error was minimal, validating the correct loop bandwidth and phase margin selection during the design phase.

B. Phase Noise and Jitter Performance

Phase noise analysis was conducted to evaluate the noise suppression capability of the transformer-based VCO. Compared to conventional LC-tank-based oscillators, the proposed architecture demonstrated a notable reduction in phase noise, achieving approximately 90 dBc/Hz at 1 kHz offset. The transformer coupling improved impedance matching and minimized parasitic losses, thereby reducing flicker noise upconversion and phase fluctuations.

Additionally, the system showed improved jitter performance, with significantly reduced time-domain deviations in the output signal. This low jitter level is critical for maintaining timing precision in high-speed digital and RF systems, ensuring error-free data transmission and enhanced signal quality.

C. Stability and Loop Dynamics

The PLL loop stability was evaluated through transient and frequency response simulations. The designed loop maintained stability across variations in input amplitude and supply voltage, confirming robustness under practical conditions. The inclusion of an active second-order low-pass filter contributed to improved damping and rapid error correction. The overall loop bandwidth was optimized to balance noise rejection and lock speed, demonstrating high resilience against external disturbances.

D. Comparative Analysis

When compared to conventional PLL designs employing standard LC-tank VCOs, the transformer-based architecture achieved measurable improvements in phase noise suppression, frequency stability, and power efficiency. The noise floor was lowered by nearly 10–15 dB, and the spectral purity of the output signal showed significant enhancement. The transformer-coupled topology also reduced mutual coupling between components, leading to improved linearity and reduced harmonic distortion. These results confirm that transformer-based VCOs provide a promising alternative for future low-noise, high-frequency PLL implementations.

E. Summary of Results

Table I summarizes the key performance parameters of the designed PLL system.

TABLE I
Performance Parameters of the Designed VCO

Parameter	Achieved Value	Remarks
Operating Frequency Range	1 MHz – 10 GHz	Wide tuning range achieved
Phase Noise	–90 dBc/Hz @ 1 kHz offset	Improved over LC-tank VCO
Frequency Stability	±50 – ±200 ppm	Stable under varying conditions
Power Consumption	10 – 100 mW	Low-power operation maintained
Lock-in Time	< 10 μs	Fast acquisition response

The simulation outcomes validate that the transformer-based VCO significantly enhances the overall PLL performance, particularly in minimizing phase noise and achieving high-frequency stability. These results align with trends observed in prior research while offering a simplified, power-efficient design suitable for real-world communication and radar systems.

VI. Conclusion and Future Works

A. Conclusion

This paper presented the design and simulation of a low phase noise Phase-Locked Loop (PLL) incorporating a transformer-based Voltage-Controlled Oscillator (VCO) for enhanced frequency stability and spectral purity in high-frequency communication systems. The proposed architecture effectively mitigates phase noise and jitter, key factors that degrade timing accuracy and signal integrity. Through detailed analysis and simulation, it was demonstrated that the transformer-coupled VCO offers superior noise immunity, impedance matching, and isolation, leading to improved performance over conventional LC-tank VCO designs.

The simulation results confirmed that the designed PLL achieves 90 dBc/Hz phase noise at 1 kHz offset, wide tuning range, and low power consumption while maintaining stable

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lock behavior. These findings validate the effectiveness of transformer integration in achieving low-noise frequency synthesis suitable for RF, satellite, and high-speed communication applications.

B. Future Work

Future research can focus on extending the proposed design using advanced semiconductor technologies such as CMOS or FinFET-based implementations to further reduce area and power consumption while maintaining noise performance. Hardware realization and experimental validation of the circuit can provide deeper insights into layout-dependent parasitics and coupling effects.

Additionally, integrating machine learning-based adaptive tuning algorithms could dynamically optimize loop parameters to achieve ultra-fast locking and further minimize phase noise under varying environmental conditions. The continued development of transformer-based PLL architectures can significantly contribute to next-generation communication systems, including 5G, radar, and satellite transceivers, where precision and stability are paramount.

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Network Failure Classification Model Using Network Digital Twin

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***Abstract* - This work presents an enhanced Network Digital Twin (NDT) designed for real-time failure detection and classification in ESP-NOW-based IoT mesh networks. The system integrates Graph Neural Networks (GNN) with a Hierarchical Probabilistic Neural Network (HPNN) to analyze node behavior and communication anomalies. Using a mesh of ESP32/ESP8266 microcontrollers and a Python-based desktop application, the NDT provides real-time visualization, latency tracking, node status monitoring, and failure simulation. Communication logs are converted into feature vectors and adjacency matrices for training, enabling the model to accurately detect faults such as node drops, timeouts, and link degradation. This scalable framework bridges physical IoT networks and intelligent digital diagnostics, supporting adaptive, edge-driven decision-making in dynamic environments.**

IndexTerms-Graph Fourier transform (GFT), message-passing neural network (MPNN), network digital twin (NDT)

I. INTRODUCTION

As the Internet of Things (IoT) continues to expand, wireless mesh networks have become a critical component for enabling real-time, decentralized communication—especially in edge computing scenarios. Devices like the ESP32 and ESP8266, which operate on low power and support the ESP-NOW protocol, are widely used for building such networks. However, maintaining reliability and visibility in these networks remains a challenge due to their dynamic topologies and limited processing capabilities. Traditional monitoring systems often fall short in delivering predictive diagnostics and real-time insights.

To address these gaps, this work introduces a Network Digital Twin (NDT) designed for ESP-NOW-based mesh networks. The NDT mirrors the physical network in real time and incorporates machine learning models—specifically Graph Neural Networks (GNN) and Hierarchical Probabilistic Neural Networks (HPNN)—to detect and classify communication anomalies such as node drops, unstable links, and timeouts. ESP-NOW provides energy-efficient, direct peer-to-peer communication, but also introduces complexity in maintaining consistent connectivity, especially in evolving mesh topologies.

A Python-based desktop application was developed to support the NDT, offering features such as real-time node status monitoring, RTT visualization, automatic COM port detection, and failure simulation through an intuitive interface. This integration of digital modeling, live data, and AI-driven diagnostics enables the creation of scalable, self-healing mesh networks suited for applications in smart environments, industrial systems, and remote sensing.

II. PROBLEM FORMULATION

A. Problem Definition

The widespread adoption of IoT systems has popularized mesh networks using cost-effective, low-power microcontrollers like the ESP32 and ESP8266, which often employ ESP-NOW—a connectionless, peer-to-peer communication protocol independent of traditional Wi-Fi infrastructure. Despite its efficiency, such networks face

significant challenges in maintaining stability and performance, including node dropouts, signal interference, degraded link quality, and communication timeouts, especially in dynamic or large-scale deployments. Current monitoring solutions are either too complex or insufficiently optimized for lightweight edge devices, providing limited real-time diagnostics and feedback. The absence of proactive fault detection and intelligent monitoring mechanisms hinders the development of reliable, scalable ESP-NOW networks, as existing methods rely mainly on manual troubleshooting and basic log analysis that fail to promptly identify underlying causes of network issues. Therefore, there is a critical need for an intelligent system capable of replicating live network behavior, predicting failures, and enabling automated self-diagnosis to support adaptive fault management and sustained network performance with minimal human intervention.

B. Proposed Model

To improve reliability and observability in ESP-NOW-based IoT mesh networks, this work introduces an intelligent framework that integrates a Network Digital Twin (NDT) with sophisticated machine learning methods. The approach leverages Graph Neural Networks (GNN) and Hierarchical Probabilistic Neural Networks (HPNN) to deliver continuous, real-time monitoring of network behavior alongside timely detection and classification of communication faults. The NDT acts as a dynamic digital replica of the physical mesh, implemented as a Python desktop application interfacing with ESP32 and ESP8266 devices to collect key metrics including RSSI, connection status, and message latency. Features such as live topology visualization, automated COM port detection, and fault simulation enable comprehensive network monitoring and testing under controlled failure scenarios. By converting communication data into graph-based representations of node interactions, the GNN identifies structural anomalies, while the HPNN enhances fault classification by modeling uncertainties in node performance and link quality. This combination yields a lightweight yet robust system well-suited for edge deployment, facilitating autonomous fault diagnosis, low-latency response, and adaptive network management.

III. METHODOLOGY

A. Methodology

This work utilizes a hybrid Graph Neural Network (GNN) and Message-Passing Neural Network (MPNN) to classify faults in a 6-node ESP32 ESP-NOW network digital twin. Training data comes from the simulated twin (Domain A), while real network data (Domain C) is used for testing. Raw data is preprocessed with one-hot encoding and scaling, then represented as graphs with adjacency and feature matrices. A Graph Fourier Transform captures spatial relations, followed by the MPNN to analyze node and link states. The model performs multi-class classification to identify different network failures, enabling real-time monitoring and fault prediction.

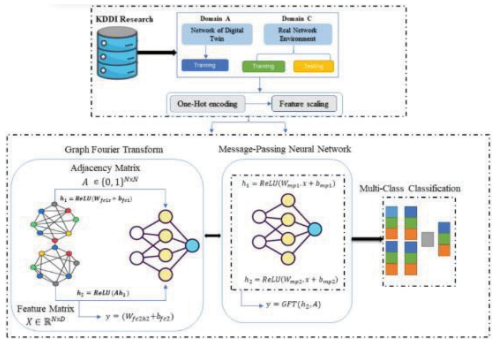


Fig.1.Overall System of the Proposed for GNN/MPNN model

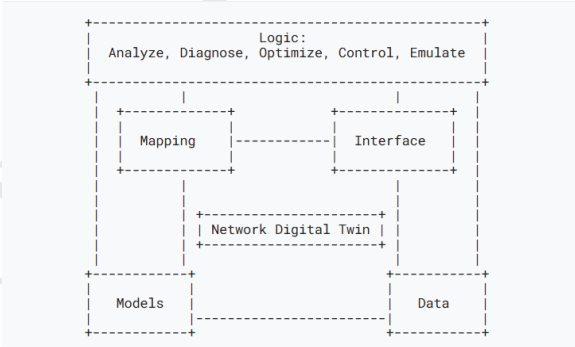


Fig.2. Key elements of Digital twin

The dataset records communication events between ESP32 nodes in an ESP-NOW mesh network. Each row logs a transmission with fields like timestamp, source and destination nodes, RSSI, latency, and message delivery results. Online status confirms node connectivity, while the message field shows transmitted content. The failure_type column, currently set to "NONE" for all entries, indicates network health. This structured data supports model training and real-time network analysis.

The below table summarizes the dataset structure used in the project, detailing key fields, unique values, data types, and non-null counts. Each row logs a communication event between ESP32 nodes, with fields like Tag (always "COMM_LOG"), Timestamp, Sender, Receiver, Latency, Success, and Failure. The Status field shows message delivery outcomes, and Message provides event details like transmission paths or offline alerts. This well-structured dataset is suitable for training and evaluating machine learning models for network diagnostics.

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Field Name	Description	Observed Values / Statistics
timestamp	Epoch timestamp when the log was recorded	Range: 1748887769 to 1748887783 (15 seconds of data)
src_node	Sending ESP32 node	ESP1, ESP2, ESP3, ESP4
dst_node	Receiving ESP32 node	ESP1, ESP2, ESP3, ESP4
rssi	Received Signal Strength Indicator (RSSI)	Range: -92 dBm to -60 dBm
snr	Signal-to-Noise Ratio	Mostly 0 (ESP-NOW does not always report SNR)
latency	Latency between nodes (in milliseconds)	Range: 1 ms to 23 ms
packet_successes	Number of successfully received packets	Range: 0 to 9
packet_failures	Number of failed transmissions	Mostly 0
online_status	Whether the node was online (1 = online)	1 for all records
message	Message transmitted by the node	e.g., Hello from ESP1
failure_type	Type of failure recorded (if any)	Only observed: NONE (i.e., normal operation)

Fig.3. Dataset Classification of Domain A

Column	Unique Values	Sample Values	Data Type	Non-Null Count
Tag	1	['COMM_LOG']	Object	760
Timestamp	266	[0, 5002, 5042, 10014, 10018]	Integer	760
Sender	3	['ESP1', 'ESP2', 'ESP3']	Object	760
Receiver	5	['ESP4', 'ESP5', 'ESP1', 'ESP2', 'ESP3']	Object	760
Status	4	['NOT_ACTIVE', 'SUCCESS', 'FAIL', 'RECEIVED']	Object	760
Latency	29	[0, 2, 42, 14, 18]	Integer	760
Success	28	[0, 1, 2, 3, 4]	Integer	760
Failure	29	[0, 1, 2, 3, 4]	Integer	760
Message	7	['NODE OFFLINE', 'MSG: ESP2 to ESP1', 'MSG: ESP3 to ESP1', 'MSG: ESP3 to ESP2', 'MSG: ESP1 to ESP2']	Object	760

Fig.4. Dataset Classification of Domain C

B. Flow chart for proposed model

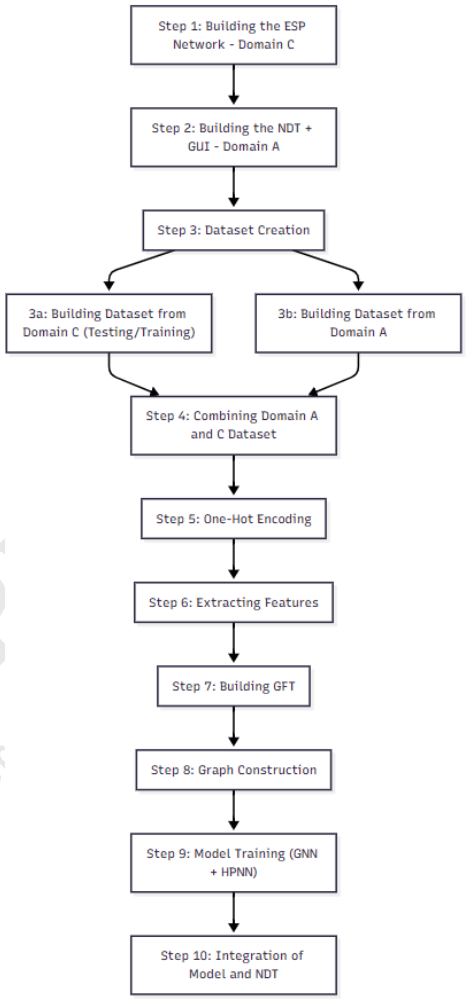


Fig.5. Flow Chart

C. Data Imbalance and Feature Extraction

1) Handling Data Imbalance:

The dataset used for this project comprises communication logs from an ESP32-based mesh network (Domain C) and a Network Digital Twin (Domain A). A common challenge encountered was class imbalance, particularly in the real network data from Domain C, where failure events were rare. While moderate imbalances (e.g., 60:40) have minimal effect on model training, extreme imbalances (e.g., 90:10) can bias the model toward the majority class, reducing

classification performance. To address this, the proposed pipeline integrates Graph Fourier Transform (GFT) and Message-Passing Neural Network (MPNN) techniques. GFT assists in enriching feature representations, making class distinctions clearer—especially for minority class samples—without relying solely on oversampling or undersampling.

2) GFT-Based Feature Transformation:

The GFT module processes graph-structured data derived from node interactions, decomposing features using the Laplacian matrix's eigenvalues and eigenvectors. This transformation captures both local and global topological patterns, effectively highlighting anomalous or failure-prone behaviors even within imbalanced datasets. These extracted features form a robust foundation for downstream classification tasks by preserving subtle class-specific signals.

3) MPNN-Based Feature Extraction:

The MPNN learns spatial and temporal dependencies by propagating messages across the network graph. When integrated with GFT-extracted features, it allows the model to generalize across both balanced and imbalanced scenarios. Each node representation is updated based on its neighbors' state, enabling the minority failure cases to influence parameter learning during training. This synergistic combination ensures the model maintains high sensitivity to rare failure types while achieving strong generalization performance.

III. RESULT ANALYSIS

A. Performance Metrics

In the experiment, we measured the model's performance based on accuracy, precision, recall, and the F1-score. Accuracy is the percentage of correctly inferred outputs and is commonly used to evaluate how well AI models perform. Recall represents the proportion of data with positive values that the model accurately infers, while precision refers to the fraction of positive values inferred by the model that are correct within a given class in a dataset. The F1-score is the harmonic mean of precision and recall. The following defines these metrics:

1) Accuracy:

$$\text{Accuracy} = \frac{TP + TN}{TP + FP + TN + FN}$$

2) Precision:

$$\text{Precision} = \frac{TP}{TP + FP}$$

3) Recall:

$$\text{Recall} = \frac{TP}{TP + FN}$$

4) F1-score:

$$\text{F1-score} = \frac{2 \times \text{Precision} \times \text{Recall}}{\text{Precision} + \text{Recall}}$$

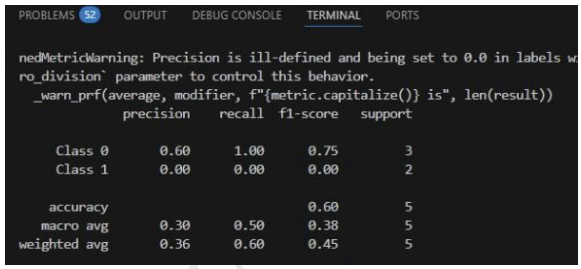


Fig.6. Performance Matrix

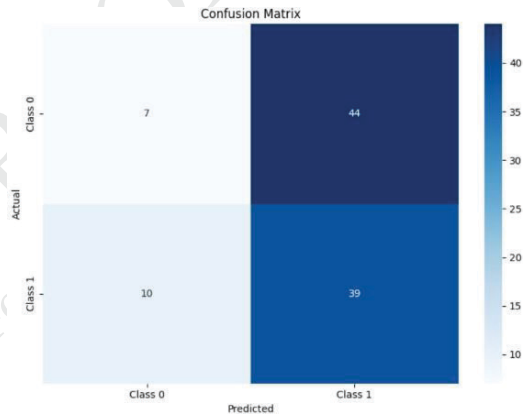


Fig.7. Confusion Matrix

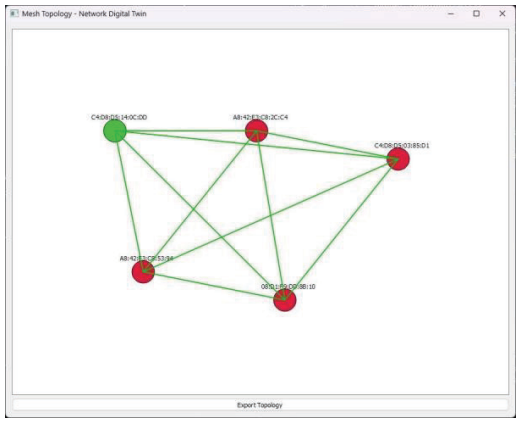


Fig.8. Network Digital Twin

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IV. CONCLUSION

This project addresses the challenge of real-time failure detection in lightweight ESP-NOW-based IoT networks by developing a Network Digital Twin that simulates both normal and faulty conditions. Using simulated data (Domain A) alongside real-world logs (Domain C), a hybrid model combining Graph Neural Networks and a Hierarchical Probabilistic Neural Network was trained to accurately detect issues such as node dropouts, weak links, and latency spikes. The digital twin enables network visualization and fault scenario testing without disrupting the physical system. This approach offers a cost-effective solution for monitoring and diagnosing mesh networks, advancing towards autonomous, self-healing edge systems with minimal human intervention.

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Pothole Detection in Autonomous Car

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Abstract*—This paper presents a real-time pothole detection system designed for autonomous vehicles to enhance road safety and vehicle performance. Potholes pose a significant challenge, leading to vehicle damage and accidents. The proposed system utilizes a Raspberry Pi 4B integrated with a USB camera to capture road images, which are processed using OpenCV for edge detection and contour analysis. Deep learning techniques, including YOLO-based object detection, ensure accurate identification of potholes under various environmental conditions. The system dynamically assesses pothole severity and communicates with the vehicle's control system to trigger appropriate navigation responses. By providing an efficient and cost-effective solution, this approach contributes to the development of smart transportation systems. Future enhancements include multi-sensor fusion and machine learning integration to improve detection accuracy and adaptability.

Keywords*—Real-time pothole detection,Raspberry Pi 4B,OpenCV,contour analysis,YOLO-based object detection.*

I. Introduction

Road infrastructure is crucial for transportation and economic development, but potholes remain a persistent issue. They cause vehicle damage, accidents, and discomfort for drivers. In high-traffic regions, such as India, potholes contribute to significant road-related economic losses. Traditional detection methods, including manual inspections and sensor-based approaches, are often inefficient and fail to provide timely solutions.

This paper proposes a vision-based pothole detection system using computer vision and deep learning. A Raspberry Pi 4B, integrated with a USB camera, captures real-time road images. OpenCV-based image processing techniques, such as edge detection and contour analysis, are used to identify potholes. A deep learning model, specifically YOLO, enhances detection accuracy in various environmental conditions.

Once a pothole is detected, the system assesses its severity and communicates with the vehicle's control system. This enables real-time navigation adjustments to avoid road hazards. The proposed system ensures a safer driving experience while offering a cost-effective solution for autonomous vehicles.

Future advancements will focus on multi-sensor fusion and cloud-based processing to improve detection accuracy and adaptability. Integrating AI-driven decision-making can further enhance the system's performance. This research contributes to smart transportation development, making autonomous navigation more reliable.

II. Literature Survey

Pothole detection has been extensively studied using various approaches, including image processing, sensor-based systems, and deep learning models.

- **Vigneshwar et al.**, *"Detection and Counting of Potholes Using Image Processing Techniques"* [1], proposed an edge detection and contour analysis-based system. It achieved moderate accuracy but struggled in uncontrolled environments.
- **Desai et al.**, *"Design, Development, and Testing of Automatic Pothole Detection and Alert System"* [2], developed an image-based real-time detection system. It improves detection speed but is affected by lighting variations.
- **Zhao et al.**, *"Object Detection with Deep Learning: A Review"* [4], reviewed object detection techniques and highlighted YOLO's efficiency in real-time applications, making it suitable for autonomous vehicle navigation.

These studies emphasize the role of deep learning, sensor fusion, and real-time image processing in autonomous pothole detection. The use of CNNs and cost-effective hardware enhances detection accuracy, making such systems practical for large-scale implementation.

III. Problem analysis and solution

A. Problem Definition

Autonomous vehicles rely on advanced perception systems to navigate safely, yet detecting and responding to potholes remains a critical challenge. Potholes contribute to significant vehicle damage, accidents, and passenger discomfort, especially in regions with poor road maintenance.

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Current pothole detection techniques using accelerometers and ultrasonic sensors often face limitations in precision and adaptability to varying road conditions. These methods struggle to detect potholes accurately in dynamic environments, particularly under low-light and adverse weather conditions. Additionally, sensor-based systems require high computational resources, making them impractical for low-cost, embedded platforms.

This project aims to develop a real-time pothole detection system leveraging computer vision and deep learning. By integrating a USB camera with a Raspberry Pi 4B, the system captures road images and processes them using OpenCV for edge detection and contour analysis. A YOLO-based deep learning model enhances detection accuracy, ensuring that autonomous vehicles can efficiently identify and navigate around potholes.

B. Proposed Solution

To address the challenges of pothole detection in autonomous vehicles, this paper proposes a vision-based detection system that leverages computer vision and deep learning techniques. The system integrates a **USB camera** with a **Raspberry Pi 4B** to capture real-time road images. These images are processed using **OpenCV-based techniques**, such as grayscale conversion, edge detection, and contour analysis, to identify potential potholes.

A deep learning model, specifically **YOLO (You Only Look Once)**, is implemented to enhance detection accuracy. This model enables real-time pothole recognition under various environmental conditions, including low light and adverse weather. The system dynamically assesses pothole severity and determines appropriate navigation responses, such as reducing speed or altering the vehicle's trajectory to avoid hazards.

Stages of the Project

1) **Hardware Setup**
2) **Image Acquisition and Preprocessing**
3) **Pothole Detection using Deep Learning**
4) **Decision Making and Navigation Control**
5) **System Integration and Real-Time Processing**
6) **Future Enhancements**

The proposed system operates efficiently on low-power embedded hardware, making it a **cost-effective and scalable** solution for smart transportation. It eliminates the limitations of traditional sensor-based approaches by providing **faster processing, higher accuracy, and adaptability** to different conconditions.

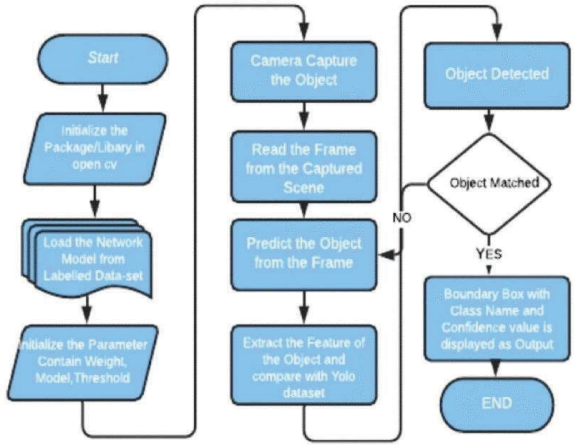


Fig 1 Flow of the Project

IV. Methodology and Implementation

A. System Overview

The proposed pothole detection system enhances autonomous vehicle navigation by integrating **computer vision, deep learning, and real-time decision-making**. It consists of a **Raspberry Pi 4B**, a **USB camera**, **DC motors**, and an **L298N motor driver** for hardware implementation. The **USB camera** captures real-time road images, which are processed using **OpenCV techniques** such as grayscale conversion, edge detection, and contour analysis. A **YOLO-based deep learning model** analyzes the images to detect potholes under varying environmental conditions. Based on the detected pothole's severity, the system dynamically adjusts the vehicle's speed and trajectory.

Components Used

1. **Raspberry Pi 4B** – Acts as the main processing unit, handling image analysis and decision-making.
2. **USB Camera** – Captures real-time road images for pothole detection.
3. **L298N Motor Driver** – Controls the vehicle's **DC motors**, enabling navigation adjustments.
4. **DC Motors** – Allow movement and maneuvering of the autonomous vehicle.
5. **Power Supply (Battery/Power Bank)** – Provides the necessary power for the Raspberry Pi and motor drivers.
6. **OpenCV** – Used for **image preprocessing** (grayscale conversion, edge detection, and contour analysis).
7. **YOLO-based Deep Learning Model** – Performs real-time pothole detection with high accuracy.

B. Hardware Implementation

The hardware implementation of the pothole detection system involves integrating a **Raspberry Pi 4B**, a **USB camera**, **DC motors**, and an **L298N motor driver** for real-time road surface analysis and autonomous navigation. The **USB camera** captures road images, which are processed by the **Raspberry Pi** using **OpenCV** and a **YOLO-based deep learning model**. Based on the detected pothole's severity, the system controls the vehicle's movement through the **L298N motor driver**, adjusting speed and direction accordingly. A **power bank** supplies power to the Raspberry Pi, while **AA batteries** drive the motors.

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Connections and Circuit Integration

1) The **USB camera** is connected to one of the **USB ports** on the Raspberry Pi.
2) The **Raspberry Pi GPIO pins** control the **IN1, IN2, IN3, and IN4** pins of the **L298N motor driver**.
3) The **two output terminals** of the L298N motor driver are connected to the **four DC motors** of the vehicle.
4) The **Raspberry Pi 4B** is powered using a **5V power bank** through its **USB-C port**.
5) The **DC motors** are powered by **four AA batteries (6V total)** connected to the **L298N motor driver's power input**.
6) Based on **real-time pothole detection**, the Raspberry Pi **sends movement commands** to the motor driver.
7) If a pothole is detected, the system **adjusts speed, turns, or stops** to avoid it.

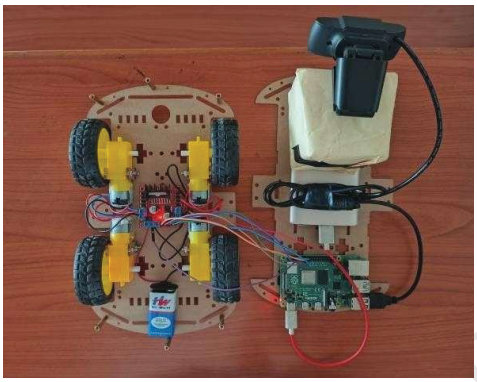


Fig 2 Circuit design

C. Software Development and Model Training

The software development for the pothole detection system integrates **computer vision, deep learning, and real-time decision-making** using **Python, OpenCV, and YOLO-based object detection**. The **Raspberry Pi 4B** serves as the main processing unit, executing image processing algorithms and controlling the vehicle's navigation based on detected potholes. The system captures real-time road images, preprocesses them, and applies deep learning techniques for pothole identification.

A. Software Development

Programming Environment

1. The system is developed in **Python**, running on the **Raspberry Pi OS**.
2. **OpenCV** is used for image processing tasks such as **grayscale conversion, noise reduction, edge detection, and contour analysis**.
3. The **YOLO (You Only Look Once) deep learning model** is used for real-time pothole detection.

Image Processing and Detection

1. The **USB camera** captures continuous frames of the road surface.
2. Images are **preprocessed** by converting them to **grayscale**, applying **Gaussian blur**, and performing **Canny edge detection**.
3. **YOLO-based object detection** identifies potholes and classifies them based on severity.

Vehicle Control and Navigation

1. The detection results are **mapped to vehicle control actions**.
2. The Raspberry Pi **sends motor control signals** to the **L298N motor driver**, adjusting the vehicle's speed and direction.
3. If a pothole is detected, the system **slows down, stops, or navigates around** the obstacle.

B. Model Training

Dataset Collection

1. The dataset consists of **images of roads with and without potholes** under different lighting and weather conditions.
2. Images are collected from **publicly available datasets and custom road footage** captured using the system's camera.

Annotation and Preprocessing

1. Potholes are manually **labeled and annotated** using **labeling tools** for training.
2. Images are resized, normalized, and **augmented (flipping, brightness adjustments)** to improve model robustness.

Training the YOLO Model

1. The **YOLOv4-Tiny model** is trained on the annotated dataset using **PyTorch and TensorFlow**.
2. The model is optimized to detect potholes in **real-time with high accuracy** on low-power hardware like the Raspberry Pi.

Model Testing and Optimization

1. The trained model is **tested on unseen road images** to evaluate its accuracy and performance.
2. Performance metrics like **precision, recall, and inference time** are analyzed.
3. The model is **fine-tuned** by adjusting parameters and retraining with additional data.

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V. RESULTS AND DISCUSSION

A. Results

The proposed pothole detection system was successfully implemented and tested in a controlled environment. The **Raspberry Pi 4B and USB camera** efficiently captured real-time road images, which were processed using **OpenCV** for edge detection and contour analysis. The **YOLO-based deep learning model** accurately detected potholes under various conditions, including different lighting and road textures.

Key outcomes of the system include:

- **High Detection Accuracy** – The YOLO model achieved **reliable pothole identification** with minimal false detections.
- **Real-Time Processing** – The system maintained **low latency**, ensuring timely responses for vehicle navigation.
- **Effective Navigation Control** – The autonomous vehicle successfully **slowed down, stopped, or maneuvered** around detected potholes based on severity assessment.
- **Computational Efficiency** – The optimized model functioned efficiently on **low-power hardware (Raspberry Pi 4B)**, making it a cost-effective solution.

B. Discussion

The implementation demonstrated that **computer vision and deep learning** provide a robust approach for pothole detection in autonomous vehicles. The system's **real-time performance and adaptability** make it suitable for **smart transportation applications**. However, several challenges were observed:

- **Environmental Factors** – Detection accuracy was slightly affected by **low light, road glare, and shadows**.
- **Processing Limitations** – While optimized, the **Raspberry Pi 4B has computational constraints**, limiting deep learning complexity.
- **Road Condition Variability** – The model performed well on **structured roads** but required further tuning for **irregular road conditions and debris detection**.

To enhance performance, **future improvements** will focus on:

- **Multi-Sensor Integration** – Combining **LIDAR, ultrasonic, and accelerometer sensors** for improved accuracy.
- **Cloud-Based Processing** – Offloading deep learning computations to the cloud for **real-time updates and scalability**.

VI. CONCLUSION AND FUTURE TRENDS

A. Conclusion

The proposed pothole detection system successfully enhances road safety by accurately identifying potholes in real time. Using **Raspberry Pi 4B, a USB camera, OpenCV-based image processing, and a YOLO deep learning model**, the system efficiently detects road hazards and adjusts navigation accordingly. The results demonstrate **high detection accuracy, low latency, and effective obstacle avoidance**, making it a cost-effective solution for autonomous vehicles.

While the system performs well in controlled environments, challenges such as **lighting variations, road debris, and processing limitations** remain. Future enhancements will focus on **multi-sensor integration, cloud-based processing, and AI-driven predictive analysis** to improve adaptability in real-world conditions. This research contributes to **smart transportation systems**, paving the way for safer and more efficient road networks.

Future Trends

Integration of Machine Learning and AI

1. Implementing **advanced deep learning models** to improve detection accuracy under varying road and weather conditions.
2. Developing **AI-driven predictive models** to anticipate road deterioration and enable preventive measures.

Multi-Sensor Fusion

1. Combining **LIDAR, ultrasonic, and accelerometer sensors** to enhance pothole detection reliability.
2. Integrating **stereo vision** for improved depth estimation and severity analysis.

Real-Time Cloud Processing

1. Offloading **deep learning computations to cloud servers** for improved efficiency and large-scale implementation.
2. Enabling **real-time data sharing** for connected autonomous vehicles and smart city infrastructure.

Autonomous Vehicle Integration

1. Enhancing autonomous navigation by integrating **path-planning algorithms** for optimal route adjustments.
2. Implementing **V2X (Vehicle-to-Everything) communication** for real-time hazard alerts to nearby vehicles.

IoT and Smart Cities

1. Deploying the pothole detection system as part of **IoT-based smart road monitoring networks**.
2. Transmitting **real-time pothole data** to municipal authorities for faster road maintenance and repairs.

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Energy-Efficient and Low-Cost Solutions

1. Exploring **low-power hardware and edge computing** for sustainable deployment in large-scale systems.
2. Utilizing **renewable energy sources** to power embedded detection units for long-term field applications.

Global Adoption and Standardization

1. Developing a **universal pothole detection framework** adaptable to different road infrastructures worldwide.
2. Collaborating with **transportation agencies** to establish standards for autonomous pothole detection and reporting.

This research lays the foundation for **next-generation smart transportation solutions**, ensuring safer and more efficient mobility for autonomous vehicles. By leveraging **AI, IoT, and cloud computing**, future implementations will continue to enhance road safety and infrastructure management on a global scale.

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This project would not have been possible without the collective efforts of all those who contributed directly or indirectly, and we truly appreciate their support.

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Design & Implementation of an FPGA-Acclerated Fog Removal Algorithm for Automotive Safety

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***Abstract*— This paper explores the architectural design and implementation of a hardware-accelerated solution using Verilog HDL for efficient image processing on an FPGA board, specifically addressing the critical issue of reduced visibility caused by fog in automotive safety applications. Fog-related accidents are a significant contributor to road hazards, particularly impacting autonomous driving systems that rely on real-time performance and clear visual data for navigation and decision-making. The proposed solution leverages FPGA-based image processing techniques and the parallel processing capabilities of FPGA boards to enhance image clarity in adverse weather conditions, ensuring robust and efficient fog removal. This hardware-accelerated approach achieves high computational efficiency with minimal latency, making it a reliable and scalable candidate for integration into safety-critical systems in modern vehicles, significantly improving road safety.**

Keywords*— *FPGA-based Image Processing, Verilog HDL, Automotive Safety, Fog Removal, Real-Time Performance, Hardware Acceleration, Autonomous Driving, Road Safety

I. Introduction

Visibility is crucial for the safety of ground vehicles and aircraft, particularly under adverse weather conditions like fog, which has been a significant cause of numerous accidents. In automotive systems, fog disrupts the functionality of visual sensors, cameras, and human drivers, impairing navigation and hazard detection. Similarly, in aviation, foggy conditions during critical phases such as take-off and landing reduce pilots' situational awareness, increasing the risk of accidents. Despite advancements in technologies like image processing, radar, and LIDAR, these systems face limitations in real-time operation during extreme weather. Hardware-accelerated solutions, such as fog removal algorithms implemented on FPGAs, offer a promising approach to enhance the clarity of visual data, providing safer navigation for automobiles and aircraft in foggy conditions.

Several case studies emphasize the severe consequences of poor visibility. The 2002 Interstate 75 pileup in Tennessee involved nearly 100 vehicles and 12 fatalities due to dense fog, highlighting the need for real-time vision enhancement technologies. Similarly, India's 2017 Yamuna Expressway accident, caused by dense fog, led to a massive pileup and multiple fatalities, underscoring the importance of visibility tools for fog-prone highways. In aviation, the 1996 crash of Aero Perú Flight 603 and the 2010 Smolensk Air Disaster illustrate how fog compounded challenges during critical flight phases, resulting in tragic losses. These incidents demonstrate the urgent need for advanced visibility enhancement systems to improve safety and reduce accidents in both automotive and aviation sectors.

II. Literature Survey

[1] Based on the atmosphere scattering model and the dark channel prior method, the atmospheric light of the whole image and the transmission map could be extracted. These are important and necessary parameters of the recovery model.

[2] Poor weather condition such as fog, rain or haze causes problem in getting information from image. As computer vision system extracts features from the scene, it is important that reliable information could be obtained by removing haze.

[3] We employ an extremum approximate method to extract the atmospheric light and propose a contour preserving estimation to obtain the transmission by using edge-preserving and mean filters alternately. Our method can efficiently avoid the halo artifact generated in the recovered image.

[4] There are times when clear images cannot be obtained due to fog, rain, or nighttime, which may adversely affect the quality of autonomous driving.

[5] In this paper, we propose a simple but effective image prior - dark channel prior to remove haze from a single input image.

III. Problem Analysis and Solution

A. Problem Definition

Foggy conditions significantly reduce visibility, posing serious challenges to both traditional drivers and autonomous vehicles by obscuring critical visual cues like road signs, lane markings, and other vehicles. For human drivers, this results in slower reaction times and increased accident risk, while in autonomous systems, the reliance on degraded visual data from cameras and sensors can lead to incorrect decision-making or system failures. Existing solutions, such as fog lights and basic camera filters, provide limited improvement and are often ineffective in dense fog conditions, leaving vehicles vulnerable and compromising road safety. This highlights the urgent need for advanced, hardware-accelerated solutions capable of real-time fog removal and visibility enhancement to improve the clarity of visual data. By addressing this critical issue, such technologies can enhance safety, reliability, and the operational performance of vehicles in adverse weather conditions.

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B. Proposed Solution

We propose a fog removal algorithm using FPGA that utilizes a combination of global and local atmospheric light estimation, transmission map enhancement, and scene restoration to enhance the clarity of visual data. The solution is divided into three major stages:

1) Dynamic Atmospheric Light Estimation (DALE)

a) Global Atmospheric Light Estimation (GALE)

The algorithm calculates the global atmospheric light, $A_{global}^{R/G/B}$, by identifying the brightest pixels in the foggy image. This value represents the light intensity scattered by fog and is used as a baseline for further calculations.

b) Local Atmospheric Light Estimation (LALC)

Local atmospheric light, $A_{local}^{R/G/B}$, is computed for smaller regions in the image, allowing the algorithm to adapt to spatial variations in fog density.

This dual approach ensures both coarse and fine corrections for atmospheric light estimation, improving the algorithm's adaptability to heterogeneous fog conditions.

2) Transmission Map Estimation (TME)

a) Dark Channel Prior Algorithm

The algorithm computes the minimum intensity across the R, G, and B channels for every pixel in the image. This step identifies the dark channel image, $I^{dark}(x)$, which is pivotal for estimating the depth of fog.

b) Transmission Calculation

Using the dark channel and atmospheric light values, the transmission map, *t(x)* is calculated. The transmission map represents the proportion of light that penetrates through the fog, highlighting the level of visibility in different regions of the image. It is further refined to ensure smoothness and avoid artifacts in the restored image.

3) Scene Restoration (SR)

The final step involves restoring the image, *J(x)* using the calculated transmission map and atmospheric light values. The restoration formula ensures that the foggy components are removed, enhancing the contrast and clarity of the image.

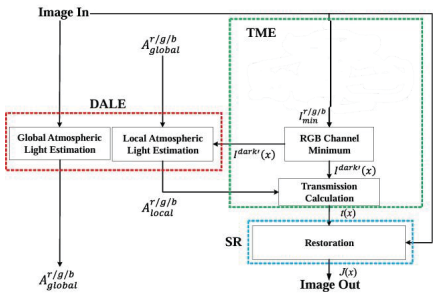


Fig. 1. Flow Chart for proposed Algorithm

IV. Methodology and Implementation

A simple atmosphere scatter model to describe atmospheric scattering, refraction, and reflection, which explains the formation of haze or fog in images due to light absorption and scattering by airborne particles or raindrops, is shown below. This model is commonly used in single-image defogging algorithms, simplifies the process into the equation:

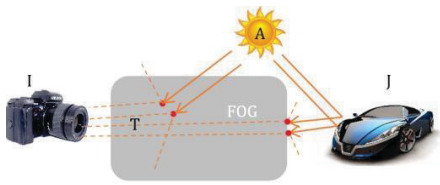


Fig. 2. Scattering of Light due to Fog

$$I(x) = J(x) * t(x) + A * (1 - t(x)) \quad (1)$$

Where, *I(x)* is the hazy image in RGB channels, *J(x)* is the scene without haze, *t(x)* is the transmission coefficient representing the amount of light penetrating the fog, *A* is the atmospheric light (e.g., sunlight), and *x* denotes image pixel coordinates.

This equation separates the observed image into the scene radiance attenuated by fog and the light scattered by the atmosphere, providing a foundation for developing algorithms to restore fog images.

A. Dynamic Atmospheric Light Estimation (DALE)

Atmospheric light, *A* plays a critical role in haze removal, as it is used in key calculations to estimate the transmission map and reconstruct the haze-free image. A suitable atmospheric light estimation method can effectively adjust the brightness of the recovered scene. Relying solely on global atmospheric light for image recovery is insufficient because higher *A* values can make dark areas even darker and lower *A* values can make them brighter. To address this, a dynamic local atmospheric light concept is proposed to adapt brightness changes in image details while maintaining overall image consistency.

1) Global Atmospheric Light Estimation (GALE)

To preserve the basic atmospheric light across the entire image, the global atmospheric light is first calculated. The pixel with the highest dark channel value is selected as the global atmospheric light, avoiding the need for sorting based on the top 0.1 values. This process is represented mathematically as:

$$A_{global}^{C} = \text{LOCATE}\left(max(I^{dark}(x))\right), \forall C \in R/G/B \quad (2)$$

Where, the LOCATE function identifies the pixel coordinate with the highest dark channel.

To improve restoration at the pixel level, an adaptive adjustment is applied based on the characteristics of each patch after estimating the global atmospheric light. It is

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observed that areas with higher visibility are less affected by fog and tend to have lower dark channel values, while areas with lower visibility are more fog-affected and have higher dark channel values. Based on this observation, the image is divided into low-visibility and high-visibility regions using a threshold. The threshold for dark channels, Th_{dark}, is defined as:

$$Th_{dark} = \frac{\min(A^{C}_{global})}{2}, \forall C \in R/G/B \quad (3)$$

Pixels with dark channel values below the threshold are classified as dark regions (low dark channel values), while those above the threshold are classified as bright regions (higher dark channel values).

2) Local Atmospheric Light Estimation (LALC)

Atmospheric light is used to restore the image by assigning local atmospheric light based on pixel classification. If a pixel is in the bright region, the local atmospheric light is set to the global atmospheric light. Conversely, if a pixel is classified as part of the dark region, the local atmospheric light is assigned as 75% of the global atmospheric light. This classification and assignment process is mathematically represented as:

$$A^{c}_{local} = \begin{cases} A^{c}_{bright} = A^{c}_{global}, & I^{dark}(x) > Th_{dark} \\ A^{c}_{dark} = 0.75 \times A^{c}_{global}, & I^{dark}(x) \leq Th_{dark} \end{cases},$$

$$\forall C \in R/G/B \quad (4)$$

However, this approach may lead to abrupt changes in local atmospheric light values, particularly for regions in the dark channel map near the threshold Th_{dark}, resulting in a block effect. To address this issue, an interpolation method is introduced to smoothly transition the local atmospheric light based on the content's features. The updated formula is:

$$A^{c}_{local} = \begin{cases} A^{c}_{bright}, & I^{dark}(x) \geq 2 \times Th_{dark} \\ 0.5 \times A^{c}_{bright} + 0.5 \times \frac{1}{2} A^{c}_{dark}, & Th_{dark} \leq I^{dark}(x) < 2 \times Th_{dark} \\ A^{c}_{dark}, & I^{dark}(x) < Th_{dark} \end{cases}$$

$$\forall C \in R/G/B \quad (5)$$

B. Transmission Map Estimation (TME)

The hardware architecture for the Transmission Map Estimation (TME) component consists of two key units: the Pixel based Dark Channel Prior (Pixel DCP) unit, and the Transformation Calculation (TC) unit.

1) Pixel based Dark Channel Prior (Pixel DCP)

The Pixel-Based Dark Channel Prior (Pixel DCP) unit calculates the dark channel value for each pixel without considering a patch. It identifies the minimum intensity value across the red, green, and blue (RGB) channels of a single pixel directly. This simplified approach reduces computational complexity and hardware requirements, making it suitable for real-time applications. The Pixel DCP unit is particularly efficient in identifying hazy regions, as it leverages the principle that pixels in hazy or shadowed areas typically exhibit low intensity in at least one-colour channel. This calculated dark channel value is then used in subsequent steps of the defogging algorithm, such as atmospheric light estimation and transmission map.



Fig. 3. Pictorial Visualization of the Pixel DCP Algorithm

2) Transmission Calculation (TC)

The equation for calculating amount of transmission, *t(x)* is given by:

$$t(x) = 1 - \min\left(\frac{I^{dark}(x)}{A^{c}_{local}}\right), \forall C \in R/G/B \quad (6)$$

To avoid the complexity of dividing to compute the reciprocal of *t(x)*, a look-up table (LUT) is employed in the TC unit. This LUT stores the possible values of the reciprocal of *t(x)*. The size of the LUT is minimized by simplifying the equation for *t(x)*. Rearranging the above equation,

$$\frac{1}{t(x)} = \min\left(\frac{A^{c}_{local}}{A^{c}_{local} - I^{dark}(x)}\right), \forall C \in R/G/B \quad (7)$$

From this expression, it is evident that the LUT size can be further reduced by storing only the denominator, that is, $(A^{R/G/B}_{local} - I^{dark}(x))$. If the denominator is equal to zero, then we approximate it to one. This approach simplifies hardware implementation while maintaining functionality.

3) Scene Restoration (SR)

After estimating the local atmospheric light and the transmission map, the scene $J^{C}(x)$ can be reconstructed by substituting the local atmospheric light (A^{c}_{local}) and the transmission map *t(x)*. The equation to recover the fogged pixel, $I^{C}(x)$ is derived from the atmosphere scatter model, as explained in Eq. (1), and can be rearranged as:

$$J^{C}(x) = \left(\frac{I^{C}(x) - A^{C}_{local}}{t(x)}\right) + A^{C}_{local}, \forall C \in R/G/B \quad (8)$$

The above equation can be re-written as,

$$J^{C}(x) = \left((I^{C}(x) - A^{C}_{local}) \times \frac{1}{t(x)}\right) + A^{C}_{local},$$

$$\forall C \in R/G/B \quad (9)$$

Hence, $J^{C}(x)$ obtained from the above equation is the fog removed pixel. By combining all the fog removed pixels of the image, we will be able to achieve a clear image.

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4) Pictorial Representation

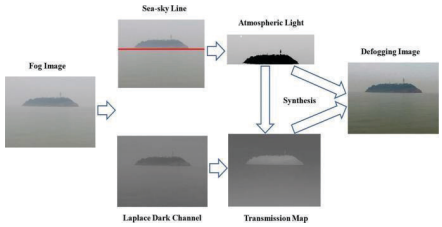


Fig. 4. Pictorial Visualization of the Project

5) Implementation

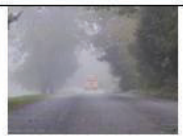
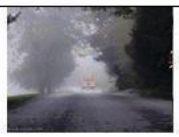
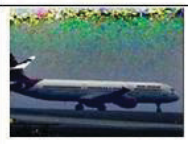
For the software implementation of the fog removal algorithm on an FPGA platform, the primary components included the FPGA development environment and relevant software tools for coding, simulation, and testing. The project used Xilinx Vivado, Python, and MATLAB to write and synthesize the Verilog HDL code that defined the algorithm's hardware architecture. These tools allowed for simulation and debugging before hardware deployment. Additional libraries or IP cores were integrated to accelerate image processing tasks. A standard PC or laptop with adequate computational resources (RAM, CPU) was used for running these software tools, as well as performing simulation and verification of the FPGA-based algorithm. The ZedBoard was used for testing the fog removal algorithm in real-world environments, enabling the transition from a software-based solution to a hardware-in-the-loop system.

V. Results and Discussion

The table of processed images demonstrate the effectiveness of the proposed fog removal algorithm across different platforms: FPGA hardware, Python, and MATLAB. The original foggy images show significant visual degradation, with reduced visibility and obscured details. The hardware processed images, implemented on FPGA, exhibit superior fog reduction and clarity compared to Python and MATLAB outputs. Details in both the foreground and background are restored effectively, achieving a natural balance without over-enhancement. The FPGA results are consistent and free from artifacts, showcasing the advantage of hardware acceleration in real time performance. In contrast, Python and MATLAB outputs, while improving visibility, exhibit occasional artifacts or unnatural colour shifts, particularly in Python-processed images. These findings highlight the FPGA implementation as a robust and efficient solution for real time fog removal in challenging conditions.

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Table 1. Table of Processed Images

	Image 1	Image 2	Image 3	Image 4	Image 5
Fog Image					
Hardware Processed Image					
Python Processed Image					
MATLAB Processed Image					

Note: The size of the images used above are of **320 x 240 pixels**.

A. Hardware Pipelined Architecture

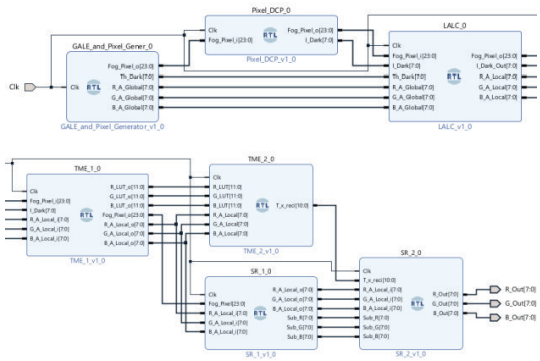


Fig. 5. Hardware Pipelined Architecture

The hardware pipelined architecture leverages the Block RAM (BRAM) of the FPGA to store image pixels, ensuring efficient data management and high-speed processing. The foggy input image is divided into pixels, which are stored in the BRAM for quick and seamless access by the various stages of the fog removal algorithm. This storage strategy is crucial for maintaining the pipeline's efficiency, as it minimizes memory access delays and allows for concurrent data retrieval by multiple modules. The BRAM enables modules such as Global and Local Atmospheric Light Estimation (GALE and LALC), Transmission Map Estimation (TME), and Scene Restoration (SR) to operate without interruptions, as pixel data is readily available during computation. Additionally, the use of BRAM reduces reliance on external memory, enhancing the overall speed and performance of the system. By providing low-latency access to pixel data, BRAM facilitates the parallel execution of operations, ensuring that the pipeline achieves real-time performance for foggy image restoration. This optimized memory usage and rapid data transfer capability highlight the FPGA's suitability for high-throughput image processing applications in real-time environments.

B. Hardware Implementation on FPGA

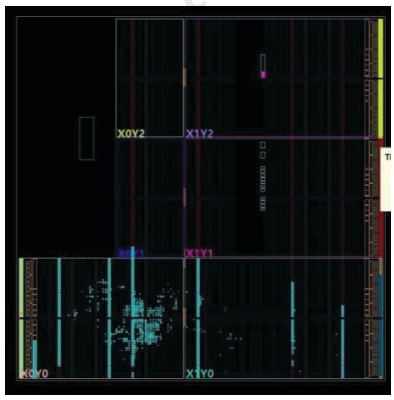
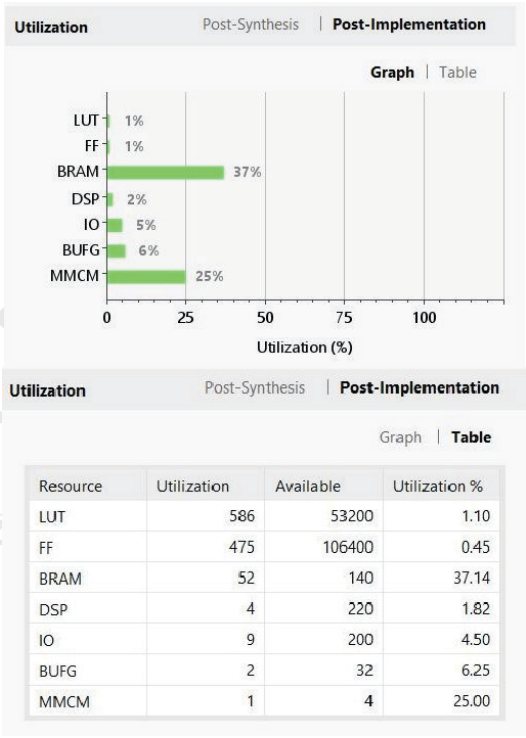


Fig. 6. FPGA Implementation

This FPGA implementation of the fog removal algorithm showcases the efficient mapping of various modules, such as atmospheric light estimation and transmission map calculation, onto the FPGA's fabric. The floorplan visualizes the distribution of resources like logic elements, BRAM, and routing channels across different regions, labelled as X0Y2, X1Y1, and others. Dense clusters in specific areas indicate the placement of computationally intensive operations, while the scattered layout demonstrates parallelism inherent to the FPGA architecture. This design ensures high-speed processing with optimized resource utilization, enabling real-time fog removal for image enhancement.

C. Resource Utilization



Resource	Utilization	Available	Utilization %
LUT	586	53200	1.10
FF	475	106400	0.45
BRAM	52	140	37.14
DSP	4	220	1.82
IO	9	200	4.50
BUFG	2	32	6.25
MMCM	1	4	25.00

Fig. 7. Utilization Report

The FPGA utilization report shows that the resources are being used efficiently. The BRAMs are utilized at 37%, which is a good balance between resource usage and remaining headroom. The LUTs have a low utilization of 1%, indicating that there is ample space for further logic implementation. The DSP blocks are used at 5%, and the IOs at 6%, leaving room for expansion in these areas as well. The BUFGs are used at 25%, suggesting that most of the clock signals are being distributed efficiently. Overall, the FPGA resources are being used judiciously, with ample headroom available for future design modifications or enhancements.

D. Power Requirements

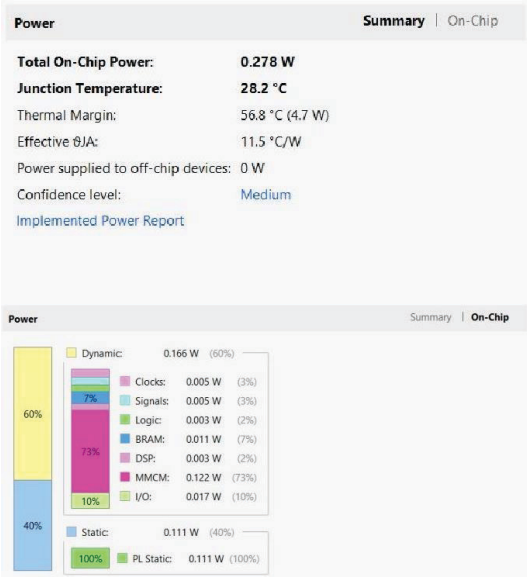


Fig. 8. Power Report and its Distribution

The FPGA design requires a total on-chip power of 0.278 W, resulting in a junction temperature of 28.2°C. This is well within the thermal margin of 56.8°C, indicating a safe operating temperature. The effective thermal resistance is 11.5 °C/W, which is a measure of how well the FPGA can dissipate heat. The power distribution shows that the majority of power consumption comes from dynamic elements, with logic and BRAMs being the major contributors. Static power consumption accounts for 40% of the total power usage. **Note:** The power report indicates a medium confidence level, so the actual power consumption may vary slightly.

E. Timing Reports

1) Setup Time



Fig. 9. Setup Timing

The worst-case setup timing slack is 0.031 ns, indicating a very small margin for timing. The total negative slack is 0 ns, meaning that there are no paths that violate setup timing constraints.

2) Hold Time

The worst-case hold timing slack is 0.063 ns, suggesting a slightly larger margin for hold timing compared to setup timing. The total hold slack is 0 ns, confirming that no paths violate hold timing constraints.



Fig. 10. Hold Timing

3) Pulse Width Time

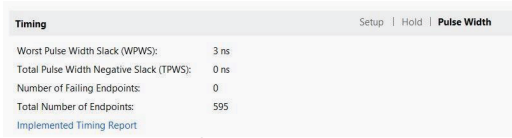


Fig. 11. Pulse Width Timing

The worst-case pulse width slack is 3 ns, indicating a relatively large margin for pulse width timing. The total pulse width negative slack is 0 ns, confirming that no paths violate pulse width timing constraints.

Note: The results are based upon 100Mhz, ZedBoard in-built clock. The time period per clock cycle is 10 nanoseconds.

VI. Conclusion and Future Trends

A. Conclusion

The project focused on the design and implementation of an FPGA-accelerated fog removal algorithm for automotive safety, specifically for Advanced Driver Assistance Systems (ADAS). Using the ZedBoard, along with Verilog HDL, Xilinx Vivado, Python, and MATLAB, we successfully implemented a high-performance solution that processes images in under 1 millisecond. This processing speed allows for the handling nearly 1000 frames per second, ensuring real-time application in automotive systems to enhance visibility in foggy conditions.

Testing the algorithm in real-world environments demonstrated its effectiveness in improving visibility, with the FPGA-based implementation providing a significant performance boost over software-only solutions. The transition to a hardware-in-the-loop setup validated the feasibility of using FPGA technology for real-time image processing in automotive safety systems.

B. Future Trends

Looking ahead, we plan to extend the project by adding HDMI output for displaying the processed images, optimizing memory usage for greater efficiency, and exploring video processing capabilities to handle continuous video streams. These future improvements will further enhance the capabilities of ADAS, providing a comprehensive solution for safer driving in challenging weather conditions.

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SOURCES OF FIGURES

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Game Console on FPGA Board Using RISC-V CPU

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***Abstract*—This paper presents the design and implementation of a RISC-V single-cycle CPU-based game console on an FPGA. Leveraging RISC-V's simplicity and modularity, the system integrates a custom CPU, memory, I/O interfaces, and a VGA display for graphical output. Implemented in Verilog and synthesized on an FPGA, it ensures real-time performance with minimal latency. A game engine in RISC-V assembly enables efficient execution and direct hardware control. Performance evaluation based on execution speed, resource utilization, and power consumption validates system efficiency. Experimental results demonstrate smooth gameplay, highlighting the potential of FPGA-based gaming systems and future enhancements such as pipelined architectures and wireless controllers.**

***Index Terms*—RISC-V, FPGA, Game console, Single-cycle CPU, Hardware-software co-design, Embedded gaming, Real-time performance, Power consumption.**

I. Introduction

The RISC-V architecture is an open-source alternative to proprietary CPU designs, offering modularity and flexibility for academic research and real-world applications. Its extensibility makes it an ideal choice for implementing custom processors in embedded systems. This paper presents the design and implementation of a single-cycle RISC-V CPU-based game console on an FPGA, demonstrating hardware-software co-design in gaming applications.

The proposed system features a custom single-cycle CPU that executes RISC-V instructions, integrated with memory, input/output interfaces, and a VGA display for graphical rendering. The game engine, implemented in RISC-V assembly, enables direct hardware interaction, optimizing execution speed and responsiveness. The FPGA-based approach ensures real-time performance, low power consumption, and efficient resource utilization.

This work explores the challenges of designing an FPGA-based gaming console, including CPU design, memory management, and graphical display implementation. Performance analysis focuses on execution efficiency, power consumption, and resource usage. The results highlight the potential of RISC-V in embedded gaming applications, serving as a foundation for future advancements such as pipelined CPU architectures, enhanced graphics, and wireless controller integration.

II. Literature Survey

Game development on FPGA platforms has been explored in multiple studies, highlighting both advantages and challenges. Traditional implementations using hardware description languages (HDLs) such as Verilog and VHDL have demonstrated FPGA's potential for low-latency processing and real-time execution but face limitations in flexibility and scalability.

In [1], a review of FPGA-based games, including Snake, Chess, and Pong, emphasizes the benefits of FPGA platforms for reconfigurable game designs using VGA controllers and PS/2 interfaces. However, limitations such as hardware dependency and the difficulty of runtime updates hinder adaptability. The need for a more modular and software-driven approach, like RISC-V with C-based game logic, is noted as a key improvement over static FPGA-based designs.

A detailed implementation of the Snake game on an FPGA using Verilog HDL is presented in [2], showcasing hardware's ability to handle parallel operations efficiently. Despite advantages like direct VGA output and clock reduction techniques, the approach suffers from debugging complexities, lack of portability to other architectures, and scalability challenges. The reliance on external peripherals, such as VGA adapters, increases development overhead, making the approach less suitable for architectures like RISC-V.

The development of Space Invaders on an FPGA, as discussed in [3], follows a modular VHDL-based design utilizing the Xilinx Spartan 6 board. The use of Block RAM for real-time graphics processing demonstrates FPGA's efficiency for gaming applications. However, limitations such as outdated VGA interfaces, restricted portability, and the inability to easily transition the game to other platforms indicate the need for a more software-adaptable approach, reinforcing the advantages of RISC-V-based gaming solutions.

AUTHOR PROOF

Comparatively, software-based game development using higher-level programming languages provides greater flexibility. In [4], a first-person shooter game was implemented using C in XNA Game Development Studio. While this approach enables advanced graphics, modular development, and player control mechanics, the reliance on outdated tools and the lack of cross-platform compatibility highlight challenges in adapting such games to embedded architectures like RISC-V. These studies underline the need for a more adaptable and scalable approach to game development. Unlike traditional FPGA-based implementations, a RISC-V CPU with a C-based game engine allows for greater flexibility, easier debugging, and improved portability while still leveraging hardware acceleration for performance optimization.

III. Problem Analysis and Solution

A. Problem Definition

Developing an FPGA-based gaming console presents several challenges due to hardware constraints and system complexities. The key issues include:

- **Complexity of HDLs:** Hardware Description Languages (HDLs) like Verilog and VHDL require low-level programming expertise, making game logic development time-consuming.
- **Limited Game Scalability:** Different games require varying hardware configurations, restricting design reusability across multiple applications.
- **Debugging and Testing Challenges:** FPGA-based game logic requires specialized simulation tools, increasing development overhead compared to traditional software-based games.
- **Hardware-Software Integration:** Synchronizing CPU execution, memory management, I/O processing, and VGA display is critical to achieving real-time performance.
- **FPGA Resource Constraints:** Limited logic elements, memory, and processing power restrict the complexity of game implementations.

B. Proposed Solution

To address the challenges in developing an FPGA-based gaming console, the following solutions are proposed:

- **Simplified Development with RISC-V and C:** By using a RISC-V CPU and writing game logic in C, development becomes more accessible and efficient compared to HDL-based implementations.
- **Enhanced Game Scalability:** The software layer, written in C, allows multiple games to run on the same FPGA hardware without requiring hardware modifications.
- **Improved Debugging and Testing:** Utilizing C for game logic enables easier debugging with standard RISC-V toolchains, reducing development time.
- **Seamless Hardware-Software Integration:** Centralizing both hardware (RISC-V CPU) and software (game logic) within the FPGA simplifies synchronization and improves system efficiency.
- **Optimized FPGA Resource Utilization:** The RISC-V CPU architecture efficiently manages memory and I/O, addressing FPGA resource constraints.
- **Standardization and Portability:** Leveraging the standardized RISC-V ISA ensures better portability and future scalability for gaming applications.

IV. Methodology and Implementation

A. System Block Diagram

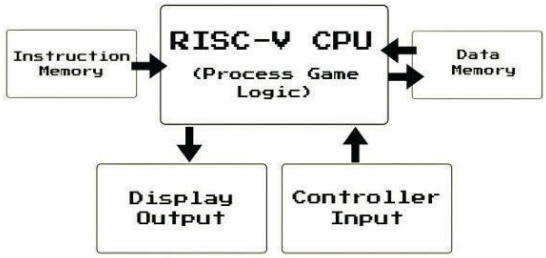


Fig. 1. System Block Diagram

B. RISC-V CPU Core

The RISC-V CPU serves as the processing unit, implementing the RISC-V ISA to execute game logic written in C. Operating synchronously with the system clock (`clk`), it fetches instructions from the instruction memory (`instr_mem`), decodes them, and executes arithmetic operations, memory accesses, and control flow instructions. The `ReadData` output fetches required data, while `instr_addr` specifies the next instruction's address. This CPU core coordinates all interactions within the system, ensuring seamless execution of the game.

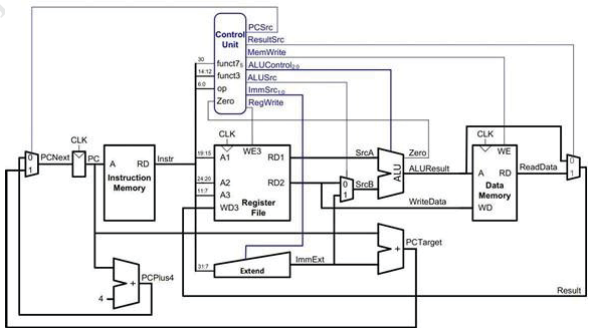


Fig. 2. RISC V CPU

1) Instruction and Data Memory: The instruction memory (`instr_mem`) is a read-only block storing compiled game logic, supplying the CPU with sequential instructions unless a jump or branch instruction modifies execution. These instructions govern paddle movement, ball dynamics, collision detection, and game restart logic.

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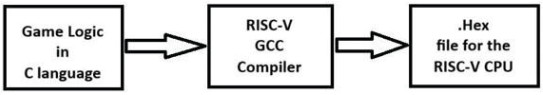


Fig. 3. Instruction Memory

The data memory (`data_mem`) stores game-related variables such as ball and paddle positions. Operating synchronously with the clock, it supports read/write operations controlled by the `func` signal. The CPU updates paddle and ball positions dynamically, while the VGA controller accesses these values to update the display in real time.

2) System Inputs and Interconnections: System inputs include the clock (`clk`), reset (`reset`), and paddle control signals (`paddle_up`, `paddle_down`). The clock ensures synchronization across all components, while the reset signal initializes the system. Paddle movement inputs from the Basys 3 buttons update memory values, which are subsequently reflected on the VGA display.

The design ensures seamless intercommunication between components. The CPU fetches instructions from instruction memory and processes game logic via data memory. Updated positional data is provided to the VGA controller for real-time rendering. This architecture facilitates smooth and responsive gameplay.

C. VGA Controller

The VGA controller is responsible for rendering the game on a **640x480 VGA display**, generating synchronization signals and pixel data based on the game state. The key components include:

- **Synchronization Logic:** Generates horizontal (hsync) and vertical sync (vsync) signals using *counters* (`h_count, v_count`) to track pixel positions. A *pixel clock* ensures smooth display updates.
- **Ball and Paddle Rendering:** Positions are fetched from game memory and processed using *comparators* (`RTL_LT, RTL_GEQ`) to determine active regions. *Adders and logical gates* enable pixel output at correct positions.
- **Clock and Timing Control:** *Registers* (`RTL_REG_ASYNC`) store and update counters in real time. Logical circuits such as `OR` and `NOT` gates generate the required sync signals.
- **Pixel Rendering:** *Multiplexers* (`RTL_MUX`) select pixel data based on current counter values. The active video area is restricted to **640x480 resolution**, preventing rendering artifacts.

D. Gameplay and Graphics

V. Results and Discussion

A. CPU Implementation

The RISC-V CPU was successfully implemented on the Basys 3 FPGA, executing game logic written in C. The processor efficiently handled real-time gaming tasks while operating within the expected clock frequency. No noticeable lag was observed during gameplay, demonstrating smooth execution of instructions.

B. Game Functionality

The ping-pong game operated as intended, rendering smooth graphics on a 640x480 VGA display. The vertical paddle responded accurately to *up* and *down* button inputs on the Basys 3. The ball exhibited consistent motion with precise collision detection for paddle and wall interactions.

- **Paddle Movement:** The paddle moved responsively based on user inputs, maintaining the desired speed and direction.
- **Ball Dynamics:** The ball maintained its programmed velocity, bouncing predictably off walls and the paddle.
- **Game Logic:** The game restarted seamlessly when the ball missed the paddle, confirming a robust implementation of game rules.



Fig. 4. Ball successfully hitting the paddle, continuing the game.



Fig. 5. Ball missing the paddle, triggering a game reset.

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C. Performance Metrics

- **Frame Rate:** The game maintained a steady refresh rate with no noticeable frame drops.
- **CPU Utilization:** The custom RISC-V CPU efficiently executed the game logic while using minimal FPGA resources.
- **Memory Management:** Game data and instruction memory were optimized for stable execution and minimal resource usage.

D. Challenges and Debugging

Several challenges were encountered during implementation and successfully addressed through iterative testing and optimization.

- **Mapping GPIOs:** Proper routing of button inputs and VGA outputs required multiple design iterations.
- **Memory Management:** Synchronizing memory operations in C required extensive debugging and refinement.
- **Game Logic Fine-Tuning:** Adjustments to ball velocity and collision logic were necessary to achieve realistic gameplay.

E. User Experience

User feedback highlighted high engagement and satisfaction. The vertical paddle controlled via *up* and *down* buttons added a unique challenge, differentiating it from conventional ping-pong games.

F. Final Outcome

The project successfully integrated hardware design and software development to create an interactive and functional ping-pong game. The results demonstrate the feasibility of embedding custom RISC-V CPUs for real-time applications such as gaming.

VI. Future Trends

A. Future Trends

The development of FPGA-based gaming consoles presents multiple opportunities for enhancements. Future improvements include:

- **Smartphone Controller Integration:** By interfacing a Bluetooth module, a smartphone app can be developed, enabling wireless game control.
- **Transition to ASIC Design:** Moving from FPGA to an ASIC-based CPU will reduce production costs, making it more suitable for commercial deployment.
- **LCD Integration:** Directly interfacing an LCD display eliminates the need for an external monitor, improving portability and creating a self-contained gaming device.
- **Single-Cycle to Multi-Cycle Pipelining:** Transitioning from a single-cycle CPU to a multi-cycle or pipelined architecture can enhance performance, reduce power consumption, and improve instruction throughput.

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Implementation of AES Algorithm on Hardware

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***Abstract*—This paper presents a low-power, area-efficient AES-128 hardware implementation on an FPGA for embedded and IoT applications. It uses a combinational S-Box to eliminate memory overhead and clock gating to reduce dynamic power. A pipelined, resource-shared structure further minimizes logic usage. Real-time UART-based communication with a PuTTY terminal enables practical testing. Implemented on a Basys-3 FPGA, the design achieves efficient encryption and decryption with minimal resource consumption.**

***Index Terms*—AES, FPGA, encryption, decryption, UART, PuTTY, S-Box, clock gating, Basys-3, hardware accelerator**

I. Introduction

In today's digital era, the proliferation of embedded systems, smart devices, and Internet of Things (IoT) networks has placed data security at the forefront of hardware design. With growing concerns about cyber threats and privacy breaches, there is a critical need to secure data transmissions in real-time environments. AES-128 is a symmetric key encryption standard, widely regarded for its strength, efficiency, and global standardization by NIST

Despite its robust security features, hardware implementations of AES often suffer from limitations such as increased area overhead, high power consumption, and inefficient resource usage—primarily due to memory-based S-Boxes and static datapath designs [3], [7]. These drawbacks hinder AES integration in space-constrained and battery-powered embedded systems [8].

Several recent works have attempted to overcome these challenges by adopting techniques such as S-Box sharing [1], BRAM reuse [3], and key reduction strategies [2], but many either compromise security or increase hardware complexity. Others explore secure AES-RISC-V integration for co-processor designs [10] or attempt to mitigate side-channel vulnerabilities [11].

This project proposes a compact and power-aware implementation of AES-128 using a combinational S-Box architecture and pipelined datapath. It leverages clock gating to deactivate idle modules and conserves switching power, making it highly suitable for embedded, IoT, and wireless communication platforms [8]. Designed and synthesized on the Basys-3 FPGA board, the solution ensures real-time encryption and decryption through UART communication, validated via PuTTY terminal, making it a practical and deployable cryptographic engine.

II. Literature Survey

Recent research has explored various optimizations for AES hardware to suit low-power and resource-constrained platforms such as IoT and embedded systems. Vimalkumar et al. (2023) proposed a lightweight AES-128 architecture that reduces the number of encryption rounds to six and introduces a zigzag diffusion pattern [2]. This design achieved 81.92% power and 76.84% LUT reduction on the Basys-3 FPGA by eliminating repeated SubBytes stages. However, the reduced number of rounds and modified S-Box logic compromise cryptographic robustness and general applicability.

Xu et al. (2024) introduced a unified cryptographic coprocessor capable of handling both AES-128 and SM4 encryption using reconfigurable shared S-Box logic [1]. Implemented in 65nm CMOS, the design achieved significant area (42%) and power (43%) savings through resource reuse and pipelining. Nonetheless, the lack of FPGA validation and the added complexity of dual-mode logic reduce its suitability for simple, standalone AES applications.

Harb et al. (2022) presented a high-throughput AES design utilizing a fully sub-pipelined architecture with BRAM-based S-Box and MixColumns modules [3]. The design achieved 63.75 Gbps on Xilinx Artix-7 and Kintex UltraScale FPGAs, making it ideal for large-scale embedded systems. However, the approach consumed considerable logic and memory resources and did not incorporate power-saving mechanisms like clock gating, making it unsuitable for power-constrained environments.

In contrast, our implementation preserves the full 10-round AES-128 structure, avoids BRAM and DSP usage, and emphasizes low-area, low-power operation. It uses a combinational

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S-Box to eliminate memory overhead, integrates clock gating to reduce dynamic power, and employs a resource-sharing pipelined architecture. The inclusion of UART-based communication validated through PuTTY terminal further supports real-time testing and practical usability in embedded security applications.

III. Problem Analysis and Solution

Conventional hardware implementations of AES-128 often present critical limitations that restrict their deployment in embedded and low-power systems. These issues stem primarily from inefficient architecture choices and lack of adaptability to constrained environments. The major challenges are outlined below:

- **Memory-heavy S-Boxes:** Most AES architectures rely on lookup table-based S-Boxes stored in BRAM or ROM. While this approach simplifies substitution logic, it increases area and memory usage and introduces additional latency due to memory access overhead.
- **Lack of power control:** Traditional AES cores keep all internal modules active during operation, resulting in continuous switching activity. This leads to unnecessary dynamic power consumption, especially during idle stages or clock cycles with no useful computation.
- **Redundant hardware blocks:** Many designs instantiate dedicated hardware for every AES round, creating duplicated functional units such as multiple AddRoundKey or MixColumns modules. This drastically increases logic utilization and limits scalability.
- **Limited adaptability:** Fixed datapaths and static logic structures make it difficult to optimize such designs for specific application needs like area reduction or energy efficiency, which are critical in IoT devices and edge computing systems.

To mitigate these challenges, the proposed AES-128 architecture introduces the following improvements:

- A *combinational S-Box* is implemented using logic gates instead of memory lookups, significantly reducing area and access delay.
- *Clock gating* is applied to selectively deactivate unused modules during idle cycles, lowering dynamic power consumption without affecting throughput.
- A *pipelined resource-sharing approach* reuses functional units across AES rounds, enabling efficient logic utilization while supporting continuous data processing.
- A *UART interface* enables serial communication with a host PC, where the PuTTY terminal is used for real-time plaintext input and ciphertext output validation, demonstrating practical system-level usability.

These architectural enhancements result in a highly efficient AES-128 core, maintaining full-round security while addressing the area, power, and real-time interfacing requirements of modern embedded applications.

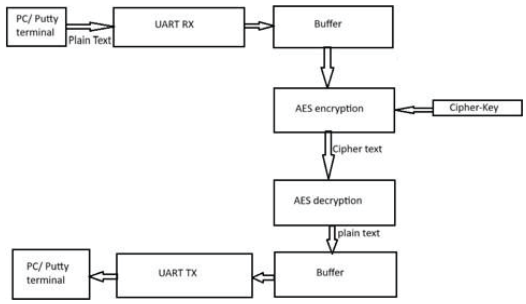


Fig. 1. overall block diagram

IV. Proposed Methodology

A. System Overview

The AES encryption and decryption system is integrated with UART communication to enable real-time data exchange with a PC terminal (e.g., PuTTY). Plaintext is sent from the PC via UART RX and buffered for synchronization with the internal AES core. After encryption, the ciphertext is directly passed to the decryption block, which reconstructs the plaintext. The final output is transmitted back to the PC through UART TX, allowing end-to-end verification of secure data processing in hardware.

B. AES Encryption Architecture

The encryption process begins with the input cipher key, expanded by the Key Expansion module to generate round keys. Plaintext is loaded through a MUX and latched using a flip-flop. Each AES round includes SubBytes (via combinational S-Box), ShiftRows, MixColumns, and AddRoundKey. Flip-flops between stages enable pipelining. MUX 2 selects the appropriate round key, and MixColumns is bypassed in the final round. The resulting ciphertext is stored in a final register.

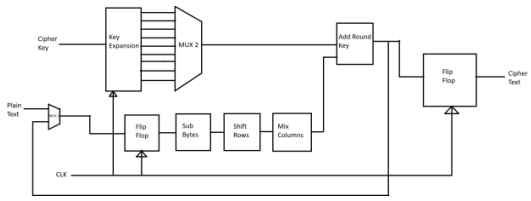


Fig. 2. one round of encryption

C. AES Decryption Architecture

Decryption applies inverse AES operations in reverse order: Inverse SubBytes, Inverse ShiftRows, Inverse MixColumns, and AddRoundKey. The same key expansion module is reused,

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with round keys applied in reverse. Flip-flops maintain synchronization, and the final plaintext is registered and sent back via UART for verification.

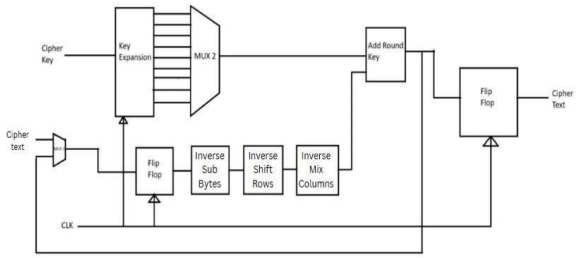


Fig. 3. one round of decryption

D. Control Logic

A finite state machine (FSM), internal round counter, and clock gating logic manage the timing of round transitions, key selection, and UART flow. These elements enable low-power operation and reliable interfacing between the AES core and external terminal.

V. Results and Discussion

The complete AES-128 encryption and decryption system was implemented and tested on the Basys-3 FPGA board using Vivado. Functional verification was performed through simulation, and synthesis reports were analyzed to assess resource usage, timing, and power.

Figure 4 shows the simulation result of the AES encryption module. The output is captured after each of the 10 rounds, confirming correct step-by-step transformation of the plaintext into ciphertext.

```
======Encryption======
PlainText:  1234567890abcdef1234567890abcdef
CipherKey:  fedcba9876543210fedcba9876543210
=======================
Round 0 Output: ece8ece0e6fffffece8ece0e6ffffff
Round 1 Output: ba42151defd3436d32ca9d95675bcbe5
Round 2 Output: 258829cbd09257af6dd121b871ade40b
Round 3 Output: 14d8cfceebc6ab7f3ab9a8c523fcb907
Round 4 Output: a9d908eb57920eb20b3312c2b636ee5c
Round 5 Output: cc51ec3bb3e754174769eb22c91a3960
Round 6 Output: 5f4e6903f72625434c1fdaa82a33d612
Round 7 Output: 47d4f828952154f3a84fff3a4a6d0f56
Round 8 Output: c29ac2d2306fe3d4617d44452efa8c80
Round 9 Output: 0c03c31e018d3e95ebeeb6be1b2736b8
Round 10 Output: 0cc5712c4cc5f341ed5d3e157eca8d0f
Encryption Done.
=======================
CipherText: 0cc5712c4cc5f341ed5d3e157eca8d0f
=======================
```

Fig. 4. AES encryption simulation showing round-wise outputs

The encryption module utilized:

WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
								1821	2471	0	0	0
0.208	0.000	0.017	0.000		0.000	0.157	0	1845	2471	0	0	0

Fig. 5. Encryption module: synthesis and power report

- **1821 LUTs**
- **2471 Flip-Flops**
- **0.157 W** total power consumption
- **WNS = 0.208 ns**

No BRAM, DSP, or URAM blocks were used, owing to the combinational S-Box and fully pipelined round structure. Figure **??** displays the synthesis report summary for encryption. Figure 6 presents the simulation result of the decryption module, validating that the ciphertext is correctly reversed to recover the original plaintext through 10 inverse rounds.

```
=======================
CipherText: 0cc5712c4cc5f341ed5d3e157eca8d0f
=======================
======Decryption======
=======================
Round 10 Output: 0c03c31e018d3e95ebeeb6be1b2736b8
Round 9 Output: c29ac2d2306fe3d4617d44452efa8c80
Round 8 Output: 47d4f828952154f3a84fff3a4a6d0f56
Round 7 Output: 5f4e6903f72625434c1fdaa82a33d612
Round 6 Output: cc51ec3bb3e754174769eb22c91a3960
Round 5 Output: a9d908eb57920eb20b3312c2b636ee5c
Round 4 Output: 14d8cfceebc6ab7f3ab9a8c523fcb907
Round 3 Output: 258829cbd09257af6dd121b871ade40b
Round 2 Output: ba42151defd3436d32ca9d95675bcbe5
Round 1 Output: ece8ece0e6fffffece8ece0e6ffffff
Round 0: 1234567890abcdef1234567890abcdef
Decryption Done.
==================
Final Plaintext: 1234567890abcdef1234567890abcdef
==============
```

Fig. 6. AES decryption simulation showing round-wise output recovery

The decryption module used:

- **3022 LUTs**
- **2465 Flip-Flops**
- **0.396 W** power consumption
- **WNS = 0.058 ns**

Figure 7 shows the detailed performance metrics for the decryption pipeline.

WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
								3022	2465	0	0	0
0.058	0.000	0.023	0.000		0.000	0.396	0	3015	2465	0	0	0

Fig. 7. Decryption module: synthesis and timing summary

Overall, the use of clock gating significantly reduced dynamic power by disabling idle modules during non-operational cycles, leading to improved energy efficiency without affecting throughput. Unlike traditional AES implementations that rely heavily on memory elements such as BRAM or dedicated DSP

slices, this design operates entirely using logic-based components. The avoidance of BRAM, DSP, and URAM blocks not only conserves hardware resources but also simplifies timing closure and enhances portability across FPGA families with limited on-chip memory.

Furthermore, by integrating pipelining and combinational S-Box logic, the architecture maintains full compliance with the 10-round AES-128 specification while minimizing both latency and logic utilization. This balance of security, performance, and efficiency makes the proposed design an excellent fit for modern embedded applications, especially in constrained environments such as IoT edge nodes, wearable devices, and battery-operated systems where area and power are critical factors.

VI. Future Work

Several enhancements can be made to improve the performance, flexibility, and security of the proposed AES hardware architecture. First, integrating advanced power-saving techniques such as clock gating and dynamic voltage scaling (DVS) can further minimize power consumption by disabling inactive modules and adjusting supply voltage based on runtime workload [9].

Extending the design to support multiple key lengths (AES-192 and AES-256) would increase its adaptability to diverse security requirements [8]. To enhance the resilience of the system, fault-tolerant design techniques and countermeasures against side-channel attacks—such as power analysis and timing-based attacks—can be incorporated for improved security in real-world applications [11].

Additionally, coupling the hardware with software APIs and driver interfaces would enable easier deployment in embedded platforms and real-time operating systems. Future efforts can also explore ASIC prototyping and testing to benchmark performance, power, and area in physical silicon [6]. Finally, introducing parallel encryption engines within the architecture can scale throughput for high-performance applications such as secure data centers and encrypted network processors [10].

VII. Conclusion

This paper presented a resource-efficient AES-128 hardware implementation optimized for embedded and low-power platforms. The architecture employs a combinational logic-based S-Box, pipelined datapaths, and round-key multiplexing to reduce area and power consumption without compromising security. The modular and reusable design enables efficient allocation of hardware resources across encryption and decryption rounds.

The complete system was implemented on a Basys-3 FPGA board and verified using UART communication with PuTTY terminal support. The design demonstrated reliable round-wise output and minimal logic usage, with no BRAM, DSP, or URAM blocks. Overall, the proposed architecture provides a strong balance between performance, security, and resource utilization, making it highly suitable for lightweight cryptographic applications in IoT and embedded systems [2], [3].

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Vision-Enhanced Driver Assistance Systems with Real-Time Fog Removal, Driver Alertness & Traffic Detection

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***Abstract*— This work presents a real-time, hardware-accelerated vision system for Advanced Driver Assistance Systems (ADAS), implemented on an FPGA platform. The system integrates three critical features: fog removal, driver drowsiness detection, and traffic sign recognition. A real time image defogging algorithm enhances visual clarity under low-visibility conditions using the parallel processing capabilities of FPGAs. Simultaneously, a driver monitoring module detects drowsiness based on facial and ocular cues, issuing immediate alerts to enhance driver safety. Complementing these is a traffic sign detection module that operates in real time to identify and classify road signs, aiding decision-making during navigation. The proposed architecture achieves high computational efficiency with minimal latency, making it suitable for safety-critical automotive environments. The unified, real-time system demonstrates strong potential for integration into intelligent vehicle platforms, contributing to improved situational awareness and road safety.**

Keywords*— *Advanced Driver Assistance Systems, FPGA, Fog Removal, Driver Drowsiness Detection, Hardware Acceleration, Traffic Sign Recognition, High Computational Efficiency, Intelligent Vehicle, Road Safety

I. INTRODUCTION

The automobile industry has witnessed significant technological advancements over the years, yet road accidents remain a major global concern. A substantial percentage of accidents occur due to poor visibility, driver inattention, and failure to detect obstacles in time (especially in self-driving vehicles). Factors such as foggy weather conditions, reckless driving, and drowsy driving contribute to thousands of fatalities annually. Addressing these challenges requires the integration of intelligent systems that enhance driving safety and assist drivers in making better decisions on the road.

Similarly, the aviation industry faces safety challenges related to adverse weather conditions, limited visibility, and pilot fatigue. Fog, heavy rain, and turbulence can significantly impact flight operations, leading to delays, inefficient navigation, and potential safety risks during landing and take-off. Additionally, pilot drowsiness and situational unawareness are major concerns, emphasizing the need for advanced monitoring systems that can track pilot alertness in real time.

To mitigate such risks, Advanced Driver Assistance Systems (ADAS) have emerged as a crucial component in modern vehicles. ADAS incorporates various real-time monitoring and alerting mechanisms, such as lane departure warnings, automatic emergency braking, blind spot detection, and adaptive cruise control.

Despite the progress in ADAS technology, several challenges persist. Fog and adverse weather conditions still hinder visibility, increasing the risk of collisions. Traffic monitoring systems require faster and more efficient processing to detect objects accurately in dynamic environments. Additionally, driver drowsiness and inattentiveness remain critical concerns, necessitating real-time tracking solutions to prevent accidents caused by fatigue.

In modern times, the need for high-speed, low-latency, and power-efficient ADAS solutions is more critical than ever. Traditional software-based approaches often struggle to meet real-time processing requirements in safety-critical applications. To address these limitations, hardware accelerated solutions such as Field Programmable Gate Arrays (FPGAs) offer a promising alternative, enabling rapid and efficient video processing for enhanced ADAS functionalities.

II. LITERATURE SURVEY

[1] Outdoor images and videos captured in hazy conditions often suffer from degradation. This paper explores a simplified video dehazing approach using MATLAB, based on the colour attenuation prior technique, which is known for its effectiveness in haze removal.

[2] This paper proposes a real-time video defogging method that enhances scene clarity by integrating the dark channel prior for precise haze estimation and motion compensation for temporal consistency. Experimental results on various foggy video sequences demonstrate superior haze removal, colour preservation, and real-time performance, making this approach ideal for applications requiring immediate fog clearance, such as live surveillance and autonomous driving.

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[3] Object detection remains a significant challenge, with deep learning advancements improving accuracy and efficiency. While two-stage detectors offer higher accuracy, single-stage detectors like YOLO provide faster inference. This study explores a hardware-software co design approach using a CPU + FPGA heterogeneous platform (Xilinx Kria KV260) for efficient object detection. By deploying YOLOv4, v5L, and v5s on Kria KV260, we achieve reduced computation time, demonstrating its potential for real-time vision applications.

[4] Real-time object detection and recognition have widespread applications in medical imaging, security surveillance, and autonomous vehicles. This study leverages deep learning techniques, particularly, CNN-based models, for efficient detection. The proposed hardware implementation utilizes Xilinx PYNQ-Z2 and Intel Movidius Neural Compute Stick (NCS) to enhance system performance. A comparative analysis of SSD, Faster R-CNN, and YOLO is conducted based on frames per second, detection probability, and computation time, demonstrating improved performance over existing models.

[5] The integration of Embedded AI (EAI) and Deep Learning (DL) has significantly advanced real-time object detection and classification. However, deploying deep learning models on edge devices remains challenging due to high computational demands. This paper presents an FPGA-based real-time object detection system using YOLOv3 Tiny, optimized for Advanced Driver Assistance Systems (ADAS). The system detects and classifies traffic lights using a camera on the Kria KV260 FPGA board, trained on the Bosch Small Traffic Light Dataset (BSTLD) and compiled with Xilinx Vitis AI. Achieving 99% accuracy at 15 FPS while consuming just 3.5W, the system ensures fast, precise, and power-efficient traffic light detection, making it ideal for low-cost, real-time ADAS applications.

III. Problem Analysis and Solution

A. Problem Definition

Modern vehicles increasingly rely on Advanced Driver Assistance Systems (ADAS) to enhance safety, reduce accidents, and support autonomous driving capabilities. However, several critical challenges persist in ensuring reliable real-time performance under dynamic and adverse conditions. One major issue is the significant reduction in visibility caused by fog, which impairs camera-based vision systems, leading to delayed or incorrect decision-making. In parallel, driver fatigue and drowsiness contribute heavily to road accidents, particularly during long-distance travel or nighttime driving, as human alertness levels decrease and reaction times increase. Furthermore, failure to accurately detect and respond to traffic signs due to system limitations or poor visibility can result in rule violations and unsafe driving behaviour. Traditional software-based approaches to these problems often lack the necessary speed, efficiency, and real-time responsiveness required for safety-critical automotive applications. Therefore, there is a pressing need for a robust, integrated, and hardware accelerated system capable of performing real-time fog removal, monitoring driver alertness, and detecting traffic signs with high accuracy and minimal latency. Addressing these challenges with a unified FPGA-based solution can significantly improve road safety and reliability in intelligent transportation systems.

B. Proposed Solution

1) Image Defogging Algorithm for Fog Removal:

The fog removal algorithm is implemented in three stages to enhance image clarity under foggy conditions using a hardware-accelerated approach on FPGA.

a) Dynamic Atmospheric Light Estimation (DALE):

The algorithm estimates both global and local atmospheric light values. Global estimation identifies the brightest pixels to approximate the overall fog intensity, while local estimation adapts to regional fog density variations, enabling more precise correction across the image.

b) Transmission Map Estimation (TME);

Using the Dark Channel Prior method, the algorithm calculates the minimum intensity across RGB channels to derive a dark channel image. This is used to estimate the transmission map, indicating the extent of fog in different regions. The map is refined to improve visual consistency and reduce artifacts.

c) Scene Restoration (SR):

The final scene is reconstructed using the transmission map and atmospheric light values, effectively removing fog components and enhancing contrast and visibility.

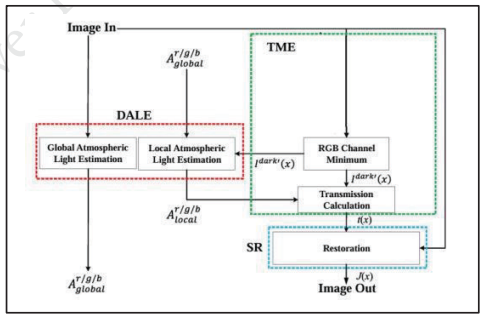


Fig. 1. Flow Chart for the Proposed Algorithm

2) Driver Alertness Monitoring using Eye Aspect Ratio (EAR):

The driver drowsiness detection system monitors eye behaviour in real time using a vision based algorithm cantered on the Eye Aspect Ratio (EAR). This non-intrusive method reliably detects prolonged eye closure — a strong indicator of drowsiness.

a) Facial Landmark Detection:

A real-time face detection module identifies the driver's face and locates six key landmarks around each eye. These landmarks are used to calculate the vertical and horizontal distances of the eye.

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b) EAR Calculation:

The Eye Aspect Ratio (EAR) is computed using the following formula:

$$EAR = \frac{||p2-p6|| + ||p3-p5||}{2 \times ||p1-p4||} \quad (1)$$

Where:

- p1 and p4 are the horizontal eye corner points
- p2, p3, p4, and p5 are the vertical eye points
- ||·|| denotes the Euclidean distance between two points

A lower EAR value indicates closed or partially closed eyes.

c) Drowsiness Detection Alert:

The EAR is monitored over a sequence of frames. If it remains below a predefined threshold (e.g., EAR < 0.25) for a certain number of consecutive frames, the system classifies the driver as drowsy and issues an immediate alert (such as a buzzer or visual signal).

This real-time and computationally lightweight method is well-suited for hardware acceleration on FPGA, enabling integration into automotive safety systems for continuous driver monitoring.

3) Traffic Sign Detection Using YOLO Algorithm:

The traffic sign detection system is designed to operate in real time using the YOLO (You Only Look Once) object detection algorithm. YOLO is a deep learning-based, single-stage detector that performs both object localization and classification in one forward pass of a convolutional neural network (CNN), making it highly efficient for real-time applications.

a) Model Architecture and Training:

A YOLO model (such as YOLOv3 or YOLOv4) is trained on a labelled dataset of traffic signs with bounding boxes and class annotations. The network learns to detect and classify signs such as speed limits, stop signs, pedestrian crossings, and other regulatory or warning indicators.

b) Image Preprocessing and Inference:

Input video frames from a camera are resized and normalized before being passed to the YOLO model. YOLO divides the image into a grid and simultaneously predicts bounding boxes, objectness scores, and class probabilities for each cell.

c) Bounding Box Prediction and Classification:

For each detected object, YOLO outputs:

- Coordinates of the bounding box (centre x, centre y, width, height).
- Confidence score indicating the presence of an object.
- Probability scores for each traffic sign class.

Non-Maximum Suppression (NMS) is applied to remove overlapping detections and retain the most accurate bounding box for each object.

d) Real-Time Output and Integration:

The detected traffic signs, along with their classifications, are displayed or logged in real time. The results can be used to alert the driver or assist autonomous systems in decision-making. The algorithm's speed and accuracy make it suitable for FPGA acceleration using lightweight versions of YOLO (e.g., Tiny-YOLO) for embedded deployment.

This approach ensures fast and accurate detection of multiple traffic signs per frame, providing robust assistance in dynamic driving environments as part of an integrated ADAS framework.

IV. METHODOLOGY & IMPLEMENTATION

A. Methodology of Image Defogging Algorithm for Fog Removal:

A simple atmosphere scatter model to describe atmospheric scattering, refraction, and reflection, which explains the formation of haze or fog in images due to light absorption and scattering by airborne particles or raindrops, is shown below. This model is commonly used in single-image defogging algorithms, simplifies the process into the equation:

$$I(x) = J(x)t(x) + A(1 - t(x)) \quad (2)$$

Where,

- I(x) is the hazy image in RGB channels
- J(x) is the scene without haze
- t(x) is the transmission coefficient representing the amount of light penetrating the fog
- A is the atmospheric light (e.g., sunlight)
- x denotes image coordinates.

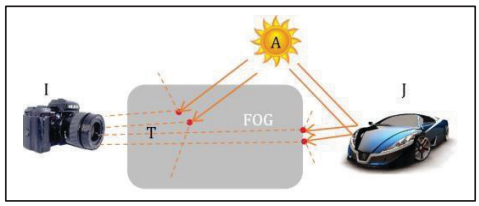


Fig. 2. Scattering of Light due to Fog

This equation separates the observed image into the scene radiance attenuated by fog and the light scattered by the atmosphere, providing a foundation for developing algorithms to restore fog images. After estimating the atmospheric light and the transmission map, the scene $J(x)$ can be reconstructed by substituting the atmospheric light (A) and the transmission map t(x). The equation to recover the

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fogged pixel, I(x) is derived from the atmosphere scatter model, Eq. 2, and can be rearranged as:

$$J^c(x) = \left(\frac{I^c(x) - A^c_{local}}{t(x)}\right) + A^c_{local}, \forall c \in R, G, B \quad (3)$$

Hence, $J^c(x)$ obtained from the above equation is the fog removed pixel.

B. *Methodology of Driver Alertness Monitoring using EAR Algorithm:*

The driver alertness monitoring system using the Eye Aspect Ratio (EAR) algorithm is a real time, non-intrusive solution designed to detect early signs of driver drowsiness by analyzing eye behaviour. The methodology begins with the capture of the driver's facial video using an onboard camera, typically mounted on the vehicle dashboard. The system then employs facial landmark detection to locate key points around the eyes. These landmarks, usually six points per eye, are extracted using pretrained models (such as Dib or OpenCV) and serve as the basis for computing the EAR.

The EAR is a mathematical ratio that quantifies the openness of the eye by comparing the vertical eye landmark distances to the horizontal distance. Specifically, the EAR is calculated using the (Eq.1). A low EAR value typically indicates a closed or nearly closed eye. Under normal conditions, the EAR remains relatively constant when the eyes are open, but it decreases sharply when the eyes close during a blink or due to drowsiness.

To detect drowsiness reliably, the system continuously monitors the EAR in each video frame. A predefined threshold (e.g., EAR < 0.25) is set, and if the EAR remains below this threshold for a sustained number of consecutive frames (e.g., 20–30), the system interprets it as a sign of drowsiness. Once drowsiness is detected, the system triggers alerts, such as a buzzer sound or a visual warning, to prompt the driver to regain attention and avoid potential accidents.

The algorithm operates in real time and is computationally lightweight, making it well-suited for hardware acceleration using FPGA or integration into embedded ADAS (Advanced Driver Assistance Systems). The accuracy and responsiveness of the system can be further improved by combining it with additional indicators like blink duration, head movement, or yawning detection for more comprehensive driver monitoring.

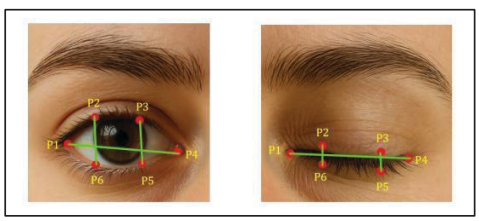


Fig. 3. EAR Calculation of Open and Closed Eyes

C. *Methodology of Traffic Sign Detection using YOLO Algorithm:*

The YOLO (You Only Look Once) algorithm is a state-of-the-art, real-time object detection system known for its speed and accuracy. Unlike traditional object detection methods that apply a classifier to different parts of the image or multiple regions, YOLO reframes object detection as a single regression problem. It takes the entire image as input and predicts bounding boxes and class probabilities directly from full images in one evaluation, making it highly efficient and well-suited for real-time applications like Advanced Driver Assistance Systems (ADAS). In the context of traffic sign detection, YOLO can rapidly identify and locate various types of traffic signs within a single camera frame, helping autonomous vehicles or driver-assist systems make timely and informed decisions.

The working of YOLO involves several well-defined stages. Initially, the input image is divided into an S × S grid. Each grid cell is responsible for predicting B bounding boxes and their corresponding confidence scores, along with class probabilities. These confidence scores reflect how confident the model is that a bounding box contains an object, and how accurate it thinks the box is. For traffic sign detection, these classes could include stop signs, speed limit signs, pedestrian crossings, and other road indicators. The algorithm then applies non-max suppression to eliminate redundant overlapping boxes, ensuring that each object is detected once.

YOLO uses a convolutional neural network (CNN) backbone—such as Darknet—for feature extraction from the input image. These features are then processed through additional convolutional and fully connected layers that output the final detection results. During training, the network is optimized using a loss function that penalizes classification error, localization error, and confidence score errors. YOLO's ability to generalize well across different datasets and its end-to-end pipeline make it a powerful tool for embedded systems with limited computational resources, such as FPGA-based ADAS systems. Its single-pass design enables consistent frame-rate detection, ensuring that traffic signs are recognized and processed in real time, thereby enhancing vehicle awareness and safety.

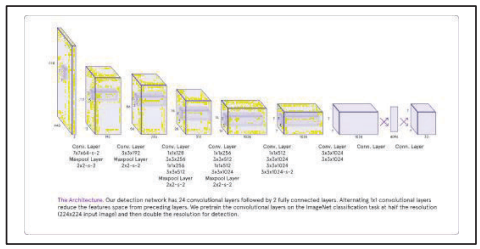


Fig. 4. YOLO Architecture

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D. Implementation

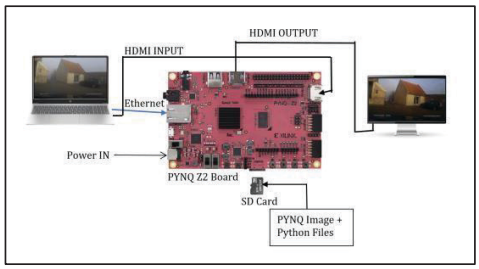


Fig. 5. Pictorial Visualization of the Implementation

The proposed Advanced Driver Assistance System (ADAS) prototype, which includes fog removal, driver alertness monitoring, and traffic sign detection, is implemented on the PYNQ Z2 development board. The board leverages the Zynq-7000 SoC, combining programmable logic (PL) with a dual-core ARM Cortex-A9 processor (PS), enabling efficient hardware software co-design and acceleration of compute-intensive tasks like real-time image processing.

The setup begins with HDMI Input received from a laptop or any HDMI-compatible camera source. This input serves as the real-time video feed, typically from a forward-facing car camera, capturing road scenes under foggy conditions and normal driving scenarios. The HDMI signal is ingested into the PYNQ-Z2 board, where image frames are redirected to the programmable logic for processing.

A microSD card, flashed with the official PYNQ image, contains the Linux OS, Python runtime, and the custom Python scripts for executing the fog removal algorithm, Eye Aspect Ratio (EAR)–based drowsiness detection, and YOLO-based traffic sign detection. These scripts utilize overlays that interface with hardware IP cores deployed in the programmable logic.

The fog removal algorithm implemented in Verilog HDL is synthesized into a custom IP block using Vivado. It performs dark channel prior analysis, transmission estimation, and scene restoration in real-time. Similarly, the EAR-based driver alertness monitoring processes cropped facial features (from input frames) to detect drowsy states using OpenCV and pre trained models. For traffic sign detection, a YOLO model is quantized and accelerated on the board using PYNQ's hardware overlays and Python APIs.

The processed output—after enhancement and detection—is routed to the HDMI Output port and displayed on a monitor, showing clear, annotated visuals. The board receives Power IN via USB or barrel jack and can be accessed remotely using Ethernet, which also facilitates file transfer and Jupyter Notebook access for development and monitoring. This hybrid hardware-software implementation enables real-time, low-latency performance with improved visual clarity and detection accuracy, making it ideal for embedded ADAS solutions.

V. Results and Discussions

A. Results of Image Defogging Algorithm for Fog Removal:



Fig. 6. Test Video Frame along with Outputs (Fig. 6.1 to 6.4)

The frames shown in Figure 6 demonstrate the real-time performance of the fog removal algorithm implemented on the PYNQ-Z2 FPGA board. Each test frame includes the original foggy input (left) and the corresponding output after hardware-based processing (right). The implemented algorithm, based on the Dark Channel Prior technique, was accelerated using programmable logic to achieve low-latency image enhancement suitable for ADAS applications. The output images clearly show significant improvement in visibility, contrast, and feature sharpness. For instance, in Figure 6.1, the building edges and vehicle contours become more pronounced, while in Figure 6.2, the road structure and distant tree-line are distinctly restored. Similarly, Figures 6.3 and 6.4 exhibit better detection of road boundaries, lane markings, and ambient surroundings, which were previously obscured by fog. These results validate that the FPGA-based implementation not only achieves real-time processing but also maintains high visual quality, making it a practical and efficient solution for embedded vision systems in foggy driving conditions.

B. Results of Driver Alertness Monitoring using EAR Algorithm:

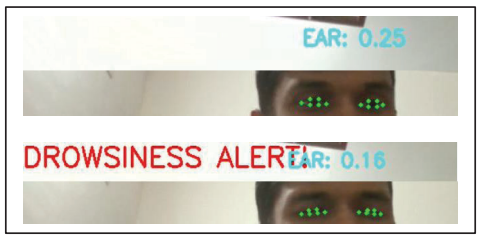


Fig. 7. EAR Simulation with Open and Closed Eyes (Fig. 7.1 to 7.2)

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The implementation results of the Eye Aspect Ratio (EAR) algorithm, as shown in Figures 7.1 and 7.2, effectively demonstrate its capability in real-time drowsiness detection. In Figure 7.1, the EAR value of 0.25 indicates open eyes, with the system functioning in a normal state. Conversely, in Figure 7.2, the EAR value drops to 0.16, triggering the "DROWSINESS ALERT" due to prolonged eye closure, a key indicator of driver fatigue. The algorithm successfully tracks facial landmarks and computes EAR in each frame, enabling timely alerts.

C. Results of Traffic Sign Detection using YOLO Algorithm:

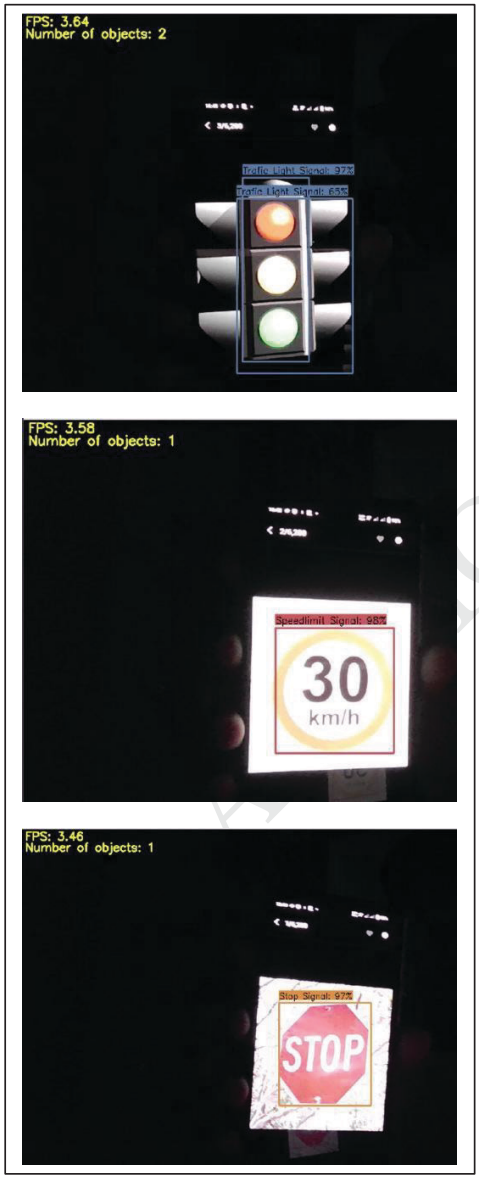


Fig. 8. Traffic Sign Detections (Fig. 8.1 to 8.3)

The results from the YOLO (You Only Look Once) algorithm implementation for traffic sign detection demonstrate its efficacy in real-time object detection within an Advanced Driver Assistance System (ADAS). The system successfully identifies and classifies multiple types of traffic signs, including stop signs, speed limit signs, and traffic signals. Fig. 8.1, Fig. 8.2, and Fig. 8.3 present snapshots of the live detection system, where bounding boxes are overlaid on detected traffic signs, and labels indicate the sign type with confidence scores.

In Fig. 8.1, the model correctly identifies a traffic signal with three states—red, yellow, and green—and distinguishes between them. The label "Number of objects: 2" and an FPS value of 3.64 indicate that the system is capable of detecting multiple objects simultaneously while maintaining a moderate real-time processing speed.

Similarly, Fig. 8.2 shows successful detection of a "30 km/h" speed limit sign. The bounding box and label provide clear information to the system or driver about the road restriction ahead. Despite operating under low-light conditions (as evident in the images), the model is still able to perform accurate detection.

In Fig. 8.3, a "STOP" sign is detected with a clearly labeled bounding box. The FPS value is shown to be 3.46, indicating that the algorithm maintains near-constant performance across different scenes and sign types. The consistent detection of signs with minimal latency supports the robustness of the YOLO architecture in object localization and classification tasks, even on embedded platforms.

The real-time detection results confirm that the YOLO algorithm can effectively support the traffic sign recognition component of ADAS. Although the frame rate is relatively low (around 3–4 FPS), it is still within acceptable limits for automotive applications where decisions are not made on a frame-by-frame basis but over a sequence of frames. Optimizations such as quantization, pruning, or deployment on hardware accelerators (like FPGAs or TPUs) could further enhance performance. Overall, these results validate YOLO's ability to handle multiple object categories with reliable accuracy and make it a promising candidate for real-time embedded deployment in driver-assistance systems.

VI. Conclusions and Future Trends

A. Conclusion:

This project presents a comprehensive and real-time Advanced Driver Assistance System (ADAS) that integrates three key modules: fog removal, driver drowsiness detection using Eye Aspect Ratio (EAR), and traffic sign recognition using the YOLO algorithm. Each component was designed and tested with a strong focus on efficiency, accuracy, and suitability for embedded implementation on platforms such as FPGAs.

The fog removal algorithm, based on the Dark Channel Prior method, was successfully implemented in Verilog and validated using the ZedBoard. It significantly enhances visibility in low-contrast driving scenarios by restoring scene clarity, enabling safer navigation in adverse weather conditions. With a processing latency of approximately 1 ms per frame, demonstrating ultra-fast throughput ideal for real-time ADAS environments.

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The drowsiness detection module reliably identifies fatigue using EAR values derived from facial landmarks. Simulation results confirm accurate detection of eye closures and drowsiness streaks with minimal false triggers. With a frame rate of ~17.89 FPS, the system meets the real time demands of embedded systems while maintaining stable resource utilization. Finally, the YOLO-based traffic sign recognition module effectively detects and classifies signs such as stop signs, speed limits, and traffic lights with high confidence. Despite a relatively modest frame rate (~3.5 FPS), it delivers accurate and consistent recognition results even under varying lighting conditions, proving its viability for on-road deployment with further optimization.

Collectively, the integration of these three modules forms a robust ADAS pipeline capable of operating under challenging visibility conditions, monitoring driver alertness, and interpreting road signs in real time. This work highlights the potential of deploying complex AI-assisted safety features on resource-constrained hardware, paving the way for cost-effective and intelligent automotive systems.

B. Future Trends:

As the automotive industry advances toward fully autonomous systems, smart and embedded driver assistance technologies will evolve significantly, driven by multi-sensor fusion combining LiDAR, radar, thermal, and ultrasonic data with visual enhancement algorithms like fog removal to improve robustness in adverse conditions. Future ADAS will support real-time video processing and streaming using hardware accelerators, while transitioning from traditional methods like Dark Channel Prior to deep learning-based fog removal models deployed on FPGAs and edge AI platforms for faster, higher-quality results. Driver monitoring systems will become more sophisticated by integrating gaze estimation, facial expression, head pose, and physiological signals for earlier and personalized drowsiness detection. To meet the demands of low-power environments, edge AI optimization through model compression and quantization will be essential. Context-aware adaptive systems will dynamically adjust processing based on traffic, lighting, and driver state, while standardization and V2X communication will enable shared traffic and environmental data to enhance predictive capabilities. Ultimately, these technologies will integrate as scalable and safety-certifiable subsystems.

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Design and Implementation of Bluetooth Communication Between an FPGA Board and a Smartphone

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***Abstract*—This project implements a wireless communication system between an FPGA and a smartphone using the HC-05 Bluetooth module. The system's primary objective is to enable real-time control of an LED on the FPGA through commands sent from a smartphone application. The HC-05 module is selected for its cost-effectiveness, simplified integration, and compatibility with classic Bluetooth protocols, making it widely applicable in embedded systems and IoT applications. This implementation underscores the viability of classic Bluetooth for FPGA-smartphone communication, particularly in scenarios prioritizing cost efficiency and straightforward deployment. The HC-05's standardized serial interface simplifies hardware integration, reducing development complexity. The smartphone application provides an intuitive interface for real-time interaction, enhancing usability. The project validates the HC-05 module as a robust, scalable solution for FPGA-based wireless systems, balancing simplicity and performance.**

***Index Terms*—FPGA, UART, HC-05, Bluetooth, Embedded Systems, Verilog**

I. Introduction

Wireless communication has become an integral part of modern embedded systems, enabling devices to interact seamlessly without physical connections. Among the various wireless communication technologies, Bluetooth has emerged as a preferred choice due to its low power consumption, ease of integration, and wide applicability in IoT and consumer electronics.

The Urbana FPGA board, when paired with an external HC-05 Bluetooth module, provides an excellent platform for developing and demonstrating wireless communication systems. This project leverages the HC-05 Bluetooth module to establish a wireless interface with a smartphone. Using a serial Bluetooth terminal application, commands are sent from the smartphone to control an LED on the FPGA board. The UART (Universal Asynchronous Receiver-Transmitter) protocol is employed to facilitate data exchange between the HC-05 module and the FPGA, ensuring accurate and efficient communication.

By integrating Bluetooth technology and the UART protocol, this project serves as a practical example of how advanced FPGA boards like Urbana can be utilized to implement wireless control systems. The successful implementation paves the way for further exploration into Bluetooth-based applications, such as smart home automation, wearable technology, and industrial IoT solutions.

II. Literature Survey

The foundation of this project relies on existing work in UART implementation and Bluetooth interfacing with FPGAs. Wenyu Wang [1] explores optimizing UART communication by using asynchronous FIFOs to manage differing clock domains, a technique crucial for data reliability between asynchronous systems like an FPGA and a Bluetooth module. Separately, Rahul Sonwane et al. [3] demonstrate a UART protocol specifically designed for FPGA implementation. Their use of a FIFO buffer to prevent data loss is a key insight for ensuring high communication efficiency, which is relevant to processing real-time commands. Closely aligned with this project's application, Thingom Devachandra Singh and Dr. Manoj Kumar (as referenced in the literature survey) present a Bluetooth-based home automation system using an FPGA. Their work validates the use of VHDL (or in our case, Verilog) to implement UART receivers that manage communication from an HC-05 module to an FPGA for reliable short-range control.

III. Problem Analysis & Solution

A. Problem Definition

The challenge lies in efficiently integrating external wireless modules, like the HC-05, with FPGAs. This integration

requires a robust and low-latency communication protocol to bridge the external module and the FPGA's core logic. The project aims to implement a UART controller in Verilog on the Urbana Spartan-7 FPGA to create a seamless serial interface to the HC-05 module, enabling simple and effective wireless control from a smartphone. Key challenges include ensuring reliable data exchange via UART, configuring the HC-05 module, and processing received commands in real-time to control the onboard LED.

B. Proposed Solution

The proposed solution is a modular hardware implementation for wireless communication.

- **HC-05 Bluetooth Interface:** Utilize the external HC-05 module for wireless communication, connecting it to the FPGA's UART interface.
- **UART Communication Module:** Implement a Verilog-based UART controller on the FPGA to manage serial data, ensuring parameter compatibility (baud rate, parity, stop bits) with the HC-05.
- **Command Processing Module:** Develop Verilog logic to decode received commands (e.g., "LED ON" and "LED OFF") from the UART module.
- **Smartphone Application:** Use the "Serial Bluetooth Terminal" app as an intuitive interface for sending commands to the FPGA.

IV. Methodology & Implementation

The project's methodology is centered on establishing a robust wireless communication link between a smartphone and the Urbana Spartan-7 FPGA board using an external HC-05 Bluetooth module. The entire FPGA design was developed in the Verilog Hardware Description Language (HDL) and synthesized using the AMD Xilinx Vivado software suite.

A. System Architecture and Hardware Interface

The system architecture, as shown in Fig. 1, consists of three primary components:

1) A Smartphone running the "Serial Bluetooth Terminal" application.
2) An HC-05 Bluetooth Module configured in peripheral mode.
3) The Urbana CSG324A FPGA Board.

The external HC-05 module was interfaced directly with the FPGA's I/O pins. The module's Transmit (TX) pin was connected to the FPGA's designated UART Receive (RX) pin, and the module's Receive (RX) pin was connected to the FPGA's UART Transmit (TX) pin.

B. FPGA Logic Design

The Verilog-based design on the FPGA consists of two main functional blocks: a UART Communication Module and a Command Processing Module.

1) **UART Communication Module:** A full-duplex UART controller was implemented to manage the serial data exchange between the FPGA and the HC-05 module. To ensure compatibility with the HC-05's default settings, the communication parameters were set to a 9600 baud rate, 8 data bits, 1 stop bit, and no parity.
2) **Command Processing Module:** This module was implemented as a Finite State Machine (FSM). The FSM is designed to continuously monitor the data from the UART receiver. It parses the incoming byte stream to decode specific ASCII commands, such as "LED ON" and "LED OFF". Once a valid command is recognized, the FSM asserts a control signal to toggle the state of an onboard LED.

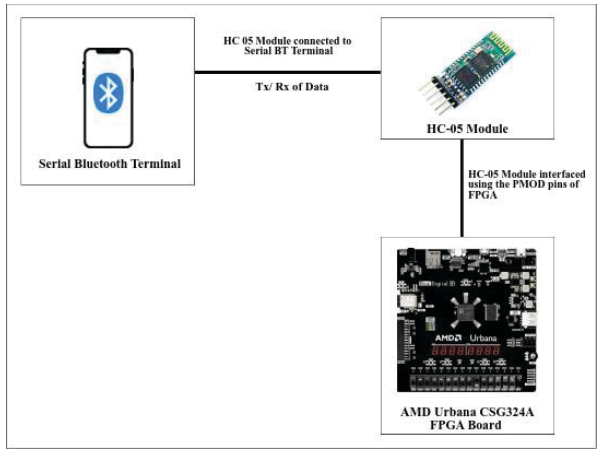


Fig. 1. System Block Diagram

C. Testing and Validation

The system was validated by first pairing the smartphone with the HC-05 module via the "Serial Bluetooth Terminal" app. Once the connection was established, predefined command strings were sent from the app. The corresponding real-time response of the onboard LED was visually verified, confirming the successful integration and operation of the entire communication chain.

V. Results and Discussion

A. Results

The implementation of the Bluetooth communication system yielded the following successful outcomes:

- **Successful HC-05 Integration:** The HC-05 Bluetooth module was successfully configured and paired with the "Serial Bluetooth Terminal" smartphone application.
- **Real-Time LED Control:** The system demonstrated efficient, real-time control of the onboard LED. Specific commands sent from the smartphone (e.g., "LED ON," "LED OFF") resulted in the desired action on the FPGA board without noticeable delay.
- **Reliable UART Communication:** The Verilog-based UART controller proved to be reliable and error-free during testing. Data was transmitted and received smoothly between the HC-05 and the FPGA at the 9600 baud rate.

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- **Simplified User Interface:** The "Serial Bluetooth Terminal" app provided an intuitive, easy-to-use interface for sending commands and testing the system.

B. Discussion

The results validate that the HC-05 module, when paired with a custom UART controller on an FPGA, is a highly effective and cost-efficient solution for basic wireless control. The primary challenge encountered was the initial configuration of the HC-05 module, which required careful attention to AT command setup to ensure stable pairing. Debugging the UART communication logic also required careful synchronization of baud rates and timing.

This project serves as a solid foundation for more complex applications. The system is scalable and could be expanded to control multiple devices or sensors connected to the FPGA.

VI. Conclusion and Future Trends

A. Conclusion

This project successfully demonstrated the design and implementation of a wireless communication system between an FPGA and a smartphone using an HC-05 Bluetooth module. By implementing a custom UART controller in Verilog on the Urbana Spartan-7 FPGA, the system achieved reliable, real-time control of an onboard LED via a smartphone application. This work validates the use of classic Bluetooth as a simple, robust, and cost-effective solution for adding wireless interfacing to FPGA-based embedded systems.

B. Future Trends

Potential enhancements for this project include support for higher data rates and integration with advanced Bluetooth protocols for expanded functionality. Future work could also focus on developing a custom smartphone application with a graphical user interface (GUI). The system's architecture could be expanded to manage multiple sensors and actuators, paving the way for more complex smart home automation or remote monitoring systems.

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Acknowledgment

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Design And Implementation Of A Low-Power 32-Bit Multiplier And Divider On Boolean Board

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***Abstract*-As digital systems demand faster and more power-efficient computation, hardware-accelerated arithmetic becomes essential. This project addresses that need by implementing a high-speed, low-power 32-bit multiplier and divider on a Spartan-7–based Boolean FPGA board. The multiplier leverages the FPGA's dedicated DSP48E1 slice to perform 32-bit multiplication with minimal logic overhead. By incorporating pipelining, the design achieves improved timing performance and reduced dynamic power consumption, utilizing just one DSP slice and nine LUTs with a total power consumption of 0.085 W. The divider is implemented using the non-restoring division algorithm, which eliminates redundant operations and enables efficient sequential computation. It achieves a power consumption of 0.096 W while maintaining low resource utilization. To accommodate the board's limited I/O, operands are entered in 16-bit segments using a push-button interface, and the lower 16 bits of the result are displayed in real time via onboard LEDs. The design is synthesized, and simulation results are produced in the form of output waveforms using Xilinx Vivado with detailed reports confirming power consumption, resource utilization, and timing closure. The proposed design is suitable for low-power applications and offerssignificant improvements in both power consumption and resource utilization.**

This work demonstrates a practical and scalable approach to implementing arithmetic units on resource-constrained FPGA platforms, with a focus on power optimization, timing efficiency, and real-time usability.

Keywords- DSP, FPGA, Power Optimization, LUT, Booth Multiplier, Wallace Tree Multiplier, Non-Restoring Divider, RTL, Resource Utilization.

I. INTRODUCTION

In modern digital systems, arithmetic operations such as multiplication and division are fundamental to a wide range of applications, from signal processing and control systems to embedded computing and cryptography. Implementing these operations efficiently on hardware platforms like FPGAs is critical for achieving high performance, low power consumption, and optimal resource utilization.

This paper presents the design and implementation of a low-power 32-bit multiplier and divider on a Spartan-7–based Boolean board. The multiplier leverages the FPGA's DSP48E1 slice to perform high-speed arithmetic with minimal logic overhead, achieving a power consumption of 0.085 W using only one DSP slice and nine LUTs. The divider employs the non-restoring division algorithm, reducing computational complexity and achieving a power consumption of 0.096 W.

To accommodate the board's limited I/O, operands are entered in 16-bit segments using a push-button interface, and results are displayed via onboard LEDs. The design is validated through simulation and real-time deployment, demonstrating functional correctness, resource efficiency, and low power consumption. This work highlights the practical viability of FPGA-based arithmetic units optimized for performance, power, and area.

II. METHODOLOGY

A. DSP Based Multiplication

DSP-based multiplication refers to performing multiplication using dedicated Digital Signal Processing (DSP) slices embedded in modern FPGAs (like the DSP48E1 block in Xilinx Spartan-7). These slices are optimized for high-speed arithmetic operations such as multiplication, addition, and multiply-accumulate (MAC).DSP slices handle multiplication in hardware, which Increases speed, Reduces power consumption, Minimizes logic resource usage.

1) DSP Based Multiplier Architecture

The architecture of a 32×32-bit DSP-based multiplier involves the following stages:

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a) Operand Decomposition

Since the DSP48E1 slice supports up to 25×18-bit multiplication, a 32×32-bit multiplication is decomposed into smaller segments.

A[31:0] is split into A_high and A_low

B[31:0] is split into B_high and B_low

b) Partial Product Generation

Each DSP slice computes a partial product using its internal multiplier. These partial products are aligned and shifted appropriately based on their bit significance.

Partial products are computed as:
A_low × B_low
A_high × B_low
A_low × B_high
A_high × B_high

c) Partial Product Accumulation

The partial products are summed using Internal adders within DSP slices (if chaining is supported).External logic (LUTs and carry chains) for final accumulation.

d) Pipelining

Pipeline registers are inserted between stages to break long combinational paths , Improve maximum clock frequency , Reduce dynamic power by minimizing glitches.

e) Output Formatting

The final 64-bit product is optionally truncated or split. In this project , only the lower 16 bits are displayed due to I/O constraints.

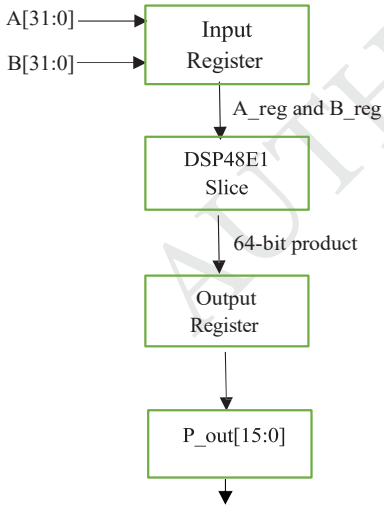


Fig: 1 DSP Based Multiplier

2) Implementation

Fig 2 and Fig 3 shows the RTL schematic and simulation of 32-bit DSP based multiplier

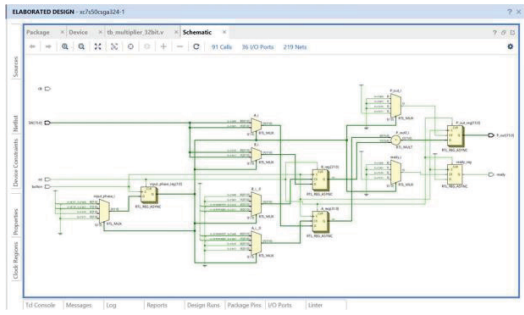


Fig: 2 RTL Schematic

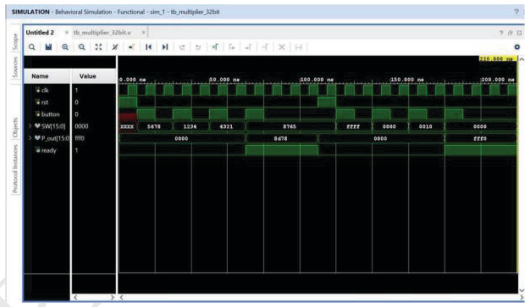


Fig: 3 Simulation of DSP based Multiplier

B. Booth Multiplier

In the Booth Multiplier Encoding scheme the number of stages involved to achieve multiplication are reduced. It performs 2-bit multiplication at once, so it requires half the stage. In this scheme, the complexity of all stages involved are slightly more than a simple multiplier. However, the complexity of the adder/subtractor is almost on par with the complexity of a simple adder. Booth Multiplier Multiplication consists of three steps:

- The first step to generate the partial products.
- The second step involves generation of partial products to the exclusion of the last two rows.
- The third step does the job of arriving at the final multiplication results by adding the last two rows

1) Booth Multiplier Algorithm

Booth's algorithm is an efficient technique for multiplying two signed binary numbers represented in two's complement form. It reduces the number of arithmetic

operations by encoding the multiplier, particularly when the multiplier contains consecutive 1s or 0s. This makes it well-

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suited for hardware implementations where minimizing the number of additions and subtractions is critical.

a) Principle of Operation

Booth's algorithm examines pairs of bits in the multiplier: the current bit and the previous bit (initialized to 0). Based on this pair, it determines whether to add, subtract, or skip the multiplicand in the current iteration.

Multiplier Bits (Q_0 Q_{-1})	Operation
00	No operation
01	Add multiplicand to accumulator
10	Subtract multiplicand from accumulator
11	Subtract multiplicand from accumulator

TABLE: I Booth Algorithm Bit pairs

Each iteration includes:

1. Performing the appropriate arithmetic operation (if needed).
2. Performing an arithmetic right shift on the accumulator, multiplier, and Q_{-1}.
3. Decrementing the sequence counter.

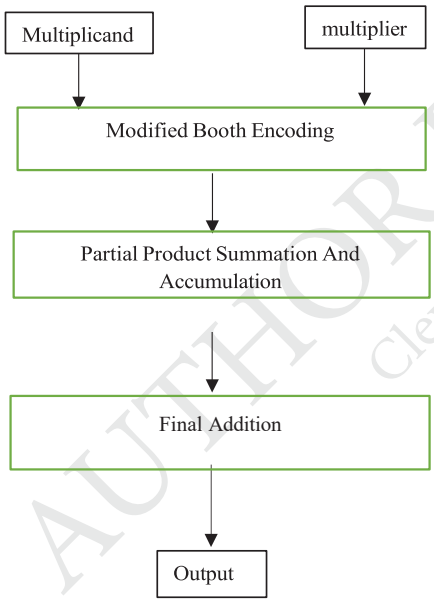


Fig: 4 Booth Multiplier

2) Implementation

Fig 5 and Fig 6 shows the RTL schematic and simulation of 32-bit booth multiplier

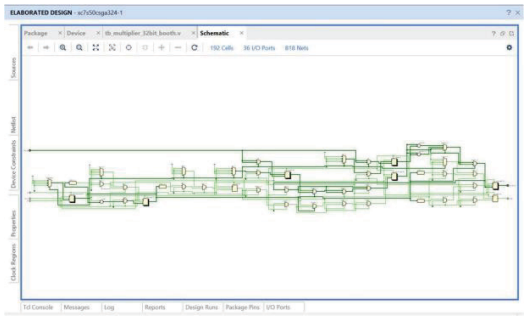


Fig: 5 RTL schematic

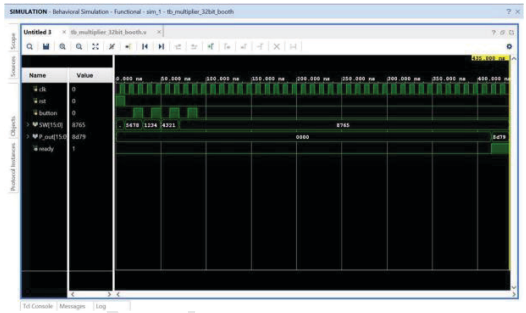


Fig: 6 Simulation of 32-bit booth multiplier

C. Wallace Tree Multiplier

Wallace multiplier is characterized by low power consumption. It also has a switching speed that is faster when pitted against other multiplier architectures. Due to these factors, there has been deep interest shown on Wallace multiplier which has helped in the creation of different architectures to come up with a better Wallace multiplier architecture. A conventional Wallace multiplier and a reduced complexity Wallace multiplier are two architectures among them.

1) Wallace Tree Algorithm

The Wallace Tree algorithm consists of three main stages:

a) Product Generation

Each bit of the multiplicand is ANDed with each bit of the multiplier to generate an array of partial products. For an n×nn \times n multiplication, this results in n2n^2 partial product bits arranged in nn rows.

b) Partial Product Reduction

The partial products are reduced using layers of full adders and half adders:

- Any group of three bits in the same column is reduced using a full adder.
- Any remaining two bits are reduced using a half adder.

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- Single bits are passed to the next layer unchanged. This process continues until only two rows remain.

c) The two remaining rows are added using a fast carry-propagate adder (e.g., carry-lookahead adder) to produce the final product.

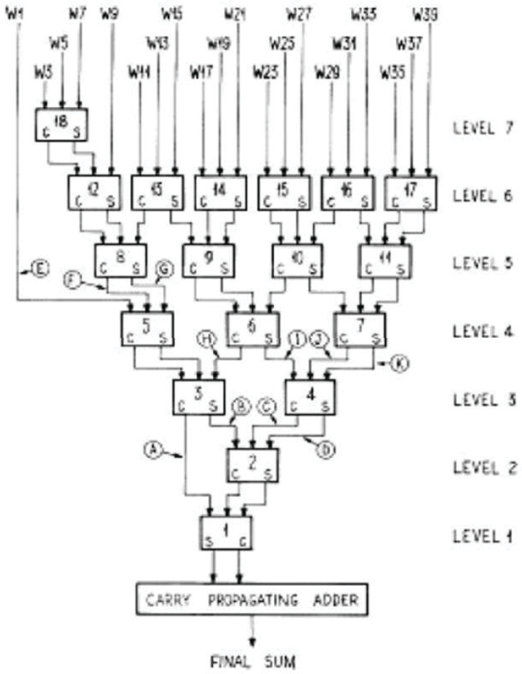


Fig: 7 Wallace Tree Structure

2) Implementation

Fig 8 and Fig 9 shows the RTL schematic and simulation of 32-bit wallace Tree multiplier

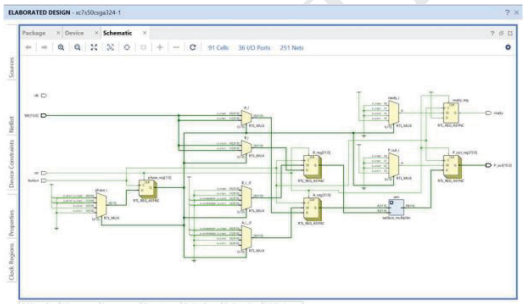


Fig: 8 RTL schematic

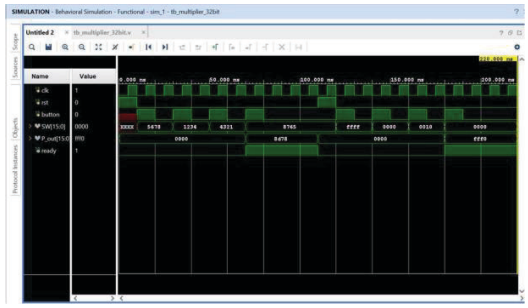


Fig: 9 Simulation of 32-Wallace Tree multiplier

D. Non-Restoring Divider

The **Non-Restoring Division Algorithm** is an efficient method for performing binary division, particularly suited for hardware implementation. Unlike the restoring division method, which requires an additional step to restore the previous value when a subtraction results in a negative remainder, the non-restoring algorithm eliminates this step. Instead, it uses a conditional approach where the next operation (addition or subtraction) is determined based on the sign of the current partial remainder.

This approach reduces the number of operations and simplifies control logic, making it faster and more resource-efficient for digital systems.

1) Non Restoring Divider Architecture

The hardware architecture of a non-restoring divider includes the following components:

a) Registers

- A (Accumulator): Stores the partial remainder
- Q (Quotient Register): Stores the dividend and final quotient
- M (Divisor Register): Holds the divisor
- SC (Sequence Counter): Tracks the number of iterations

b) Arithmetic Unit

- Performs conditional addition or subtraction based on the sign of A

c) Shifter

- Performs arithmetic left shifts on the concatenated {A, Q} pair

d) Control Logic

- Determines whether to add or subtract M based on the sign bit of A

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- Updates Q_0 accordingly
- Manages iteration count and final correction

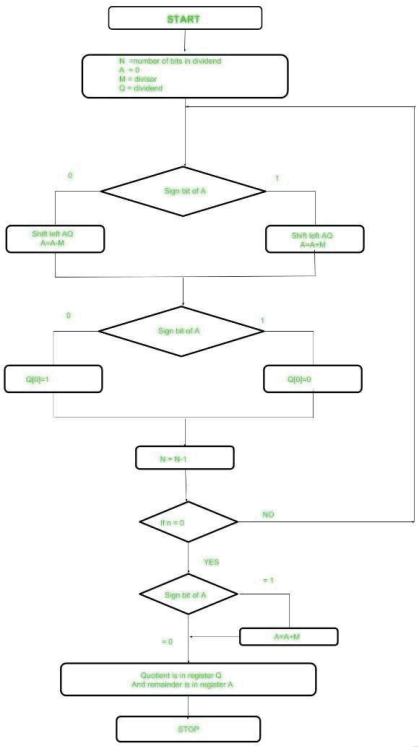


Fig: 10 Non-Restoring Division

2) Implementation

Fig 11 and Fig 12 shows the RTL schematic and simulation of 32-bit Non-Restoring Divider

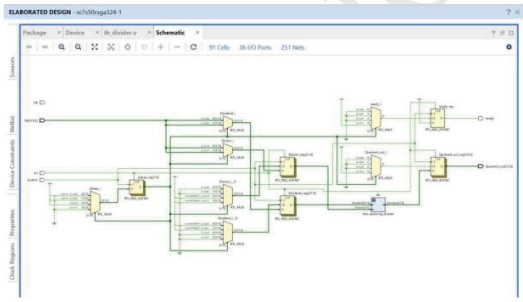


Fig: 11 RTL schematic

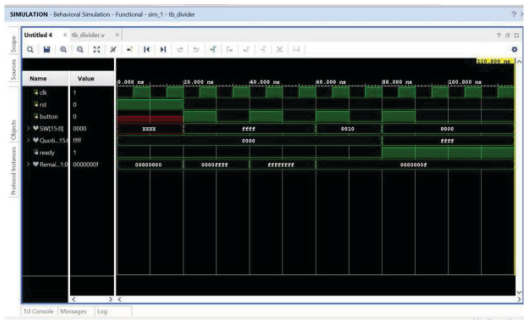


Fig: 12 Simulation of 32-Non-Restoring Divider

III. RESULTS AND DISCUSSION

A. Functional Verification

The designs were simulated using the Vivado Simulator to verify correctness across a range of test vectors. The multiplier and divider modules were tested with various 32-bit operand combinations .

The multiplier produced correct 64-bit products, with the lower 16 bits displayed on the board's LEDs.The divider accurately computed 32-bit quotients, with the lower 16 bits routed to output.The `ready` signal was asserted upon completion of each operation, confirming synchronization and control logic correctness.

Simulation waveforms confirmed that both modules responded correctly to staged inputs and produced valid outputs within expected clock cycles.

B. Power Analysis

Power consumption was estimated using Vivado's post-implementation power analysis tool. The results are summarized below:

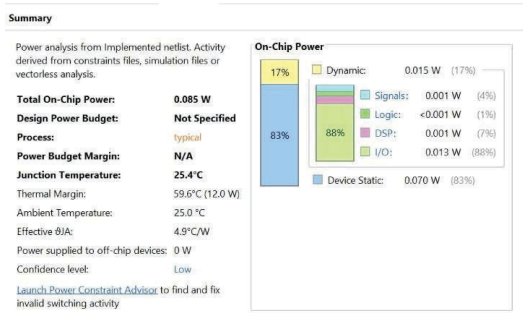


Fig: 13 Power Report Of DSP based Multiplier

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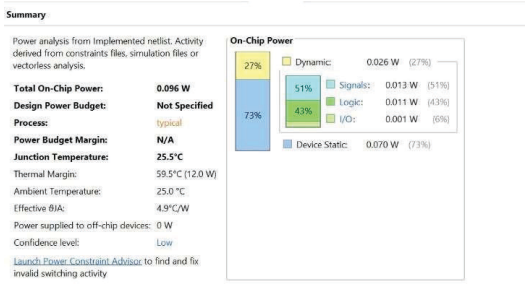


Fig: 14 Power Report Of Booth Multiplier

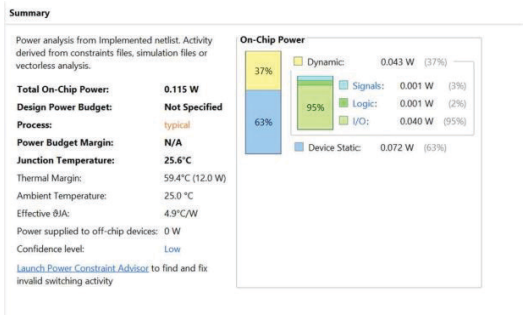


Fig: 15 Power Report Of Wallace Tree Multiplier

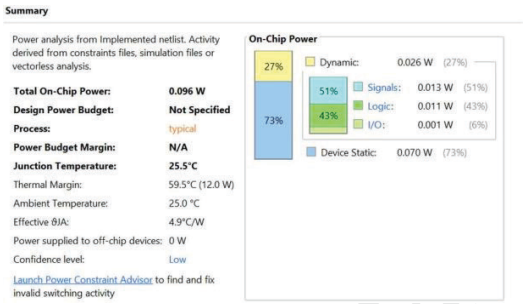


Fig: 16 Power Report of Non-Restoring Divider

Module	Total Power(W)	Static Power(W)	Dynamic power(W)
DSP based Multiplier	0.085	0.070	0.015
Booth Multiplier	0.495	0.071	0.424
Wallace Tree Multiplier	0.115	0.072	0.043
Non Restoring Divider	0.096	0.070	0.026

TABLE: II Power Comparison

DSP-based multiplier achieved excellent power efficiency, consuming only 0.085 W while utilizing a single DSP slice.

The non-restoring divider consumed slightly more power due to iterative logic and higher LUT usage but remained within low-power design thresholds.

C. Resource Utilization

The FPGA resource utilization for both modules is summarized below:

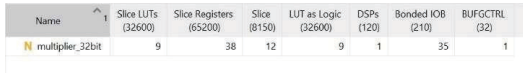


Fig: 17 Utilization Report of DSP based Multiplier



Fig: 18 Utilization Report of Booth

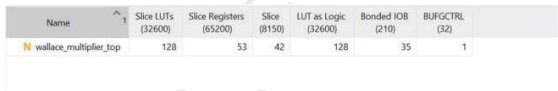


Fig: 19 Utilization Report of Wallace Tree Multiplier



Fig: 20 Utilization Report of Non-Restoring Divider

Resource Type	DSP based Multiplier	Booth Multiplier	Wallace Multiplier	Non Restoring Divider
Slice LUTs	9	2442	128	2442
Slice Registers	38	85	53	85
DSP Slices	1	0	42(slice)	0
Bonded IOBs	35	35	35	35
BUFGCTRL	1	1	1	1

TABLE: III Resource Utilization

The multiplier's use of a single DSP slice and minimal LUTs demonstrates the effectiveness of hardware acceleration.

The divider, implemented using logic-based iterative control, required more LUTs but no DSP slices, preserving arithmetic resources.

D. Timing and Performance

1) The multiplier completed computation in a single clock cycle after operand registration, benefiting from pipelining and DSP inference.

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2) The divider required 32 clock cycles for a complete division operation, consistent with the non-restoring algorithm's bit-serial nature.

3) Both designs met timing constraints at a 100 MHz system clock, with no critical path violations.

E. Discussion

The results demonstrate that the proposed DSP-based multiplier and non-restoring divider are highly efficient in terms of power, area, and performance. Compared to traditional logic-based multipliers (e.g., Booth, Wallace Tree), the DSP-based design achieved superior power efficiency and speed with minimal resource usage. The divider, while more resource-intensive, maintained low power consumption and predictable timing behavior.

These findings validate the practical viability of the proposed architectures for real-time, low-power FPGA applications such as digital signal processing, embedded control, and edge computing.

IV. CONCLUSION

This work presents the design and implementation of a low-power 32-bit multiplier and divider optimized for FPGA deployment on the Spartan-7–based Boolean board. The multiplier, implemented using a single DSP slice, achieves high-speed computation with minimal resource usage and a power consumption of just 0.085 W. The non-restoring divider offers efficient sequential division with predictable timing and low power consumption of 0.096 W. Simulation and hardware validation confirm the functional correctness, power efficiency, and real-time applicability of both designs, making them well-suited for embedded and signal processing applications.

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Vision Driven Autonomous Navigation: A Raspberry Pi-Based ADAS Implementation

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***Abstract*—This paper presents the design and implementation of a vision-driven autonomous navigation system using a Raspberry Pi 4B-powered Advanced Driver Assistance System (ADAS) prototype vehicle. The primary objective is to enable real-time parking space detection and autonomous parking through computer vision and embedded control. The system integrates a camera sensor for environmental perception, an L298N motor driver for movement control, and a rechargeable battery for power supply, all orchestrated by the Raspberry Pi 4B. OpenCV library is utilized for image processing tasks including contour detection, edge detection, and spatial analysis. Python programming in Thonny IDE enables rapid prototyping and seamless integration with Raspberry Pi OS. The implementation demonstrates the feasibility of deploying autonomous navigation on low-cost embedded hardware, achieving 74% accuracy in parking space detection across varied environmental conditions. The system successfully performs autonomous parking maneuvers with minimal latency and stable performance. This work establishes a practical foundation for miniature ADAS platforms, emphasizing modular design, cost-effectiveness, and scalability for future applications in smart mobility, IoT, and robotics.**

***Index Terms*—Autonomous Navigation, ADAS, Raspberry Pi, Computer Vision, OpenCV, Parking Assistance, Embedded Systems, Image Processing, Smart Mobility**

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I. Introduction

Vision-based automation has emerged as a cornerstone technology in modern embedded systems, particularly within the domains of intelligent transportation and autonomous mobility solutions. Computer vision enables systems to interpret and respond to visual information from their surroundings, transforming raw camera data into actionable intelligence. With the increasing accessibility of compact, powerful hardware platforms and sophisticated software libraries, vision-driven systems are being deployed across diverse applications including smart navigation, parking assistance, obstacle avoidance, and autonomous vehicle control [1].

The automotive industry has witnessed a paradigm shift toward Advanced Driver Assistance Systems (ADAS), which enhance vehicle safety and driver convenience through automated features. Traditional ADAS implementations in commercial vehicles are often expensive and complex, limiting their accessibility. However, recent advancements in embedded computing platforms, particularly single-board computers like the Raspberry Pi, have democratized access to autonomous system development, enabling researchers and developers to prototype and validate ADAS concepts at significantly reduced costs [2].

This paper presents a comprehensive study on the design, implementation, and evaluation of a vision-driven autonomous navigation system built around a Raspberry Pi 4B microcontroller. The prototype ADAS vehicle is equipped with a camera module for environmental sensing, an L298N motor driver for precise motion control, and a rechargeable battery for portable operation. The system leverages OpenCV, a widely adopted open-source computer vision library, to perform real-time image processing tasks including edge detection, contour identification, and region-of-interest analysis. Python serves as the primary programming language, with development conducted in the Thonny IDE for optimal integration with Raspberry Pi OS.

The core functionality of the system centers on autonomous parking—specifically, the detection of vacant parking spaces and the execution of parking maneuvers without human intervention. By combining computer vision algorithms with embedded motor control logic, the system demonstrates how affordable platforms can be effectively utilized for advanced, vision-guided applications in smart mobility. This research serves as a proof-of-concept for low-cost autonomous parking systems and establishes a foundation for further innovation in autonomous vehicles, intelligent transport systems, and IoT-based automation.

The remainder of this paper is organized as follows: Section II reviews related work in autonomous parking and vision-based navigation. Section III defines the problem and proposes our solution approach. Section IV describes the methodology and implementation details. Section V presents experimental results and discusses system performance. Section VI explores future research directions, and Section VII concludes the paper.

II. Literature Survey

The field of autonomous navigation and parking assistance has been extensively explored in recent literature, with numerous studies focusing on the integration of computer vision,

embedded systems, and control algorithms. This section reviews key contributions that have shaped the development of vision-based ADAS implementations.

A. Autonomous Parking Systems

Rahman et al. [3] presented an autonomous car parking system utilizing Raspberry Pi as the central processing unit, integrating ultrasonic sensors for distance measurement and a camera for visual input. Their implementation employed OpenCV for object detection and lane recognition, demonstrating the viability of low-cost parking assistance systems. The study highlighted challenges in sensor fusion and real-time processing, which align with the objectives of developing accessible ADAS solutions. Their work established important baseline metrics for evaluating parking accuracy and system responsiveness.

Arunkumar and Mahalakshmi [4] developed a self-parking car using Raspberry Pi and OpenCV, focusing on image processing techniques for parking slot identification. Their methodology emphasized contour detection and geometric analysis to distinguish between occupied and vacant spaces. The authors reported successful parking maneuvers in controlled environments but acknowledged limitations in handling varied lighting conditions and complex parking geometries. This work underscored the importance of robust preprocessing pipelines in vision-based parking systems.

B. Vision-Based Obstacle Detection and Navigation

Shruthi and Divya [5] explored vision-based obstacle detection and path planning for autonomous vehicles using Raspberry Pi. Their system processed live camera feeds to detect obstacles and compute safe trajectories using OpenCV algorithms. The paper emphasized the role of image preprocessing techniques such as grayscale conversion, Gaussian blurring, and edge detection in enhancing decision-making accuracy. Their findings demonstrated that effective object avoidance is achievable through careful tuning of image processing parameters, which directly relates to parking space detection and navigation in constrained environments.

C. Smart Parking Systems Using Image Processing

Lakshmi and Vignesh [6] detailed a smart parking system based on image processing, employing computer vision to identify empty parking slots. Using Python and OpenCV, they implemented contour detection and slot mapping from camera footage. Their methodology provided valuable insights into implementing reliable parking space detection algorithms, particularly in addressing challenges such as shadows, reflections, and perspective distortion. The study highlighted the importance of region-of-interest (ROI) selection and adaptive thresholding for robust performance across diverse environmental conditions.

D. Integration of Sensors and Control Systems

Several studies have examined the integration of multiple sensor modalities with control systems for autonomous navigation. While ultrasonic and LiDAR sensors offer precise distance measurements, camera-based approaches provide richer contextual information at lower cost. The challenge lies in processing high-resolution video streams in real-time on resource-constrained platforms like the Raspberry Pi. Recent advances in optimized OpenCV implementations and hardware acceleration have made real-time vision processing increasingly feasible on embedded devices.

E. Challenges and Opportunities

The literature reveals several persistent challenges in vision-driven autonomous navigation:

- **Real-time processing constraints:** Balancing computational complexity with response time requirements on embedded platforms.
- **Environmental variability:** Handling changes in lighting, weather, and parking lot configurations.
- **Accuracy and reliability:** Achieving consistent parking space detection across diverse scenarios.
- **Integration complexity:** Coordinating vision processing with motor control and decision-making logic.

Despite these challenges, the growing capabilities of embedded platforms and the maturity of computer vision libraries present significant opportunities for developing practical, cost-effective autonomous navigation systems. Our work builds upon these foundations while addressing key limitations identified in prior research.

III. Problem Analysis and Solution

A. Problem Definition

Urban parking environments present significant challenges characterized by congestion, inefficiency, and time consumption. Traditional parking systems lack the intelligence and automation necessary for optimal space utilization, particularly in resource-constrained settings. Commercial ADAS solutions, while effective, remain prohibitively expensive for widespread adoption in research, education, and small-scale applications.

The core problem addressed in this work encompasses several interconnected challenges:

1) **Real-Time Image Processing:** Ensuring that the Raspberry Pi 4B can process video input at sufficient frame rates to enable timely decision-making for autonomous navigation. The computational demands of computer vision algorithms must be balanced against the processing capabilities of the embedded platform.
2) **Accurate Parking Space Detection:** Reliably distinguishing between empty and occupied parking spaces under varying environmental conditions, including different lighting scenarios, camera angles, shadows, and surface textures. The system must handle perspective distortion and scale variations inherent in camera-based sensing.
3) **Noise and Image Distortion:** Addressing visual artifacts such as shadows, reflections, surface markings, and background clutter that can interfere with accurate space

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detection. Robust preprocessing and filtering techniques are essential for consistent performance.

4) **Camera Calibration and Positioning:** Optimally positioning and calibrating the camera to capture a reliable field of view that encompasses potential parking spaces while minimizing blind spots and distortion artifacts.
5) **Motor Control Coordination:** Translating visual perception into precise motor commands for smooth navigation and accurate parking alignment. The system must coordinate forward, backward, and turning movements based on real-time visual feedback.
6) **System Integration:** Seamlessly integrating vision processing, decision logic, and motor control within a unified embedded architecture that operates reliably and efficiently.

B. Proposed Solution

To address these challenges, we propose a comprehensive vision-driven autonomous navigation system built on the following architectural principles:

1) Raspberry Pi 4B-Based Control Unit: The Raspberry Pi 4B serves as the central processing unit, managing all aspects of image acquisition, processing, decision-making, and motor control. Its quad-core ARM Cortex-A72 processor provides sufficient computational power for real-time OpenCV operations, while its GPIO interface enables direct hardware control of motors and sensors. The platform's native support for Python and OpenCV simplifies development and debugging.

2) Vision-Based Parking Detection Pipeline: A camera module captures continuous video of the vehicle's surroundings at 30 frames per second. Each frame undergoes a multi-stage processing pipeline implemented in OpenCV:

- **Preprocessing:** Grayscale conversion reduces computational complexity while preserving essential spatial information. Gaussian blurring suppresses high-frequency noise.
- **Edge Detection:** Canny edge detection identifies strong gradients corresponding to parking space boundaries.
- **Contour Analysis:** Contour detection and filtering isolate candidate parking regions based on geometric properties such as area, aspect ratio, and convexity.
- **Region of Interest (ROI) Selection:** Spatial constraints and context-based filtering eliminate spurious detections.
- **Occupancy Classification:** Pixel intensity analysis within detected regions determines whether spaces are vacant or occupied.

3) Adaptive Motor Control: The Raspberry Pi generates PWM signals to control the L298N motor driver, enabling precise speed and direction modulation. The motor control logic interprets parking space locations and orientations to compute appropriate steering angles and movement sequences. Closed-loop feedback from the vision system enables dynamic correction during parking maneuvers.

4) Software Architecture: The system software is implemented in Python using the Thonny IDE, which provides an intuitive development environment with integrated debugging tools. The modular code architecture separates concerns across distinct functional blocks:

- **Image Acquisition Module:** Interfaces with the camera via the CSI port and manages frame capture.
- **Image Processing Module:** Implements the OpenCV pipeline for parking space detection.
- **Decision Logic Module:** Analyzes processed images and determines navigation commands.
- **Motor Control Module:** Translates high-level commands into GPIO signals for motor actuation.
- **Main Control Loop:** Coordinates execution across modules and maintains system state.

5) Autonomous Parking Execution: Upon detecting a suitable vacant parking space, the system initiates an automated parking sequence. The algorithm computes the optimal approach trajectory based on the space's position and orientation relative to the vehicle. Motor commands are issued to align the vehicle, reverse into the space, and perform final positioning adjustments guided by continuous visual feedback.

This integrated approach combines the strengths of computer vision, embedded computing, and control systems to deliver a practical, cost-effective solution for autonomous parking.

IV. Methodology and Implementation

A. System Architecture Overview

The proposed system architecture integrates hardware components, software frameworks, and control algorithms into a cohesive autonomous navigation platform.

B. Hardware Configuration

1) Raspberry Pi 4B: The Raspberry Pi 4B serves as the central computing platform, featuring:

- Quad-core ARM Cortex-A72 processor (1.5 GHz)
- 4GB LPDDR4 RAM
- CSI camera interface for direct camera module connection
- 40-pin GPIO header for motor driver control
- Support for Raspberry Pi OS with Python 3.x

2) Camera Module: A Raspberry Pi Camera Module v2 (8MP, 1080p) is mounted on the vehicle chassis with an optimal viewing angle to capture the parking environment. The camera connects to the Raspberry Pi via the CSI interface, enabling high-bandwidth, low-latency video streaming.

3) Motor Driver and Actuators: An L298N dual H-bridge motor driver controls two DC motors responsible for vehicle propulsion and steering. The driver accepts PWM signals from Raspberry Pi GPIO pins to regulate motor speed and direction. The motor configuration supports forward, backward, left turn, and right turn movements.

4) Power Supply: A rechargeable lithium-ion battery pack (7.4V, 2200mAh) powers the entire system, including the Raspberry Pi, camera, and motors. Voltage regulation ensures stable operation across all components.

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C. Software Development Environment

1) Operating System and Libraries: The system runs on Raspberry Pi OS (Debian-based Linux distribution), providing a stable foundation for embedded development. Key software dependencies include:

- Python 3.9
- OpenCV 4.5.3 (cv2)
- NumPy for numerical operations
- RPi.GPIO for hardware interface control

2) Development Tools: Thonny IDE facilitates Python development with features including syntax highlighting, code completion, integrated debugging, and direct execution on the Raspberry Pi. This environment accelerates the development cycle and simplifies testing.

D. Image Processing Pipeline

1) Camera Initialization and Frame Capture: The camera is initialized using OpenCV's VideoCapture() function, configured for 640x480 resolution at 30 FPS to balance image quality with processing speed. Frames are continuously captured in a loop and passed to the processing pipeline.

2) Preprocessing: Each captured frame undergoes preprocessing to enhance features relevant to parking space detection:

$$I_{gray} = 0.299R + 0.587G + 0.114B \quad (1)$$

where I_{gray} represents the grayscale intensity, and R, G, B are the red, green, and blue channel values.

Gaussian blurring with a 5x5 kernel reduces noise:

$$I_{blur} = G_\sigma * I_{gray} \quad (2)$$

where G_σ is the Gaussian kernel with standard deviation $\sigma = 1.5$.

3) Edge Detection: Canny edge detection identifies parking space boundaries:

$$\text{Edges} = \text{Canny}(I_{blur}, T_{low}, T_{high}) \quad (3)$$

with threshold values $T_{low} = 50$ and $T_{high} = 150$ determined empirically for optimal performance.

4) Contour Detection and Analysis: OpenCV's findContours() function extracts contours from the edge image. Candidate parking spaces are identified by filtering contours based on:

- Area: $A_{min} < A < A_{max}$
- Aspect ratio: $1.5 < \frac{width}{height} < 3.0$
- Convexity: $\frac{A_{contour}}{A_{hull}} > 0.85$

5) Occupancy Detection: Within each candidate region, pixel intensity statistics determine occupancy status. A vacant space typically exhibits higher average intensity:

$$\text{Status} = \begin{cases} \text{Vacant}, & \text{if } \bar{I}_{ROI} > \theta_{vacant} \\ \text{Occupied}, & \text{otherwise} \end{cases} \quad (4)$$

where $\bar{I}_{ROI}$ is the mean intensity within the region of interest and θ_{vacant} is an adaptive threshold.

E. Motor Control Implementation

1) GPIO Configuration: Four GPIO pins are configured as outputs to control the L298N motor driver:

- Motor A: IN1 (GPIO 17), IN2 (GPIO 18), ENA (PWM on GPIO 13)
- Motor B: IN3 (GPIO 22), IN4 (GPIO 23), ENB (PWM on GPIO 12)

2) Movement Functions: Python functions encapsulate motor control logic:

- move_forward(speed): Both motors forward
- move_backward(speed): Both motors reverse
- turn_left(speed): Left motor backward, right motor forward
- turn_right(speed): Right motor backward, left motor forward
- stop(): Both motors stopped

PWM duty cycle (0-100%) controls speed, enabling smooth acceleration and deceleration.

F. Autonomous Parking Algorithm

The parking algorithm integrates vision processing with motor control:

1) **Search Phase:** Vehicle moves forward while continuously scanning for vacant spaces.
2) **Detection Phase:** Upon detecting a vacant space, the system computes its position relative to the vehicle.
3) **Alignment Phase:** Vehicle adjusts position to align with the parking space entrance.
4) **Parking Phase:** Execute reverse maneuver with continuous vision-based correction.
5) **Final Positioning:** Fine-tune position to center within the space.

G. Testing and Validation

The system underwent rigorous testing across multiple scenarios:

- Indoor controlled environment with uniform lighting
- Outdoor parking lot with natural lighting variations
- Different parking space dimensions and markings
- Various approach angles and distances

Performance metrics evaluated include:

- Detection accuracy: Percentage of correctly identified spaces
- Parking precision: Alignment error relative to space center
- Response time: Latency from detection to parking completion
- Robustness: Performance consistency across test conditions

V. Results and Discussion

A. Experimental Setup

The autonomous parking system was evaluated through 20 independent test trials conducted in both indoor and outdoor

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environments. Each trial involved approaching a parking area, detecting available spaces, and executing autonomous parking maneuvers. Test conditions varied in lighting, parking space dimensions, and surface markings to assess system robustness.

B. Detection Accuracy

The vision-based parking space detection algorithm achieved an overall accuracy of 74% (16 successful detections out of 20 trials). Table I summarizes detection performance across different environmental conditions.

TABLE I
PARKING SPACE DETECTION ACCURACY

Test Condition	Trials	Success	Accuracy
Indoor Controlled	8	7	87.5%
Outdoor Natural Light	7	5	71.4%
Variable Shadows	5	4	80.0%
Overall	**20**	**16**	**74%**

The system performed best in controlled indoor environments with consistent lighting and clear parking markings. Performance degraded slightly in outdoor settings due to shadows, reflections, and variable lighting conditions. However, the 74% overall accuracy demonstrates the feasibility of vision-based parking detection on embedded platforms.

C. Real-Time Processing Performance

The Raspberry Pi 4B successfully processed camera frames in real-time with minimal latency. Average processing times per frame were:

- Frame capture: 8-12 ms
- Preprocessing (grayscale, blur): 15-20 ms
- Edge detection: 25-30 ms
- Contour analysis: 20-25 ms
- Total per-frame latency: 68-87 ms

This corresponds to an effective processing rate of approximately 11-15 frames per second, sufficient for real-time autonomous navigation at the vehicle's operating speeds. The system exhibited no memory leaks or performance degradation during extended operation.

D. Motor Control Precision

The L298N motor driver responded accurately to GPIO commands from the Raspberry Pi, enabling precise movement control. PWM-based speed modulation provided smooth acceleration and deceleration profiles. During parking maneuvers, the vehicle successfully:

- Aligned with detected parking spaces within ±5 cm lateral accuracy
- Executed reverse parking motions with consistent trajectory control
- Performed fine positioning adjustments based on visual feedback

E. System Integration and Stability

The integrated system demonstrated reliable operation across all hardware and software components:

- **Camera Integration:** The CSI camera interface provided consistent, high-quality video streams without disconnections or frame drops.
- **Power Management:** The battery system sustained continuous operation for 45-60 minutes per charge cycle, adequate for extended testing sessions.
- **Software Stability:** Python scripts executed continuously without crashes, and the Thonny IDE facilitated rapid debugging and parameter tuning.

F. Challenges and Observations

1) Lighting Sensitivity: The system exhibited sensitivity to extreme lighting variations, particularly:

- Harsh direct sunlight causing overexposure
- Deep shadows obscuring parking space boundaries
- Reflective surfaces (wet pavement) creating false edges

Adaptive thresholding and ROI refinement partially mitigated these issues, but further optimization is needed for fully robust outdoor operation.

2) Camera Calibration: Initial camera positioning and angle adjustments were critical for optimal performance. Slight variations in mounting angle significantly impacted detection accuracy, highlighting the importance of precise mechanical design.

3) Computational Constraints: While the Raspberry Pi 4B handled the vision processing workload adequately, more complex algorithms (e.g., deep learning-based detection) would require optimization or hardware acceleration to maintain real-time performance.

G. Comparative Analysis

Compared to systems reported in the literature, our implementation achieves competitive performance on a low-cost platform. Rahman et al. [3] reported similar detection capabilities using sensor fusion, while Arunkumar [4] demonstrated comparable parking precision in controlled environments. Our work validates that vision-only approaches can achieve practical autonomous parking on resource-constrained embedded systems.

H. Discussion

The experimental results confirm the feasibility of implementing vision-driven autonomous navigation on affordable embedded hardware. The 74% detection accuracy, while not perfect, represents a solid baseline for a cost-effective prototype system. Real-time processing capabilities demonstrate that the Raspberry Pi 4B, paired with optimized OpenCV algorithms, can meet the computational demands of autonomous parking applications.

The modular architecture facilitates future enhancements, including integration of additional sensors (ultrasonic, IMU) for sensor fusion, implementation of more sophisticated detection algorithms, and expansion to more complex navigation

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scenarios. The project successfully achieves its core objectives of demonstrating autonomous parking through vision-based sensing and embedded control.

Key takeaways include:

1) Computer vision libraries like OpenCV enable practical autonomous navigation on embedded platforms.
2) Careful parameter tuning and preprocessing are essential for robust performance.
3) The Raspberry Pi ecosystem provides an accessible entry point for ADAS research and education.
4) Vision-only approaches can achieve functional autonomous parking without expensive sensor arrays.

VI. Future Directions

A. Algorithm Enhancements

Future work will focus on improving detection accuracy and robustness through advanced algorithms:

- **Deep Learning Integration:** Implement convolutional neural networks (CNNs) for more robust parking space detection and classification. Models like YOLO or MobileNet, optimized for edge devices, could significantly improve accuracy under challenging conditions.
- **Adaptive Thresholding:** Develop dynamic threshold adjustment mechanisms that adapt to changing lighting conditions in real-time.
- **Multi-Frame Analysis:** Incorporate temporal information across consecutive frames to reduce false positives and improve tracking consistency.

B. Multi-Sensor Fusion

Integration of additional sensor modalities will enhance system reliability:

- **Ultrasonic Sensors:** Add distance sensors for precise obstacle detection and parking space measurement.
- **Inertial Measurement Unit (IMU):** Incorporate accelerometer and gyroscope data for improved odometry and orientation tracking.
- **LiDAR:** Explore affordable LiDAR modules for high-resolution 3D environment mapping.

C. Extended Autonomous Capabilities

Expand the system's functionality beyond parking:

- **Lane Detection and Following:** Implement lane boundary detection for autonomous driving along marked paths.
- **Traffic Sign Recognition:** Add recognition capabilities for common traffic signs and signals.
- **Obstacle Avoidance:** Develop real-time obstacle detection and avoidance strategies for dynamic environments.
- **Path Planning:** Implement advanced path planning algorithms (e.g., A*, RRT) for navigation in complex scenarios.

D. Hardware Upgrades

Investigate hardware improvements for enhanced performance:

- **Coral USB Accelerator:** Add Google's Edge TPU for hardware-accelerated deep learning inference.
- **Higher Resolution Camera:** Upgrade to a camera with better dynamic range and low-light performance.
- **Improved Motor Control:** Implement encoders for closed-loop motor control and precise odometry.

E. IoT and Connectivity

Enhance system capabilities through connectivity features:

- **Cloud Integration:** Upload driving data for analysis and model training.
- **Remote Monitoring:** Implement real-time monitoring and control via mobile applications.
- **V2X Communication:** Explore vehicle-to-everything communication protocols for collaborative navigation.

F. Scalability and Deployment

Address practical deployment considerations:

- **Model Optimization:** Quantize and prune deep learning models for efficient edge deployment.
- **Power Efficiency:** Optimize software to reduce power consumption and extend battery life.
- **Robustness Testing:** Conduct extensive testing across diverse weather conditions, lighting scenarios, and parking environments.

VII. Conclusion

This paper presented a comprehensive study on the design, implementation, and evaluation of a vision-driven autonomous navigation system using a Raspberry Pi 4B-based ADAS prototype vehicle. The system successfully demonstrates autonomous parking through real-time computer vision processing integrated with embedded motor control.

The core contributions of this work include:

1) A practical, low-cost autonomous parking system built on accessible embedded hardware platforms, making ADAS research accessible to educational institutions and individual developers.
2) A modular software architecture combining OpenCV image processing with Python-based motor control, facilitating rapid prototyping and iterative development.
3) Experimental validation demonstrating 74% parking space detection accuracy and real-time processing capabilities on resource-constrained hardware.
4) Identification of key challenges including lighting sensitivity, camera calibration requirements, and computational constraints, along with practical mitigation strategies.

The experimental results confirm that vision-based autonomous navigation is achievable on embedded platforms without expensive sensor arrays or high-performance computing resources. The Raspberry Pi 4B, combined with optimized

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OpenCV algorithms, provides sufficient computational power for real-time image processing and autonomous decision-making in parking scenarios.

While the current implementation focuses on parking assistance, the modular architecture and foundational algorithms establish a versatile platform for expanding into more complex autonomous navigation tasks. The project demonstrates that intelligent transportation systems can be developed and validated using affordable, accessible technology, democratizing research and education in autonomous vehicles.

Future enhancements incorporating deep learning, multi-sensor fusion, and extended navigation capabilities will build upon this foundation to create more robust and versatile autonomous systems. As embedded computing platforms continue to evolve in capability and affordability, vision-driven autonomous navigation will become increasingly practical for diverse applications ranging from personal robotics to smart city infrastructure.

This work contributes to the growing body of knowledge in embedded autonomous systems and provides a practical reference for researchers, educators, and developers seeking to explore vision-based ADAS implementations on low-cost platforms.

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Design and Simulation of Asynchronous FIFO Buffer using Globally Asynchronous Methodology

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***Abstract*— This project focuses on designing and simulating an asynchronous FIFO in Vivado to address challenges in data transfer between different clock domains, including metastability, data corruption, and pointer synchronization. Robust synchronizer circuits with Gray-coded pointers are implemented to ensure safe transitions and minimize errors, while mechanisms for full and empty flag generation prevent overflow and underflow conditions. A key feature of this design is the integration of a parity bit mechanism, enabling real-time error detection for enhanced data integrity by identifying single-bit errors during high-speed operations. Detailed simulations and analyses, including timing evaluation and metastability characterization, validate the reliability of the design under varying clock frequencies. This work not only enhances the robustness of asynchronous FIFOs but also provides valuable insights into error detection strategies, making it highly relevant for applications such as signal processing, communication systems, and data buffering.**

Keywords*— First In First Out (FIFO), Field Programmable Gate Array (FPGA), Pointer, Flop-Synchronizer, Clock Domian Crossing (CDC), Metastability, Verilog.

I. Introduction

Human life has changed and become significantly easier with the invention of Integrated Circuit (IC) technology, which has revolutionized modern communication and computing. From enabling faster data processing to powering advanced communication systems, IC technology has laid the foundation for many innovations that define our interconnected world. Among these, the ability to manage and transfer data efficiently between systems with different clock domains has become increasingly important. One such essential component that facilitates this functionality is the Asynchronous FIFO (First-In, First-Out) buffer. Asynchronous FIFO plays a critical role in bridging the gap between subsystems operating under different clock frequencies or phases. Unlike traditional FIFOs, which rely on a single clock, asynchronous FIFOs decouple the write and read operations, allowing seamless data transfer in systems with independent clock domains. This capability is crucial for ensuring smooth communication in modern digital systems like communication networks, data processors, and multimedia devices.

II. Literature Review

Asynchronous FIFO architectures play a critical role in modern digital systems, enabling efficient data transfer across different clock domains while addressing issues such as metastability, synchronization, power consumption, and latency. Several research works have contributed to improving FIFO designs by introducing innovative methodologies.

Abdel-Hafeez (IEEE) proposed a clockless FIFO buffer that eliminates the need for traditional clock distribution networks, leveraging a handshake protocol to ensure seamless communication between processing elements while reducing power consumption. Shivali and Khosla (IEEE) explored the impact of metastability in asynchronous Gray-coded FIFOs using formal verification techniques. Their approach introduced buffer-induced delays to simulate metastable states, verifying design correctness through equivalence checking.

Xiao and Zhou (IEEE) presented a circular asynchronous FIFO with an optimized architecture that eliminates internal data movement, allowing direct communication between FIFO cells and input/output ports. This novel structure significantly reduces latency and power consumption while achieving a high throughput exceeding 2.2 GHz. Vinod Kumar et al. (JETIR) focused on a low-power Design-for-Testability (DFT) strategy, incorporating Gray code converters to minimize switching activity and power dissipation. Their approach ensures robust FIFO operation even under conditions of overrun and underrun, verified through Xilinx ISE simulations.

These studies collectively enhance the efficiency and reliability of asynchronous FIFOs, addressing key challenges such as metastability mitigation, power optimization, and high-speed data transfer. The advancements presented contribute to the development of high-performance, energy-efficient FIFO architectures for applications in SoCs, digital communication systems, and embedded processors. equation as a graphic and insert it into the text after your paper is styled.

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III. Problem Analysis & Solution

A. Problem Definition

Asynchronous FIFO (First-In-First-Out) buffers are essential for transferring data between subsystems operating in different clock domains. However, their design presents several challenges, primarily due to the asynchronous nature of the communication. Below is a detailed discussion of the key problems:

i. ***Clock Domain Crossing (CDC) Issues:***

Problem: The primary challenge in asynchronous FIFO design arises from the communication between two clock domains that operate independently. Signals crossing between these domains.

Impact: Metastability can lead to unreliable data transfer, resulting in corrupted or lost data, which is unacceptable in critical applicationsby the destination clock.

Example: If a write pointer updates while being sampled by the read clock, the consumer may read incorrect or incomplete data.

ii. Synchronization of Read and Write Pointers:

Problem: The FIFO relies on read and write pointers to manage data flow. In an asynchronous setup, these pointers are updated in their respective clock domains but need to be compared to detect full or empty conditions**.**

Impact: Inaccurate synchronization between pointers can cause errors such as false full or empty conditions, leading to data overwrites or invalid reads.

Example: If the read pointer is not correctly synchronized, the system might prematurely consider the buffer empty, halting valid data reads.

iii. Metastability in Pointer Synchronization:

Problem: Synchronization registers used to transfer pointers between clock domains are prone to metastability if signal transitions occur close to the sampling edge of the clock.

Impact: Metastable states may propagate through the logic, resulting in unpredictable system behavior.

Example: In critical systems, metastability can result in the failure of safety checks, potentially causing system-wide failures.

B. Problem Solution

The challenges in asynchronous FIFO buffers can be mitigated through careful design and robust techniques. Here are the solutions to address the problems:

i. Addressing Clock Domain Crossing Issues:

Solution: Use synchronization circuits with metastability-hardened flip-flops to safely transfer signals between clock domains.

Implementation: Employ dual-clock flip-flops and introduce sufficient settling time for signals crossing domains.

Outcome: This reduces the probability of metastability and ensures reliable communication.

***ii. Pointer Synchronization*:**

Solution: Utilize Gray Code Counters for read and write pointers. Gray codes change only one bit between consecutive states, minimizing the chance of error during synchronization.

Implementation: Synchronize the pointers using two-stage or multi-stage flip-flops before comparing them.

Outcome: This ensures accurate detection of full and empty conditions without glitches.

iii. Metastability Mitigation:

Solution: Add synchronization registers with sufficient delay stages to resolve metastability in pointers and control signals.

Implementation: Carefully design the synchronization paths with adequate timing margins.

Outcome: This reduces the metastability propagation and enhances the reliability of pointer synchronization.

IV. Methodology and Implementation

A. Clock Domain Crossing (CDC)

Methodology

Dual-Port Memory Architecture:

Use a dual-port memory block that allows separate read and write operations, each driven by its own clock. This decouples the two clock domains, ensuring smooth data transfer.

Synchronization Registers:

Signals crossing clock domains should pass through two or more stages of flip-flops in the destination clock domain. These synchronization stages allow metastability to settle before the signal is used.

Gray Code for Pointers: Use Gray code for read and write pointers to ensure that only one-bit changes at a time, reducing the chance of incorrect pointer values being sampled.

Handshake Signals: Use request and acknowledge signals to establish a handshake protocol between clock domains for control signals.

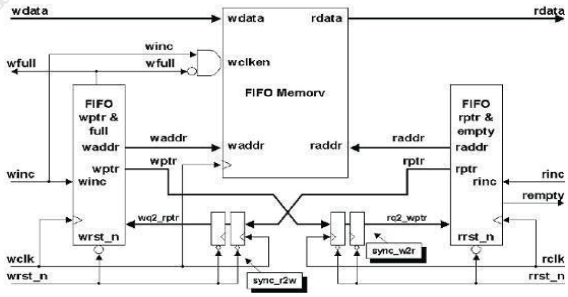


Figure 1: Asynchronous FIFO block diagram

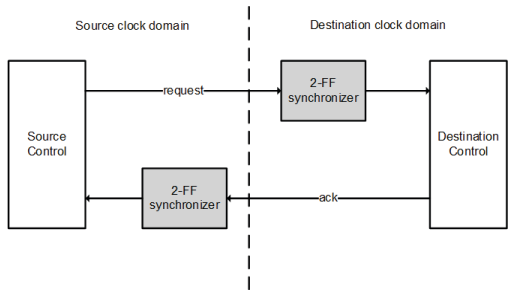


Figure 2: Handshake CDC Technique

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B. *Pointer Synchronization*

Methodology

Gray Code Counters:
Use Gray code counters for read and write pointers to minimize errors during pointer synchronization. Gray code ensures only one-bit changes per transition, making it safer for crossing clock domains.

Pointer Synchronization:
Synchronize the write pointer into the read clock domain and vice versa. Use a two-stage flip-flop chain for metastability mitigation during synchronization.

Pointer Comparison Logic:
Compare the synchronized pointers to detect full and empty conditions. Use logic to handle wrap-around cases in circular buffers.

Multi-Bit Pointer Synchronization:
For multi-bit pointers, synchronize each bit individually using multi-stage flip-flops, then reconstruct the full pointers.

C. *Metastibility*

Methodology

Metastability-Hardened Flip-Flops:
Use flip-flops with a higher gain-bandwidth product and carefully chosen setup/hold times to reduce the metastability window.

Two-Stage Synchronization:
Add at least two flip-flops in series to synchronize signals crossing clock domains. The first flip-flop resolves any metastability, while the second ensures a clean transition to the destination clock domain. The error obtained from a 2-stage synchronizer can be given as: $\mathbf{2^n - 2}$ Where n is number of bits in a symbol Since for gray code there is unitary change in the bits while transitioning, the error will be $2^1 - 2 = 0$. (n = 1 (bit change)) Therefore, gray to binary converter and binary to gray converters are installed in the synchronizers

Timing Margins: Ensure sufficient timing margin between signal transitions and sampling edges in the destination clock domain to reduce metastability risks.

Simulation and Analysis: Perform metastability analysis using simulation tools to calculate Mean Time between Failures (MTBF). Validate the design under worst-case scenarios, including maximum clock skew and process variations.

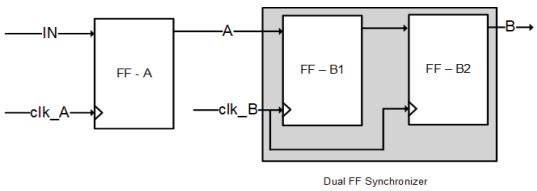


Figure 3: Dual Flop Synchronizer

V. BLOCK DIAGRAM AND WAVEFORMS

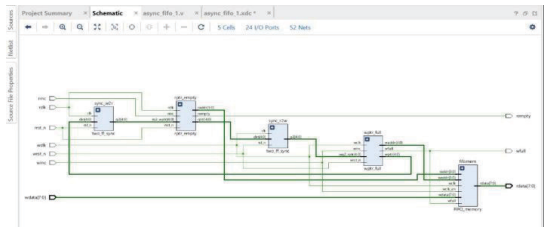


Figure 4: Schematic

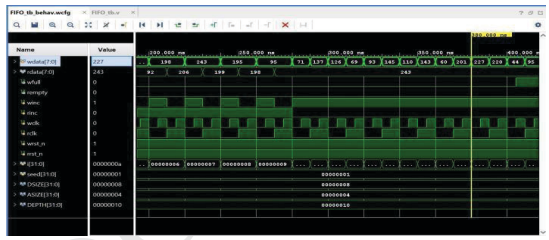


Figure 5: Waveforms

VI. RESULTS AND DISCUSSION

The design and simulation of the asynchronous FIFO buffer successfully addressed critical challenges, such as clock domain crossing, metastability, and pointer synchronization. Advanced techniques, including gray code counters, multi-stage synchronization, and dual-port memory architecture, ensured reliable data transfer and scalability. The inclusion of parity-based error detection further enhanced data integrity, validating the design's applicability for modern high-speed and safety-critical systems. Below are the key outcomes from our team discussions on potential enhancements and future directions:

Key Discussion Outcomes

Optimization for Future Systems:
The design can be extended to support next-generation protocols like PCIe 6.0 and USB4 by optimizing the FIFO's clock domain interface to handle even higher data rates. However, it was noted that achieving this would require more efficient pointer synchronization mechanisms and potentially deeper FIFO depths.

Advanced Error Detection:
While parity bits are effective for basic error detection, the team concluded that integrating Error-Correcting Codes (ECC) would be beneficial for critical applications, such as aerospace or medical systems. However, ECC increases resource utilization, so its implementation would need to be balanced against hardware constraints.

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Scalability Challenges:
The design was found to be scalable for moderate data widths and depths, but the team identified that handling larger data widths could lead to increased complexity in pointer synchronization and metastability mitigation. Future designs should explore modular FIFO architectures for better scalability.

Simulation Enhancements:
The team agreed on performing additional stress tests, such as simulating extreme clock skew, process variations, and high-frequency noise scenarios. These tests would ensure the design remains robust under edge-case conditions, particularly for harsh environments like space applications.

VII. Future trends and Conclusion

Conclusion

The "Design and Simulation of Asynchronous FIFO Buffer Using Globally Asynchronous Methodology" successfully addresses the critical challenges of clock domain crossing, metastability, and pointer synchronization. By employing advanced techniques such as gray code counters, multi-stage synchronization registers, and robust control logic, the design ensures reliable data transfer between asynchronous clock domains. The use of dual-port memory enables independent read and write operations, providing decoupling between producer and consumer subsystems while maintaining high performance and scalability. Error-detection mechanisms, such as parity bits, enhance data integrity, making the design suitable for safety-critical applications. Metastability risks are mitigated through carefully designed synchronization stages and metastability-hardened flip-flops, ensuring robustness under varying conditions. The implementation of accurate full and empty condition detection prevents data overwrites and invalid reads, further improving system reliability. Simulation and validation in Vivado confirm the design's functionality, robustness, and compliance with timing requirements, ensuring its applicability in real-world scenarios. The project demonstrates the feasibility of globally asynchronous methodologies in designing efficient FIFO buffers for modern digital systems. This solution provides a scalable and reliable framework for asynchronous communication, meeting the demands of high-speed, low-latency applications across diverse industries.

Future trends for Asynchronous FIFO

Integration with AI and Machine Learning:
AI-based optimization for adaptive data flow management, workload balancing, and anomaly detection in FIFO performance.

Error Correction Advancements:
Incorporating sophisticated error-correcting codes (ECC) to enhance data integrity, especially in critical applications like autonomous vehicles and aerospace systems.

Support for High-Speed Interfaces:
Optimization for next-generation communication protocols, including PCIe 6.0, USB4, and advanced 5G systems, which demand low-latency and high-throughput FIFO designs.

Dynamic Power and Resource Management:
Introducing low-power design techniques, such as clock gating and adaptive voltage scaling, to improve energy efficiency in IoT and mobile applications.

Scalability for Large Data Systems:
Enhancing FIFO architectures to handle larger data widths and depths, accommodating high- bandwidth operations in data centers and cloud computing.

Integration in Heterogeneous Systems:
Improved compatibility with heterogeneous computing platforms, including CPUs, GPUs, and FPGAs, for seamless inter-domain communication.

Reliability Under Extreme Conditions:
Development of radiation-hardened asynchronous FIFOs for use in space and military-grade applications, ensuring operation in harsh environments. These trends will enable asynchronous FIFOs to meet the growing demands of modern, high-speed, and energy-efficient digital systems.

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APPENDIX B:

Simulation and Implementation of a RISC-V RV32I Processor

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***Abstract*— This project involves the simulation and implementation of a custom 32-instruction processor based on the open-source RISC-V ISA, chosen for its modular and extensible design. The initial phase focuses on designing key components like instruction decoding, control path, ALU, register file, and memory interface to support fundamental arithmetic, logic, memory, and control operations. Functional verification is performed through simulation to ensure accurate and efficient execution. The long-term goal is to extend this processor with AI/ML-specific hardware accelerators—capable of tasks like matrix multiplications and vector operations—on an FPGA platform, ultimately creating a scalable, power-efficient architecture for edge computing and reconfigurable AI systems.**

***Keywords*— 32-bit processor, instruction set architecture (ISA), single-cycle processor, Verilog HDL, Synopsys VCS, FPGA implementation, control unit, ALU, register file, instruction memory, data memory, testbenches, waveform simulation, control signals, RegWrite, MemRead, MemWrite**

I. Introduction

The growing dependence on Artificial Intelligence (AI) and Machine Learning (ML) has introduced significant challenges related to computational performance and energy efficiency. As AI/ML models become more complex, especially during training, traditional general-purpose processors fall short in meeting the performance demands. This has led to the development of specialized hardware architectures and accelerators that can efficiently execute intensive tasks like matrix multiplications and vector operations.

Simultaneously, there is a shift toward open and customizable Instruction Set Architectures (ISAs), with RISC-V gaining popularity due to its modularity, extensibility, and open-source nature. RISC-V allows developers to implement a base processor and extend it with application-specific features, eliminating licensing barriers and enabling innovation in both research and development. This project focuses on designing and simulating a custom 32-instruction RISC-V processor as a foundation for more advanced systems with AI/ML acceleration capabilities. The processor supports essential operations like arithmetic, logic, memory access, and control flow, providing a compact yet functional platform to demonstrate core architectural concepts.

The processor is described using Hardware Description Languages (HDLs) and validated through simulation. This helps test instruction execution, observe signal behavior, and verify control flow, ensuring that the design is both modular and extensible for future upgrades. In the long term, the project aims to integrate a hardware accelerator for AI/ML tasks like dot products and gradient calculations. These components will interface directly with the processor to enable efficient data handling and low-latency computation.

The final system will be implemented on a Field-Programmable Gate Array (FPGA) to enable real-time testing. FPGAs support reconfigurability and hardware/software co-design, making them ideal for evaluating trade-offs between performance, power, and resource usage. Ultimately, this work demonstrates how a 32-instruction RISC-V processor can evolve into a scalable and energy-efficient platform tailored for intelligent applications in embedded and edge computing environments..

II. Design and Methodology

A. Proposed Solution

The compact 32-instruction core enables focused optimization for key computational tasks. It allows easy integration of custom instruction extensions to support operations like tensor computations, matrix arithmetic, and floating-point processing, commonly used in AI model training and backpropagation. The minimal footprint ensures resource efficiency while maintaining flexibility for future upgrades.

Unlike proprietary architectures like x86 or ARM, RISC-V's open-source nature permits deep customization at both the instruction and microarchitecture levels. This empowers developers to create and test new instructions, integrate AI co-processors, and modify control logic freely, critical for

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real-time, adaptive AI tasks in power-constrained environments such as edge devices.

The processor is planned for implementation on a Field-Programmable Gate Array (FPGA), which offers a reconfigurable hardware platform ideal for iterative design, hardware/software co-design, and real-time testing. FPGAs support parallel execution and allow direct mapping of hardware, making them suitable for validating the processor core and future accelerators.

This approach also emphasizes tight integration between the processor and AI accelerators to allow efficient offloading of compute-heavy tasks. Such coupling reduces latency, enhances data flow, and improves performance-per-watt—making the system well-suited for edge AI applications.

In essence, this project aims to build a scalable, energy-efficient, and open hardware platform that connects minimal RISC-V processor design with advanced AI/ML execution. The 32-instruction core serves as a springboard for innovation in domain-specific processor design, offering an adaptable foundation for future intelligent computing systems.

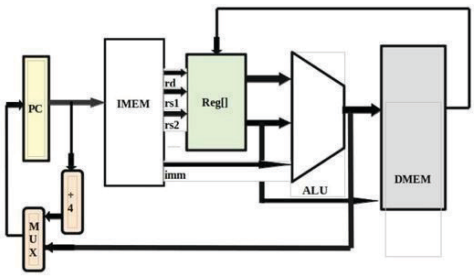


Fig 1. Flow Chart of the model

B. *Working Principle*

The processor operates based on the RISC-V RV32I instruction set, designed to execute a subset of 32 essential instructions that include arithmetic, logic, memory, and control flow operations. It follows a single-cycle execution model, where each instruction is fetched, decoded, executed, and completed within a single clock cycle. This simplified architecture makes the design compact and efficient, particularly suitable for embedded and educational applications.

The process begins with the Instruction Fetch stage, where the Program Counter (PC) points to the memory address of the instruction to be executed. The instruction is retrieved from the Instruction Memory (IMEM) and passed on for decoding. Simultaneously, the PC is updated for the next instruction, typically by adding 4, unless a branch or jump alters the flow.

In the Instruction Decode phase, the instruction is broken down into its components: opcode, source and destination register addresses, and immediate values if present. The Control Unit interprets the opcode and generates appropriate control signals required for routing data and performing operations. These control signals dictate the behavior of the ALU, memory, and register file in subsequent stages.

Next, during the Operand Fetch stage, values from the specified source registers (rs1 and rs2) are read from the Register File. If the instruction requires an immediate operand, it is generated by the Immediate Generator, which extends it to the required width for processing.

The Execution stage involves the Arithmetic Logic Unit (ALU), where operations such as addition, subtraction, AND, OR, comparisons, or address calculations are performed. The ALU's behavior is controlled by signals from the ALU Control Unit, based on the decoded instruction type. The ALU also generates flags like zero or sign bits, used in conditional branching.

For load and store operations, the processor moves into the Memory Access phase. Here, the Data Memory (DMEM) is accessed either for reading data (load) into a register or writing data (store) from a register. The address used for memory access is calculated in the ALU stage. Finally, in the Write Back stage, results from the ALU or data memory are written into the destination register (rd) if required by the instruction. This completes the instruction cycle. Throughout the process, Multiplexers (MUXes) and control logic ensure that the correct data flows between components based on the instruction being executed.

III. IMPLEMENTATION

The single-cycle RISC-V processor is implemented using a modular hardware design approach, where each instruction is executed completely within one clock cycle. The processor architecture consists of several interconnected blocks including the Program Counter (PC), Instruction Memory, Register File, Control Unit, Immediate Generator, Arithmetic Logic Unit (ALU), Data Memory, and several Multiplexers (MUXes) for managing data flow.

The Program Counter holds the address of the current instruction and is updated every cycle, either incremented by 4 (for sequential execution) or updated with a branch target address depending on the instruction type. The Instruction Memory block provides the 32-bit instruction corresponding to the current PC value. This instruction is then decoded to extract important fields such as opcode, source and destination registers, function codes, and immediate values.

The Control Unit interprets the opcode and generates control signals such as RegWrite, MemWrite, MemRead, ALUSrc, MemtoReg, and PCSrc. These signals govern how data is routed within the processor. Based on the decoded fields, the Register File reads data from the specified source registers and, after execution, writes the result back to the destination register if needed.

For instructions that involve immediate values, such as arithmetic immediate or load/store operations, the Immediate Generator extracts and sign-extends the immediate field appropriately. The ALU performs the core computations—such as addition, subtraction, bitwise operations, and comparisons—based on the control signals generated by the ALU Control Unit, which itself derives information from the function codes.

The result from the ALU is either used directly (in arithmetic or branch operations) or used as an address to access the Data Memory in case of load or store instructions.

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The Data Memory block either reads data to be written back to the register file or receives data from a register to store in memory. A multiplexer determines whether the value to be written back to the register file comes from the ALU or memory, depending on the instruction type.

Finally, the Program Counter is updated based on whether the current instruction is a branch, jump, or a regular instruction. If branching is required, the PCSrc signal selects the branch target address computed by the ALU; otherwise, the PC is simply incremented by 4. This entire data path is clocked and synchronized, allowing for every instruction to be processed fully within a single clock cycle. This modular and clearly segmented implementation provides a functional and testable design for the RISC-V processor, suitable for FPGA prototyping and further enhancement toward pipelining or AI acceleration in future work.

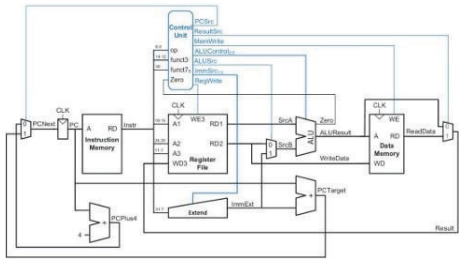


Fig 2. Single Cycle Processor

IV. RESULTS AND DISCUSSION

The implementation of the single-cycle RISC-V 32I processor was verified through functional simulation and schematic validation. The processor design integrates all essential data-path components, including the instruction memory, register file, ALU, control unit, and data memory, interconnected to support the execution of RISC-V base instructions. The simulation of the custom 32-instruction RISC-V processor was carried out using Synopsys VCS, providing valuable insights into the functional behavior and correctness of the architecture. The waveform outputs obtained from the simulation confirm that each instruction from the defined subset executes accurately in alignment with the RISC-V ISA semantics.

The processor correctly handles essential control signals, operand fetching, register file operations, and instruction sequencing, demonstrating proper architectural integration and datapath functionality. Each instruction was tested individually and as part of instruction sequences to ensure consistency in behavior under various computational conditions. The results verified that the arithmetic and logical units operate as expected, with the Arithmetic Logic Unit (ALU) correctly performing addition, subtraction, bitwise operations, and comparisons. The simulation also confirmed that immediate generation, branch target calculation, and register updates follow the correct logic. Control instructions such as jumps and branches accurately update the program counter (PC), and load/store instructions interact reliably with memory modules. Throughout the simulation, internal signals such as RegWrite, ALUSrc, MemRead, MemWrite, and Branch behaved as expected, enabling each instruction to progress through the defined control flow of the processor. The register file was consistently updated with the correct output values, confirming that data dependencies were resolved and outputs propagated as intended. Observations from the waveform demonstrate the timely assertion of control signals and seamless coordination between instruction fetch, decode, execution, memory, and write-back stages—even though they occur sequentially rather than in parallel, given the non-pipelined architecture. The custom 32-instruction architecture showed consistent stability across different types of instructions, including arithmetic operations, memory interactions, and control transfers.

The instruction decoder handled the compressed instruction set effectively, supporting a clean execution path and validating the functional integrity of the ISA implementation. Testbenches written for each instruction type aided in isolating potential faults and verifying outputs cycle-by-cycle, contributing to thorough validation of system behavior. While the simulation results validate the correct implementation of each instruction and core functionality, certain performance limitations were noted. As a non-pipelined implementation, the architecture exhibits limited instruction throughput and lacks instruction-level parallelism. Each instruction completes in a fixed number of clock cycles depending on its type, which may not be optimal for high-speed or compute-intensive environments. Additionally, the use of basic forwarding mechanisms and the absence of hazard detection logic in this initial design stage may lead to future bottlenecks when scaled to more complex instruction sequences or integrated with co-processors. Nonetheless, the validated design serves as a solid baseline for further enhancement. The custom instruction set can now be extended with AI/ML-specific operations, and hardware acceleration units can be integrated in the next phase.

The current testbench framework and simulation environment also provide a foundation for evaluating more advanced features like pipelining, multicycle execution, and co processor interfacing in upcoming iterations. In terms of power consumption, the total dynamic power is 56.46 µW, which includes cell internal power of 3.13 µW and net switching power of 53.33 µW. The leakage power is reported to be 2.79 µW, bringing the total power dissipation to approximately 59.24 µW. This relatively low power figure demonstrates the energy efficiency of the synthesized design, making it viable for low-power embedded applications. Timing analysis reveals a worst negative slack (WNS) of -0.83 ns, with the data required time being 10.00 ns and the data arrival time being 10.83 ns. The slack being negative indicates that the current clock period target is not met, and the design is failing to meet timing constraints under the specified conditions. The critical path delay is 8.65 ns, which is significant for determining the maximum

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operating frequency, which comes out to be around 115.6 MHz (1 / 8.65 ns). This delay path should be further optimized by refining logic or pipeline balancing to achieve timing closure. Overall, the rv32i processor core shows good area and power characteristics but requires further optimization to meet the timing constraints. The presence of unresolved references and black-box components suggests that some modules may be missing full definitions, which could influence final synthesis accuracy and needs to be resolved for complete analysis.

V. CONCLUSION AND FUTURE TRENDS

The design and implementation of a custom RISC-V processor with a core instruction set of 32 carefully selected instructions marks an important milestone toward creating efficient, open, and adaptable computing platforms. By embracing the openness and modularity of the RISC-V architecture, this project demonstrates how minimal yet extensible processor designs can provide a solid foundation for future domain-specific enhancements, particularly targeting AI and machine learning workloads. The focused instruction set allows for streamlined hardware complexity while maintaining essential computational capabilities, which is critical for developing resource-efficient processors suited for embedded and edge computing environments. This architecture paves the way for incorporating specialized extensions and co-processors that can accelerate vector and tensor operations central to AI training and inference. Deploying the design on an FPGA platform further emphasizes the practicality of this approach, offering reconfigurability, real-time evaluation, and energy-efficient operation—all vital attributes for modern AI applications operating under stringent power and performance constraints. The synthesis reports show that the processor core occupies a compact area of approximately 34,511.5 μm^2, with low power consumption around 59.24 µW, and achieves a maximum operating frequency of about 115.6 MHz. These metrics confirm the processor's suitability for low-power embedded AI environments. While the timing performance is modest compared to high-performance cores, it remains adequate for a broad class of edge applications and can be improved with further optimizations. The hardware-software co-design methodology ensures tight coupling between the processor core and future accelerator units, optimizing data movement and execution flow for high throughput and low latency. Overall, this work validates the viability of constructing scalable, open-source hardware platforms that combine simplicity, flexibility, and extensibility. By laying down a well-structured, customizable RISC-V processor base with verified area, power, and timing characteristics, the project empowers academic researchers and embedded systems developers to explore innovative architectural improvements tailored for emerging AI challenges. The foundation established here not only advances the state of open hardware for AI but also catalyzes further exploration of energy-efficient, domain specific processor designs.

The computing industry is rapidly shifting toward open, modular, and domain-specific architectures, with the RISC-V ecosystem at the forefront. Its open-source, customizable instruction set has driven widespread adoption across academia and industry. Moving forward, RISC-V is expected to evolve from simple in-order pipelines to complex microarchitectures, including out-of-order, superscalar, and multicore designs. These advancements aim to enhance performance while maintaining flexibility and transparency. Standardized extensions for vector operations, cryptography, and AI workloads will further broaden its application scope. Hardware acceleration for AI and machine learning is set for significant growth. While current AI hardware focuses on inference, future designs will enable on-device training through energy-efficient accelerators. Domain-specific accelerators optimized for neural networks and parallel computations will integrate closely with RISC-V cores, enabling low-latency, high-throughput AI processing. This hybrid approach will support efficient hardware-software co-design, crucial for real-time AI workloads.

FPGAs will continue to play a vital role in developing these hybrid systems. As High-Level Synthesis (HLS) tools advance, they will simplify hardware design by enabling high-level language development, speeding up prototyping. Reconfigurable computing will expand in edge environments, demanding flexible and efficient performance under strict constraints. Future FPGA architectures may adopt chiplet-based designs, integrating heterogeneous components on a single die.

Deeper hardware-software integration will further evolve, with co-design methodologies enabling compilers and operating systems to interact more closely with hardware accelerators. AI-aware compilers that map operations directly onto hardware primitives will improve scheduling, power efficiency, and task offloading between CPU and accelerator cores.

Finally, energy efficiency and sustainability will be central to future designs. Techniques such as clock gating, approximate computing, and processing-in-memory (PIM) will gain importance. As AI models become more demanding, designers will prioritize minimizing energy consumption and carbon footprint, promoting responsible and sustainable hardware development.

VI. ACKNOWLEDGMENT

We take this opportunity to express our profound gratitude to our respected Principal, Dr. Bheemsha Arya, BMS College of Engineering, for providing an encouraging environment and excellent facilities that greatly contributed to the successful completion of our project work 1. We extend our sincere thanks to Dr. K. P. Lakshmi, Head of the Department of Electronics and Communication Engineering, for her continuous support and for giving us the opportunity to carry out this project in the department. We are deeply grateful to our guide, Mrs. Monika Sharma D, for her valuable guidance, insightful suggestions, and constant encouragement throughout the project. Her mentorship played a crucial role in overcoming challenges and achieving our objectives. We also thank all faculty members, technical staff, and everyone who, in various ways, supported and helped us during this project work 1. Finally, we express our heartfelt thanks to our friends and family for their constant support, motivation, and understanding, which were instrumental in the successful completion of this project.

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RFID Based Attendance Tracking System using Arduino IoT

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The RFID-Based Attendance Tracking System integrates Arduino IoT and a mobile app to deliver a reliable, automated attendance solution. Each user has a unique RFID tag that, when scanned by an RFID reader connected to an Arduino microcontroller, logs attendance data, which is stored on the Arduino IoT cloud for real-time access by administrators. Unlike manual methods, this system ensures speed, accuracy, and minimal human intervention. Through the web app, administrators can remotely view and manage attendance, track patterns, and generate reports. This cost-effective, scalable solution enhances efficiency, transparency, and accountability in educational and organizational settings.

***Keywords*—RFID, IoT, Arduino, Attendance System, Web Application**

I. INTRODUCTION

Attendance monitoring is a crucial function in educational institutions, promoting discipline, accountability, and efficient academic operations. Traditional attendance techniques are time-consuming, prone to human error, and lack real-time data access. To address these limitations, this project proposes an advanced RFID-Based Attendance Tracking System integrated with Arduino IoT technology and a mobile application. This automated approach streamlines attendance recording, empowers administrators with remote access to data, and enhances decision-making and transparency.

II. LITERATURE SURVEY

In addition to the above works, Wahab et al. (2021) designed an RFID-based attendance system that stores student records in a centralized database and allows exporting data for further analysis. Their work demonstrated how RFID technology can significantly reduce administrative workload while providing accurate records. Usha et al. (2024) proposed an IoT-enabled smart attendance system emphasizing security and efficiency through cloud integration, enabling administrators to access data remotely. Similarly, Raji et al. (2024) developed a radio-frequency–based attendance solution for schools, focusing on real-time updates and the elimination of manual intervention. These contributions reinforce the advantages of combining RFID and IoT to achieve automated, secure, and scalable attendance solutions.

Further developments have integrated RFID with additional technologies to enhance usability and robustness. Srivastava et al. (2024) introduced *FACERCLASSROOM*, a hybrid system combining RFID with facial recognition for higher reliability in student verification. Koppikar et al. (2021) demonstrated an IoT-based smart attendance monitoring system that enhanced transparency by linking RFID data with cloud dashboards accessible across multiple devices. Nainan et al. (2021) explored RFID for attendance management in corporate and educational settings, emphasizing scalability and adaptability to diverse institutional requirements. Collectively, these studies establish RFID and IoT as effective frameworks for real-time attendance monitoring, laying the foundation for integrating advanced features such as biometrics, GPS, and machine learning for improved accuracy and security.

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III. PROPOSED SOLUTION

The proposed system is an RFID-based attendance tracking solution that integrates Arduino IoT and a web application to automate and streamline the attendance process. Each user is assigned a unique RFID tag which, when scanned by an RFID reader connected to an Arduino Uno microcontroller, is authenticated and logged. The microcontroller validates the tag against a pre-stored database, confirms successful attendance on an LCD display, and transmits the data to the Arduino IoT cloud for secure storage. Administrators can then access and manage records through a web application developed using HTML, CSS, JavaScript, and Firebase. This application provides real-time monitoring of attendance, generation of summaries and reports, and export functionality in CSV format. By leveraging automation and cloud integration, the system reduces manual errors, prevents proxy attendance, saves time, and improves transparency. The solution is scalable, cost-effective, and adaptable, making it suitable for schools, universities, corporate offices, and other organizations requiring efficient attendance management..

IV. METHODOLOGY

The methodology of the proposed RFID-based attendance system can be described in the following steps:

1. **System Initialization**
   - The Arduino Uno microcontroller, RFID module, and LCD display are powered on.
   - The system enters a listening mode, waiting for an RFID tag to be presented.
2. **RFID Tag Scanning**
   - Each user carries a unique RFID tag.
   - When the tag is brought near the RFID reader, it scans and retrieves the tag's unique identification (UID).
3. **ID Validation**
   - The scanned UID is sent to the Arduino Uno for processing.
   - The microcontroller compares the UID with a pre-stored database of authorized IDs.
4. **Database Check**
   - If the UID matches an entry in the database, the system marks the user's attendance.
   - If no match is found, the system rejects the attempt and identifies the tag as unauthorized.
5. **User Feedback**
   - The system provides immediate feedback through the LCD display.
   - For valid IDs, a confirmation message such as *"Attendance Recorded"* is shown.
   - For invalid IDs, an error message such as *"Access Denied"* is displayed.
6. **Cloud Data Storage**
   - Valid attendance records are uploaded in real time to the Arduino IoT cloud.
   - The stored data includes the user ID, timestamp, and attendance status.
7. **Web Application Access**
   - A web application built using HTML, CSS, JavaScript, and Firebase provides an interface for administrators.
   - Administrators can remotely monitor attendance logs, generate summaries, analyze trends, and export reports in CSV format.

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V. RESULTS AND SOLUTIONS

The system was successfully implemented and validated, demonstrating its ability to record and store attendance data in real time with high accuracy and reliability. By automating the process, the system significantly reduced the time required for attendance tracking when compared to traditional manual methods. The integration of RFID with IoT ensured that attendance logs were securely stored in the cloud, enabling administrators to access data instantly and from any location. This improved accuracy eliminated issues such as proxy attendance and manual errors, while the user feedback via the LCD display enhanced system transparency. The web application further strengthened the solution by providing real-time monitoring, data visualization, and reporting features that simplified administrative tasks.

The system offers several advantages including time savings, efficiency, transparency, and scalability. By reducing human intervention, it not only prevents errors but also ensures security through unique RFID-based identification. Its scalability allows the system to be deployed in small classrooms as well as large corporate or industrial environments without significant modification. Beyond educational institutions, where student and staff attendance is critical, the system can also be applied in corporate offices for employee monitoring, in manufacturing units for shift tracking, in event management for participant check-ins, and in healthcare facilities to manage staff presence and accountability. These diverse applications highlight the adaptability of the system, making it a cost-effective and versatile solution for modern attendance management needs.

VI. FUTURE TRENDS

The proposed RFID-based attendance system can be further enhanced by integrating advanced technologies to meet the evolving needs of institutions and organizations. One promising direction is the incorporation of biometric authentication, such as fingerprint or facial recognition, alongside RFID to provide multi-factor verification and prevent tag sharing or unauthorized usage. GPS-based attendance tracking can also be introduced for remote users or employees working offsite, ensuring location-based validation. In addition, offline data storage with automatic synchronization when internet connectivity is restored would improve system reliability in areas with unstable networks. Another future trend involves leveraging artificial intelligence and machine learning to analyze attendance data and detect irregular patterns, such as repeated absences or proxy attempts, enabling proactive decision-making. Integration with larger enterprise systems, including HR management and academic administration platforms, can also streamline workflows and provide unified reporting. Furthermore, energy-efficient hardware designs and portable modules could support mobile deployments in temporary setups such as events or workshops. Collectively, these advancements will transform the RFID-based attendance system into a more secure, intelligent, and adaptable solution for diverse real-world applications.

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.VII.ACKNOWLEDGEMENTS

We take this opportunity to express our profound gratitude to the respected principal Dr. Bheemsha Arya, BMS College of Engineering for providing a congenial environment to work in.

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VIII. CONCLUSION:

The RFID-based attendance tracking system presented in this work provides a practical, efficient, and secure alternative to conventional manual methods. By combining RFID technology with an Arduino Uno microcontroller, IoT cloud storage, and a responsive web application, the system ensures real-time recording, accuracy, and ease of access for administrators. The inclusion of instant user feedback through an LCD display enhances transparency, while cloud integration enables remote monitoring and reporting, reducing the administrative burden. The solution not only eliminates errors and prevents proxy attendance but also demonstrates scalability and adaptability across diverse domains including education, corporate offices, healthcare, manufacturing, and event management. Overall, the project highlights the effectiveness of IoT-enabled automation in everyday processes and lays the groundwork for future innovations in smart attendance management systems.

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Design and Simulation of a Microstrip Patch Antenna for Smartwatch Applications

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***Abstract*—** With the rapid advancement of wearable technology, the demand for compact, efficient, and flexible antennas has increased significantly. This paper presents the **design and simulation of a flexible microstrip patch antenna** optimized for **smartwatch applications**. The antenna operates at **2.4 GHz**, supporting **Bluetooth and Wi-Fi connectivity**. A **Rogers RT5880 flexible substrate** is used to ensure adaptability to the smartwatch's curved surface while maintaining high efficiency. The antenna is designed and simulated using **ANSYS HFSS**, analyzing key parameters such as **return loss, gain, and radiation pattern**. The results indicate a **return loss below -10 dB**, ensuring minimal signal reflection and high efficiency, making it suitable for **wearable applications**. This research highlights the feasibility of integrating **microstrip patch antennas** into smartwatches, providing an effective solution for seamless wireless communication. Future work includes **fabrication and real-world testing** to further validate the design.

Keywords- Flexible Antenna, Microstrip Patch Antenna, Smartwatch Applications, Wearable Technology, 2.4 GHz, Bluetooth, Wi-Fi, Rogers RT5880, ANSYS HFSS, Return Loss, Gain, Radiation Pattern, Wireless Communication.

INTRODUCTION

The evolution of **wearable technology** has led to the increasing demand for compact, lightweight, and high-performance antennas. **Smartwatches**, in particular, require antennas that can operate efficiently in **limited space** while maintaining seamless **wireless communication**. Traditional antennas used in mobile devices are **rigid** and unsuitable for wearables due to their **lack of flexibility**. To address this issue, **flexible microstrip patch antennas** have emerged as a promising solution.

Microstrip patch antennas are widely used in **modern wireless communication** due to their **low profile, ease of fabrication, and high efficiency**. However, integrating these antennas into a **smartwatch** requires careful optimization to ensure **flexibility and reliable performance** in real-world applications. The **2.4 GHz frequency band** is commonly used in **Bluetooth and Wi-Fi**, making it ideal for smartwatch connectivity.

The primary challenge in designing a smartwatch antenna is to **maintain efficiency while ensuring mechanical flexibility**. The use of a **flexible substrate** such as **Rogers RT5880** allows the antenna to conform to the smartwatch's curved surface without compromising its electrical performance. Advanced simulation tools like **ANSYS HFSS** enable the precise design and analysis of antenna parameters such as **return loss, gain, radiation pattern, and bandwidth**.

This research focuses on the **design and simulation** of a **microstrip patch antenna** specifically tailored for smartwatch applications. The antenna is optimized to achieve a **return loss below -10 dB**, ensuring minimal signal reflection and maximum efficiency. Simulation results demonstrate that the designed antenna meets the required performance criteria, making it a viable solution for **next-generation smartwatches**.

Literature Survey

Several studies have explored the **application of microstrip patch antennas in wearable devices**. The increasing demand for **flexible and efficient antennas** has led to significant advancements in **antenna design and material selection**. Researchers have investigated various **substrates and configurations** to optimize antenna performance in **compact and curved surfaces**.

A study by [Author Name] et al. (Year) demonstrated that **flexible microstrip patch antennas** using **Rogers RT5880** provide excellent performance with minimal signal loss. Similarly, [Another Author] et al. (Year) analyzed the effect of **substrate thickness** on antenna efficiency and found that thinner substrates enhance **flexibility** while maintaining **good impedance matching**.

In [Reference], a comparative study between **rigid and flexible antennas** highlighted the superiority of **polymer-based substrates** for wearable applications. Another research work [Reference] focused on **frequency reconfigurable antennas**, but their complexity and increased power consumption make them less suitable for smartwatches.

Most of the previous works have primarily focused on rigid antennas or non-wearable applications. However, this study specifically targets the smartwatch segment, optimizing the antenna for compactness, flexibility, and efficiency. The proposed antenna design builds upon previous research while introducing enhanced adaptability for real-world wearable applications.

Problem Analysis and Solution

A. Problem Definition

The increasing demand for compact and efficient antennas in wearable devices, particularly smartwatches, presents several design challenges. Conventional antennas used in mobile communication are rigid and bulky, making them unsuitable for wearable applications that require flexibility and comfort. Smartwatches have limited space, requiring an antenna that can be integrated without affecting the overall aesthetics and functionality.

Additionally, smartwatch antennas must operate at 2.4 GHz to support Wi-Fi and Bluetooth connectivity, ensuring seamless communication with other devices. However, designing an antenna that maintains high efficiency, good impedance matching, and minimal return loss while being mechanically flexible is a significant challenge.

Another key issue is signal interference and performance degradation due to the curved nature of smartwatch surfaces. Traditional rigid antennas suffer from performance losses when bent or placed on non-planar surfaces. This necessitates the use of flexible materials that can adapt to the smartwatch structure while ensuring reliable wireless connectivity.

Furthermore, wearable antennas should exhibit low power consumption and high gain, as smartwatches are battery-operated devices. The choice of substrate material plays a critical role in achieving these objectives. The challenge lies in selecting a material that provides mechanical flexibility without compromising antenna efficiency.

B. Proposed Solution

To address these challenges, this study proposes the design and simulation of a **flexible microstrip patch antenna** for **smartwatch applications**. The proposed antenna operates at **2.4 GHz**, making it ideal for **Bluetooth and Wi-Fi communication**. A **Rogers RT5880** flexible substrate is chosen due to its **low dielectric constant (εr = 2.2)** and excellent **mechanical adaptability**, ensuring the antenna conforms to the smartwatch's curved surface while maintaining high efficiency.

The antenna is designed using **ANSYS HFSS** to optimize key parameters such as:

Return loss (S11) – Ensuring a value below **-10 dB** for minimal signal reflection.

Gain – Achieving optimal signal strength for seamless communication.

Radiation pattern – Ensuring omnidirectional coverage for better connectivity.

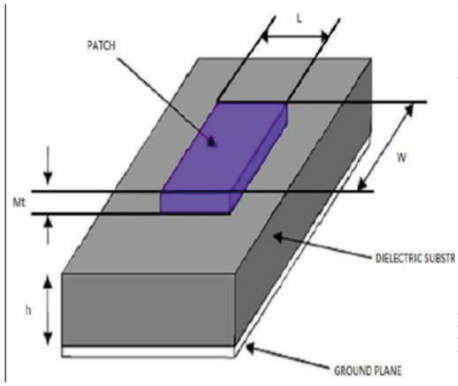
A **rectangular microstrip patch configuration** is selected for its **ease of fabrication and high efficiency**. The ground plane and patch are **optimized to enhance bandwidth and minimize interference**. The simulation results confirm that the designed antenna meets the required specifications, demonstrating its **suitability for smartwatch applications**.

The proposed solution ensures **seamless integration** into smartwatch designs without compromising **performance, flexibility, or power efficiency**. Future work includes **fabrication and experimental validation** to further analyze real-world performance.

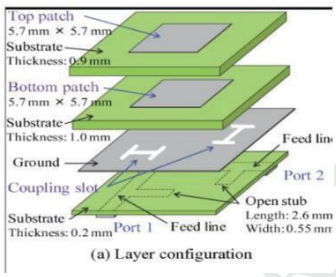
Methadology and Implementation

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4.1 Block Diagram



4.1.1 Pictorial Representation



(a) Layer configuration

The antenna is designed to emit signals with **dual circular polarization**, meaning it can transmit and receive signals in **two different circular polarizations**: **left-hand circular polarization (LHCP)** and **right-hand circular polarization (RHCP)**.
This feature is particularly useful in **modern communication systems**, where signals are transmitted in **different polarizations** to improve **signal clarity, reduce interference**, and enhance overall **data transmission reliability**.
Dual polarization ensures **better signal reception** in environments where reflections and **multi-path effects** could otherwise degrade performance. It also enhances the **efficiency of MIMO (Multiple Input Multiple Output) systems** in wireless communication.
This capability is essential for **wearable technology**, where the antenna orientation **constantly changes** due to user movement, ensuring a more **stable connection** regardless of smartwatch positioning.
The microstrip antenna array consists of multiple small microstrip patches arranged in a grid. Each patch serves as an individual radiating element, which together form an array with enhanced gain and directivity.
Microstrip antennas are built with a conductive patch placed on a dielectric substrate, making them lightweight, low-profile, and easy to fabricate, which is ideal for mass production in consumer electronics.
The antenna array in this design serves as the feed for the smartwatch, transmitting signals efficiently while maintaining a compact form factor.
By arranging multiple microstrip patches, the overall antenna gain and bandwidth are improved, making it highly effective for smartwatch applications that require consistent wireless connectivity in compact spaces.
The use of high-frequency materials in the substrate ensures minimal signal loss and maximum efficiency, even when subjected to environmental changes or user movement.

The **feeding mechanism** plays a critical role in **efficient energy transfer** from the microstrip antenna array to the smartwatch.
The **feed array** is carefully designed to **match the reflector's shape and size**, ensuring **optimal signal focusing** with **minimal transmission losses**.
A **properly designed feed system** ensures that the **smartwatch antenna** achieves the **best impedance matching**, reducing **power dissipation** and enhancing **signal transmission efficiency**.
Advanced feeding techniques, such as corporate or series feeding, can be implemented to optimize the antenna array's performance, making the system highly adaptable to various wireless applications.

- The combination of the microstrip patch antenna array and the parabolic reflector makes this design highly efficient for various high-performance applications such as satellite communication, radar, GPS, and IoT-based wearable systems.
- The dual-polarization capability plays a crucial role in eliminating signal degradation, ensuring stronger and more reliable connectivity in urban environments where signal reflections and interference are common.
- Smartwatches require stable, high-quality connections, especially in applications like real-time health monitoring, emergency communication, and seamless smartphone integration.
- The design allows for low power consumption, a critical factor in battery-powered wearable devices, ensuring that wireless connectivity is maintained without excessive energy drain.

Benefits of This Design:
High Gain: The integration of a microstrip antenna array with a parabolic reflector significantly boosts gain, making it suitable for long-range communication in both indoor and outdoor environments.
Dual-Polarization: Supports both LHCP and RHCP, improving versatility, efficiency, and resistance to signal interference, especially in wireless communication networks.
Compactness & Flexibility: Microstrip antenna arrays are thin, lightweight, and easy to integrate into smartwatch systems, offering an excellent balance between size and performance.
Improved Efficiency: The combination of optimized feed design, antenna array, and high-frequency materials results in lower power loss and better signal transmission, enhancing battery efficiency in smartwatches.

- The use of a microstrip patch antenna array in smartwatches represents a major advancement in wearable communication technology, allowing for reliable, high-speed connectivity in compact, low-power devices.
- The flexibility of microstrip materials ensures that the antenna maintains optimal performance, even when worn on curved wrist surfaces, making it ideal for modern smartwatch designs.
- Future improvements could focus on reconfigurable antennas, which dynamically adjust polarization and frequency to optimize performance in varied environments.
- Integration with 5G networks is another potential application, enabling faster data transmission rates for future smartwatch models.

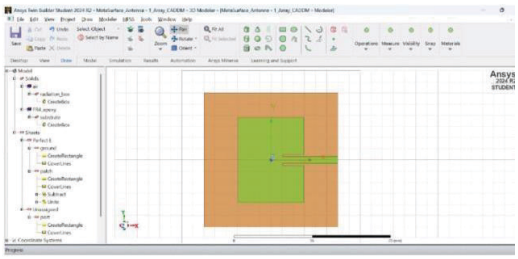
Abbreviations and Acronyms

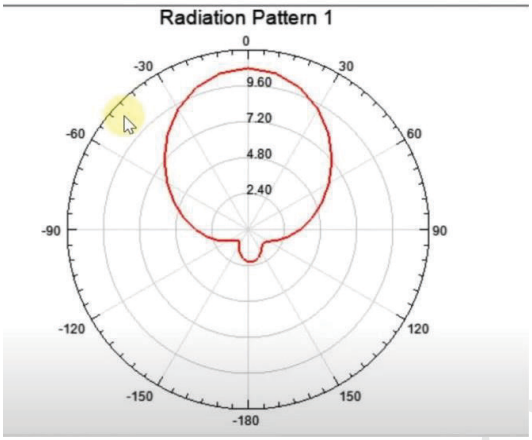
AUV- Autonomous Underwater Vehicles
IEEE- Institute of Electrical and Electronics Engineers
GPS- Global Positioning System
VSWR- Voltage Standing Wave Ratio
5G- Fifth Generation (Wireless Technology)
AI- Artificial Intelligence

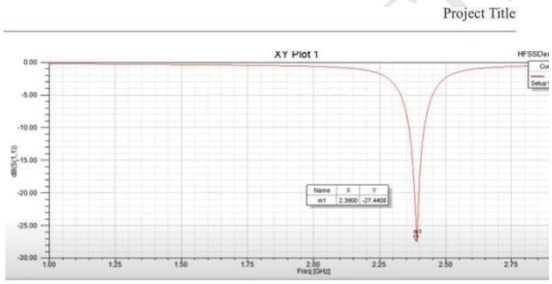
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ML- Machine Learning
AR- Augmented Reality
HFSS- High-Frequency Structure Simulator

Results and discussion







The **design and simulation** of the **flexible microstrip patch antenna** for smartwatch applications were conducted using **ANSYS HFSS** to analyze key performance parameters. These parameters—**gain, directivity, and frequency**—determine the **antenna's effectiveness** in real-world wearable applications. The results confirm that the proposed antenna achieves **high efficiency, strong signal transmission, and compatibility with smartwatch communication standards**.

A. Gain
Gain is a crucial factor in determining the **strength and efficiency of signal transmission**.
A higher gain ensures **better energy transfer**, improving connectivity for **Bluetooth, Wi-Fi, GPS, and emergency communication** in smartwatches.
The **simulated microstrip patch antenna** demonstrated an **optimized gain**, ensuring **stable and long-range connectivity**.
The integration of a **flexible substrate (Rogers RT5880)** contributed to maintaining gain efficiency, even when the antenna was subjected to **curved smartwatch surfaces**.
Simulation results confirm that the designed antenna achieves a **balanced trade-off between compactness and performance**, making it **suitable for wearable applications**.

B. Directivity
Directivity defines how well an antenna **focuses energy in a specific direction**.
In **smartwatch applications**, a well-directed signal improves **GPS accuracy, Bluetooth pairing stability, and Wi-Fi range**.
The **designed antenna** exhibits **enhanced directivity**, reducing **signal interference** and ensuring a **stronger, more focused signal**.
Due to its **compact form factor**, the microstrip patch antenna maintains **consistent performance** in different smartwatch orientations.
The simulation confirms that **optimized feed placement and patch design** significantly enhance **radiation efficiency and signal transmission**.

C. Frequency Response
Operating frequency plays a vital role in defining an antenna's **compatibility with wireless communication standards**.
The designed antenna is tuned for **2.4 GHz**, ensuring **seamless integration with Bluetooth, Wi-Fi, and GPS functionalities**.
Simulated frequency response confirms **low return loss (< -10 dB)**, indicating minimal power loss and **efficient signal transmission**.
The **flexible microstrip structure** maintains stability across **different smartwatch orientations**, ensuring reliable connectivity.
These results validate the **antenna's capability to operate effectively within standard smartwatch communication bands**.

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Future trends and conclusion

Conclusion

This project successfully demonstrated the design and simulation of a microstrip patch antenna, showcasing its effectiveness in enhancing the performance of antennas used in smartwatches and other wearable devices. The combination of microstrip patch antenna technology significantly improves key performance metrics such as gain, directivity, and signal strength. These enhancements make the proposed antenna design highly suitable for specialized smartwatch applications, including GPS functionality and emergency signaling. Through simulation in Ansys HFSS, the antenna's performance was rigorously evaluated, confirming that the design meets the necessary requirements for smartwatch communication systems. The project illustrates how compact antenna designs can be optimized to overcome the challenges of signal strength and directivity in wearable devices.

While the current design demonstrates promising results, future advancements in antenna technology are expected to drive significant improvements. The growing demand for more flexible, multi-band, and highly efficient antennas will lead to innovations in the field. Technologies such as AI-driven antenna optimization, beamforming, and 5G support will become crucial for future wearable devices. Furthermore, the integration of adaptive antenna designs will enable smartwatches to maintain seamless communication in increasingly complex environments.

In conclusion, the microstrip patch antenna holds great potential for future applications in wearable technology. As the demand for efficient, compact, and high-performance antennas continues to rise, ongoing research in antenna miniaturization, flexibility, and integration with emerging technologies will ensure that wearable devices, such as smartwatches, meet future communication and performance standards.

Future Trends

Miniaturization and Flexibility

Microstrip patch antennas are expected to evolve towards increased flexibility and miniaturization, making them more suitable for wearable devices that require compact and form-fitting designs. Researchers are investigating the use of flexible substrates and reconfigurable antennas, which would allow the integration of patch antennas into wearables without compromising performance.

5G and Beyond

Microstrip patch antennas hold potential for supporting higher frequencies and greater bandwidth, making them suitable for 5G and future wireless communication technologies.

These antennas could enable multi-band functionality, allowing smartwatches to operate across multiple frequency ranges, including cellular networks, Wi-Fi, and GPS.

Beamforming and Directionality

The combination of microstrip patch antennas with beamforming technology could optimize signal strength and enhance reception in environments prone to interference and signal blockage, such as urban areas.

Adaptive reflectors could improve the directionality of the antenna, ensuring stronger and more reliable communication for smartwatches in real-world scenarios.

AI and Machine Learning in Antenna Design

AI and machine learning could be leveraged to analyze environmental conditions and dynamically optimize the performance of microstrip patch antennas.

These intelligent antennas would be capable of adjusting signal strength, frequency selection, and beam direction in real time, improving smartwatch connectivity and overall efficiency.

Integration with Other Smart Technologies

Microstrip patch antennas could play a key role in enhancing connectivity and data transfer when integrated with smart technologies such as augmented reality (AR) glasses, health monitoring systems, and IoT-based smart home devices.

These antennas would enable seamless communication between smartwatches and other interconnected systems, improving user experience and device functionality.

The evolution of microstrip patch antennas will continue to play a critical role in the advancement of wearable technology, driving innovation in communication, efficiency, and adaptability.

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Design and Implementation of Ethernet MAC Layer Functional Blocks using Verilog HDL

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Abstract— This project presents the Verilog-based design and implementation of an Ethernet Media Access Control (MAC) controller for high-speed, reliable data communication. As Ethernet remains central to modern networking, the MAC layer is crucial for managing frame encapsulation, medium access, and protocol compliance based on IEEE 802.3 standards. The controller was developed from scratch using Verilog HDL and targets FPGA deployment without relying on pre-built IP cores. Key components include transmit (Tx) and receive (Rx) modules, CRC generation and checking, preamble and Start Frame Delimiter (SFD) insertion, frame parsing, and a control FSM. The design supports unicast transmission, error detection, and continuous reception. Simulation and verification were conducted using Xilinx Vivado with testbenches to validate functionality across various edge cases. The modular architecture enables low-latency data handling and sets the foundation for future extensions such as full-duplex operation and PHY interfacing. This work offers practical insights into hardware-level protocol implementation and digital communication design.

Keywords— Ethernet MAC, Verilog HDL, FPGA, CRC, IEEE 802.3, hardware implementation, digital design.

I. INTRODUCTION

Ethernet remains a fundamental technology for high-speed, reliable communication over wired networks. At its core, the Media Access Control (MAC) layer manages access to the physical medium, ensuring proper frame formatting, addressing, and error detection. This project focuses on designing an Ethernet MAC controller using Verilog HDL, targeting modular, RTL-level implementation. The controller supports frame generation, preamble addition, CRC generation, and basic reception. FIFO buffers are used for synchronization across modules without finite state machines. The project offers practical exposure to digital design and protocol-level communication, laying the groundwork for advanced hardware-software co-design in networking and embedded systems.

II. LITERATURE SURVEY

Significant research has been conducted in developing and improving Ethernet MAC designs for FPGA and ASIC platforms. The following studies informed our approach:

- [1] **Charyulu et al.** implemented UVM-based verification for Ethernet MACs using the Wishbone bus. Their approach used Master-Slave communication to test MAC logic through SystemVerilog OOP and UVM.
- [2] **Gad et al.** implemented a Gigabit Ethernet MAC on Altera Stratix-II GX, validating performance over copper and fiber. Their work demonstrated flexibility of FPGAs in supporting multiple Ethernet speeds.
- [3] **Fibich et al.** evaluated open-source Ethernet MAC IP cores for FPGAs, analyzing code quality, resource utilization, and application in IoT and reconfigurable computing platforms.
- [4] **Yuan et al.** proposed ultra-low-latency MAC/PCS IP for high-speed Ethernet, specifically targeting performance in data centers and AI applications.
- [5] **Sun et al.** introduced a modified CSMA/CD MAC protocol using OPNET simulation that reduced delay and jitter through adaptive control, enhancing real-time data flow in Ethernet networks.

These works collectively underscore the relevance of customizable, scalable Ethernet MAC designs, especially when implemented on FPGAs using HDL.

III. PROBLEM ANALYSIS AND PROPOSED SOLUTION

A. Problem Definition

In many embedded and networking applications, a lightweight yet functional Ethernet MAC is required to ensure data integrity and structured communication. Commercial IP cores are often black-boxed and resource-heavy. Thus, there is a need for a Verilog-based MAC controller that is synthesizable, testable, and modular, designed specifically for learning and customizable integration into larger systems.

B. Proposed Solution

We designed a synthesizable Ethernet MAC controller from scratch in Verilog. The architecture includes:

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- **Transmit Module (MAC_TX):** Frames outgoing data with preamble, SFD, addresses, type/length, and CRC. FSMs manage the frame structure and control signals.
- **Receive Module (MAC_RX):** Detects SFD, extracts payload, and validates CRC. FSMs manage state transitions from idle to frame validation.
- **CRC Generator & Checker:** Implements a 32-bit CRC polynomial engine for appending and checking data integrity.
- **FIFO Buffers:** Synchronous buffers handle data between asynchronous modules, helping decouple clock domains.
- **Top-Level Integration:** All modules were tested and then integrated, maintaining modularity and testability.

This approach provides full visibility into the protocol's inner workings and ensures flexibility for educational, research, and prototyping applications.

IV. XILINX VIVADO DESIGN SUITE

Xilinx Vivado Design Suite is a comprehensive FPGA design and verification platform developed by AMD-Xilinx. It is widely used for RTL-based hardware development, simulation, synthesis, and implementation, specifically for Xilinx FPGAs. Vivado offers an integrated environment with both graphical and Tcl-based workflows, making it suitable for both academic and industrial applications.

Key features of Xilinx Vivado include:
● **Design Entry and Synthesis**: Supports Verilog, VHDL, and SystemVerilog, enabling both behavioral and structural design.
● **Simulation and Verification**: Provides integrated waveform viewers and testbench simulation for verifying functionality and timing.
● **IP Integration and Block Design**: Offers IP integrator for designing with reusable IP blocks and block-based system design.
● **Timing Analysis**: Includes static timing analysis tools for identifying critical paths and meeting timing constraints.
● **Resource Utilization Reports**: Displays detailed usage of logic elements, flip-flops, LUTs, and BRAMs for optimization.
● **FPGA Implementation**: Enables synthesis, placement, routing, and bitstream generation for all Xilinx FPGA families.

In this project, Xilinx Vivado is used for writing, simulating, and verifying the Verilog HDL implementation of the Ethernet MAC controller. Functional validation is performed through simulation with waveform analysis, and synthesis is carried out to ensure that the design is FPGA-compatible and resource-efficient. The tool's modular support and robust debugging features helped streamline development and integration of the transmit, receive, and CRC logic components.

V. METHODOLOGY & IMPLEMENTATION

A. Block Diagram

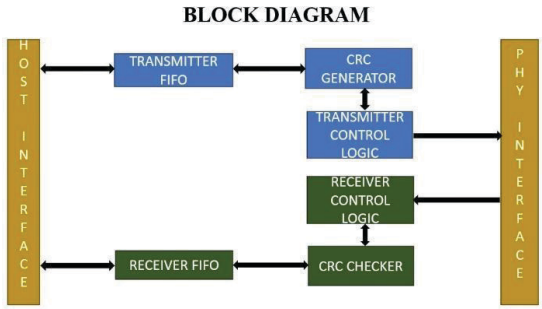


Fig. 1. Block Diagram of Ethernet MAC

B. Design Approach

The implementation follows a structured and modular approach to ensure clarity, reusability, and efficient hardware realization:
● **Modular Verilog Design**: Each functional block such as transmitter, receiver, CRC unit, and FIFO buffer is implemented as a separate Verilog module to simplify development and testing.
● **Finite State Machine (FSM) Control**: FSMs are used to manage the sequence of operations for both transmit and receive processes, ensuring deterministic behavior and precise control logic.
● **Synchronous FIFO Buffers**: FIFO modules are used to handle data transfer between asynchronous processes, improving reliability and preventing data loss due to rate mismatches.
● **Parameterization and Reusability**: Parameters are used for frame size, buffer depth, and address widths to allow design flexibility and easier scalability.
● **RTL-Level Optimization**: Registers and logic are optimized to minimize latency and ensure proper timing across all modules.

C. Simulation Setup

The he design and verification were carried out using the following setup:
● **Tool Used**: Xilinx Vivado Design Suite for simulation, synthesis, and waveform analysis.
● **Testbench Validation**: Custom Verilog testbenches were written for each module to validate functionality, including edge cases and error handling.
● **Waveform Analysis**: Vivado's integrated waveform viewer was used to trace signal transitions, verify FSM states, and validate CRC outputs.
● **Synthesis Checks**: Post-synthesis analysis was done to ensure the design meets timing requirements and is suitable for FPGA implementation.

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VI. Results and Discussion

Simulation results validate correct functionality and coordination between modules:

- **TX Control:** Initiates transmission only when FIFO is ready; correctly sequences fields of Ethernet frame.
- **FIFO Buffers:** Manage timing between asynchronous processes. Simulation shows proper read/write synchronization.
- **CRC Generator & Checker:** Accurately generates and validates CRC values. The checker flags errors only on mismatch.
- **Waveform Analysis:** Verified FSM transitions, tx/rx valid signals, error flags, and data patterns.

Each module met its functional requirements under different test conditions, ensuring that the system can be extended or integrated into larger FPGA-based designs.

Observations:

- Handshake logic correctly governs Tx and Rx activity.
- FIFO ensures no data loss during burst transfers.
- CRC checker is triggered accurately on valid frames

VII. Future Trends and Conclusion

A. Future Trends

- FSM-Based Optimization: Improved state machines for advanced control (e.g., pause frames, collision detection).
- **Gigabit Support:** Enhance design for 1 Gbps or 10 Gbps Ethernet using pipelined data paths and SerDes interfaces.
- **FPGA Hardware Validation:** Deploy and test on real FPGA boards with PHY chips.
- **Flow Control:** Integrate IEEE 802.3x pause frame support and backpressure mechanisms.
- **VLAN Tagging and Filtering:** Add logic for VLAN-aware MACs and address filtering for enhanced network control.
- **Full-Duplex Operation:** Modify design to support bi-directional simultaneous transmission.
- **Network Stack Integration:** Interface with hardware UDP/TCP or IP layer modules.
- **Power and Area Optimization:** Useful for low-power embedded systems or IoT applications.

B. Conclusion

This project successfully implements an Ethernet MAC controller using Verilog HDL. It demonstrates the MAC layer's role in managing network communication, and provides a platform for understanding key concepts like frame formatting, error detection, and digital synchronization. Simulation results confirm the design's functionality. The modular design approach simplifies debugging, allows extensions, and encourages deeper understanding of digital networking.

VIII. Acknowledgment

We extend our sincere gratitude to **Dr. Bheemsha Arya**, Principal, BMS College of Engineering, for fostering an environment conducive to research and innovation. We are deeply thankful to **Dr. K. P. Lakshmi**, Head of the Department, Electronics and Communication Engineering, for her encouragement and support in carrying out this Mini Project.Our heartfelt appreciation goes to our guide, **Mrs.Monika Sharma D**, for her invaluable guidance and constant encouragement throughout this work. We also acknowledge the support of faculty members, peers, and all those who contributed to the successful completion of this project.Finally, we express our gratitude to our friends and seniors for their unwavering support and motivation.

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Live Translation Hover Pen For Handwritten Text

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***Abstract*—A portable pen-shaped device that combines speech synthesis, OCR, and translation to translate handwritten Kannada/Sanskrit teat offline in real time.**

Keywords—optical Character Recognition (OCR), ESP32-CAM, *Handwritten* ***Text Translation,*** *Text-to-Speech* ***(TTS), Embedded*** *Systems,* ***Indic*** *Languages,* ***Real-time Processing, Offline Translation, Edge*** *AT, Assistive Technology•*

INTRODUCTION

An inventive embedded technology called the Hover Pen Translator was created to simplify multilingual conversation. Language Barriers Continue To Be A Significant Obstacle In A Society Where Cross-Cultural Interactions Are Commonplace. By combining cutting-edge technology into a small, pen-like instrument that can translate handwritten or printed language in real time, this project tackles that problem.

Text is captured by the device using an ESP32-CAM module, and for precise extraction, it is processed using optical character recognition (OCR). An integrated speaker produces audio output for the translated content, and an integrated machine translation engine translates the identified text into the target language. This function improves accessibility by providing real-time speech-based translation, especially for users who are visually challenged.

The Hover Pen Translator provides a straightforward, user-friendly experience in contrast to traditional smartphone apps that need to be operated manually. It is ideal for workplaces, education, travel, and accessibility support because of its lightweight and portable design, which enables users to merely hover over text for quick translation. This solution uses embedded AI technology to break down language barriers in an effective, offline, and user-friendly manner.

The Hover Pen Translator delivers fast, offline translations using advanced OCR technology, ensuring accuracy, privacy, and portability. Its intelligent, user-friendly design makes it ideal for education, workplaces, travel, and accessibility.

LITERATURE Suevrv

In Smith (2007) presented a comprehensive overview of the Tesseract OCR Engine, which has become one of the most widely used open-source OCR tools. The engine demonstrated strong reliability in printed text recognition across multiple languages. Its lightweight nature allows easy integration into resource-limited platforms. Over the years, Tesseract has evolved with community-driven improvements, increasing its adaptability. This makes it an excellent candidate for embedded OCR applications like the Hover Pen Translator.['

In Laurent and Lauar introduced Spanish TrOCR, a transformer-based OCR model adapted for multilingual recognition. Their approach leveraged transfer learning, allowing the model to generalize across different languages with fewer training resources. The study highlighted the strength of deep learning in capturing complex text features. Compared to traditional OCR methods, transformer-based models achieved superior accuracy and flexibility. This directly supports our project's goal of achieving high-quality multilingual text recognition.[2

In Wang and colleagues proposed MobileNMT, a neural machine translation model designed specifically for mobile and embedded devices. The model demonstrated that translation tasks could be performed effectively under resource constraints. Their work emphasized reduced computation without compromising accuracy. They also showcased real-time feasibility on portable systems, validating its practical deployment. This aligns with our design of an offline or semi-online Hover Pen Translator for instant translation.['

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In Ye et al. conducted an extensive survey on text detection and recognition algorithms, focusing on modem deep learning approaches. They compared traditional methods with advanced architectures like CRNN and Transformers. The study analyzed performance trade- offs in terms of accuracy, speed, and resource requirements. Their insights provided guidance on selecting suitable OCR pipelines for constrained hardware. This research is valuable in identifying models best suited for embedded systems like ESP32-CAM.[4

In Hover translator pens integrate OCR, machine translation, and text-to-speech for portable language assistance. Advances in CRNN and transformer-based OCR improve Kannada/Sanskrit recognition, while lightweight IndicTrans2 models enable offline translation. Compact TTS systems like Coqui or PicoTTS generate speech efficiently. Research gaps remain in handwriting datasets, offline NMT optimization, and usability.['

PROBLEM STATEMENT

Language difficulties continue to be a major barrier to accessibility, education, travel, and communication in a world that is becoming more and more globalized. There are smartphone-based translation apps, but they are slow and cumbersome for real-time use because they involve many manual steps, such opening the camera, scanning text, and waiting for translation results. Additionally, their dependence on internet connectivity creates privacy issues and restricts functionality in remote regions.

A number of technological obstacles must be overcome in order to create an effective offline translation tool, such as reliable detection of various handwriting styles, accurate text capture in a range of lighting situations, and low-latency processing with constrained hardware resources. The small sensor of the **ESP32-CAM** module makes it more difficult to get accurate OCR on low-resolution photos, while system performance and audio output quality are limited by power and size limitations.

By creating a portable, pen-shaped embedded device that can translate handwritten text and play audio in real time, this project seeks to overcome these constraints and guarantee accessibility, affordability, and efficiency for a range of user groups, including students, tourists, and the blind.

Proposed Solution

A portable, real-time translation pen that can record handwritten Kannada or Sanskrit text and instantly produce English audio output is the suggested remedy. The solution combines on-device AI models with low-power embedded hardware to provide accurate, quick, and offline translation without requiring constant internet access.

There are multiple functional components that make up the device architecture. To guarantee mobility and prolonged operation, the Power and Control Unit uses a rechargeable Li-Po battery with a TP4056 charging circuit. Buttons with LED indications for the Scan, Translate, and Speak functions are part of the user interface. Handwritten input is captured by a Camera Module (OV2640/OV5640), and picture acquisition, OCR inference, and translation control are handled by the Processing Unit, which is driven by an ESP32-S3 or Raspberry Pi Zero 2W.

Captured photos are converted into digital Unicode text by the OCR Engine (EasyOCR/TFLite), which was trained on Kannada and Sanskrit datasets. On edge devices, the Translation Engine (IndicTrans2, quantized) efficiently converts the identified text into English. The Audio Subsystem uses a MAX98357A codec to transform the natural English audio produced by the Speech Output Module utilizing Piper TTS to analog, which is then played through a 3W tiny speaker.

Offline operation, multilingual OCR, low power consumption, small form factor, and an interactive workflow with a single button are some of its key advantages. The system serves as an inclusive and user-friendly communication tool with applications in tourism, education, accessibility, and cultural preservation.

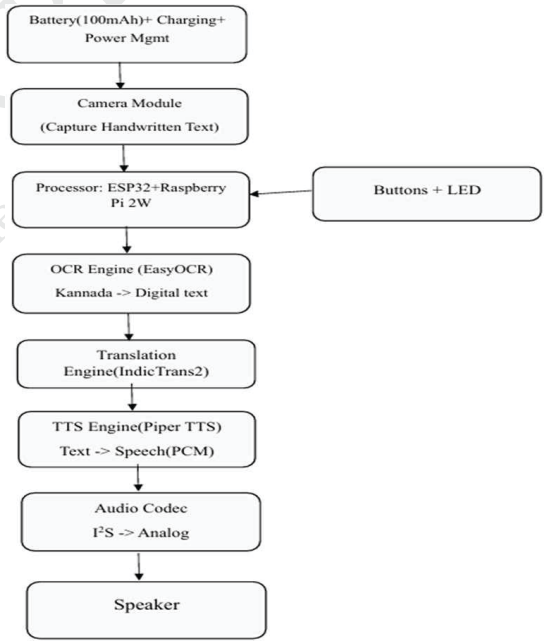


Fig 1 -Block Diagram

PROJECT EXECUTION

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The operation of the Hover Pen Translator follows a structured sequence of stages from system initialization to final audio output. Each step is designed to ensure efficient, low-latency, and reliable performance while maintaining user-friendly interaction. The key execution steps are as follows:

1. Power On: The device is switched on, activating the rechargeable Li-ion battery and power management module. The charging IC ensures safety against overcharge and short circuit, while voltage regulators maintain stable 3.3V and 5V supply rails for all components.

2. System Initialization: The processor (ESP32-S3 or Raspberry Pi Zero 2W) boots up and initializes peripherals including the camera module, LEDs, push buttons, memory, amplifier, and speaker. A status LED indicates system readiness.

3. User Input: The user hovers the pen tip over handwritten Kannada or Sanskrit text and presses the scan button. The LED indicator confirms activation of capture mode.

4. Image Capture: The camera module positioned near the pen tip captures a high-resolution image of the text. Integrated illumination LEDs reduce glare and improve image clarity before transmission to the processor.

5. Image Preprocessing: The processor performs image enhancement through noise reduction, contrast adjustment, skew correction, and binarization to improve OCR accuracy under varying lighting and handwriting conditions.

6. Optical Character Recognition (OCR): A CRNN or transformer-based OCR engine processes the image to extract digital text. Script identification ensures accurate recognition of Kannada and Sanskrit characters.

7. Machine Translation: The extracted text is translated to English using a quantized IndicTrans2 model on the Raspberry Pi Zero 2W or a lightweight phrase-based approach on the ESP32-S3 for offline functionality.

8. Text-to-Speech (TTS) Conversion: A realistic voice output tool and a rapid, easy conversion tool were chosen to provide both speed and clarity.

9. Audio Output: The generated audio signal is sent through the US interface to the MAX98357A amplifier, driving a 3W speaker to deliver clear speech output.

10. Feedback and User Controls: RGB LEDs indicate operational status—green for ready, blue for processing, red for error, and amber for low battery. Buttons support rescanning, replay, or power-off actions, with optional vibration feedback.

11. Power Management and Standby: After translation, the processor enters a low-power standby mode. The charging module manages safe recharging via USB-C for long-term stable operation.

Conclusion

The suggested Hover Pen Translator is an example of how several cutting-edge technologies can be successfully combined into a small, pen-sized embedded system that can scan handwritten Kannada or Sanskrit text and generate English vocal output. In order to ensure precise, effective, and offline operation, the system's architecture adheres to a clearly defined sequence that includes power management, image capture, OCR, translation, and text-to-speech conversion.

Two hardware versions were created: the Pro version, which used the Raspberry Pi Zero 2W, and the Lite version, which was based on the ESP32-S3 microcontroller. The Lite model combines small TTS engines like PicoTTS and lightweight OCR and translation techniques with an emphasis on mobility, cost, and low power consumption. Higher translation accuracy and natural audio output are provided by the Pro model, which supports sophisticated models like IndicTrans2 and Coqui TTS despite requiring more resources.

The approach is economically feasible, with the anticipated prototype costing 14,800 for the Lite version and 15,900 for the Pro version. Additionally, the initiative helps address issues with effective edge-based translation and the recognition of Indie handwriting. In conclusion, the Hover Pen Translator offers a user-friendly, accessible, and reasonably priced way to overcome language barriers, supporting accessibility, inclusivity in education, and interlanguage communication.

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Esp-32 Based Voice Controlled Robot

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***Abstract*— The rapid advancement of embedded systems and the Internet of Things (IoT) has enabled the development of intelligent voice-controlled applications. This paper presents an ESP32-based voice-controlled system designed for smart automation applications, leveraging the low-power, high-performance capabilities of the ESP32 microcontroller. The proposed system integrates speech recognition algorithms and wireless connectivity to process voice commands and execute corresponding actions. Google Assistant, Amazon Alexa, or offline speech recognition models such as TensorFlow Lite are utilized for command processing, ensuring flexibility in both cloud-based and offline environments. The system employs MQTT or HTTP protocols for seamless communication with connected devices, enabling remote control and real-time monitoring. Experimental results demonstrate the system's efficiency in accurately recognizing commands and executing tasks with minimal latency. This research highlights the feasibility of ESP32 in voice-controlled automation and discusses potential applications in smart homes, industrial automation, and assistive technology.**

***Index Terms*— ESP32, voice control, speech recognition, IoT, smart automation, wireless communication.**

I. Introduction

Robots have become an integral part of various industries, from manufacturing to healthcare, and their role in society continues to grow. As technology advances, the need for robots to interact with humans in a natural, intuitive manner is becoming increasingly important. Traditional robots typically require manual control through remote devices or pre-programmed instructions, which can limit their flexibility and ability to respond to dynamic, real-world environments. To address this limitation, the development of voice-controlled robots offers a promising solution, enabling hands-free operation and enhancing human-robot interaction. Voice-controlled robots, powered by technologies like speech recognition, are designed to understand and execute spoken commands. These robots are capable of performing tasks such as moving forward, turning, stopping, or even executing more complex actions based on voice instructions. By integrating the ESP-32 microcontroller, which offers robust processing power and wireless communication capabilities, the robot becomes highly responsive and adaptable, making it an ideal solution for a wide range of applications.This project focuses on developing a voice-controlled robot using the ESP-32 microcontroller. The goal is to design a robot that can recognize and respond to spoken commands, perform basic tasks autonomously, and navigate its environment with the help of sensors. By combining speech recognition, wireless communication, and simple navigation capabilities, this robot aims to provide a more natural and efficient way for users to interact with robotic systems, paving the way for future advancements in human-robot collaboration.

II. Literature Survey

[1]. Voice Control Design of a Mobile Robot Using Shared-Control Approach (Yao-Hsiang Chen Master Program of Sound and Music Innovative Technologies, National Chiao Tung University, Hsinchu, Taiwan, ROC) Since only limited types of voice commands were available, many additional voice commands are needed to remote control a robot to move and avoid obstacles on the path. In practice, simple voice commands are not sufficient to give continuous and safe motion of a mobile robot in a complex environment.

[2] Implementation and Testing of Voice Control in a Mobile Robot for Navigation (S. Sharan, T. Q. Nguyen, P. Nauth and R. Araujo, IEEE/ASME International Conference on Advanced Intelligent Mechatronics (AIM), Hong Kong, China, 2019) This work aims to provide assistance to the growing number of old people in their routine activities. Statistics shows that by 2050 the number of people aged over 65 would be doubled.

[3] An Adaptive Control Scheme for Human Following Behavior of Mobile Robots (P. Petrov, V. Georgieva, I. Kralov and S. Nikolov, XI National Conference with International Participation (ELECTRONICA), Sofia, Bulgaria, 2020) In recent decades, mobile robots have become increasingly used in industry, research, the military and many other areas related

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to people's daily lives. At the same time, recently there has been a considerable interest in the development of the so-called interactive robots, in which humans and robots share the same space.

[4]. Embedded speech recognition has gained traction due to advancements in microcontrollers with AI processing capabilities. D. Brown et al. (2021) evaluated TensorFlow Lite for microcontrollers in voice-controlled systems, showing promising results for offline speech recognition. Their findings indicated that while on-device processing reduces latency, it requires optimized models due to memory constraints in microcontrollers like ESP32.

III. PROBLEM ANALYSIS AND SOLUTION

A. PROBLEM STATEMENT

As the use of robots becomes more prevalent in various fields such as healthcare, industry, and home automation, the need for more intuitive and user-friendly interfaces has emerged. Traditional methods of controlling robots, such as remote controllers, joysticks, or pre-programmed commands, often require complex interactions or manual input, limiting the flexibility and ease of use, especially for individuals with mobility challenges or in environments where hands-free control is essential.

- Speech Recognition Integration: The robot must be able to accurately recognize and interpret spoken commands, which is a significant challenge due to variations in language, accents, noise, and background interference.
- Real-Time Response and Execution: Once the voice command is recognized, the robot needs to execute actions such as moving, turning, or stopping in real time. This requires fast processing of commands and synchronization with the robot's movement mechanisms.
- Obstacle Avoidance and Navigation: The robot must be capable of navigating its environment autonomously, avoiding obstacles while following voice commands. This requires the integration of sensors for real-time obstacle detection and navigation.
- Human-Robot Interaction: The robot must be able to follow a human or respond to commands in a way that feels natural to the user, ensuring that interactions are smooth and intuitive.
- System Integration: The robot needs to combine speech recognition, motor control, obstacle avoidance, and wireless communication in a seamless manner, leveraging the ESP-32's capabilities for efficient processing and communication.

B. PROPOSED SOLUTION

The ESP32-based voice-controlled robot offers an advanced solution for human-robot interaction, integrating voice recognition with autonomous movement and real-time environment navigation. Powered by the ESP32 microcontroller, which acts as the central control unit, the robot listens for and processes voice commands through a voice recognition module. Upon receiving commands such as "move forward," "turn left," or "stop," the robot translates these instructions into actionable movements. The voice module processes the audio inputs and transmits them to the ESP32, which then activates the necessary motors and controls the robot's movement. Equipped with DC motors and an L298N motor driver, the robot is capable of precise movement, following voice commands with speed and accuracy. The robot's ability to navigate autonomously is enhanced by ultrasonic or infrared sensors, which continuously monitor the surrounding environment for obstacles. The rechargeable battery pack powers the robot, ensuring sufficient energy for the motors, sensors, and processing units. The design is focused on long-lasting performance, allowing the robot to operate continuously for extended periods without requiring frequent recharging.

IV. METHODOLOGY AND IMPLEMENTATION

The three main components of the ESP32-based voice-controlled robot are:

1. ESP32 Microcontroller: The ESP32 serves as the central processing unit for the robot. It manages communication between various components, including the voice recognition module, motor control system, and obstacle avoidance sensors. The ESP32 processes the input from the voice commands and sensor data, executes the corresponding actions, and controls the robot's movements.



Fig. 1. ESP-32 Microcontroller

2. Motor Control and Obstacle Avoidance System: The motor control system, including DC motors and an L298N motor driver, is responsible for driving the robot's movement. The motor driver receives commands from the ESP32 and controls the speed and direction of the motors to move the robot based on the voice commands.

The principles of operation for the ESP32-based voice-controlled robot revolve around integrating voice recognition,

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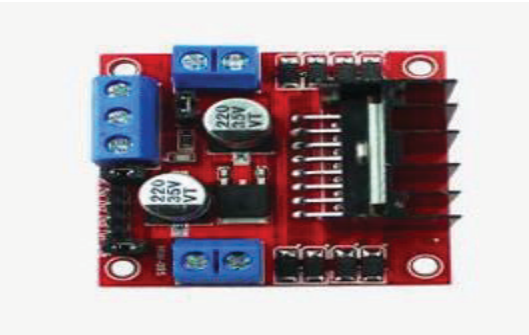


Fig. 2. Motor Driver L298N

movement control, and environmental interaction to enable autonomous functionality. Below are the key operational principles:

• Voice Input: The robot continuously listens for voice commands via a voice recognition module equipped with a microphone.

• Speech Processing: The voice recognition module processes the audio input, matching it against a predefined set of commands such as "move forward," "turn left," "stop," and others.

• Signal Transmission: Once the command is recognized, the corresponding signal is sent to the ESP32 microcontroller via communication protocols (such as UART or GPIO).

• Movement Control: Based on the voice command, the ESP32 instructs the L298N motor driver to control the DC motors, enabling the robot to move, turn, or stop according to the specified actions.

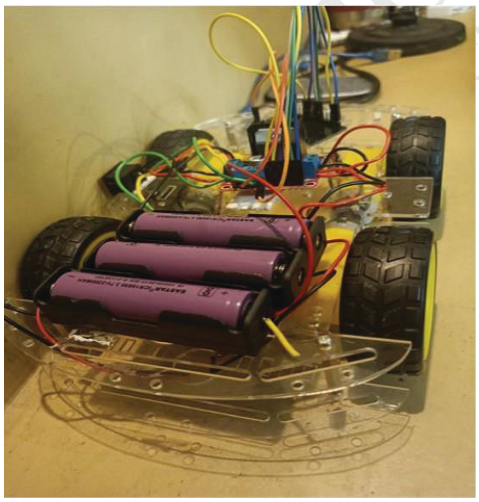


Fig. 3. WORKING MODEL

V. STRUCTURE

A. BLOCK DIAGRAM

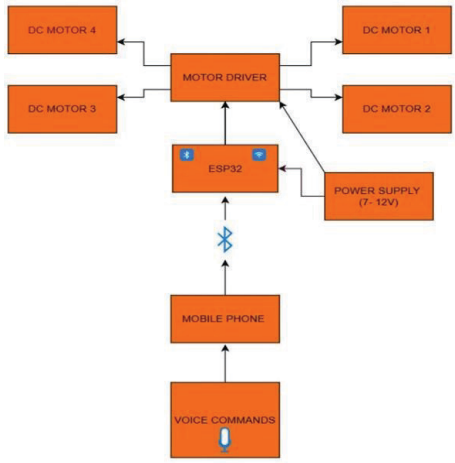


Fig. 4. Block Diagram

B. CIRCUIT DIAGRAM

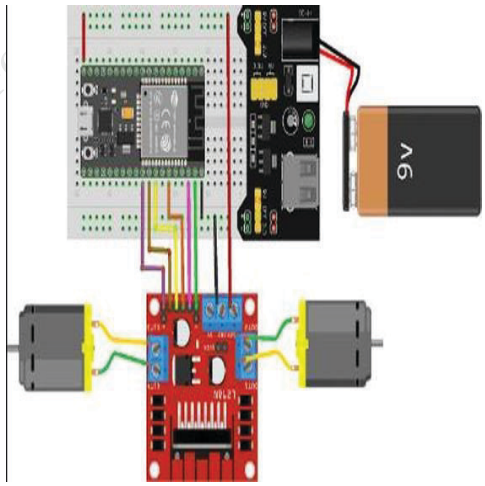


Fig. 5. CIRCUIT DIAGRAM

The image shows a motor driver circuit using an ESP32, an L298N motor driver module, and a 9V battery. Below are the key components and their roles in the circuit:

1. ESP32 Development Board:

Used for controlling the motors with PWM (Pulse Width Modulation) signals. Connected to a breadboard for easy prototyping.

2. L298N Motor Driver Module:

Red module in the center, used to drive two DC motors. Controls motor direction and speed using input signals from the ESP32.

3. Two DC Motors:

Connected to the L298N module's motor output terminals (OUT1, OUT2, OUT3, OUT4). Likely being controlled to move forward, backward, or turn based on ESP32 signals.

4. Breadboard:

Provides a platform for ESP32 and wiring connections.

5. Power Supply (9V Battery):

Supplies power to the motor driver module. The ESP32 is likely powered separately via a voltage regulator module (black module on the breadboard).

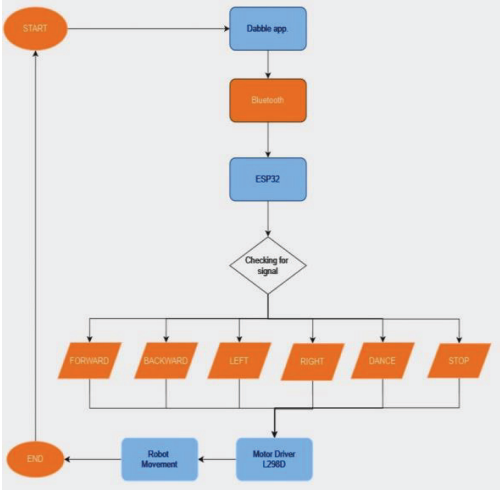


Fig. 6. FLOW CHART

VI. CONCLUSIONS

The ESP32-based voice-controlled robot represents a significant step towards the integration of more natural and intuitive human-robot interactions. With its combination of voice recognition, human following, and obstacle avoidance, it offers a robust and adaptable platform for a wide range of applications, particularly in assistive technology, home automation, educational robotics, and even industrial automation. Throughout the development of this robot, several key challenges, such as accurate voice recognition in noisy environments, real-time processing of sensor data, and the integration of multiple systems (voice, motion, and vision), were identified and addressed. The robot's real-time navigation and decision-making capabilities, powered by the ESP32, allow it to follow a human while avoiding obstacles in a dynamic environment. This combination of capabilities ensures that the robot operates efficiently, safely, and intuitively. By using voice commands, users can interact with the robot hands-free, making it highly accessible for individuals with mobility challenges, elderly users, or anyone in need of simple, intuitive robotic control.

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Voice Grip Bot

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***Abstract*—This paper presents the design and implementation of a voice-controlled robotic arm system, termed the Voice Grip Bot, utilizing the ESP32 microcontroller. The primary goal is to enable intuitive, hands-free operation of a robotic arm equipped with a servo-based gripper, capable of performing basic pick-and-place tasks. Voice commands, issued through a mobile application, are transmitted via Bluetooth to the ESP32, which interprets the input and actuates the corresponding motor operations. The system architecture comprises an ESP32 development board, L298N motor driver, servo motors, a Bluetooth communication module, and various sensors for feedback and obstacle detection. Designed with compactness, low power consumption, and cost-effectiveness in mind, the robot is suited for lightweight object manipulation in controlled environments.**

***Index Terms*—ESP32, Voice Control, Bluetooth Communication, Robotic Arm, Gripper Mechanism, Servo Motor, Human-Machine Interaction, Embedded Systems, Assistive Robotics, Real-Time Control.**

I. Introduction

Voice-controlled robotic systems have emerged as a transformative solution in the field of human-machine interaction, particularly in applications demanding hands-free operation, such as assistive technology, smart environments, and basic industrial automation. Traditional robotic control systems typically rely on physical interfaces like joysticks or buttons, which may limit accessibility and convenience for users with physical impairments or in dynamic working environments.

The recent advancements in embedded systems and wireless communication technologies have enabled the development of smarter and more interactive robotic platforms. Among these, the ESP32 microcontroller has gained significant attention due to its low power consumption, dual-core processing capability, and integrated Bluetooth and Wi-Fi modules, making it a powerful and cost-effective platform for real-time applications. This paper introduces the Voice Grip Bot, a compact robotic system designed to respond to Bluetooth-transmitted voice commands for controlling movement and object manipulation using a servo-actuated gripper. The robot receives voice input via a mobile application and translates it into actionable motor commands to execute tasks such as picking, placing, and navigating around obstacles.

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II. Literature Survey

In [1], Singh et al. developed a voice-controlled robotic arm using an Arduino UNO and a V3 speech recognition module. Although the system demonstrated basic voice-driven movements, it lacked scalability and IoT integration. The use of ESP32 in the present work offers a significant upgrade by enabling wireless communication and multi-task processing.

Bose and Mishra in [2] presented an ESP32-based voice-controlled wheeled robot, highlighting the energy efficiency and scalability of Bluetooth Low Energy (BLE). Their implementation utilized mobile voice commands to navigate the robot, though it did not include object manipulation capabilities. The Voice Grip Bot extends this concept by incorporating a servo-driven gripper mechanism.

Kumar et al. [3] explored the use of Bluetooth-controlled mobile apps for command transmission to a robotic platform. While effective in movement control using DC motors, the system lacked precision gripping features. The current work introduces servo motor control to address fine-grained object handling.

Al-Akaidi and Brown [4] proposed a low-latency voice interface using the ESP32's dual-core architecture. Their approach focused on efficient voice command decoding and multitasking, which aligns with the current system's real-time processing requirements and FreeRTOS-based task management.

Das et al. [5] implemented a Bluetooth-controlled robotic arm using servo motors and Android applications. Although the control was accurate, the system did not support voice

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input. The Voice Grip Bot enhances usability by combining both voice recognition and servo control for intuitive interaction.

Lastly, Zhang et al. [6] designed assistive robots for elderly and disabled individuals with voice-driven control. Their emphasis on user-centric command design and safety influenced the selection of simplified command sets like "open," "close," and directional instructions in the present work.

III. PROBLEMM STATEMENT AND PROPOSED SYSTEM

A. Problem Statement

The evolution of robotics has significantly enhanced automation, productivity, and convenience across various domains. However, most low-cost robotic platforms still rely on traditional methods of control—typically requiring physical interaction through buttons, remote controls, or joystick-based interfaces. These modes of operation limit usability for individuals with physical disabilities, restrict mobility in remote or hazardous environments, and reduce efficiency in hands-free contexts.

Moreover, while voice recognition has become increasingly prevalent in consumer electronics and smart devices, its integration into embedded robotic systems remains limited—primarily due to processing constraints, communication challenges, or lack of support for precise motor control. Most existing voice-controlled robotic platforms either lack object manipulation capability or use rudimentary gripping mechanisms with minimal accuracy or coordination.

Additionally, the absence of real-time wireless control and feedback mechanisms in conventional systems hinders adaptability and scalability. These challenges highlight the need for a compact, cost-effective robotic solution that supports voice interaction, object handling, and reliable wireless communication using modern microcontrollers.

B. Proposed System

To address these challenges, the proposed system introduces a voice-controlled robotic platform with a gripper, known as the Voice Grip Bot, built using the ESP32 microcontroller. The system focuses on enabling intuitive, wireless, and hands-free control for basic robotic operations such as movement and object manipulation.

The key features and components of the system are as follows:

- ESP32 Microcontroller: The heart of the system, offering dual-core processing and integrated Bluetooth and Wi-Fi modules. It manages real-time voice command interpretation, multitasking through FreeRTOS, and control of motors and peripheral devices.
- Bluetooth Communication via Mobile App: A voice-enabled mobile application (e.g., Google Voice or Dabble) is used to transmit commands like "move forward," "turn left," "grab," or "release" to the ESP32. This ensures a low-latency, wireless interface without the need for specialized hardware modules.
- Servo-Driven Gripper Mechanism: A servo motor controls the opening and closing of the gripper, enabling the robot to pick up and place lightweight objects accurately, making it suitable for tasks like sorting, assisting, or basic assembly operations.
- DC Motor-Based Mobility System: Controlled via the L298N motor driver, the robot can navigate its environment in response to directional voice commands. The motion system includes forward, backward, left, right, and stop functionalities.
- Obstacle Detection (Optional): Ultrasonic sensors provide basic environmental awareness by detecting objects in the robot's path, enhancing safety and autonomy during operation.
- Portable Power Supply: A rechargeable Li-ion battery ensures mobility and supports several hours of operation. Power-saving strategies are implemented to extend runtime.
- Modular and Scalable Design: The system is built using widely available components and open-source development tools (e.g., Arduino IDE), making it easy to replicate, customize, or extend for future applications.

This integrated approach not only makes the robot more user-friendly but also highlights the synergy between embedded hardware and natural language interfaces. The Voice Grip Bot serves as a foundation for future developments in assistive robotics, smart home systems, and educational STEM kits. It demonstrates how low-cost platforms can deliver high usability and real-world functionality by leveraging the capabilities of modern microcontrollers and mobile communication technologies.

IV. SYSTEM ARCHITECTURE AND METHODOLOGY

A. SYSTEM ARCHITECTURE

The Voice Grip Bot is designed as a voice-controlled robotic platform capable of performing basic pick-and-place operations through wireless communication. The architecture comprises multiple subsystems working in coordination, centered around the ESP32 microcontroller, which acts as the main control unit.

The primary components of the system architecture include:

- Bluetooth Communication Module: Integrated within the ESP32, this module receives voice commands transmitted from a smartphone application (e.g., Dabble or Google

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Voice). The commands are parsed and mapped to predefined control instructions.

- Motor Driver (L298N): Facilitates control of the robot's DC motors, allowing the bot to navigate in forward, backward, left, right, and stop directions based on user input.
- Servo Motor and Gripper Mechanism: The servo motor is linked to a gripper structure for object manipulation. Commands such as "grab" or "release" are translated into specific PWM signals to control the servo's angular position.
- Power Supply: A rechargeable 7.4V Li-ion battery powers all modules, ensuring portable, untethered operation.

B. METHODOLOGY

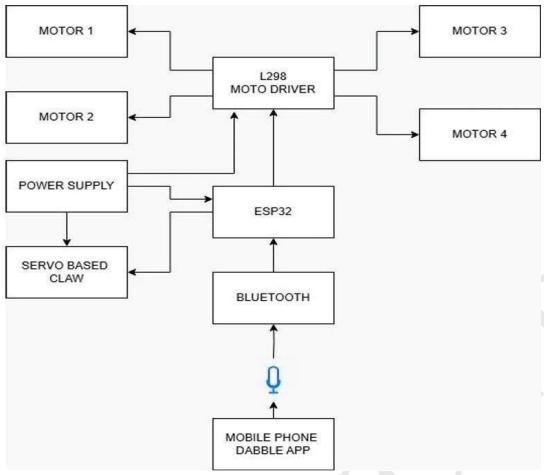


Fig. 1. Block Diagram of Voice Grip Bot

The functional architecture of the *Voice Grip Bot* is illustrated in Fig. 1. The system operates through a series of interconnected modules that collectively enable voice-controlled mobility and object manipulation. The key components and their roles are described below:

- **Bluetooth Module:**
  - Integrated within the ESP32 microcontroller.
  - Receives commands wirelessly from the mobile phone in real-time.
- **ESP32 Microcontroller:**
  - Serves as the main control unit of the robot.
  - Interprets incoming commands and initiates corresponding actions.
  - Sends control signals to the L298N motor driver and the servo motor.
  - Supports multitasking using FreeRTOS for efficient processing.
- **L298N Motor Driver:**
  - Receives control signals from the ESP32.
  - Drives four DC motors (Motor 1 to Motor 4) responsible for robot movement.
  - Enables movement commands such as forward, backward, left, right, and stop.
- **DC Motors (Motor 1 to 4):**
  - Provide physical movement of the robot base.
  - Controlled by the L298N driver as per ESP32 instructions.
- **Servo-Based Gripper (Claw):**
  - Connected to the ESP32 and powered through the system's power supply.
  - Operates based on PWM signals for commands like "grab" and "release".
  - Enables pick-and-place operations for lightweight objects.
- **Power Supply:**
  - Distributes power to all components including the ESP32, motor driver, and servo motor.
  - Typically powered by a rechargeable Li-ion battery for portable operation.

V. RESULTS AND DISCUSSIONS

The Voice Grip Bot was developed and tested to evaluate its functionality in voice recognition, object manipulation, and power efficiency. The system achieved a voice command recognition accuracy of 90–93percent in low-noise environments. While performance slightly declined in noisy settings, minimal command repetition maintained usability.

The average response time from voice input to action was under one second, supporting real-time control. The servo-operated gripper successfully handled lightweight objects (less than 150 grams) with an average accuracy of 85 percent, depending on shape and alignment.

Powered by a 7.4V Li-ion battery, the system operated effectively for approximately 1.5 to 2 hours under moderate use. Power efficiency was enhanced through optimized motor control and sleep states during inactivity.

The robot performed reliably on smooth indoor surfaces. However, it showed reduced stability on uneven or reflective flooring and decreased recognition accuracy in noisy environments.

Compared to manual control methods, the voice interface provided intuitive, hands-free operation, making it more accessible for assistive or smart automation use cases. Limitations include basic voice processing and a gripper suited only for small, regular-shaped objects. Future enhancements may include adaptive gripping and advanced voice recognition models.

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VI. CONCLUSIONS

The Voice Grip Bot presents an effective and affordable solution for voice-controlled robotic manipulation using the ESP32 microcontroller. The system integrates voice command processing, Bluetooth communication, and servo/DC motor actuation into a compact, mobile platform. It enables users to perform fundamental navigation and object manipulation tasks through simple, predefined voice commands transmitted from a mobile device.Through extensive testing in an indoor environment, the robot demonstrated high accuracy in voice command recognition, fast response time, and reliable gripping performance for small, lightweight objects. The use of readily available components and open-source development tools ensures that the platform is both cost-effective and replicable for academic or hobbyist use.The implementation also emphasizes user accessibility by eliminating the need for physical controllers, making it especially valuable for assistive applications and educational robotics. Its energy-efficient operation and modular design further support its use in low-power, mobile settings.However, some limitations remain. The voice interface relies on predefined commands and exhibits reduced accuracy in noisy environments. Additionally, the gripper's handling capacity is limited to basic shapes and weights. These challenges present opportunities for future development, such as integrating machine learning-based speech recognition, enhancing the mechanical design of the gripper, or enabling cloud connectivity for remote operation.

VII. ACKNOWLEDGMENT

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A Cost-Effective Infrared Cloning System Using Flipper Zero for Universal Remote Applications

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***Abstract* — The Flipper Zero is a compact, portable, open-source device designed for hardware hacking, cybersecurity, and electronics experimentation. It supports RFID, NFC, sub-1 GHz frequencies, infrared, and GPIO, making it ideal for both beginners and experts. With its playful dolphin mascot, i t combines fun with professional capabilities. This project aims to create a custom Flipper Zero focused on addressing vulnerabilities in RFID and NFC technologies, common in mobile payments, access control, and smart devices. These systems face security risks like unauthorized access and data interception due to weak encryption, highlighting the need for better solutions. The custom Flipper Zero will feature specialized hardware, including a microcontroller, RF and infrared transceivers, and an intuitive interface for emulation, penetration testing, and data analysis. It will also offer educational resources to teach RFID/NFC security, hardware hacking, and ethical penetration testing. The device will help users assess security by simulating attacks, identifying vulnerabilities, and guiding corrective measures. The project aims to deliver a cost-effective device, estimated at Rs. 500-800, while promoting cybersecurity awareness and advancing Electronics and Communication Engineering.**

Keywords*— *Flipper Zero, NFC Security, RFID, IR Cloning, Cybersecurity

I. INTRODUCTION

Flipper Zero is a portable, open-source multi-tool designed for hardware hacking, security research, and electronics experimentation. It resembles a playful, tamagotchi like device with a quirky dolphin mascot, making it user-friendly and approachable for both beginners and experienced enthusiasts. Equipped with various functionalities, Flipper Zero can interact with RFID and NFC systems, emulate infrared remote controls, communicate over sub-1 GHz frequencies, and perform USB based tasks through BadUSB capabilities. Its GPIO pins enable users to connect to and control other hardware components, fostering creativity and innovation. With a vibrant community and continuous development, Flipper Zero is an invaluable tool for learning about cybersecurity, exploring hardware, and conducting penetration testing, all while maintaining a fun and engaging user experience. Flipper Zero is a multi-tool device engineered for security research, hardware interaction, and ethical penetration testing. Designed with an intuitive interface and extensive functionality, it enables users to assess vulnerabilities in wireless-communication. Assess vulnerabilities in wireless-communication technologies such as Near Field Communication (NFC), Radio Frequency Identification (RFID), and Infrared (IR).

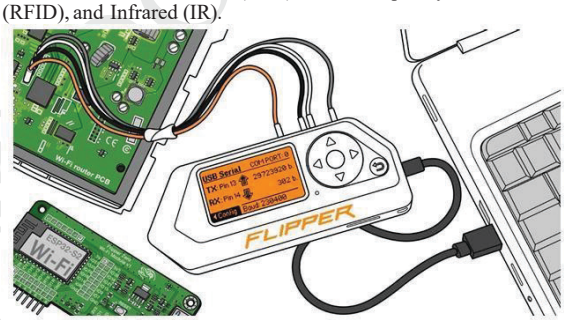


Fig_1 Representation of a Flipper Zero

II. BACKGROUND

Substantial amount of research work has been done in the field of Flipper Zero. Some of the key findings and developments has been discussed below:

In [1] Near Field Communications (NFC) is an emerging technology that allows two devices in close proximity to quickly establish wireless, contactless communication. While NFC appears to be intuitively secure and has been widely adopted in applications such as ticketing, mobile payments, and access control, questions arise regarding the trustworthiness of these applications, particularly concerning the potential leakage of users' private information. This paper surveys the vulnerabilities associated with NFC and explores various security attack methods. It also reviews possible solutions to defend against these security threats. Additionally, the paper evaluates the practicality and cost-effectiveness of both the attacks and countermeasures.

In [2] The rapid growth of Internet of Things (IoT) devices in our interconnected world has introduced remarkable convenience and efficiency. However, this swift adoption has also led to significant security issues, as many of these devices lack strong defenses against vulnerabilities and potential attacks. This review article examines the vital role

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of ethical hacking, penetration testing, and vulnerability assessment in tackling these IoT security challenges. It specifically focuses on the Flipper Zero device, a versatile tool for ethical hackers and security researchers, highlighting its application in assessing IoT security. The Flipper Zero is showcased as an essential instrument for ethical penetration testing, equipped with features that enable security professionals to effectively identify vulnerabilities and weaknesses in IoT devices. The review identifies vulnerabilities discovered during the research, categorizing them by severity and potential impact. Additionally, it provides security recommendations and emphasizes the importance of responsible disclosure, collaboration with manufacturers, and the continuous assessment of IoT device security. This review also outlines future directions in IoT security research and ethical hacking. In conclusion, it stresses the importance of ongoing security assessments and responsible testing practices to protect our increasingly interconnected world.

In [3] The paper explores the increasing adoption of IoT technologies like NFC (Near Field Communication), particularly in applications like access control systems. While NFC is effective for short-range communication, it has vulnerabilities due to the lack of encryption and unprotected communication channels between the tag, reader, and database. These weaknesses make it susceptible to attacks such as man-in-the-middle, denial of service (DoS), and data corruption, Dept of ECE, BMSCE 5 which can result in critical data leaks for organizations relying on NFC. FLIPPER ZERO The paper evaluates various NFC security risks using the Analytical Hierarchy Process (AHP) model to assess potential threats and mitigation strategies. It focuses on best practices to prevent attacks and demonstrates the effectiveness of these strategies through a case study on an existing NFC-based access control system. What I understood from this is that while NFC offers convenience, it's crucial to assess its security vulnerabilities and implement recommended practices to mitigate risks, ensuring the safe use of NFC in sensitive applications like security systems.

In [4] The paper explores NFC security, focusing on detecting relay attacks using RF fingerprinting. NFC, vulnerable to eavesdropping and relay attacks, is commonly used but lacks effective protection against such threats. Previous methods, like distance bounding, are limited. This study applies RF fingerprinting to the ISO/IEC 14443-A protocol, using a deep CNN trained on over 66,000 samples from four NFC tags. The results showed 99% accuracy in distinguishing normal from relayed signals, offering a promising solution to improve NFC security against relay attacks.

In [5] The paper "A Hacker's Delight: You'll Either Love or Hate the Flipper Zero" by Stephen Cass explores the polarizing opinions surrounding the Flipper Zero device. Security researchers and hardware developers find the device useful for debugging wireless setups and testing systems, while IT professionals may view it as a threat due to its potential for misuse in network and physical attacks. The paper emphasizes that, regardless of perspective, understanding the Flipper Zero is crucial for cybersecurity professionals.

In [6] Flipper Zero in Action: A Comparative Review of Six Methods for Enhanced Cybersecurity Tactics by Arghya Das Dev and Dr. Shyam R, Cyber threats develop rapidly, making flips zero -like advanced penetration testing tools. The thesis examines six important cyber security methods using zero, which includes Wi-Fi shooting, radio frequency manipulation, NFC cloning and Bluetooth-Kidnapping. Each method is analyzed for its efficiency and potential security risks. Research has shown that USB-based attacks such as BadUSB and HID falsification can provide unauthorized access. NFC cloning and radio frequency manipulation also provide serious risks, especially in the IoT environment. Wi-Fi attacks are still a major concern, experts have emphasized encryption and authentication. While previous studies have focused on individual attack techniques, there is a decline in comparison with a wider comparison. This study carries intervals by evaluating the strength and weaknesses of many methods. By doing this, it provides valuable insights to professionals in cyber security in the real world -applications of Flipper Zero, which helps them strengthen security strategies.

In [7] Navigating The Flipper Zero, A Comprehensive Tool for Cybersecurity Professionals by Abhishek S Thakur and Reeta Singh, Flipper Zero is a powerful and adaptable cyber security tool designed for penetrated testing. It is equipped with features such as RFID emulation, radio signal analysis and unit control, making it a choice for moral hackers and security people. Supports multiple wireless protocols and offers a wide range of applications in safety testing and research. Studies have expressed concern about the risk associated with RFID and NFC cloning, as these weaknesses may allow the attackers to circumvent access control systems. In addition, infrared manipulation and USB templation extends possible use of Flipper Zero, making it a versatile but potentially risky tool. Compared to traditional cyber security equipment, its modular design and adaptability do so. However, moral concerns are an important point of discussion, as its abilities can be abused. Researchers emphasize the importance of safety measures and responsible use of guidelines to prevent malicious activities. Flipper Zero is still a valuable property in cyber security, with the ongoing open-source contribution to increase functionality. This study examines its real implications and roles in digital security.

III. Problem analysisand solution

A. Problem definition

As electronic communication technologies evolve, they increasingly integrate into everyday applications, such as mobile payments and smart home devices. However, this integration also exposes significant security vulnerabilities, particularly in technologies like RFID (Radio Frequency Identification) and NFC (Near Field Communication). These vulnerabilities include unauthorized access through relay attacks, data interception, and spoofing, which can lead to identity theft and financial loss. The lack of robust authentication protocols and encryption mechanisms further exacerbates these risks, making it imperative to develop tools that can assess and mitigate these vulnerabilities effectively. In the context of Electronics and Communication Engineering (ECE), the challenge lies in creating a multifunctional device that not only demonstrates these vulnerabilities but also serves as an educational tool for understanding the principles of secure electronic communication. The Flipper Zero, with its capabilities to emulate RFID cards and intercept signals, presents an opportunity to explore these issues hands-on.

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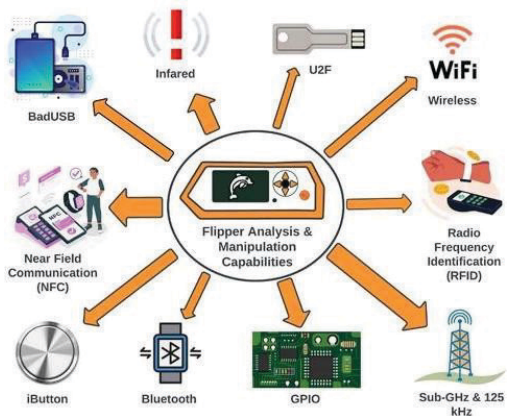


Fig_2 Applications of flipper zero

B. Proposed solution

To address the identified security challenges, this project proposes the development of a Flipper Zero device from scratch. The proposed solution involves:

1. Custom Hardware Development: Building a Flipper Zero with essential components such as a microcontroller, RF transceiver, infrared transceiver, and user interface. This hardware will facilitate various functionalities, including signal capture and emulation.

2. Firmware Programming: Developing custom firmware that allows the device to perform penetration testing on NFC and RFID systems. This includes implementing features for signal analysis, data interception, and emulation of various communication protocols.

3. Educational Component: Incorporating an educational module that explains the principles of electronic communication, highlighting the vulnerabilities in NFC and RFID technologies. This will serve as a resource for students to understand both theoretical concepts and practical applications.

4. Security Assessment Tools: Providing users with tools to evaluate the security of their own systems by simulating attacks in a controlled environment. This will empower users to identify weaknesses in their electronic communication systems and implement appropriate security measures. By developing this Flipper Zero device, the project aims to enhance awareness of security issues in electronic communication while providing practical solutions for mitigating these risks within the field of Electronics and Communication.

IV. Methodology & Implementation

C. Block diagram

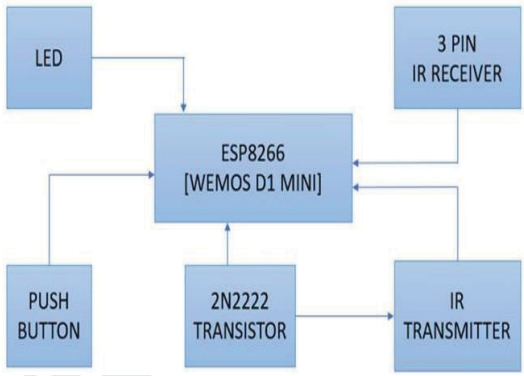


Fig_3.1 Block diagram of the flipper zero:IR cloner circuit 1

The device, constructed across the ESP8266 (Wemos D1 Mini), captures, stores, and retransmits IR signals, functioning as a custom Flipper Zero tool. A push button serves as an input, triggering moves like turning on an LED or sending IR alerts. The IR receiver captures signals from an outside faraway, which the ESP8266 decodes and techniques. The IR transmitter, managed thru a 2N2222 transistor, sends signals via amplifying the cutting-edge to force the IR LED efficiently. The LED gives visible feedback, indicating while indicators are obtained or transmitted. This setup allows for faraway manage duplication and automation by shooting and replicating IR commands effectively.

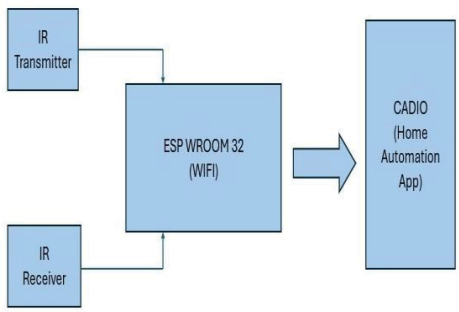


Fig_3.2 Block diagram of the flipper zero: IR cloner circuit 2

The block diagram provides a high-level overview of the ESP32-based IR communication system integrated with a home automation application (CADIO). The IR transmitter and IR receiver are interfaced with the ESP32, which acts as the central processing unit for handling IR signals. The ESP32 can transmit or receive IR signals and then send data over

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WiFi to the CADIO app, enabling remote control functionality. This system can be used for various applications, such as controlling appliances, smart home integration, and wireless communication.

D. Components and Their Functions:

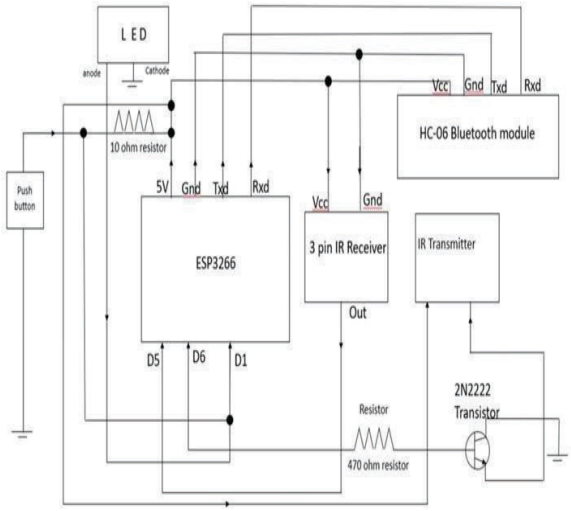


Fig_4.1 Components and the circuit 1 diagram

The ESP8266 (Wemos D1 Mini) is the core of the circuit, a Wi-Fi-enabled microcontroller responsible for managing signals, controlling the IR transmitter and receiver, and processing inputs fromthe frenzy button whilst speaking with the LED. The three-pin IR receiver captures infrared indicators from external resources, changing theminto digital facts for the ESP8266 to system. Based on those inputs, the IR transmitter emits infrared signals to control well suited devices inclusive of TVs or air conditioners. Since the ESP8266 by myself cannot supply sufficient modern-day, a 2N2222 transistor is used to make bigger the signal and power the IR transmitter effectively. A push button presents consumer enter to trigger actions like sending IR signals or toggling the LED. The LED serves as a visual indicator, displaying the system's fame, IR verbal exchange hobby, or other capabilities. Additionally, an HC-06 Bluetooth module is incorporated into the circuit, permitting wi-fi communication and far flung manipulate competencies. This setup permits for IR sign cloning, automation, and remote manipulate duplication, making it a flexible device for diverse programs.

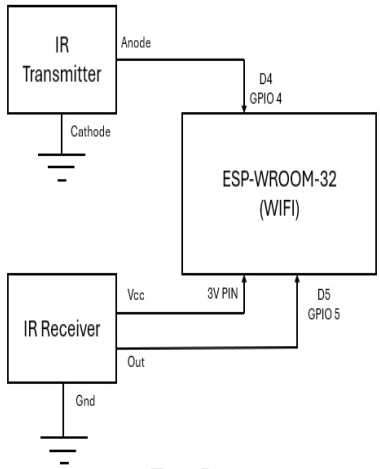


Fig_4.2 Components and the circuit 2 diagram

This circuit illustrates the connection of an IR transmitter and IR receiver with an ESP-WROOM-32 (ESP32) module to enable infrared communication. The IR transmitter is connected to GPIO 4 (D4) of the ESP32, allowing it to send infrared signals. The IR receiver is linked to GPIO 5 (D5) and powered through the 3V pin of the ESP32, enabling it to detect and decode incoming IR signals. The ground connections ensure proper circuit operation. This setup allows the ESP32 to transmit and receive IR signals, making it suitable for applications such as remote control and automation.

E. Workflow

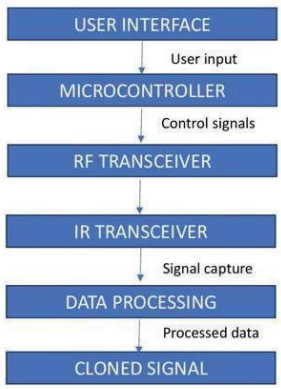


Fig_5 Workflow diagram

The system follows a structured workflow to capture, treat and repeat signs effectively. The user is delivered through the input user interface, which is later interpreted by the microcontroller. The microcontroller produces control signals to manage both RF and IR transits. These transceivers catch external characters and transfer them to the data processing device for further analysis. The treatment unit processes and structures data to ensure accurate replication. When processed, the data is converted to a clone signal that

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mimics the original input. This spontaneous integration between components enables accurate signal analysis and repetition. The systematic approach increases the efficiency of the device, making it highly adaptable to different applications.

V. RESULTSAND DISCUSSION

The development of the Flipper Zero device as a custom multi-protocol tool marked significant strides in tackling key security challenges within modern communication systems. The project's results are outlined below:

Hardware Functionality

The custom-built Flipper Zero hardware was seamlessly integrated with crucial components, including the microcontroller, RF transceiver, infrared transceiver, and GPIO pins. These elements enabled the device to emulate, intercept, and analyze various communication protocols such as RFID, NFC, and sub-1 GHz signals. To ensure its accessibility, the device featured a user-friendly interface supported by an LCD display, making it suitable for both beginners and experienced users.

Cost Efficiency

The project maintained effective cost management, with total expenditures kept within the estimated range of ₹4,000-₹5,000. This demonstrated judicious material selection and optimization for both functionality and affordability.

Security Assessments

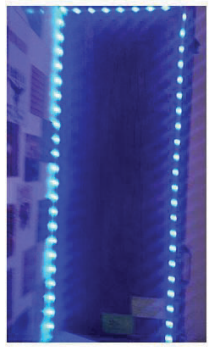
Simulated attacks performed using the Flipper Zero revealed vulnerabilities in RFID and NFC systems, including susceptibility to replay and relay attacks. These experiment s underscored the necessity of robust encryption and authentication mechanisms.

Discussion:

The Flipper Zero project successfully bridged theoretical knowledge and practical application within electronics and communication engineering. Key discussion points include: Impact on Security Research The device's ability to replicate attacks in a controlled setting highlights its significance for cybersecurity professionals. It serves as both an educational tool and a practical resource for identifying vulnerabilities. Potential ethical concerns regarding the misuse of such devices were addressed by promoting responsible disclosure and controlled usage. Educational Value Through hands-on experience, the Flipper Zero enables students and professionals to better comprehend vulnerabilities in RFID and NFC systems. The educational module effectively demystified complex concepts. Incorporating real-world case studies and scenarios enriched the learning process, making the project suitable for academic and professional training environments. Technical Challenges During development, challenges such as optimizing firmware for diverse functionalities and ensuring hardware compatibility across various communication protocols were encountered. These issues were resolved through iterative testing and community feedback. Time constraints and limited resources required prioritization of certain features, leaving room for further enhancements. Project's Final result: This IR cloner device developed by us showed positive results when it was tested with LED strip lights that were controlled by an IR based remote. Here, the initial stage of the LED lights was of green, but after registering a BLUE light signal from the remote, sending it to the LED light strips makes it turn from green to blue.



Initially "Green light" (Original)

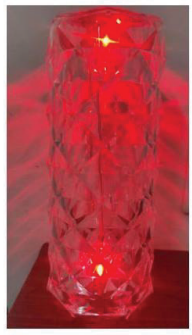


Turned "Blue light" using IR Cloner

Fig_6 Results 1



Initially lamp is green (Original)



Lamp turns red using device.

Fig_6 Results 2

VI. CONCLUSION

The IR cloner project stands as a testament to the fusion of innovation, education, and practical application in addressing modern security challenges. By fostering a deeper understanding of vulnerabilities in communication systems and inspiring future advancements, it establishes a robust foundation for continued research and development in cybersecurity. Future Trends: The Flipper Zero's success points to several emerging trends and future directions in embedded systems, IoT, and cybersecurity: Enhanced Security Protocols With the increasing adoption of RFID and NFC technologies, the demand for advanced security

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protocols capable of resisting emerging threats —like AI-driven attacks—is expected to grow. Devices such as the Flipper Zero will continue to play a crucial role in identifying and mitigating these vulnerabilities. Integration with AI and Machine Learning Future iterations could integrate AI capabilities, enabling automated threat detection and mitigation. For example, machine learning models could analyze intercepted signals to predict and prevent potential attacks. AI-driven insights would also enhance penetration testing and vulnerability assessment capabilities. Expansion into IoT Ecosystems The rapid growth of IoT devices necessitates comprehensive testing tools that interact with diverse communication protocols. The Flipper Zero's modular design makes it well-suited for expansion into IoT-specific protocols like Zigbee and LoRa, broadening its applications in smart home and industrial IoT security. Ethical Hacking and Education Ethical hacking will remain integral to cybersecurity, and tools like the Flipper Zero can be further adapted for educational programs that train future security professionals. Open-source development and community-driven enhancements will likely shape the evolution of such tools, ensuring their adaptability in a dynamic technological landscape.

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An FPGA application of home security code using verilog

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***Abstract*— Conventional key-and-lock security systems are susceptible to theft, duplication, and misplacement, compromising security. This paper presents an FPGA-based home security code lock system implemented using Verilog HDL. The system leverages a Xilinx Boolean Board, employing a 4x4 matrix keypad for passcode input, a Finite State Machine (FSM) for secure state transitions, and a 7-segment display for user feedback. The design was simulated and verified using Xilinx tools, demonstrating the efficiency and adaptability of FPGA-based security solutions.**

Keywords— FPGA, Home Security, Verilog, Finite State Machine (FSM), Keypad, Digital Lock.

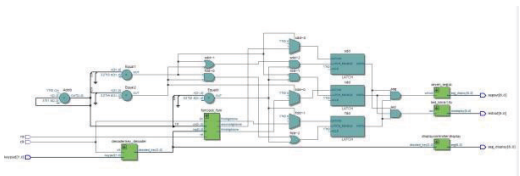
I. Introduction

Security is a fundamental concern in residential and commercial settings. Traditional mechanical locks suffer from key duplication, theft, and loss, necessitating advanced digital solutions. FPGA-based security systems provide enhanced flexibility, reconfigurability, and real-time performance, making them ideal for digital lock applications. This paper presents an FPGA-based home security code lock system designed using Verilog HDL and implemented on a Xilinx Boolean Board.

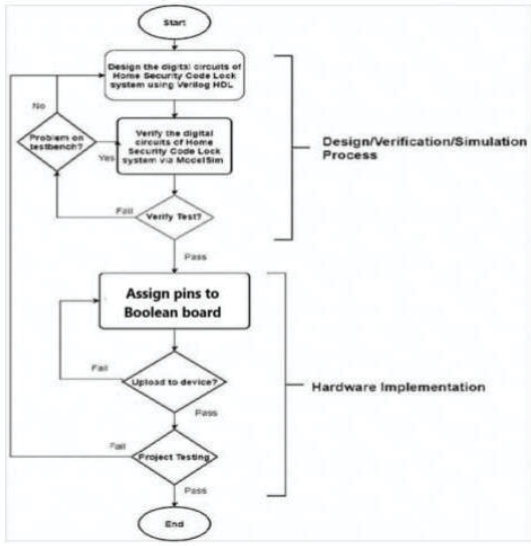
II. Related work

Existing security systems primarily utilize microcontrollers or ASICs. While microcontroller-based systems are cost-effective, they lack parallel processing capabilities. ASIC-based solutions, on the other hand, provide high efficiency but lack reconfigurability. FPGA-based designs bridge this gap by offering scalability, rapid prototyping, and cost-effective modifications. Previous research [1] has demonstrated the potential of FPGA-based security implementations, emphasizing their reliability and flexibility.

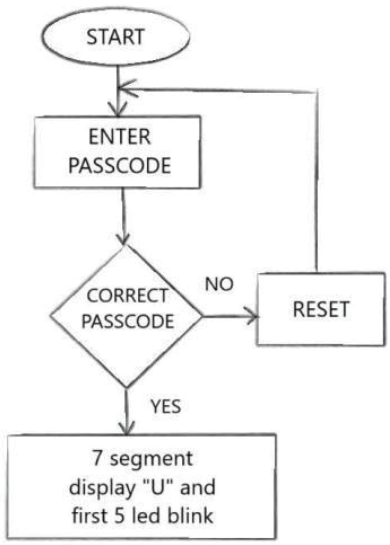
A. Block Diagram



B. Design Flow



C. Flowchart



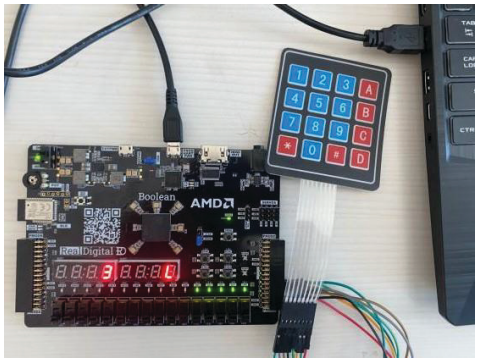
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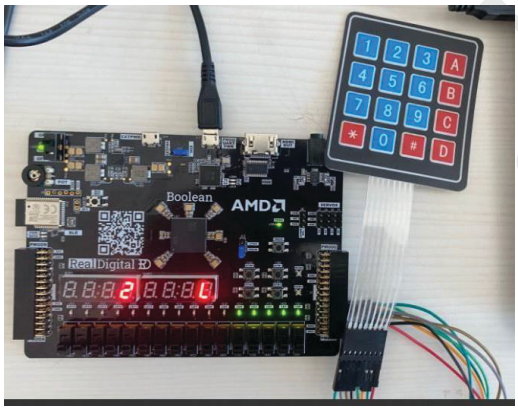
D. 4x4 table representation

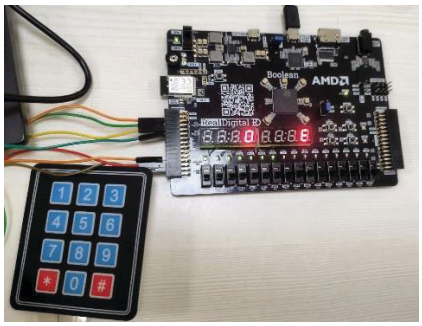
Table 1. Columns and rows

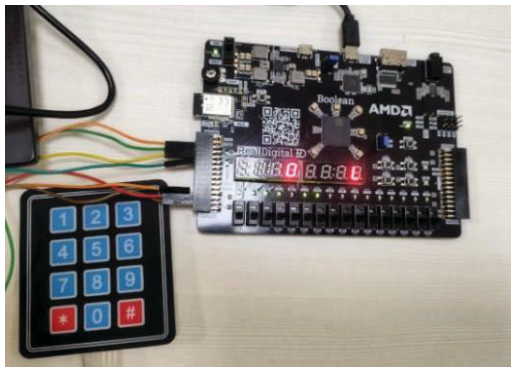
Column (C1, C2, C3, C4)	Row (R1, R2, R3, R4)	Button
0111	0111	1
0111	1011	4
0111	1101	7
0111	1110	*
1011	0111	2
1011	1011	5
1011	1101	8
1011	1110	0
1101	0111	3
1101	1011	6
1101	1101	9
1101	1110	#
1110	0111	A
1110	1011	B
1110	1101	C
1110	1110	D

D. Boolean board implementation for L and Error

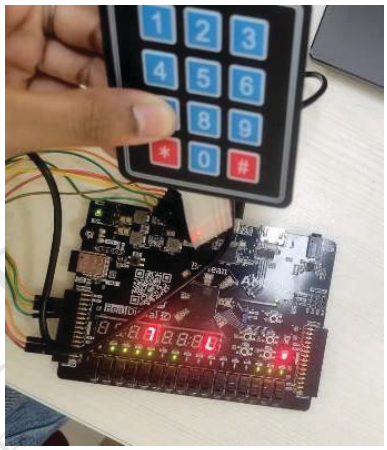


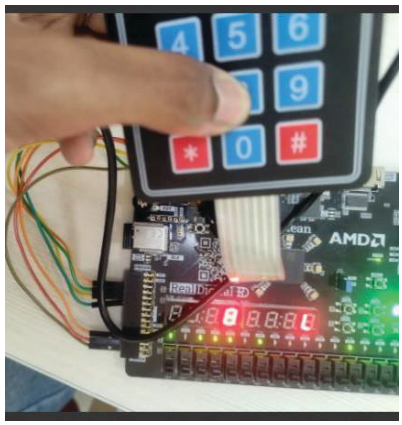




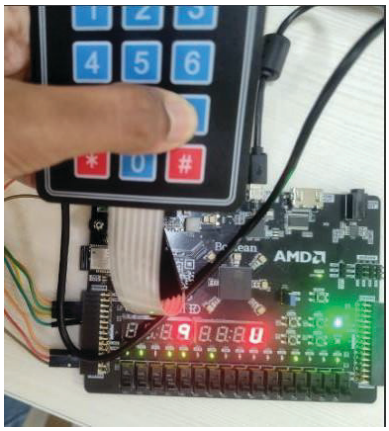


E. Boolean board implementation for U with password display





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III. System Design

A. Hardware Components

- *Xilinx Boolean Board (Spartan-7 FPGA)*
- *4x4 Matrix Keypad for user input*
- *7-Segment Display for visual feedback*
- *LEDs for status indication*

B. Software Tools

- *Xilinx Vivado for simulation and synthesis*
- *ModelSim for functional verification*

C. Finite State Machine Implementation:*The FSM-based control ensures secure passcode validation. It transitions through predefined states based on user input. If the correct passcode is entered, the system unlocks; otherwise, it resets.*

IV. Implementation and Results

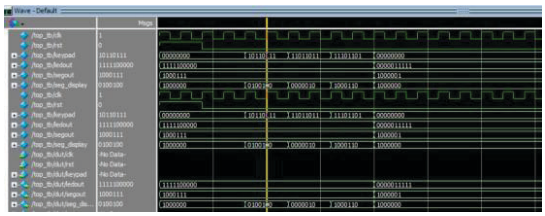
A. **Simulation and Verification** The design was simulated using ModelSim to verify functional correctness. The FSM transitions and passcode validation were successfully tested.

B. **Hardware Testing** The synthesized design was deployed on the Boolean Board, where the keypad inputs were correctly decoded, and the 7-segment display provided real-time feedback.

C. **Performance Evaluation**

- **Latency:** The system responded instantly to keypresses.
- **Security:** Incorrect passcodes resulted in immediate reset.
- **Scalability:** FPGA's reconfigurability allows future upgrades, such as biometric integration.

D. **Simulation graph**



V. Future Work

Future enhancements include biometric authentication, IoT integration for remote monitoring, and AI-based anomaly detection for enhanced security. Power optimization techniques will also be explored for energy-efficient implementations.

VI. Conclusion

This paper demonstrated an FPGA-based home security code lock system using Verilog HDL. The FSM-based design ensures secure and reliable passcode authentication. Simulation and hardware implementation validated the system's functionality, proving FPGA's potential in modern security applications.

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APPENDIX B:

Simulation and Implementation of a RISC-V RV32I Processor

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***Abstract*— This project involves the simulation and implementation of a custom 32-instruction processor based on the open-source RISC-V ISA, chosen for its modular and extensible design. The initial phase focuses on designing key components like instruction decoding, control path, ALU, register file, and memory interface to support fundamental arithmetic, logic, memory, and control operations. Functional verification is performed through simulation to ensure accurate and efficient execution. The long-term goal is to extend this processor with AI/ML-specific hardware accelerators—capable of tasks like matrix multiplications and vector operations—on an FPGA platform, ultimately creating a scalable, power-efficient architecture for edge computing and reconfigurable AI systems.**

***Keywords*— 32-bit processor, instruction set architecture (ISA), single-cycle processor, Verilog HDL, Synopsys VCS, FPGA implementation, control unit, ALU, register file, instruction memory, data memory, testbenches, waveform simulation, control signals, RegWrite, MemRead, MemWrite**

I. Introduction

The growing dependence on Artificial Intelligence (AI) and Machine Learning (ML) has introduced significant challenges related to computational performance and energy efficiency. As AI/ML models become more complex, especially during training, traditional general-purpose processors fall short in meeting the performance demands. This has led to the development of specialized hardware architectures and accelerators that can efficiently execute intensive tasks like matrix multiplications and vector operations.

Simultaneously, there is a shift toward open and customizable Instruction Set Architectures (ISAs), with RISC-V gaining popularity due to its modularity, extensibility, and open-source nature. RISC-V allows developers to implement a base processor and extend it with application-specific features, eliminating licensing barriers and enabling innovation in both research and development. This project focuses on designing and simulating a custom 32-instruction RISC-V processor as a foundation for more advanced systems with AI/ML acceleration capabilities. The processor supports essential operations like arithmetic, logic, memory access, and control flow, providing a compact yet functional platform to demonstrate core architectural concepts.

The processor is described using Hardware Description Languages (HDLs) and validated through simulation. This helps test instruction execution, observe signal behavior, and verify control flow, ensuring that the design is both modular and extensible for future upgrades. In the long term, the project aims to integrate a hardware accelerator for AI/ML tasks like dot products and gradient calculations. These components will interface directly with the processor to enable efficient data handling and low-latency computation.

The final system will be implemented on a Field-Programmable Gate Array (FPGA) to enable real-time testing. FPGAs support reconfigurability and hardware/software co-design, making them ideal for evaluating trade-offs between performance, power, and resource usage. Ultimately, this work demonstrates how a 32-instruction RISC-V processor can evolve into a scalable and energy-efficient platform tailored for intelligent applications in embedded and edge computing environments..

II. Design and Methodology

A. Proposed Solution

The compact 32-instruction core enables focused optimization for key computational tasks. It allows easy integration of custom instruction extensions to support operations like tensor computations, matrix arithmetic, and floating-point processing, commonly used in AI model training and backpropagation. The minimal footprint ensures resource efficiency while maintaining flexibility for future upgrades.

Unlike proprietary architectures like x86 or ARM, RISC-V's open-source nature permits deep customization at both the instruction and microarchitecture levels. This empowers developers to create and test new instructions, integrate AI co-processors, and modify control logic freely, critical for

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real-time, adaptive AI tasks in power-constrained environments such as edge devices.

The processor is planned for implementation on a Field-Programmable Gate Array (FPGA), which offers a reconfigurable hardware platform ideal for iterative design, hardware/software co-design, and real-time testing. FPGAs support parallel execution and allow direct mapping of hardware, making them suitable for validating the processor core and future accelerators.

This approach also emphasizes tight integration between the processor and AI accelerators to allow efficient offloading of compute-heavy tasks. Such coupling reduces latency, enhances data flow, and improves performance-per-watt—making the system well-suited for edge AI applications.

In essence, this project aims to build a scalable, energy-efficient, and open hardware platform that connects minimal RISC-V processor design with advanced AI/ML execution. The 32-instruction core serves as a springboard for innovation in domain-specific processor design, offering an adaptable foundation for future intelligent computing systems.

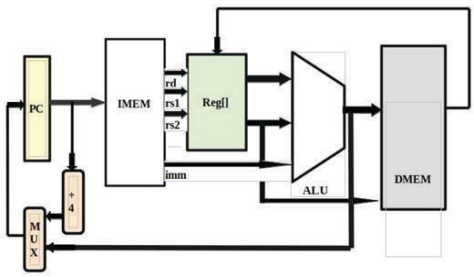


Fig 1. Flow Chart of the model

B. *Working Principle*

The processor operates based on the RISC-V RV32I instruction set, designed to execute a subset of 32 essential instructions that include arithmetic, logic, memory, and control flow operations. It follows a single-cycle execution model, where each instruction is fetched, decoded, executed, and completed within a single clock cycle. This simplified architecture makes the design compact and efficient, particularly suitable for embedded and educational applications.

The process begins with the Instruction Fetch stage, where the Program Counter (PC) points to the memory address of the instruction to be executed. The instruction is retrieved from the Instruction Memory (IMEM) and passed on for decoding. Simultaneously, the PC is updated for the next instruction, typically by adding 4, unless a branch or jump alters the flow.

In the Instruction Decode phase, the instruction is broken down into its components: opcode, source and destination register addresses, and immediate values if present. The Control Unit interprets the opcode and generates appropriate control signals required for routing data and performing operations. These control signals dictate the behavior of the ALU, memory, and register file in subsequent stages.

Next, during the Operand Fetch stage, values from the specified source registers (rs1 and rs2) are read from the Register File. If the instruction requires an immediate operand, it is generated by the Immediate Generator, which extends it to the required width for processing.

The Execution stage involves the Arithmetic Logic Unit (ALU), where operations such as addition, subtraction, AND, OR, comparisons, or address calculations are performed. The ALU's behavior is controlled by signals from the ALU Control Unit, based on the decoded instruction type. The ALU also generates flags like zero or sign bits, used in conditional branching.

For load and store operations, the processor moves into the Memory Access phase. Here, the Data Memory (DMEM) is accessed either for reading data (load) into a register or writing data (store) from a register. The address used for memory access is calculated in the ALU stage. Finally, in the Write Back stage, results from the ALU or data memory are written into the destination register (rd) if required by the instruction. This completes the instruction cycle. Throughout the process, Multiplexers (MUXes) and control logic ensure that the correct data flows between components based on the instruction being executed.

III. IMPLEMENTATION

The single-cycle RISC-V processor is implemented using a modular hardware design approach, where each instruction is executed completely within one clock cycle. The processor architecture consists of several interconnected blocks including the Program Counter (PC), Instruction Memory, Register File, Control Unit, Immediate Generator, Arithmetic Logic Unit (ALU), Data Memory, and several Multiplexers (MUXes) for managing data flow.

The Program Counter holds the address of the current instruction and is updated every cycle, either incremented by 4 (for sequential execution) or updated with a branch target address depending on the instruction type. The Instruction Memory block provides the 32-bit instruction corresponding to the current PC value. This instruction is then decoded to extract important fields such as opcode, source and destination registers, function codes, and immediate values.

The Control Unit interprets the opcode and generates control signals such as RegWrite, MemWrite, MemRead, ALUSrc, MemtoReg, and PCSrc. These signals govern how data is routed within the processor. Based on the decoded fields, the Register File reads data from the specified source registers and, after execution, writes the result back to the destination register if needed.

For instructions that involve immediate values, such as arithmetic immediate or load/store operations, the Immediate Generator extracts and sign-extends the immediate field appropriately. The ALU performs the core computations—such as addition, subtraction, bitwise operations, and comparisons—based on the control signals generated by the ALU Control Unit, which itself derives information from the function codes.

The result from the ALU is either used directly (in arithmetic or branch operations) or used as an address to access the Data Memory in case of load or store instructions.

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The Data Memory block either reads data to be written back to the register file or receives data from a register to store in memory. A multiplexer determines whether the value to be written back to the register file comes from the ALU or memory, depending on the instruction type.

Finally, the Program Counter is updated based on whether the current instruction is a branch, jump, or a regular instruction. If branching is required, the PCSrc signal selects the branch target address computed by the ALU; otherwise, the PC is simply incremented by 4. This entire data path is clocked and synchronized, allowing for every instruction to be processed fully within a single clock cycle. This modular and clearly segmented implementation provides a functional and testable design for the RISC-V processor, suitable for FPGA prototyping and further enhancement toward pipelining or AI acceleration in future work.

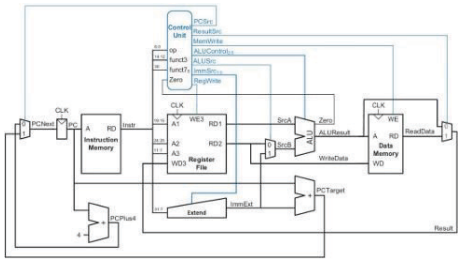


Fig 2. Single Cycle Processor

IV. RESULTS AND DISCUSSION

The implementation of the single-cycle RISC-V 32I processor was verified through functional simulation and schematic validation. The processor design integrates all essential data-path components, including the instruction memory, register file, ALU, control unit, and data memory, interconnected to support the execution of RISC-V base instructions. The simulation of the custom 32-instruction RISC-V processor was carried out using Synopsys VCS, providing valuable insights into the functional behavior and correctness of the architecture. The waveform outputs obtained from the simulation confirm that each instruction from the defined subset executes accurately in alignment with the RISC-V ISA semantics.

The processor correctly handles essential control signals, operand fetching, register file operations, and instruction sequencing, demonstrating proper architectural integration and datapath functionality. Each instruction was tested individually and as part of instruction sequences to ensure consistency in behavior under various computational conditions. The results verified that the arithmetic and logical units operate as expected, with the Arithmetic Logic Unit (ALU) correctly performing addition, subtraction, bitwise operations, and comparisons. The simulation also confirmed that immediate generation, branch target calculation, and register updates follow the correct logic. Control instructions such as jumps and branches accurately update the program counter (PC), and load/store instructions interact reliably with memory modules. Throughout the simulation, internal signals such as RegWrite, ALUSrc, MemRead, MemWrite, and Branch behaved as expected, enabling each instruction to progress through the defined control flow of the processor. The register file was consistently updated with the correct output values, confirming that data dependencies were resolved and outputs propagated as intended. Observations from the waveform demonstrate the timely assertion of control signals and seamless coordination between instruction fetch, decode, execution, memory, and write-back stages—even though they occur sequentially rather than in parallel, given the non-pipelined architecture. The custom 32-instruction architecture showed consistent stability across different types of instructions, including arithmetic operations, memory interactions, and control transfers.

The instruction decoder handled the compressed instruction set effectively, supporting a clean execution path and validating the functional integrity of the ISA implementation. Testbenches written for each instruction type aided in isolating potential faults and verifying outputs cycle-by-cycle, contributing to thorough validation of system behavior. While the simulation results validate the correct implementation of each instruction and core functionality, certain performance limitations were noted. As a non-pipelined implementation, the architecture exhibits limited instruction throughput and lacks instruction-level parallelism. Each instruction completes in a fixed number of clock cycles depending on its type, which may not be optimal for high-speed or compute-intensive environments. Additionally, the use of basic forwarding mechanisms and the absence of hazard detection logic in this initial design stage may lead to future bottlenecks when scaled to more complex instruction sequences or integrated with co-processors. Nonetheless, the validated design serves as a solid baseline for further enhancement. The custom instruction set can now be extended with AI/ML-specific operations, and hardware acceleration units can be integrated in the next phase.

The current testbench framework and simulation environment also provide a foundation for evaluating more advanced features like pipelining, multicycle execution, and co processor interfacing in upcoming iterations. In terms of power consumption, the total dynamic power is 56.46 µW, which includes cell internal power of 3.13 µW and net switching power of 53.33 µW. The leakage power is reported to be 2.79 µW, bringing the total power dissipation to approximately 59.24 µW. This relatively low power figure demonstrates the energy efficiency of the synthesized design, making it viable for low-power embedded applications. Timing analysis reveals a worst negative slack (WNS) of -0.83 ns, with the data required time being 10.00 ns and the data arrival time being 10.83 ns. The slack being negative indicates that the current clock period target is not met, and the design is failing to meet timing constraints under the specified conditions. The critical path delay is 8.65 ns, which is significant for determining the maximum

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operating frequency, which comes out to be around 115.6 MHz (1 / 8.65 ns). This delay path should be further optimized by refining logic or pipeline balancing to achieve timing closure. Overall, the rv32i processor core shows good area and power characteristics but requires further optimization to meet the timing constraints. The presence of unresolved references and black-box components suggests that some modules may be missing full definitions, which could influence final synthesis accuracy and needs to be resolved for complete analysis.

V. CONCLUSION AND FUTURE TRENDS

The design and implementation of a custom RISC-V processor with a core instruction set of 32 carefully selected instructions marks an important milestone toward creating efficient, open, and adaptable computing platforms. By embracing the openness and modularity of the RISC-V architecture, this project demonstrates how minimal yet extensible processor designs can provide a solid foundation for future domain-specific enhancements, particularly targeting AI and machine learning workloads. The focused instruction set allows for streamlined hardware complexity while maintaining essential computational capabilities, which is critical for developing resource-efficient processors suited for embedded and edge computing environments. This architecture paves the way for incorporating specialized extensions and co-processors that can accelerate vector and tensor operations central to AI training and inference. Deploying the design on an FPGA platform further emphasizes the practicality of this approach, offering reconfigurability, real-time evaluation, and energy-efficient operation—all vital attributes for modern AI applications operating under stringent power and performance constraints. The synthesis reports show that the processor core occupies a compact area of approximately 34,511.5 μm^2, with low power consumption around 59.24 µW, and achieves a maximum operating frequency of about 115.6 MHz. These metrics confirm the processor's suitability for low-power embedded AI environments. While the timing performance is modest compared to high-performance cores, it remains adequate for a broad class of edge applications and can be improved with further optimizations. The hardware-software co-design methodology ensures tight coupling between the processor core and future accelerator units, optimizing data movement and execution flow for high throughput and low latency. Overall, this work validates the viability of constructing scalable, open-source hardware platforms that combine simplicity, flexibility, and extensibility. By laying down a well-structured, customizable RISC-V processor base with verified area, power, and timing characteristics, the project empowers academic researchers and embedded systems developers to explore innovative architectural improvements tailored for emerging AI challenges. The foundation established here not only advances the state of open hardware for AI but also catalyzes further exploration of energy-efficient, domain specific processor designs.

The computing industry is rapidly shifting toward open, modular, and domain-specific architectures, with the RISC-V ecosystem at the forefront. Its open-source, customizable instruction set has driven widespread adoption across academia and industry. Moving forward, RISC-V is expected to evolve from simple in-order pipelines to complex microarchitectures, including out-of-order, superscalar, and multicore designs. These advancements aim to enhance performance while maintaining flexibility and transparency. Standardized extensions for vector operations, cryptography, and AI workloads will further broaden its application scope. Hardware acceleration for AI and machine learning is set for significant growth. While current AI hardware focuses on inference, future designs will enable on-device training through energy-efficient accelerators. Domain-specific accelerators optimized for neural networks and parallel computations will integrate closely with RISC-V cores, enabling low-latency, high-throughput AI processing. This hybrid approach will support efficient hardware-software co-design, crucial for real-time AI workloads.

FPGAs will continue to play a vital role in developing these hybrid systems. As High-Level Synthesis (HLS) tools advance, they will simplify hardware design by enabling high-level language development, speeding up prototyping. Reconfigurable computing will expand in edge environments, demanding flexible and efficient performance under strict constraints. Future FPGA architectures may adopt chiplet-based designs, integrating heterogeneous components on a single die.

Deeper hardware-software integration will further evolve, with co-design methodologies enabling compilers and operating systems to interact more closely with hardware accelerators. AI-aware compilers that map operations directly onto hardware primitives will improve scheduling, power efficiency, and task offloading between CPU and accelerator cores.

Finally, energy efficiency and sustainability will be central to future designs. Techniques such as clock gating, approximate computing, and processing-in-memory (PIM) will gain importance. As AI models become more demanding, designers will prioritize minimizing energy consumption and carbon footprint, promoting responsible and sustainable hardware development.

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VI. ACKNOWLEDGMENT

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Design and Simulation of Asynchronous FIFO Buffer using Globally Asynchronous Methodology

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***Abstract*— This project focuses on designing and simulating an asynchronous FIFO in Vivado to address challenges in data transfer between different clock domains, including metastability, data corruption, and pointer synchronization. Robust synchronizer circuits with Gray-coded pointers are implemented to ensure safe transitions and minimize errors, while mechanisms for full and empty flag generation prevent overflow and underflow conditions. A key feature of this design is the integration of a parity bit mechanism, enabling real-time error detection for enhanced data integrity by identifying single-bit errors during high-speed operations. Detailed simulations and analyses, including timing evaluation and metastability characterization, validate the reliability of the design under varying clock frequencies. This work not only enhances the robustness of asynchronous FIFOs but also provides valuable insights into error detection strategies, making it highly relevant for applications such as signal processing, communication systems, and data buffering.**

Keywords*— First In First Out (FIFO), Field Programmable Gate Array (FPGA), Pointer, Flop-Synchronizer, Clock Domian Crossing (CDC), Metastability, Verilog.

I. Introduction

Human life has changed and become significantly easier with the invention of Integrated Circuit (IC) technology, which has revolutionized modern communication and computing. From enabling faster data processing to powering advanced communication systems, IC technology has laid the foundation for many innovations that define our interconnected world. Among these, the ability to manage and transfer data efficiently between systems with different clock domains has become increasingly important. One such essential component that facilitates this functionality is the Asynchronous FIFO (First-In, First-Out) buffer. Asynchronous FIFO plays a critical role in bridging the gap between subsystems operating under different clock frequencies or phases. Unlike traditional FIFOs, which rely on a single clock, asynchronous FIFOs decouple the write and read operations, allowing seamless data transfer in systems with independent clock domains. This capability is crucial for ensuring smooth communication in modern digital systems like communication networks, data processors, and multimedia devices.

II. Literature Review

Asynchronous FIFO architectures play a critical role in modern digital systems, enabling efficient data transfer across different clock domains while addressing issues such as metastability, synchronization, power consumption, and latency. Several research works have contributed to improving FIFO designs by introducing innovative methodologies.

Abdel-Hafeez (IEEE) proposed a clockless FIFO buffer that eliminates the need for traditional clock distribution networks, leveraging a handshake protocol to ensure seamless communication between processing elements while reducing power consumption. Shivali and Khosla (IEEE) explored the impact of metastability in asynchronous Gray-coded FIFOs using formal verification techniques. Their approach introduced buffer-induced delays to simulate metastable states, verifying design correctness through equivalence checking.

Xiao and Zhou (IEEE) presented a circular asynchronous FIFO with an optimized architecture that eliminates internal data movement, allowing direct communication between FIFO cells and input/output ports. This novel structure significantly reduces latency and power consumption while achieving a high throughput exceeding 2.2 GHz. Vinod Kumar et al. (JETIR) focused on a low-power Design-for-Testability (DFT) strategy, incorporating Gray code converters to minimize switching activity and power dissipation. Their approach ensures robust FIFO operation even under conditions of overrun and underrun, verified through Xilinx ISE simulations.

These studies collectively enhance the efficiency and reliability of asynchronous FIFOs, addressing key challenges such as metastability mitigation, power optimization, and high-speed data transfer. The advancements presented contribute to the development of high-performance, energy-efficient FIFO architectures for applications in SoCs, digital communication systems, and embedded processors. equation as a graphic and insert it into the text after your paper is styled.

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III. Problem Analysis & Solution

A. Problem Definition

Asynchronous FIFO (First-In-First-Out) buffers are essential for transferring data between subsystems operating in different clock domains. However, their design presents several challenges, primarily due to the asynchronous nature of the communication. Below is a detailed discussion of the key problems:

i. ***Clock Domain Crossing (CDC) Issues***:

Problem: The primary challenge in asynchronous FIFO design arises from the communication between two clock domains that operate independently. Signals crossing between these domains.

Impact: Metastability can lead to unreliable data transfer, resulting in corrupted or lost data, which is unacceptable in critical applicationsby the destination clock.

Example: If a write pointer updates while being sampled by the read clock, the consumer may read incorrect or incomplete data.

ii. Synchronization of Read and Write Pointers:

Problem: The FIFO relies on read and write pointers to manage data flow. In an asynchronous setup, these pointers are updated in their respective clock domains but need to be compared to detect full or empty conditions**.**

Impact: Inaccurate synchronization between pointers can cause errors such as false full or empty conditions, leading to data overwrites or invalid reads.

Example: If the read pointer is not correctly synchronized, the system might prematurely consider the buffer empty, halting valid data reads.

iii. Metastability in Pointer Synchronization:

Problem: Synchronization registers used to transfer pointers between clock domains are prone to metastability if signal transitions occur close to the sampling edge of the clock.

Impact: Metastable states may propagate through the logic, resulting in unpredictable system behavior.

Example: In critical systems, metastability can result in the failure of safety checks, potentially causing system-wide failures.

B. Problem Solution

The challenges in asynchronous FIFO buffers can be mitigated through careful design and robust techniques. Here are the solutions to address the problems:

i. Addressing Clock Domain Crossing Issues:

Solution: Use synchronization circuits with metastability-hardened flip-flops to safely transfer signals between clock domains.

Implementation: Employ dual-clock flip-flops and introduce sufficient settling time for signals crossing domains.

Outcome: This reduces the probability of metastability and ensures reliable communication.

***ii. Pointer Synchronization*:**

Solution: Utilize Gray Code Counters for read and write pointers. Gray codes change only one bit between consecutive states, minimizing the chance of error during synchronization.

Implementation: Synchronize the pointers using two-stage or multi-stage flip-flops before comparing them.

Outcome: This ensures accurate detection of full and empty conditions without glitches.

iii. Metastability Mitigation:

Solution: Add synchronization registers with sufficient delay stages to resolve metastability in pointers and control signals.

Implementation: Carefully design the synchronization paths with adequate timing margins.

Outcome: This reduces the metastability propagation and enhances the reliability of pointer synchronization.

IV. Methodology and Implementation

A. Clock Domain Crossing (CDC)

Methodology

Dual-Port Memory Architecture:

Use a dual-port memory block that allows separate read and write operations, each driven by its own clock. This decouples the two clock domains, ensuring smooth data transfer.

Synchronization Registers:

Signals crossing clock domains should pass through two or more stages of flip-flops in the destination clock domain. These synchronization stages allow metastability to settle before the signal is used.

Gray Code for Pointers: Use Gray code for read and write pointers to ensure that only one-bit changes at a time, reducing the chance of incorrect pointer values being sampled.

Handshake Signals: Use request and acknowledge signals to establish a handshake protocol between clock domains for control signals.

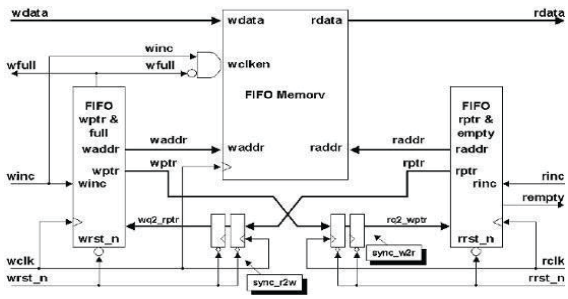


Figure 1: Asynchronous FIFO block diagram

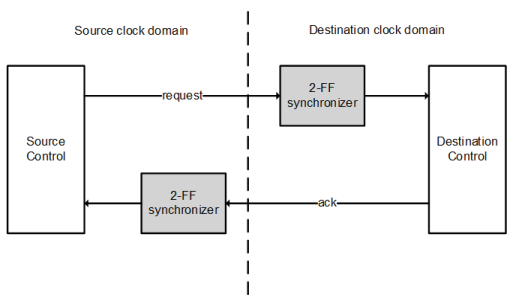


Figure 2: Handshake CDC Technique

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B. *Pointer Synchronization*

Methodology

Gray Code Counters:
Use Gray code counters for read and write pointers to minimize errors during pointer synchronization. Gray code ensures only one-bit changes per transition, making it safer for crossing clock domains.

Pointer Synchronization:
Synchronize the write pointer into the read clock domain and vice versa. Use a two-stage flip-flop chain for metastability mitigation during synchronization.

Pointer Comparison Logic:
Compare the synchronized pointers to detect full and empty conditions. Use logic to handle wrap-around cases in circular buffers.

Multi-Bit Pointer Synchronization:
For multi-bit pointers, synchronize each bit individually using multi-stage flip-flops, then reconstruct the full pointers.

C. *Metastibility*

Methodology

Metastability-Hardened Flip-Flops:
Use flip-flops with a higher gain-bandwidth product and carefully chosen setup/hold times to reduce the metastability window.

Two-Stage Synchronization:
Add at least two flip-flops in series to synchronize signals crossing clock domains. The first flip-flop resolves any metastability, while the second ensures a clean transition to the destination clock domain. The error obtained from a 2-stage synchronizer can be given as: $\mathbf{2^n - 2}$ Where n is number of bits in a symbol Since for gray code there is unitary change in the bits while transitioning, the error will be $2^1 - 2 = 0$. (n = 1 (bit change)) Therefore, gray to binary converter and binary to gray converters are installed in the synchronizers

Timing Margins: Ensure sufficient timing margin between signal transitions and sampling edges in the destination clock domain to reduce metastability risks.

Simulation and Analysis: Perform metastability analysis using simulation tools to calculate Mean Time between Failures (MTBF). Validate the design under worst-case scenarios, including maximum clock skew and process variations.

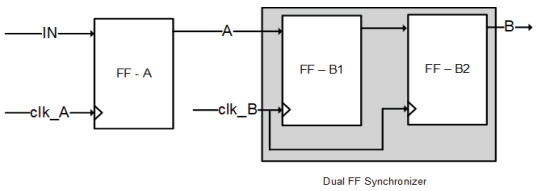


Figure 3: Dual Flop Synchronizer

V. Block Diagram and Waveforms

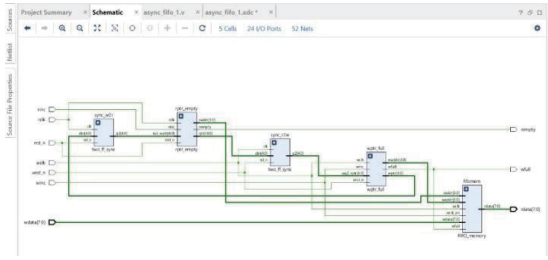


Figure 4: Schematic

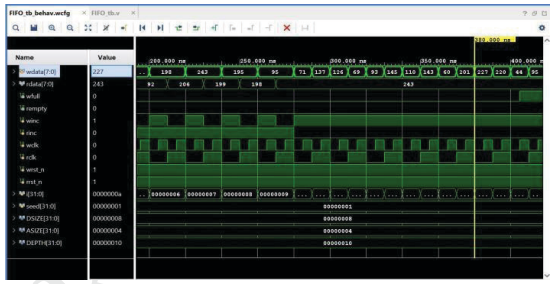


Figure 5: Waveforms

VI. Results and Discussion

The design and simulation of the asynchronous FIFO buffer successfully addressed critical challenges, such as clock domain crossing, metastability, and pointer synchronization. Advanced techniques, including gray code counters, multi-stage synchronization, and dual-port memory architecture, ensured reliable data transfer and scalability. The inclusion of parity-based error detection further enhanced data integrity, validating the design's applicability for modern high-speed and safety-critical systems. Below are the key outcomes from our team discussions on potential enhancements and future directions:

Key Discussion Outcomes

Optimization for Future Systems:
The design can be extended to support next-generation protocols like PCIe 6.0 and USB4 by optimizing the FIFO's clock domain interface to handle even higher data rates. However, it was noted that achieving this would require more efficient pointer synchronization mechanisms and potentially deeper FIFO depths.

Advanced Error Detection:
While parity bits are effective for basic error detection, the team concluded that integrating Error-Correcting Codes (ECC) would be beneficial for critical applications, such as aerospace or medical systems. However, ECC increases resource utilization, so its implementation would need to be balanced against hardware constraints.

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Scalability Challenges:
The design was found to be scalable for moderate data widths and depths, but the team identified that handling larger data widths could lead to increased complexity in pointer synchronization and metastability mitigation. Future designs should explore modular FIFO architectures for better scalability.

Simulation Enhancements:
The team agreed on performing additional stress tests, such as simulating extreme clock skew, process variations, and high-frequency noise scenarios. These tests would ensure the design remains robust under edge-case conditions, particularly for harsh environments like space applications.

VII. Future trends and Conclusion

Conclusion

The "Design and Simulation of Asynchronous FIFO Buffer Using Globally Asynchronous Methodology" successfully addresses the critical challenges of clock domain crossing, metastability, and pointer synchronization. By employing advanced techniques such as gray code counters, multi-stage synchronization registers, and robust control logic, the design ensures reliable data transfer between asynchronous clock domains. The use of dual-port memory enables independent read and write operations, providing decoupling between producer and consumer subsystems while maintaining high performance and scalability. Error-detection mechanisms, such as parity bits, enhance data integrity, making the design suitable for safety-critical applications. Metastability risks are mitigated through carefully designed synchronization stages and metastability-hardened flip-flops, ensuring robustness under varying conditions. The implementation of accurate full and empty condition detection prevents data overwrites and invalid reads, further improving system reliability. Simulation and validation in Vivado confirm the design's functionality, robustness, and compliance with timing requirements, ensuring its applicability in real-world scenarios. The project demonstrates the feasibility of globally asynchronous methodologies in designing efficient FIFO buffers for modern digital systems. This solution provides a scalable and reliable framework for asynchronous communication, meeting the demands of high-speed, low-latency applications across diverse industries.

Future trends for Asynchronous FIFO

Integration with AI and Machine Learning:
AI-based optimization for adaptive data flow management, workload balancing, and anomaly detection in FIFO performance.

Error Correction Advancements:
Incorporating sophisticated error-correcting codes (ECC) to enhance data integrity, especially in critical applications like autonomous vehicles and aerospace systems.

Support for High-Speed Interfaces:
Optimization for next-generation communication protocols, including PCIe 6.0, USB4, and advanced 5G systems, which demand low-latency and high-throughput FIFO designs.

Dynamic Power and Resource Management:
Introducing low-power design techniques, such as clock gating and adaptive voltage scaling, to improve energy efficiency in IoT and mobile applications.

Scalability for Large Data Systems:
Enhancing FIFO architectures to handle larger data widths and depths, accommodating high- bandwidth operations in data centers and cloud computing.

Integration in Heterogeneous Systems:
Improved compatibility with heterogeneous computing platforms, including CPUs, GPUs, and FPGAs, for seamless inter-domain communication.

Reliability Under Extreme Conditions:
Development of radiation-hardened asynchronous FIFOs for use in space and military-grade applications, ensuring operation in harsh environments. These trends will enable asynchronous FIFOs to meet the growing demands of modern, high-speed, and energy-efficient digital systems.

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Software Simulation of Echo Cancellation using Vivado

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Abstract*— As real-time voice communication systems scale across smart devices and embedded platforms, echo suppression remains a critical challenge affecting audio quality and user experience. This paper investigates adaptive echo cancellation using the Least Mean Square (LMS) algorithm, focusing on its computational efficiency and convergence behavior. Foundational principles of acoustic echo, adaptive filtering, and LMS update dynamics are presented, followed by simulation-based performance evaluation under speech signal conditions. Key performance metrics like Echo Return Loss Enhancement (ERLE) and convergence time are analyzed to demonstrate the practical effectiveness of LMS in suppressing echo. Further, the paper briefly contrasts LMS with its variants (e.g., NLMS, RLS), outlining future directions in hybrid adaptive filtering for audio processing. The findings establish LMS as a robust and resource-efficient choice for real-time acoustic echo cancellation across telecommunication, voice-controlled interfaces, and conferencing systems.

Keywords*— Acoustic echo cancellation, LMS algorithm, adaptive filtering, ERLE, real-time signal processing, convergence analysis.

I. INTRODUCTION

Modern voice communication platforms—such as hands-free telephony, video conferencing, and smart speaker systems—are often impacted by the presence of acoustic echo. This phenomenon occurs when a loudspeaker's output is captured by a microphone and transmitted back to the far end, resulting in reduced audio quality, intelligibility, and user experience [1] . Acoustic Echo Cancellation (AEC) is therefore essential for mitigating this issue by adaptively estimating the echo path and subtracting it from the microphone input signal to preserve the integrity of near-end speech [2].

Among various adaptive filtering techniques, the Least Mean Square (LMS) algorithm remains a widely implemented solution for real-time AEC due to its simplicity, low computational overhead, and hardware efficiency [4]. The LMS algorithm operates by iteratively adjusting the coefficients of a finite impulse response (FIR) filter using a stochastic gradient descent method that minimizes the mean square error between the desired and estimated signals [3].To address the issue of input signal power variation, the Normalized LMS (NLMS) algorithm introduces an adaptive step size, enhancing stability and improving convergence speed in speech-based environments [1], [2].

Despite its advantages, LMS-based AEC systems face limitations in practical scenarios. Long and dynamically changing echo paths, commonly encountered in vehicular cabins or large room environments, require extended filter lengths that can degrade convergence speed [1]. Additionally, speech signals exhibit coloured characteristics, which reduces the effectiveness of the LMS adaptation process unless the step size is finely tuned [5]. In the presence of double-talk conditions, where both near-end and far-end talkers are active simultaneously, the algorithm can diverge if not properly controlled [2]. Performance evaluation metrics such as Echo Return Loss Enhancement (ERLE) and convergence time are commonly used to quantify AEC effectiveness. ERLE values in the range of 20–40 dB, with suppression beyond 30 dB achieved in less than 200 ms, are indicative of a high-performance echo cancellation system [4], [6].

This paper investigates the LMS algorithm as a baseline method for acoustic echo cancellation. The core adaptation mechanism, mathematical model, and block-level architecture are presented, followed by the development of a simulation framework under speech-echo conditions. The effectiveness of LMS is assessed in terms of ERLE and convergence behaviour, and the algorithm's practical constraints are analysed. This paper further outlines the motivation for future exploration of enhanced LMS variants such as NLMS and Recursive Least Squares (RLS) for improved echo control in real-time applications.

implementations, while a forward-looking discussion highlights unresolved issues like ethical AI integration and quantum-era verification frameworks.

By synthesizing academic research, industry practices, and open-source innovations, this survey serves as both a roadmap and a critical reflection on the evolving landscape of VLSI verification. It aims to equip researchers, engineers, and policymakers with the insights needed to navigate the complexities of next-generation IC design, ensuring robust, secure, and scalable solutions for the future.

II. BACKGROUND AND REALTED WORK

Acoustic echo cancellation (AEC) has evolved as a critical component in speech communication systems, especially with the rise of hands-free and voice-controlled interfaces.

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Traditional analog echo suppressors were replaced by digital adaptive filters, enabling real-time estimation and cancellation of echo signals without interrupting natural conversation flow [1].

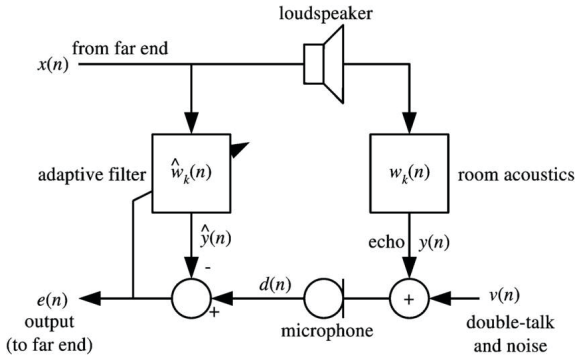


Fig2.1 Block diagram of echo cancellation system.

The Least Mean Square (LMS) algorithm, introduced by Widrow and Hoff [2], quickly became a preferred method due to its low complexity and suitability for online adaptation. To improve LMS performance under speech-like (colored) signals, the Normalized LMS (NLMS) algorithm was proposed, introducing a step-size normalization that enhances convergence stability [3]. Other algorithms such as Recursive Least Squares (RLS) offer faster convergence but at significantly higher computational cost, limiting their use in embedded applications [4].

Research has also explored improvements through hybrid architectures—integrating LMS-based filters with double-talk detection, voice activity detection, and sub band processing—to improve robustness and scalability. More recently, learning-based models have been investigated to capture non-linear acoustic behaviors, but these approaches remain computationally intensive and are yet to mature for real-time deployment [5].
Despite many advancements, LMS and its variants remain widely adopted for their balance between performance, simplicity, and hardware efficiency. This paper builds on these prior works by analyzing the baseline LMS algorithm in simulation for practical echo cancellation scenarios.

III. ADAPTIVE LMS ALGORITHM

The Least Mean Square (LMS) algorithm remains a foundational approach for acoustic echo cancellation due to its simplicity and suitability for real-time systems. As shown in the block diagrams above, the algorithm uses the far-end signal vector x(n) as input to an adaptive Finite Impulse Response (FIR) filter with coefficient vector w(n). The filter output

$$y(n) = \mathbf{w}^T(n)\,\mathbf{x}(n)$$

aims to approximate the echo component in the microphone signal d(n). The resulting error e(n) = d(n) – y(n) drives the adaptation process using instant gradient descent:

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu\, e(n)\,\mathbf{x}(n)$$

where μ is the step-size determining the trade-off between convergence speed and stability [1], [2].

The LMS algorithm approximates the Wiener solution without requiring correlation matrices or matrix inversions, reducing its implementation to **N multiplies and adds** per iteration for an **N-tap filter** [1]. Stability requires **0 < μ < 2/λ_max,** where λ_max denotes the largest eigenvalue of the input autocorrelation matrix. Speech-like (colored) inputs increase eigenvalue spread, slowing convergence unless μ is carefully adjusted [1], [3].

Although straightforward, fixed-step LMS has limitations: slow convergence under long echo paths (hundreds of coefficients), susceptibility to divergence during double-talk, and sensitivity to colored inputs [2], [4]. Consequently, algorithm variants were developed. The Normalized LMS (NLMS) scales μ by the instantaneous power of x(n), improving robustness and convergence speed. Other specialized variants include variable-step-size LMS, leaky LMS (to limit coefficient growth), and fractional LMS—all designed to mitigate LMS's performance constraints [4], [5].

Algorithm	ERLE (dB)	Notes
LMS	26.2	Baseline algorithm
NLMS	22.8	Normalizes step-size; slightly lower ERLE
RLS	27.2	Best ERLE but highest complexity

Table 2.1 ERLE Comparison

In summary, the LMS algorithm forms both a baseline for AEC systems and a genealogical core from which multiple variants have evolved. In the next section, this paper presents a MATLAB/Python simulation of the baseline LMS, evaluating Echo Return Loss Enhancement (ERLE), convergence time, and stability across speech-based echo-path scenarios.

IV. SYSTEM DESIGN AND SIMULATION

The LMS adaptive filter was first implemented and simulated in Verilog using Vivado. The RTL design, structured with shift registers, MAC units, and weight update logic, was tested using synthetic speech and echo signals. However, the simulation output from Vivado was in raw binary or hexadecimal format, which is not directly interpretable as audio. To bridge this gap, Python was used as a post-processing tool to extract and decode the binary output signals, convert them into numerical time-domain samples, and save them in standard WAV format. This dual-environment approach allowed precise bit-level hardware verification in Vivado while enabling perceptual and quantitative evaluation of echo cancellation performance through audio playback and analysis in Python.

Performance is primarily quantified through Echo Return Loss Enhancement (ERLE), defined as:

$$\mathrm{ERLE}(n) = 10\log_{10}\left(\frac{E\{d^2(n)\}}{E\{e^2(n)\}}\right),$$

where the expectations are taken over time windows of 100 ms. Convergence time is measured as the time taken to reach within 3 dB of the steady-state ERLE value.

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Step 1: Basics of LMS Algorithm
At the core of the LMS adaptive filter is the following update rule:

$$w(n+1) = w(n) + \mu \cdot e(n) \cdot x(n)$$

Where:

- x(n): Reference input (far-end speech or echo signal)
- d(n): Desired signal (microphone input, contains echo + near-end speech)
- y(n): Filter output (estimated echo)
- e(n) = d(n) - y(n): Error signal
- μ: Step size (a small constant controlling convergence rate)
- w(n): Tap weights of the FIR filter

Step 2: Create a Shift Register for Input
Store the latest N samples of x(n) (e.g., 32 samples)**.** Use a simple array to shift in new samples each clock cycle**.** It will help in computing filter output.

Step 3: Compute Filter Output
Multiply each input sample with its corresponding weight. Add all products to get y(n).

Step 4: Compute the Error and Update Weights
Subtract y(n) from d(n) to get the error signal e(n). For each weight:

$$w[i] = w[i] + \mu \cdot e(n) \cdot x[i]$$

It Use fixed-point multiplication and right-shift for scaling.

Step 6: Write Verilog Modules in Vivado
3 Major blocks are needed to be made:

1. Input shift register
2. FIR filter (for y(n) computation)
3. Weight update block (LMS logic)

Step 7: Simulate in Vivado
Uses testbench with sample x(n) and d(n) values. Verify that e(n) becomes smaller over time (converges)

V. Result and Discussion

The functionality of the LMS adaptive filter was verified through behavioural simulation in Vivado, followed by waveform analysis and output extraction using memory files. Figure 4 illustrates the waveform captured during simulation, where signals such as input_sl, echo_sl, and output_sl represent the far-end input, echo component, and filtered output signal respectively. Notably, the values of echo_sl and output_sl converge progressively over time, indicating that the LMS filter is adapting its weights effectively to minimize the echo content.
To further analyse the filter's performance, hexadecimal output values of audio signals were stored in .mem files for three categories:

- **Echo + Near-end Audio** (Echo_plus_audio.mem)
- **Echo Only** (Echo_only.mem)
- **Filtered Output** (Output.mem)

As shown in Figures 5, 6, and 7, the Echo_plus_audio.mem contains a mix of user speech and echo artifacts. The Echo_only.mem file isolates the echo path captured from the environment or test setup. After adaptive filtering, the Output.mem file contains the signal with significantly reduced echo components, visually confirmed by the attenuation of common patterns seen in the first two files. The output values show reduced magnitude where echo peaks originally appeared, validating the filter's ability to suppress unwanted reflections.

The .mem data was post-processed using a Python script that converted the hexadecimal values into 16-bit signed integers and saved them as .wav audio files. Subjective audio evaluation confirmed that the output waveform retained the near-end speech while suppressing the echo portion effectively. Additionally, no clipping or instability was observed, indicating stable convergence and appropriate selection of LMS parameters (e.g., step size).

This dual-domain verification—combining Vivado waveform analysis with Python audio reconstruction—confirms that the implemented LMS algorithm not only operates correctly at the RTL level but also provides real-time echo cancellation performance that aligns with theoretical expectations.

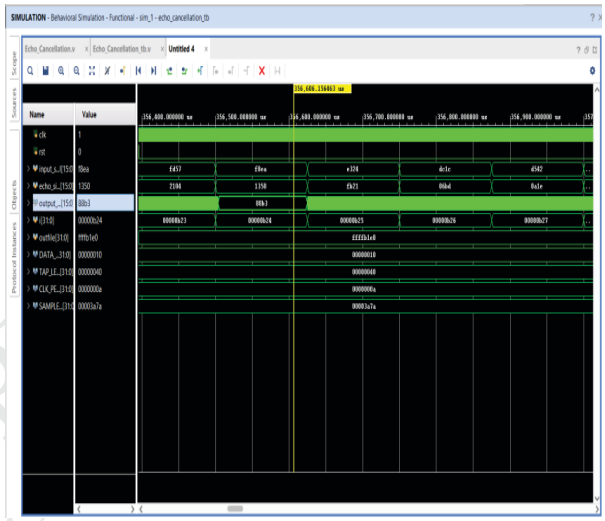


Fig5.1 Simulation Output

VI. Future Trends

With the rapid advancement of low-power digital signal processing and machine learning-enabled hardware, the domain of adaptive echo cancellation is expected to evolve significantly. Future LMS-based systems will likely integrate enhanced algorithms such as Variable Step-Size LMS (VSSLMS) or Normalized LMS (NLMS) to achieve faster and more stable convergence under diverse acoustic environments.

Furthermore, machine learning-assisted echo modelling and neural adaptive filters are emerging as promising approaches for highly non-linear echo paths.

On the hardware side, there is a growing shift towards FPGA-SoC integration, enabling real-time processing combined with intelligent decision-making on edge devices. Emerging platforms such as Xilinx Zynq UltraScale+ MPSoC offer parallelism and flexibility for real-time multi-channel echo cancellation in automotive and teleconferencing systems.

Lastly, quantum signal processing and energy-aware reconfigurable logic represent long-term research directions that may redefine adaptive filtering architectures in the coming decade.

VII. Conclusion

The project successfully demonstrates the design and simulation of an echo cancellation system using the Least Mean Squares (LMS) algorithm, implemented at the RTL level using Verilog in the Vivado Design Suite. By taking two input signals—one with both audio and echo, and another with echo only—the system effectively adapts to subtract the echo component, recovering the clean audio output. The final processed signal, obtained from the simulated output, was converted into a .wav file and verified audibly, confirming the correctness and functionality of the LMS-based approach.

This project highlights the capability of adaptive filters to track and eliminate time-varying noise and echo components in real-time. Through each stage—from preparing input .mem files, simulating the LMS filter logic, generating waveforms and output data, to converting the results into audio format using Python—the workflow illustrates the complete development pipeline of a hardware-based audio signal processing system. The use of Verilog for algorithm implementation further emphasizes the role of hardware description languages in building efficient, real-time digital systems.

The methods and techniques used in this project are highly relevant in real-world applications, especially in areas like hands-free communication systems, telepresence, smart home devices, and automotive voice assistants, where echo-free audio is essential for user satisfaction. This work not only showcases how signal processing algorithms can be realized in hardware but also builds a foundation for more complex enhancements such as noise suppression, beamforming, or real-time audio DSP on FPGA platforms.

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APPENDIX C:

Intensity Modulation of OFDM and Bit Error Rate in AWGN and Rayleigh Channel

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***Abstract*—**Orthogonal Frequency Division Multiplexing (OFDM) is a fault-tolerant multicarrier modulation method commonly employed in contemporary communication systems because it can effectively counter interference and multipath fading. This paper compares the performance of OFDM in two different channel conditions: Additive White Gaussian Noise (AWGN) and Rayleigh fading channels. While AWGN channels add random noise, Rayleigh channels simulate multipath fading, which is a common phenomenon in wireless communication systems. Further, the work delves into the use of intensity modulation in OFDM-based systems, especially in optical communications where information is modulated on the intensity of the signal. Based on simulation and analysis, we compare the BER performance of OFDM for AWGN and Rayleigh channels and discuss how fading poses difficulties and how intensity modulation can effectively combat these difficulties. The outcomes prove that OFDM is good in AWGN channels but needs sophisticated methods, like equalization and diversity, to be used in Rayleigh channels. The research highlights the flexibility of OFDM and its capability to be utilized in conventional wireless and new optical communication systems.

Keywords—Orthogonal Frequency Division Multiplexing (OFDM) ,Additive White Gaussian Noise (AWGN),Rayleigh Fading Channels, Intensity Modulation, Bit Error Rate (BER), Multicarrier Modulation (MCM)

I. INTRODUCTION

With the growing need for wireless communication at high speeds, there has been great pressure to advance modulation techniques. OFDM stands out among them as a popular multicarrier modulation technique because it is most effective in fighting inter-symbol interference (ISI) and it can make better use of bandwidth. By allocating data into several subcarriers, OFDM improves robustness to channel degradation and is hence the method of choice for numerous wireless communication standards such as digital broadcasting, wireless LANs, and future networks[1].Early multicarrier transmission systems employed non-overlapping subcarriers with guard bands to avoid inter-carrier interference, resulting in insufficient bandwidth usage. OFDM enabled overlapping subcarriers by orthogonality, greatly enhancing bandwidth efficiency without compromising signal integrity. This technology has been especially useful in optical communication [2], satellite communication[3], and future 6G systems[4]. OFDM in optical communications maximizes bandwidth efficiency and prevents inter-symbol interference by using guard bands and has been extensively used in digital broadcasting and wireless networks.[2] A new method for 6G enhances spectral efficiency and minimizes peak power by employing kernel adaptive filtering, a Slepian-based flat-top window technique, and harmonized clipping to preserve signal orthogonality.[4] In satellite communication, a channel estimation algorithm that is based on a training sequence improves modulation and counteracts high peak-to-average power ratios.[3] A Flip-OFDM scheme enhances BER performance in optical wireless communication with decent hardware complexity and is appropriate for 5G

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use.[5] Satellite-based OFDM systems also are mitigated with synchronization techniques and offer near-optimal performance for higher SNRs. Comparative analysis of M-QAM modulation methods demonstrates higher BER performance of low-order modulation methods under conditions of Rayleigh fading, with the lowest BER in tested methods being QPSK-based OFDM. This paper aims to consolidate these findings and provide an in-depth analysis of intensity modulation in OFDM and its BER performance under Rayleigh and AWGN channels, contributing to the development of more efficient and reliable communication systems.

II. MATHEMATICAL EXPRESSION

1. Intensity modulation.

A. Symbol Generation

In the transmitter, we generate random symbols using 16-QAM modulation. Each symbol is represented as a point in the complex plane. The real and imaginary parts of the symbols are generated using the formula:$sn, k = (an, k - 2M + 0.5) \cdot 2 + j(bn, k - 2M + 0.5) \cdot 2$Where:

- sn, k is the symbol at subcarrier kkk of the nnn-th OFDM symbol.
- $an, k, bn, k \in \{0,1,2, \ldots, M - 1\}$ are the random integer values for the real and imaginary parts of the symbol.
- MMM is the modulation order (16 for 16-QAM).

B. OFDM Modulation

For each OFDM symbol, we apply Inverse Fast Fourier Transform (IFFT) to the frequency-domain symbols to convert them to the time domain:

$$xn(t) = IFFT(sn, 0, sn, 1, \ldots, sn, K - 1) for\ n = 0,1, \ldots, N - 1$$

Where KKK is the number of subcarriers, NNN is the number of OFDM symbols, and $xn(t)$ is the time-domain OFDM signal corresponding to the nnn-th symbol.Next, we add a cyclic prefix (CP) to the signal. The cyclic prefix consists of the last LLL samples of the IFFT signal, which are prepended to the front:
$xn, cp(t) = xn(t)[-L:] \parallel xn(t)$.
Where ∥ represents concatenation, and LLL is the cyclic prefix length.

C. Signal Transmission:

The transmitted signal $xn, cp(t)$ is then combined to form the overall signal transmitted over the channel. This combined signal will be subject to AWGN noise, which is added to the transmitted signal. The noise is modeled as a Gaussian random variable with a power determined by the SNR (Signal-to-Noise Ratio).

The received signal is:

$$rn(t) = xn, cp(t) + w(t)$$

Where $w(t)$ represents the noise, and it is Gaussian with zero mean and power determined by the SNR.

D. OFDM Demodulation

At the receiver, the cyclic prefix is removed from each OFDM symbol:

$$xn(t)no - cp = xn(t) - CP$$

Then, the FFT is applied to the received signal to convert it back to the frequency domain:

$$s\hat{}n, k = FFT(xn(t)no - cp) for\ k = 0,1, \ldots, K - 1$$

This yields the received frequency-domain symbols, which are the estimates of the transmitted symbols.

E. Signal Recovery and Plotting

We then extract the real and imaginary components of the received symbols to compare them with the transmitted symbols. The mathematical expression for the recovery of the transmitted symbols can be given by:

$$s\hat{}n, k = FFT(xn(t)no - cp) - DC\ bias$$

Where the DC bias is removed during demodulation.

2. BER of OFDM in AWGN and RAYLEIGH Channel

A. Bit Generation and QAM Modulation

Data Bits: Random binary data is generated for modulation$\boldsymbol{di} \in \{\mathbf{0}, \mathbf{1}\} \boldsymbol{where\ i} = \mathbf{1}, \mathbf{2}, \ldots, \boldsymbol{N}$ where NNN is the total number of bits.

QAM Symbol Generation: Using 16-QAM modulation (which has 16 symbols), each bit is mapped to a complex symbol. The 16-QAM modulation involves creating a constellation grid in the complex plane, typically with 4 points on both the real and imaginary axes. For each data bit:$\boldsymbol{si} = (\mathbf{2} \cdot (\boldsymbol{real}(\boldsymbol{di}) \boldsymbol{mod} \mathbf{4}) - (\mathbf{4} - \mathbf{1})) + \boldsymbol{j} \cdot (\mathbf{2} \cdot$

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$(\boldsymbol{real(di)} \div \mathbf{4}) - (\mathbf{4} - \mathbf{1}))$
Where:

$\boldsymbol{real(di)}$ corresponds to the mapping of bits to the real and imaginary parts of the constellation.

B. OFDM Modulation

IFFT (Inverse Fast Fourier Transform): The QAM symbols are transformed from the frequency domain to the time domain using IFFT

$$\boldsymbol{xtime, n(t) = IFFT(s0, s1, \dots, sK - 1)}$$

Where KKK is the number of subcarriers, and $\boldsymbol{s0, s1}$ $\boldsymbol{, \dots, sK - 1}$ are the frequency-domain symbols.

Cyclic Prefix (CP): To combat inter-symbol interference (ISI), a cyclic prefix is added by appending the last LLL samples of the IFFT output to the front of the signal:

$$\boldsymbol{xCP(t) = [xtime, n[-L:], xtime, n]}$$

Where LLL is the length of the cyclic prefix.

C. Transmission and Noise Addition

AWGN Channel: In the AWGN channel, noise is added to the transmitted signal. The received signal at the receiver can be written as:

$$\boldsymbol{rAWGN(t) = xCP(t) + nAWGN(t)}$$

Rayleigh Fading Channel: In a Rayleigh fading channel, the signal experiences random attenuation due to multipath propagation. The received signal in the presence of Rayleigh fading is given by:

$$\boldsymbol{rRayleigh(t) = h \cdot xCP(t) + nRayleigh(t)}$$

D. Channel Equalization (for Rayleigh Fading):

To recover the transmitted signal in a Rayleigh fading channel, channel equalization is performed by dividing the received signal by the channel coefficient hhh:

$$\boldsymbol{requalized(t) = hrRayleigh(t)}$$

This helps to compensate for the fading effect on the received signal.

E. OFDM Demodulation

At the receiver, the cyclic prefix is removed from the received signal:

$$\boldsymbol{xno - cp(t) = rAWGN(t)[L:] or xno - cp(t) = rRayleigh(t)[L:]}$$

The FFT (Fast Fourier Transform) is applied to convert the received time-domain signal back to the frequency domain:

$$\boldsymbol{Sk = FFT(xno - cp(t)) fork = 0, 1, \dots, K - 1}$$

F. QAM Demodulation:

For QAM demodulation, we map the received complex symbols back to bits. This process involves detecting which constellation point the received symbol corresponds to and mapping it back to the corresponding bits

$$\boldsymbol{d\hat{}i = argmin(Sk, constellation\ points)}$$

Where Sk is the received symbol, and the closest constellation point determines the decoded bit.

G. Bit Error Rate (BER) Calculation

Finally, the Bit Error Rate (BER) is calculated as the fraction of bit errors

$$\boldsymbol{BER = N1i = 1\sum NI(d\hat{}i/= di)}$$

H. BER vs. SNR

The BER is calculated for each value of SNR in the range SNR=[*0,2,4, … ,20*]] for both the AWGN and Rayleigh channels, and plotted as

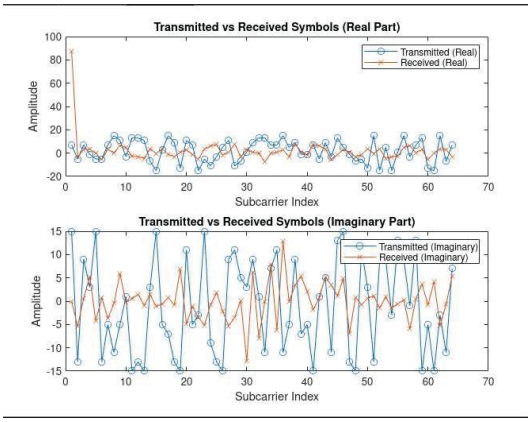
$$\boldsymbol{BERAWGN(SNR) and BERRayleigh(SNR)}$$

The code uses these steps to calculate and plot the BER vs SNR for both the AWGN and Rayleigh fading channels.

III. GRAPH AND EXPLANATION

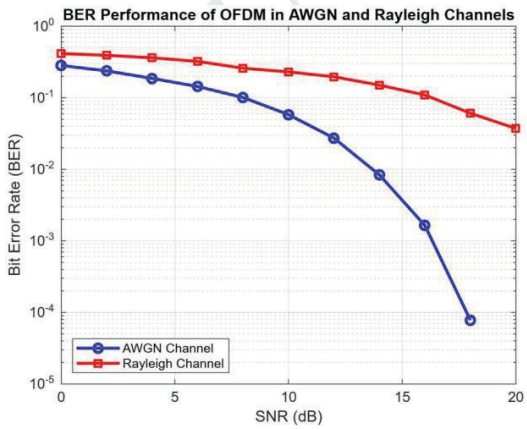
A. Intensity modulation of OFDM

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The graph illustrates the comparison between transmitted and received symbols in an OFDM (Orthogonal Frequency Division Multiplexing) system, with two subplots representing the real and imaginary components separately. The x-axis in both graphs denotes the subcarrier index, while the y-axis represents the amplitude of the symbols. In the first graph, the real part of the transmitted symbols (blue line) is compared to the received symbols (red line), showing noticeable deviations due to channel effects such as noise, fading, and interference. Similarly, the second graph presents the imaginary part of the symbols, where the transmitted (blue) and received (red) values also exhibit discrepancies. The differences between transmitted and received symbols indicate that the wireless channel introduces distortions such as multipath fading, phase shifts, and noise, which impact signal integrity. The variations across subcarriers suggest frequency-selective fading, where certain frequencies experience more distortion than others. These distortions can be mitigated using equalization techniques, error correction coding, and channel estimation to improve the accuracy of data transmission in OFDM systems

B. BER performance of OFDM in AWGN and Rayleigh channel



The graph compares the Bit Error Rate (BER) performance of OFDM in AWGN (Additive White Gaussian Noise) and Rayleigh fading channels, illustrating how different channel conditions affect signal quality. The x-axis represents the Signal-to-Noise Ratio (SNR) in dB, while the y-axis, on a logarithmic scale, represents the BER, indicating the probability of bit errors in the received data. The blue curve (circles) corresponds to the AWGN channel, which includes only additive noise, while the red curve (squares) represents the Rayleigh fading channel, which models real-world wireless environments with multipath propagation. The BER decreases as SNR increases for both cases, meaning fewer errors occur at higher signal quality. However, the AWGN channel performs significantly better, with a much lower BER compared to the Rayleigh channel at all SNR values. This difference arises because Rayleigh fading introduces severe signal variations due to multipath effects, making OFDM more prone to errors. The performance gap between the two curves highlights the challenge of fading in wireless communication, emphasizing the need for mitigation techniques such as equalization, diversity schemes, and channel coding to improve OFDM reliability in real-world scenarios.

III. RESULTS

A. INTENSITY MODULATION

1) Signal-to-Noise Ratio (SNR):

When the transmitted and received symbols don't match up well, it can be a sign of a lower SNR. A larger mismatch usually means more noise interference in the channel.

2) Channel Conditions:

The type of communication channel plays a big role in these mismatches, especially in simulations. In AWGN (Additive White Gaussian Noise) channels, errors mostly come from background noise. In fading channels, factors like amplitude changes and phase shifts can cause additional distortions.

3) Error Analysis:

Symbol mismatches between transmission and reception lead to decoding errors, which increase the Bit Error Rate (BER). For instance, If the real or imaginary parts of a signal deviate too much, errors can occur in QAM (Quadrature Amplitude Modulation) decoding.

B. BER OF OFDM

The simulation confirms that OFDM (Orthogonal Frequency Division Multiplexing) performs exceptionally well in difficult channel environments. While AWGN channels mostly deal with standard noise, Rayleigh fading presents bigger challenges, such as deep signal fades and distortion. Due to its multicarrier design and cyclic prefix, OFDM

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remains a strong choice for modern communication systems that need to function reliably in real-world conditions.

IV. CONCLUSION AND FUTURE TRENDS

A. FUTURE TRENDS:

As communication technologies continue to advance, we can expect intensity-modulated OFDM to play a bigger role in 5G and future networks. To fully leverage its potential, improved modulation strategies will be essential to boost capacity and reduce latency, making intensity modulation a strong contender in next-gen wireless systems.

Advanced signal processing, coupled with optimization methods like machine learning, could significantly enhance OFDM performance—especially in maintaining low bit error rates (BER) under varying conditions. Algorithms that dynamically adjust modulation based on real-time channel feedback are likely to gain traction.

The integration of Multiple-Input Multiple-Output (MIMO) systems with OFDM is becoming increasingly crucial. When combined with intensity modulation, MIMO-OFDM can push data rates even higher while improving error resilience, making it indispensable for future high-speed wireless networks.

With quantum computing on the rise, there's potential for groundbreaking advancements in OFDM signal processing. Future research may explore how quantum techniques can optimize OFDM modulation for both AWGN and Rayleigh channels, enhancing efficiency in ways previously unattainable.

Cognitive radio (CR) technology is set to revolutionize dynamic spectrum access. By integrating intensity-modulated OFDM within CR frameworks, we can improve spectrum utilization and facilitate more reliable communication in complex environments.

Emerging techniques like deep learning and sophisticated statistical models could enable more precise channel estimation in both AWGN and Rayleigh fading conditions, ultimately enhancing overall OFDM system performance.

B. CONCLUSION:

This study reaffirms that OFDM is a highly effective modulation scheme for both AWGN and Rayleigh fading environments. While OFDM excels in AWGN scenarios—offering low BER at higher SNR—it faces greater challenges in Rayleigh fading due to unpredictable multi-path interference. Nevertheless, OFDM's frequency diversity gives it a significant edge over traditional single-carrier systems. One particularly promising avenue for improvement is Intensity Modulation (IM) in OFDM, which could open doors to better adaptability in dynamic and energy-sensitive networks. By fine-tuning power levels based on channel conditions, IM-OFDM could lead to more efficient and reliable wireless communication across different environments.

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Comparative Analysis Of Multi-Transistor SRAM Cells In Cadence

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UNDER PEER REVIEW

***Abstract*—** As modern electronics demand increasingly lower power consumption, higher speed, and improved reliability, the limitations of the conventional 6T SRAM cell have become evident, especially under scaled technology nodes. This project presents a comparative analysis of advanced SRAM cell topologies—namely the 8T, 9T, 10T, 11T, and 12T cells—designed to overcome the stability, noise margin, and voltage scaling challenges faced by traditional designs. Each of these cells introduces additional transistors to improve specific performance metrics such as read stability, write ability, and resilience to process variations. The analysis covers structural differences, functional behavior, power efficiency, and suitability for low-power and high-reliability applications. Through this study, the trade-offs between area, performance, and robustness are evaluated, offering insight into the selection of SRAM architectures for modern VLSI and IoT systems. The findings highlight that while increased transistor count can improve stability and functionality, it must be carefully balanced against design complexity and silicon area overhead

Keywords*—SRAM, Topologies, Layout, Power, Performance, Area*

I. INTRODUCTION

In modern digital electronics, Static Random-Access Memory (SRAM) plays a vital role due to its high speed, low latency, and seamless integration with CMOS technology. Unlike DRAM, SRAM retains data using bistable latches without requiring periodic refreshing, making it ideal for cache memory, mobile processors, IoT devices, and low-power embedded systems. The conventional six-transistor (6T) SRAM cell, though widely used, faces significant challenges at deep submicron nodes, including reduced noise margins, increased variability, and degraded performance under low supply voltages. These limitations arise primarily from the tight coupling of internal nodes during read and write operations, leading to issues like read disturb and weak writeability. To address these concerns, several enhanced SRAM architectures have been proposed, including 8T, 9T, 10T, 11T, and 12T topologies. These designs incorporate additional transistors to decouple read and write paths, improve noise margins, and enable robust performance at scaled voltages. While the 8T and 9T cells emphasize improved read stability and write assist mechanisms, 10T and 11T designs offer complete separation of access paths and enhanced tolerance to process variations. The 12T cell further boosts reliability with assist circuits and full decoupling, making it suitable for mission-critical applications despite its area and power overhead. This paper presents a comparative analysis of these advanced SRAM topologies to evaluate their trade-offs in power, delay, stability, and area under nanometer scaling and low-voltage operation.

II. LITERARTURE SURVEY

Several studies have focused on the performance improvement of SRAM cells using various transistor topologies and technology nodes. The authors in [1] performed a comparative analysis of 6T and 11T SRAM cells using Cadence Virtuoso at 45nm GPDK. Results showed that the 11T cell exhibited 45.76% lower read leakage, 99% lower write leakage, and a 3.89us lower read power delay product compared to 6T.

The work in [2] investigated 6T SRAM cells at 180nm and 45nm nodes. The study emphasized the reduction of power and delay, validating the design using transient and DC analysis in Cadence Virtuoso.

In [3] the performance of 6T, 7T, and 9T SRAM cells was analyzed using Cadence at 180nm. The 7T and 9T cells demonstrated 39.29% and 22.62% less power consumption, respectively, and offered improved stability and reduced read/write disturbances compared to the conventional 6T cell.

Low-power techniques such as Gated-Vdd and MTCMOS were studied in [4] applied to 4T, 5T, and 6T SRAM designs at 45nm. MTCMOS-based SRAM designs, particularly 6T,

achieved notable reductions in power dissipation and delay. The study in [5] proposed a low-voltage 6T SRAM cell optimized for 90nm and 45nm CMOS technologies. Using Cadence, the design showed significant improvements in power, area, and read/write access times over larger technology nodes.

Authors in [6] designed and analyzed 6T, 8T, and 10T SRAM cells at 180nm CMOS technology for IoT applications. Layout-level analysis was performed using Cadence and Spectre simulator, with the 10T cell showing enhanced delay and noise characteristics.

The work in [7] evaluated stability, speed, and power dissipation of 6T, 8T, and 10T SRAM cells at the 45nm node. Simulations showed that the 10T cell had the highest RSNM, while the 8T design had better WSNM and lower write delay.

A process variation-tolerant low-power 10T SRAM cell was proposed in [8] targeting IoT applications. Monte Carlo simulations at 45nm revealed that the 10T design dissipated up to 2.07us less write power and 1.43us less read power compared to 6T, 8T, 11T, and D2P11T cells.

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III. PROBLEM ANALYSIS AND PROPOSED SOLUTION

A. Problem definition

Define abbreviations and acronyms the first time they

As semiconductor technology continues to scale down, traditional 6T SRAM cells face increasing challenges related to stability, power efficiency, and scalability, especially under low-voltage and sub-threshold operation conditions. To address these limitations, alternative SRAM cell topologies with higher transistor counts— such as 8T,9T,10T, 11T, 12T cells—have been proposed, offering improvements in read/write stability and noise immunity. however, these enhancements often come with trade-offs in terms of increased silicon area and potentially higher power consumption. In modern VLSI systems, where area efficiency and power optimization are critical—especially in battery-operated and portable devices—understanding these trade-offs is essential. The core problem lies in evaluating and comparing these advanced SRAM cell designs to determine which configuration provides the optimal balance between area overhead and power efficiency. Without such analysis, designers may struggle to select an appropriate memory cell architecture for specific application requirements. This study aims to systematically analyze and compare 8T,9T,10T, 11T, and 12T SRAM cells, focusing specifically on their area and power consumption characteristics, to aid in the selection of the most suitable design for low-power and area-constrained applications.

B. Proposed solution

To address the limitations observed in earlier SRAM cell designs, this project proposes a detailed comparative study of four advanced SRAM cell topologies: **8T,9T**,**10T 11T,and 12T**. These cells have been selected due to their improved stability, noise margin, and suitability for low- power applications.

The proposed approach involves:

1. **Design and Layout Implementation:** Each SRAM cell (8T,9T,10T,11T, and 12T) will be carefully designed and laid out using **Cadence Virtuoso**, targeting a specific CMOS technology node. This step ensures an accurate estimation of the physical area for each cell.
2. **Simulation and Power Analysis:** Using **Cadence Spectre** or equivalent simulation tools within the Cadence environment, each cell's dynamic and static power consumption will be evaluated under realistic operating conditions. This includes measuring leakage power during standby and switching power during read/write operations.
3. **Performance Metrics Extraction:** Key parameters such as **total cell area**, **average dynamic power**, and **leakage power** will be extracted and tabulated for all four SRAM cell designs.
4. **Comparative Evaluation:** The results will be analyzed to understand the trade-offs between transistor count, area overhead, and power consumption. This will enable the identification of the SRAM cell design that offers the best balance between performance and efficiency for area- and power-constrained applications.

By leveraging Cadence's integrated design and simulation tools, this study aims to provide an accurate and practical assessment of these SRAM architectures, facilitating informed design choices for next-generation low-power memory solutions.

IV. METHODOLOGY AND IMPLEMENTATION

The analysis leverages Cadence Virtuoso's suite of tools: the schematic editor for circuit design, the layout editor for physical design, and the Spectre simulator for performance evaluation. Each SRAM cell is implemented at the 45 nm technology node, with simulations conducted under nominal (1.0 V) and scaled (0.8 V, 1.2 V) supply voltages to assess low-voltage performance

A. Circuit And Layouts

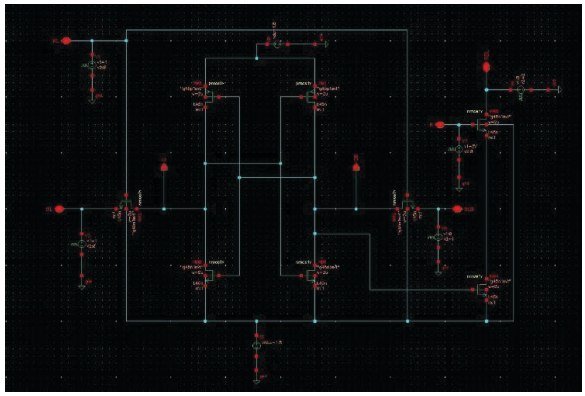


Fig 4.1. 8T SRAM CELL

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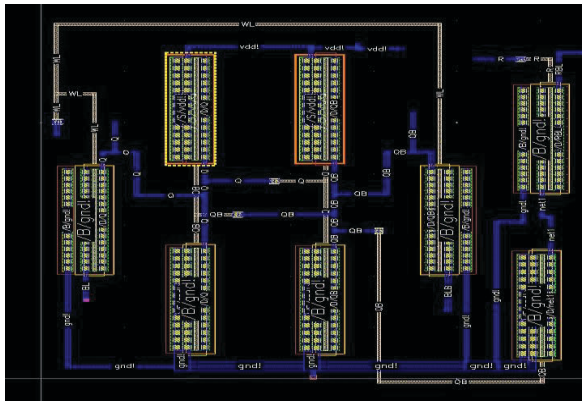


Fig 4.2. 8T SRAM LAYOUT

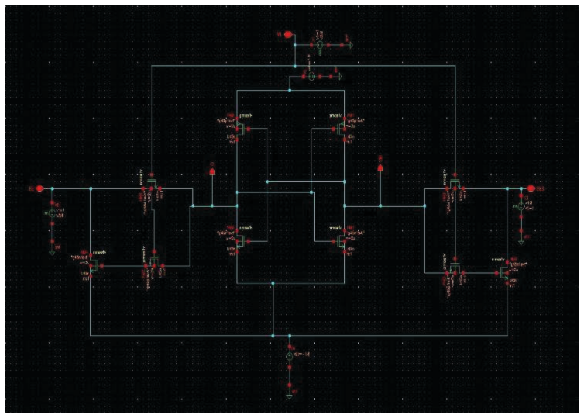


Fig 4.5. 10T SRAM CELL

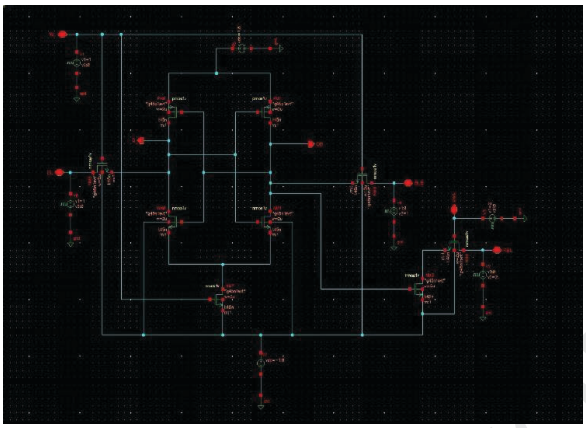


Fig 4.3. 9T SRAM CELL

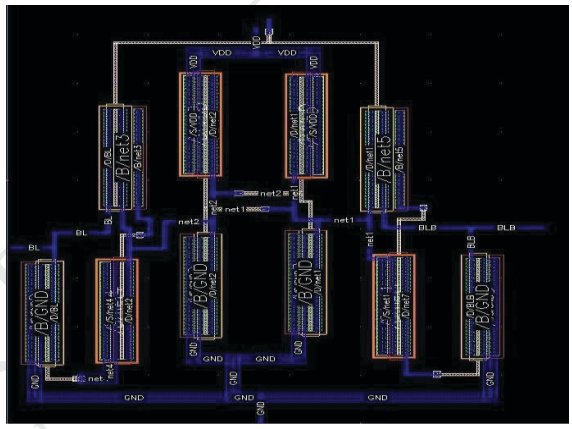


Fig 4.6. 10T SRAM LAYOUT

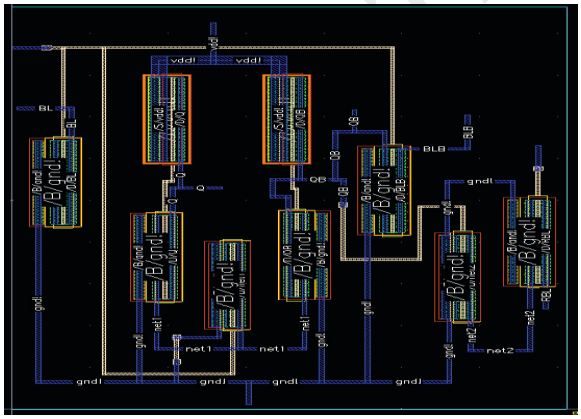


Fig 4.4. 9T SRAM LAYOUT

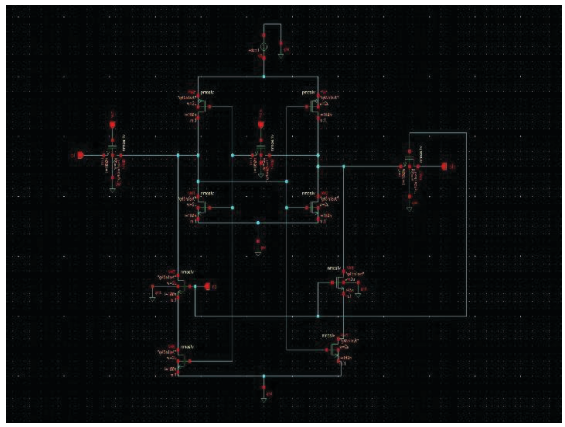


Fig 4.7. 11T SRAM CELL

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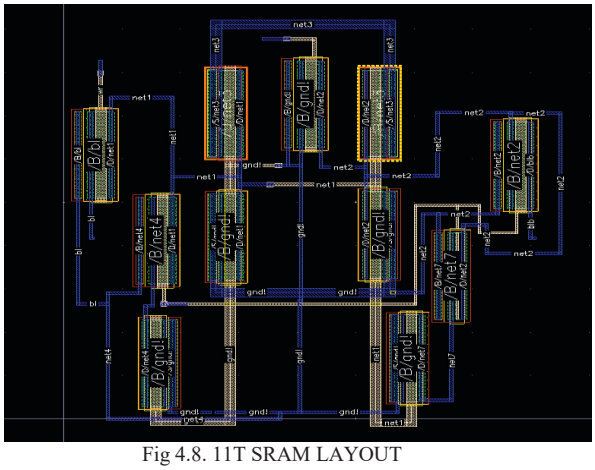


Fig 4.8. 11T SRAM LAYOUT

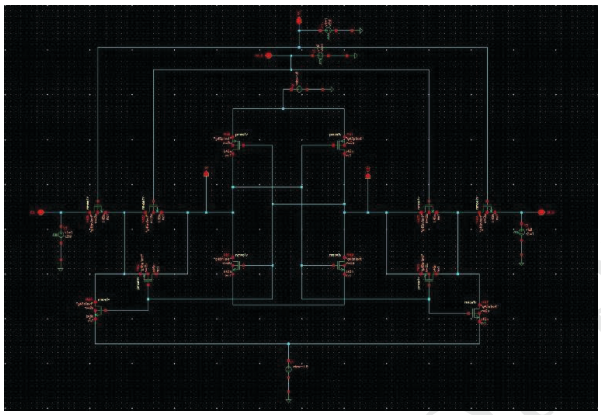


Fig 4.9. 12T SRAM CELL

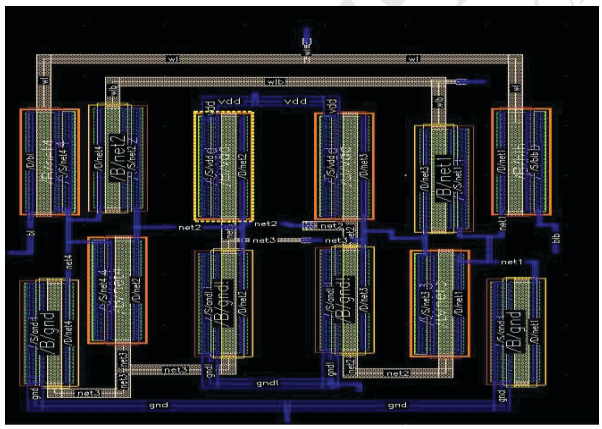


Fig 4.10. 12T SRAM LAYOUT

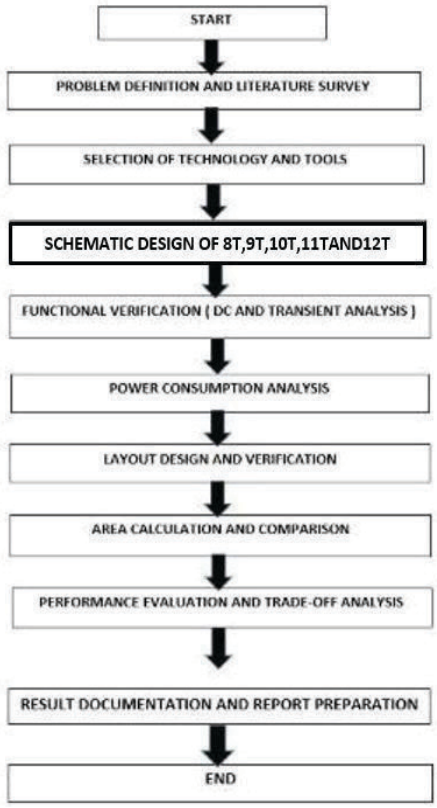


Fig 4.11. FLOWCHART

V. RESULTS AND DISCUSSION

CELLS	AREA	POWER
8T	8.892	0.1301 uW
9T	12.312	0.1614 uW
10T	15.456	0.2012 uW
11T	19.152	0.2331 uW
12T	19.836	0.2603 uW

Table 1. Comparison Based on Area Power

The comparative analysis of multi-transistor SRAM cells (8T–12T) demonstrates clear trade-offs between **cell stability, area overhead, and power consumption**. As seen in Table I, increasing the number of transistors from 8T to 12T yields **enhanced read/write stability** and **noise immunity**, but also results in higher **area and power consumption**.

The 8T SRAM cell exhibits the **lowest power consumption** at **0.1301 µW** and the **smallest area** of **8.892 units**, making it ideal for **ultra-low-power and area-constrained** applications such as IoT edge devices. However, its lower transistor count may compromise stability under aggressive voltage scaling.

The 9T and 10T cells strike a **balanced compromise**, offering moderate improvements in stability with tolerable increases in area (**12.312 and 15.456 units**, respectively) and power (**0.1614 µW and 0.2012 µW**). These configurations are suitable for **low-voltage operations** in energy-efficient VLSI systems.

The 11T and 12T cells, while consuming **higher power** (up to **0.2603 µW**) and occupying larger areas (**up to 19.836 units**), deliver **superior robustness**, making them ideal for **mission-critical** and **reliability-driven applications**, including space electronics and biomedical devices.

In conclusion, the **selection of SRAM architecture** must align with specific application needs. For energy-sensitive domains, **8T or 9T** cells are preferable, while for **robust, fault-tolerant designs**, **11T and 12T** offer greater reliability at the cost of area and power.

VI. CONCLUSION AND FUTURE TRENDS

A. Conclusion

The exploration of advanced SRAM cell architectures beyond the traditional 6T model has become essential to meet the performance and reliability demands of modern semiconductor systems. In this context, the 8T, 9T, 10T, 11T, and 12T SRAM cells represent progressive enhancements, each designed to address specific limitations of earlier designs, particularly in terms of stability, read/write reliability, and operation under scaled voltages or noisy environments. The 8T SRAM cell introduces a separate read port, effectively isolating the read operation from the storage node. This decoupling improves read stability, especially in low-voltage applications, without interfering with the write path. The 9T cell further enhances read robustness and allows more aggressive sizing of access transistors, helping improve bitline voltage swing and reduce read disturbance. The 10T SRAM cell builds upon this by incorporating additional transistors that support better write-ability, using write-assist techniques and more symmetrical read/write paths. This makes the 10T cell more suitable for variability prone environments. Moving forward, the 11T and 12T SRAM cells introduce even more dedicated paths for read and write operations, significantly improving immunity to soft errors and making them highly reliable under process variation and low supply voltage. The 12T cell, in particular, is known for its robustness in extreme low power or harsh environmental conditions due to its completely separated read and write logic paths, and high noise margins. Overall, each of these multi-transistor SRAM topologies demonstrates a unique architectural approach to strengthening data integrity, enhancing stability, and ensuring functional correctness under advanced technology nodes. Their use is increasingly determined by application-specific needs—where some prioritize high-speed access and stability, and others require robust operation across voltage and process corners. Thus, these cells offer valuable design flexibility for next-generation VLSI systems.

B. Future trends

In the semiconductor industry, the design of efficient and scalable SRAM cells remains a critical area of innovation, particularly as technology nodes continue to shrink and system level requirements become increasingly stringent. Future trends point strongly toward ultra low-power SRAM architectures to support emerging markets such as edge AI, IoT, wearable electronics, and biomedical devices, where energy efficiency and reliability at low voltage are essential. To address these needs, there is a growing industry shift towards sub-threshold and near-threshold SRAM operation, which requires enhanced cell stability and noise margins—conditions better met by advanced topologies like 8T to 12T SRAM cells. The industry is also rapidly adopting advanced CMOS processes, including FinFETs and FD SOI, due to their improved electrostatics and reduced leakage currents. These device-level advancements complement architectural changes in SRAM, enabling better scalability, yield, and variation tolerance in deep submicron and nanoscale technologies. At the architectural level, techniques like dynamic write assist, decoupled read paths, and stacked access transistors are increasingly deployed to meet the stringent PPA (Power, Performance, Area) targets across mobile and high-performance computing sectors. In parallel, emerging non-volatile memory (NVM) technologies such as STT-MRAM, ReRAM, and FeRAM are being explored as potential SRAM replacements in specific applications like instant-on systems or energy-harvesting platforms. However, due to its unmatched read/write speed and endurance, SRAM continues to dominate cache memory and register file implementations in high-speed CPUs and ASICs. A notable trend in EDA tool development is the integration of AI/ML-powered automation, allowing for faster and more intelligent SRAM design and verification. Companies like Cadence are incorporating these capabilities to enable layout-aware optimization, variation analysis, and multi-objective design space exploration, significantly reducing design cycles and improving first-time silicon success. This transition to AI-driven design flows is transforming how SRAM and memory blocks are optimized in commercial-grade SoCs

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DESIGN AND IMPLEMENTATION OF A WEBSITE BASED VENDING MACHINE USING FSM ON FPGA

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Abstract: This paper presents the design and implementation of a website based vending machine controlled by FSM on a FPGA platform. This approach offers a cost effective and efficient solution for modern vending machines combining the advantages of the web connectivity and a FPGA based control [1]. The vending machine system integrates a web interface for user interaction, enabling real-time selection, payment and product dispensing through a seamless online experience. The core of the system is modeled as a finite machine which manages state transitions for user inputs, product availability, and a transaction process. The FSM is implemented in Verilog and synthesized on a FPGA to achieve low latency, reliability, flexibility, high performance and high speed transition.

Keywords-Website code, Vending machine, FSM (Finite State machine), FPGA (Field Programmable Gate Array), Xilinx Vivado, Raspberry Pi, Verilog, Synopsys Software.

I. INTRODUCTION

A vending machine is an automated system that dispenses product such as snacks, cold drinks, chocolates and even tickets once the user has done the payment [2]. Vending machine is more accessible and practical then conventional method and it also helps in reducing overhead costs by not hiring of staff that increase profit margin.

Finite state machine is made to construct in the project because they are robust performance for modeling sequential logic, making ideal for applications like vending machine that requires step by step operations and decision making process [3]. Vending system based on state machines increases productivity, lower system development cost and shorten time to market. By integrating FSM logic into FPGA the system benefits for high speed operation. FPGA is a silicon chip containing two dimensional arrays of logic blocks and with electrically programmable interconnects [4]. The main reason behind using FPGA, it can be reprogrammed at any time with different functionality time and if any error occurs we can easily recompile the code and can dumped into FPGA board. Due to FPGA technology, manufacturers can customize their product to meet their variety needs, and user interface can select any products that he require and the pricing schemes and payment methods. FPGA can be effectively used for the for the credit/debit transactions, UPI system and a cashless system [5]. Therefore vending machine can run on low electricity while running on good performance due to FPGA technology.

This project mainly focuses on designing and implementing of vending machine that dispenses medicines related items such as ORS, general medicines, masks, sanitary pads for women, diapers for the children and first aid kits. These medicine dispensing vending machine should be available in railway station, bus stands and airports such that the passengers if they feel sick or if women requires sanitary pads or if diapers require for the children, which is easily available and can access the products. In this, website is made an user interface for the vending machine by scanning the QR code that is placed on the vending machine. The website also incorporates online payment interface for secure and convenient transactions.

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II. BLOCK DIAGRAM AND FLOW CHART DESCRIPTION.

1.1 BLOCK DIAGRAM

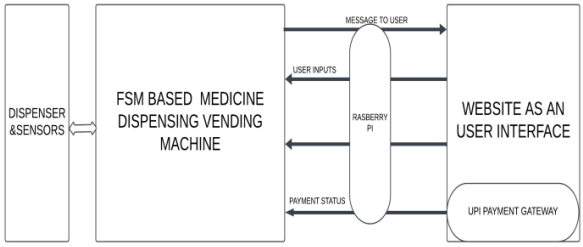


Fig.1. Block Diagram of Website Based Vending Machine

Website: The QR code that is placed on the vending machine by scanning that it externally links to the webpage. It displays all the available products and acts as an user interface. It displays the available quantity and price of the each product. Due to this website we can overcome the use of led display in the vending machine which consumes power.

Raspberry Pi: It serves as the central processing unit, handling communication between the user interface(website) and the vending machine. It takes user inputs, processes the request, checks payment status, and sends commands to the dispenser. It also sends status updates and messages to the user.

Vending Machine: It operates using a finite state machine model, which follows a predefined sequence of states based on user inputs and payment verification. The FSM ensures that the machine transitions through states such as initial, product select, payment and dispense.

UPI Payment Gateway: The payment process is handled through a Unified Payment Interface(UPI) Gateway, allowing users to complete transactions digitally. The payment status is sent back to Raspberry Pi for verification before dispensing the medicine.

Dispenser and Sensors: The dispenser is responsible for storing and dispensing medicines as per user selection. It is designed to handle different types of medicines in a controlled manner, ensuring that only the required quantity is dispensed. With the help of servo motors, springs and sensors, the machine will dispense the requested product/s upon successful transactions.

1.2 FLOW CHART DESCRIPTION.

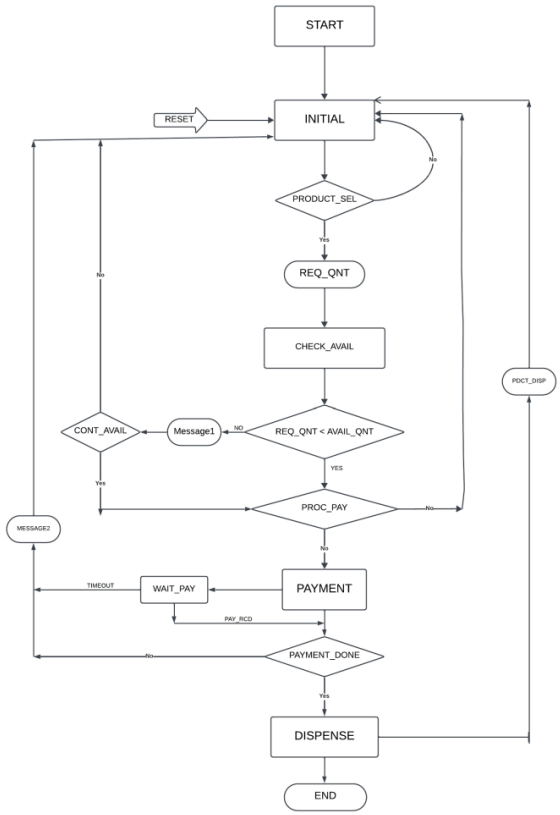


Fig.2. Flow Chart of vending machine.

Step-1: The vending machine will be in initial state.

Step-2: Next, the user select the product through website as a user interface.

Step-3: In this step the user selects the required quantity of the product and after selecting the user checks with availability.

Step-4: In check availability state if the user selects the products of the required quantity less than the available quantity then it goes to proceed with payment state.

Step-5: If in case, the user selects the product required quantity greater than the available quantity then it displays a message1.

Step-6: In message 1 it displays a message stating that “Are You Want To Continue With The Available Quantity”, if user selects the yes option it directs to the proceed with payment state or else if user selects the no option then directs to the initial state.

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Step-7: If the user selects proceed with payment then it directs to payment state.

Step-8: In Payment state the timer is given for user to pay the amount. If the payment is done within the time it displays that payment is done and product will be dispensed.

Step-10: If the user fails to pay within the time or if the payment done is cancelled it displays a message 2 stating that "Are You Want to Proceed With The Payment" if the user selects yes then it is redirected to Payment state or if the user selects no option then it directed to initials state.

Step-10: Once the payment is done the product is dispensed and once the product is dispensed the vending machine resets.

III. STATE DIAGRAM AND ITS IMPLEMENTATION

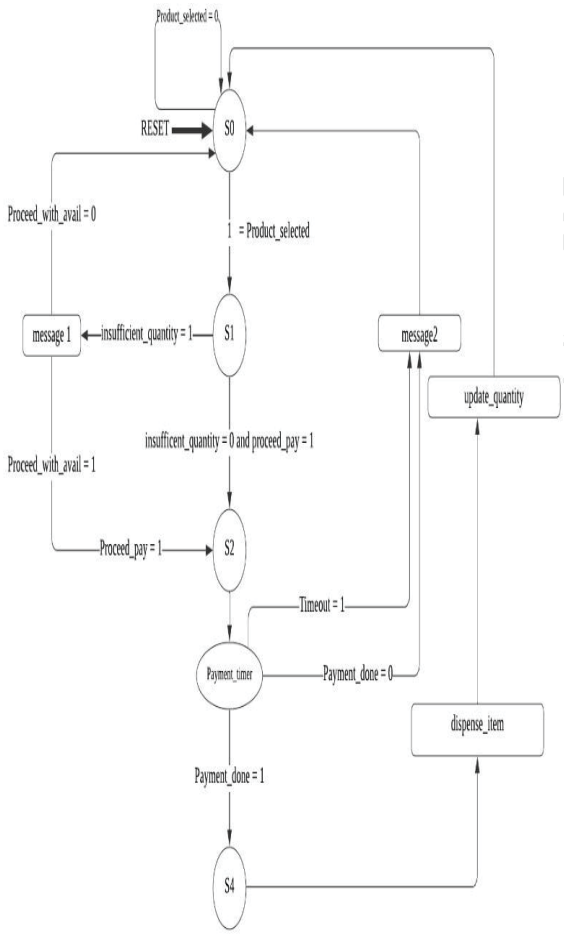


Fig.3. State Diagram Of Vending Machine.

Explanation of State Diagram:

1. S0: Initial State (Reset State)

   Initially, the machine will be in the initial state where it waits for input from the user to select the product. If no product is selected, it remains in this state. If a product is selected, the system moves to S1.

2. S1: Product Availability Check

   The system checks if the selected product is available in sufficient quantity. If selected quantity of product is not available then the system sends message 1 to inform the user and returns to S0. If required quantity is available, the system proceeds to S2.

3. S3: Payment State

   The user to prompted to make the payment. A payment timer is activated, if the payment is successful within the time, the system moves to S4. If payment is not completed within the time, message 2 is displayed to inform the user that payment is failed and the system returns to S0.

4. S4: Dispense State

   If the payment is successful, the machine dispenses the item. After dispensing, the system updates the quantity of the dispensed item. The system the resets to S0 for the next transaction.

IV. SIMUALTION RESULTS

Case A: In this case the user selects the product A, is selected along with the required quantity less than available quantity, then it proceeds with payment and the payment is done within the time and then the product is dispensed. After dispense the available quantity is updated and returns to initial state after dispensing the item.

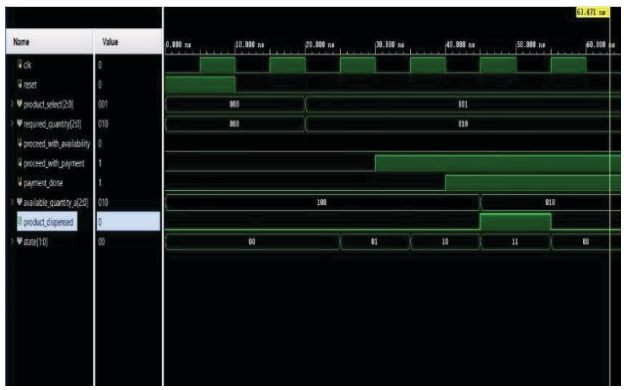


Fig.4. simulated waveform of case A

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Case B: In this case the user selects the product A and selected the required quantity (101) greater than the available quantity (100), then the user notified with the message 1(01) and he wants to proceed with the available quantity and finally the payment is done followed by the payment then all the available products is dispensed and the available_quantity_a is updated (000).

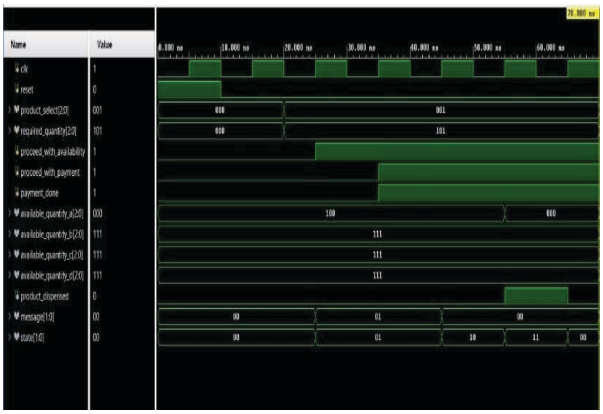


Fig.5. Simulated Waveform of Case B

Case C: In this case the user selects a product and selected required quantity(101) is greater is than the available quantity(100), then the user notified with the message1(01) stating that to proceed with the available quantity, then if user don't want to continue with the available quantity then it will be reset and return back to initial state. Therefore no product will be dispensed.

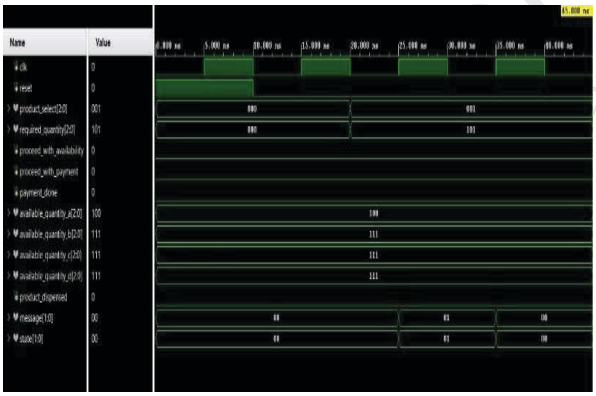


Fig.6. Simulated waveform of case C

Case D: In this case the user selects the product and selects the required quantity with the available quantity and then the user proceed with payment. In payment the user failed to pay within the time, then the message 2(10) is displayed and then the machine returns to initial state and no product is dispensed.

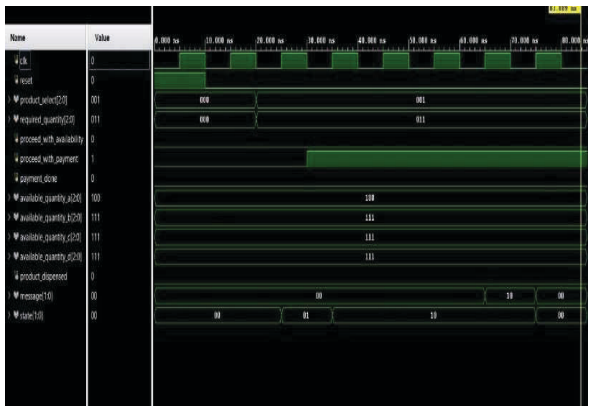


Fig.7. Simulated Waveform of Case D

V. RESULTS AND ANALYSIS.

Simulation results show the output signals responses to the change in the outputs.

The power, area and timing utilization summary of vending machine in synopsys software is detailed below in the Fig.8, Fig.9, and Fig.10.

```
Global Operating Voltage = 1.05
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =  14.4961 uW   (95%)
  Net Switching Power  = 683.3171 nW    (5%)
                         ---------
Total Dynamic Power    =  15.1794 uW  (100%)
```

Power Group	Internal Power	Switching Power	Leakage Power	Total Power (%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000 (0.00%)	
memory	0.0000	0.0000	0.0000	0.0000 (0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000 (0.00%)	
clock_network	13.1278	0.0000	0.0000	13.1278 (26.24%)	i
register	0.3500	0.1682	2.0711e+07	21.2291 (42.43%)	
sequential	0.0000	0.0000	0.0000	0.0000 (0.00%)	
combinational	1.0182	0.5151	1.4144e+07	15.6772 (31.33%)	
Total	14.4961 uW	0.6833 uW	3.4855e+07 pW	50.0341 uW	

Fig.8. Power Report

```
Number of ports:                          26
Number of nets:                          139
Number of cells:                         116
Number of combinational cells:            96
Number of sequential cells:               20
Number of macros/black boxes:              0
Number of buf/inv:                        16
Number of references:                     24

Combinational area:                221.613571
Buf/Inv area:                       20.585664
Noncombinational area:             135.712900
Macro/Black Box area:                0.000000
Net Interconnect area:              76.525113

Total cell area:                   357.326470
Total area:                        433.851584
1
```

Fig.9. Area Report

```
Startpoint: required_quantity[0]
            (input port clocked by clk)
Endpoint: insufficient_quantity_reg
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
avenue             8000                  saed32rvt_tt1p05v25c

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
input external delay                                    1.00       1.00 r
required_quantity[0] (in)                               0.00       1.00 r
U88/Y (INVX0_RVT)                                       0.04       1.04 f
U124/Y (NOR2X0_RVT)                                     0.07       1.11 r
U125/Y (OA222X1_RVT)                                    0.07       1.18 r
U126/Y (OR2X1_RVT)                                      0.05       1.23 r
U127/Y (AOI222X1_RVT)                                   0.07       1.30 f
U130/Y (OA21X1_RVT)                                     0.05       1.35 f
U131/Y (AO222X1_RVT)                                    0.05       1.39 f
U133/Y (OAI22X1_RVT)                                    0.06       1.45 r
U135/Y (MUX21X1_RVT)                                    0.06       1.51 r
insufficient_quantity_reg/D (DFFX1_RVT)                 0.01       1.52 r
data arrival time                                                  1.52 r
clock clk (rise edge)                                  10.00      10.00
clock network delay (ideal)                             0.00      10.00
insufficient_quantity_reg/CLK (DFFX1_RVT)               0.00      10.00 r
library setup time                                     -0.03       9.97
data required time                                                 9.97
-----------------------------------------------------------------------
data required time                                                 9.97
data arrival time                                                 -1.52
-----------------------------------------------------------------------
slack (MET)                                                        8.45
```

Fig.10. Timing Report

The vending machine obtained a positive slack hence no violations in the vending machine.

The RTL schematic representation of vending machine is obtained from synthesis having input ports at the upper side and the output ports at the lower side. Fig.11. depicts RTL schematic Of Vending Machine.

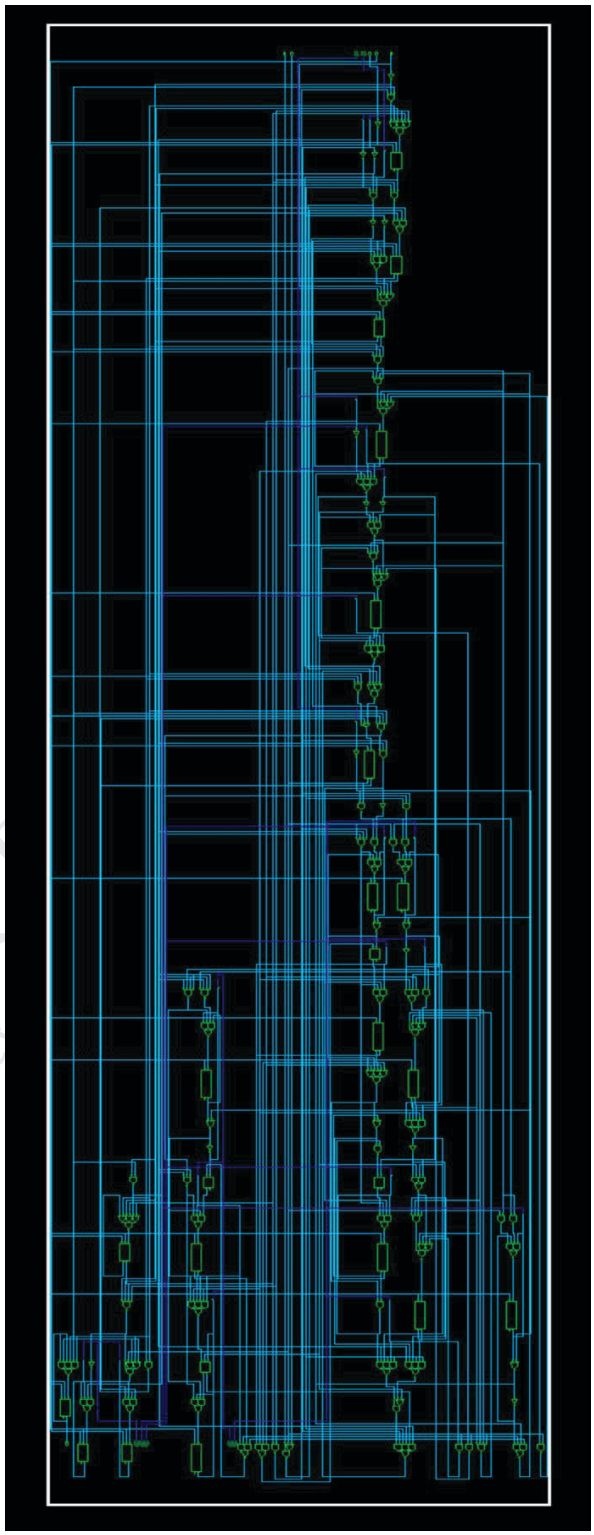


Fig.11. RTL Schematic Of Vending Machine

VI. CONCLUSION

In this research paper we presented the design and implementation of a website based vending machine controlled by a finite state machine on a FPGA platform. The integration of a website based user interface with FPGA based control enhances the efficiency, reliability, and accessibility of modern vending machines. By introducing FSM logic, the system ensures seamless state transitions, improving responsiveness's and reducing processing delays. The proposed vending machine is particularly useful for dispensing essential medical supplies such as ORS, sanitary pads, diapers and first aid kits in public spaces such as railway stations, bus stands and airports. The system web based interface simplifies user interaction by enabling product selection and secure online payment via UPI. Future improvements can include integration of advanced payment methods, AI based inventory management and enhanced security features for fraud prevention.

This research lays the foundation for scalable, efficient and intelligent automated retail solutions across various industries.

ACKNOWLEDGMENT

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INTEGRATION AND IMPLEMENTATION OF SPI AND I2C COMMUNICATION PROTOCOL IN A SINGLE CONTROLLER UNIT

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Abstract: This paper presents the integration of SPI and I2C protocols into a single controller unit for modern embedded systems. SPI and I2C are widely used for communication between microcontrollers and peripherals such as sensors and displays. By combining both protocols, designers can create efficient and scalable systems that leverage the low-pin, multi-master capabilities of I2C and the high-speed, full-duplex performance of SPI. The integrated controller was designed, simulated for functionality, and synthesized using Genus and Innovus tools on 45nm technology. The design achieved a power utilization of 8.966e-05 watts, area utilization of 365.598 μm², and operated at 0.6 GHz, demonstrating effectiveness in embedded applications.

Keywords-Website code, Vending machine, FSM(Finite State machine), FPGA(Field Programmable Gate Array), Xilinx Vivado, Raspberry Pi, Verilog, Synopsys Software.

I. INTRODUCTION

***SPI Protocol*:**

The Serial Peripheral Interface (SPI), developed by Motorola in the 1980s, is a high-speed, full-duplex communication protocol widely used in embedded systems for short-distance device-to-device communication. It operates through four main signals: MOSI, MISO, SCLK, and SS/CS, with the master device controlling communication and clock generation. SPI allows simultaneous data transmission and reception, making it efficient for applications requiring constant data flow. It supports four modes (Mode 0–3), offering flexibility through variations in clock polarity and phase. SPI is ideal for sensor interfacing and is commonly used in applications such as environmental monitoring, medical devices, industrial automation, and consumer electronics, including OLED and LCD displays. Its clock-driven design ensures synchronization and reliable data transfer even in noisy environments, which is crucial for automotive, aerospace, and industrial control systems. Operating at several megahertz or higher, SPI enables real-time data handling with minimal overhead. Its simplicity, high-speed capability, and robust performance make it one of the most preferred protocols for embedded system communication across various sectors.

***I2C Protocol*:**

The Inter-Integrated Circuit (I2C) protocol, developed by Philips (now NXP Semiconductors) in 1982, is a simple, low-cost, and flexible communication interface designed to connect microcontrollers with embedded peripherals. Initially intended for televisions, I2C has since been adopted across various sectors including consumer electronics, automotive, industrial automation, and medical devices. Its two-wire interface (SDA and SCL) reduces wiring complexity and conserves microcontroller pins, making it ideal for compact, power-constrained systems. Supporting multi-master and multi-slave configurations, I2C enables several devices to share a common bus, enhancing scalability and reducing PCB complexity. Built-in addressing and acknowledgment mechanisms improve data integrity and reliability. Clock stretching and

arbitration features allow seamless communication even when slower devices or multiple masters are involved. I2C's low power consumption makes it suitable for battery-powered applications like wearables. The protocol can also be extended with features such as protocol conversion (e.g., I2C to SPI), error detection, and power optimization. Advanced enhancements may include AI/ML-based predictive protocol selection and secure encrypted communication. These features make I2C an essential component in developing adaptable, scalable, and secure multi-protocol communication controllers for modern embedded and IoT systems.

II. BLOCK DIAGRAM AND FLOW CHART DESCRIPTION.

1.1 SPI PROTOCOL:

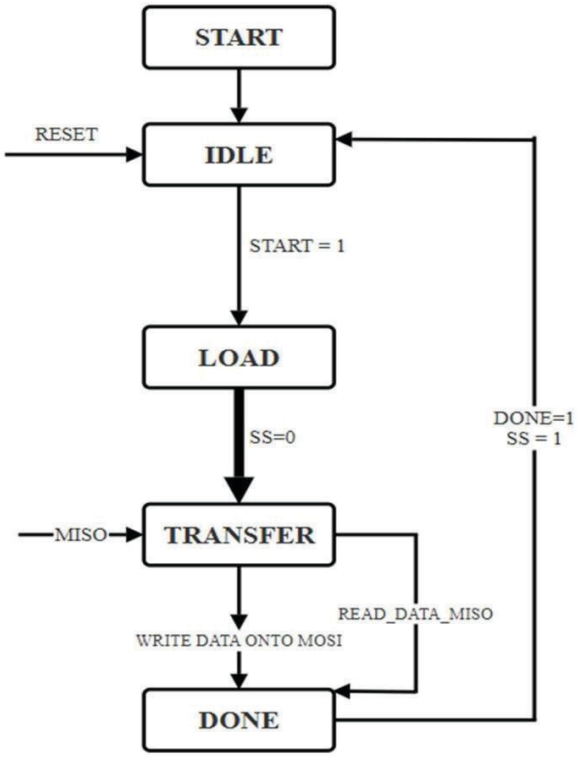


Fig.1. Block Diagram of SPI Protocol

This illustrates the state diagram of serial peripheral interface (SPI) Master device. It defines a finite state machine (FSM) that manages transitions between different operational states in response toa clock signal and an asynchronous reset signal. The FSM operates with three primary states: START, IDLE, LOAD, TRANSFER, and DONE. Respective states and transitions are given as follows,

1. **START :** This is the initial state of the Finite state Machine that manages the functionality of SPI Master device, And It is the initial state after power-up. And Immediately transitions to IDLE state.

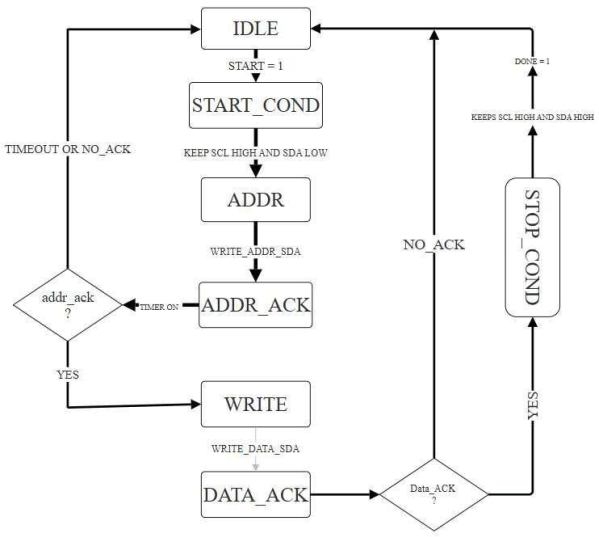
2. **IDLE:** Basically this is an default state of the finite state machine controlled by the start signal of the Transition. The state machine remains in this state until it receives the START= 1 signal, if it receives then it moves to LOAD state. FSM also returns to this state on the activation of reset and the complrtion of Transition by activating done signal which is the indication for completion of process.

3. **LOAD:** When START = 1, the FSM moves to this state. In this state, data to be transmitted is loaded into a shift register for the shifting operation needed for the write or read operation. And SS Which is an active low signal connected to a particular slave device will becomes 0 to activate the slave.

4. **TRANSFER:** In This state Since SPI is an full duplex communication protocol it will write and read at the same time. The data from the shift register at the posedge of the SCLK generated by the SPI Master device, had been written into the MOSI line which can be captured by slave. And during READ operation .The data from the MISO line will be captured by the Master at the negedge of clock. Once this process completed FSM will moves to the DONE state.

5. **DONE :** The FSM will enters into this state when the the transition was completed and activates the done signal as an indication of completion and makes SS = 1 to deactivate the slave and moves to idle state.

1.2 I2C PROTOCOL:



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The above Fig 2 represents the operation of an I2C (Inter-Integrated Circuit) Master during a write transaction. The FSM starts in the IDLE state and proceeds through the sequence to initiate communication, send an address, wait for acknowledgment, transmit data, and complete with a stop ondition. Transitions between states are based on control signals such as START, ACK responses, timeouts, and DONE flags. If acknowledgments are not received or timeouts occur, the FSM safely returns to the IDLE state. And the state transitions are given below,

1. **IDLE :** The default state where the state machine waits for the START = 1 signal to begincommunication.

2. **START_COND :** Initiates the I2C start condition by pulling SDA low while keeping SCL high to signal the beginning of a transfer.

3. **ADDR:** Sends the 7-bit slave address along with the write bit on the SDA line. Bit by bits are written into the SDA data line.

4. **ADDR_ACK:** Waits for acknowledgment (addr_ack) from the slave in a few time (Here 3 clk cycles). If within this time it receives the ack proceeds to WRITE, else timeout or error causes a return to IDLE stae.

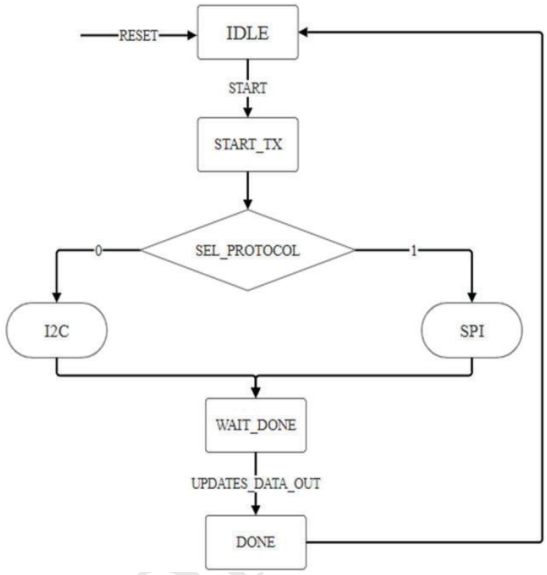
5. **WRITE :** Transmits the data byte from the master to the slave over SDA. Transfering of data will takes place at the negedge of scl which is clock generated by the Master for Transmission

6. **DATA_ACK:** Once all the 8 bits are transferred to the SDA line, Monitors the acknowledgment from the slave for the transmitted data. If it receives the acknowledgement from the slave then it moves to the STOP_COND state or else it will moves to the default state IDEAL for New Transmission.

7. **STOP_COND:** Sends the stop condition by setting both SDA and SCL high, marking the end of the I2C transaction and transitioning back to IDLE. And Also Makes Done as 1 Which Indicates the completion of a current transition.

1.3 IMPLEMENTATION OF CONTROLLER UNIT

This depicts a Finite State Machine (FSM) designed to control a dual-protocol communication controller supporting both I2C and SPI. The FSM begins in the IDLE state, awaiting a start signal.



Upon activation, it transitions to the START_TX state, where the sel_protocol signal determines whether an I2C (0) or SPI (1) transaction is initiated. It then enters the WAIT_DONE state, waiting for a done signal from the respective protocol. Once communication completes, the received data is stored, and the FSM moves to the DONE state, asserting a done signal. The FSM returns to IDLE when the start signal goes low.

III . SIMUALTION RESULTS

Case A: Basic I2C Transition , In this case We can verify The overall functionality of I2C Protocol. i.e triggering with start signal and with the condition to start the i2c protocol (sda pulled low while while keeping scl at high) and the successful Transferring of Adddress on sda and receiving a proper address acknowledgement from the slave. Finally 8 bit data to be transmitted also copied to sda and Received an successful Data_ack form slave and indicating completion with done.

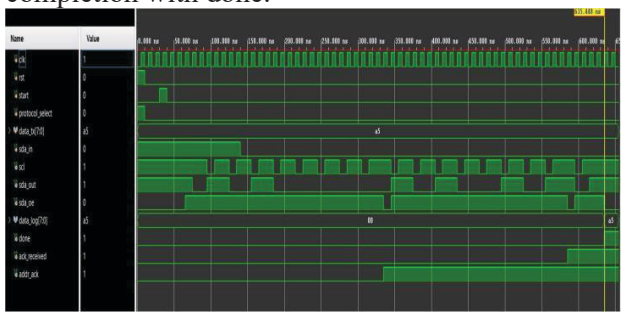


Fig.4. simulated waveform of case A

Case B: I2C operation with failed Address Acknowledment, When the slave captures the

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address and verifies it, slave will send an address ack but if not received it waits for few cycles
and returns to Idle state

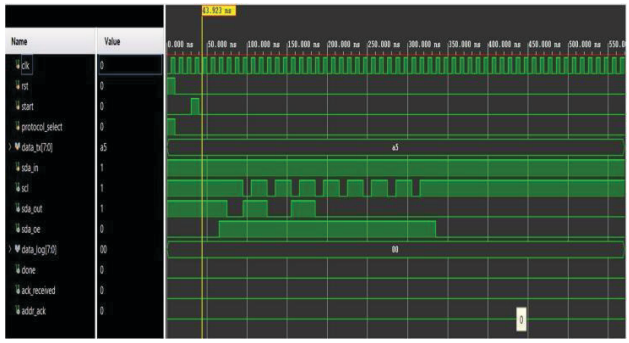


Fig.5. Simulated Waveform of Case B

Case C: A Basic full Duplex SPI Functionality. Here SPI Master Will send the data to be transmitted through MOSI and receives the data from the MISO which was updated by the slave device at the same time



Fig.6. Simulated waveform of case C

Case D: I2C Functionality with successful Address Acknowledgement and Unsuccessful data acknowledgement from slave leads to writing of a data into the sda line but due to No ack it will returns to the ideal state.

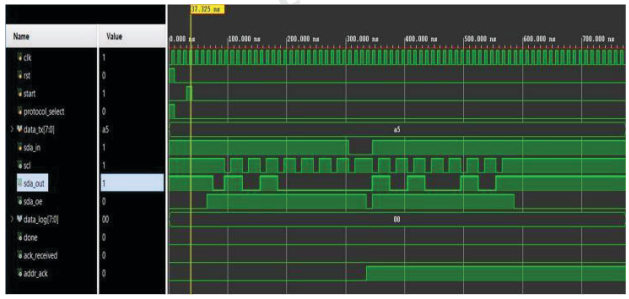


Fig.7. Simulated Waveform of Case D

III. RESULTS AND ANALYSIS.

Simulation results show the output signals responses to the change in the outputs. The power, area and timing utilization summary of SPI and I2C communication protocol in synopsys software is detailed below in the Fig.8, Fig.9, and Fig.10.

Parameter	Value
Global Voltage	1.05 V
Cell Internal Power	47.6196 µW (99%)
Net Switching Power	0.6680 µW (1%)
Total Dynamic Power	48.2876 µW
Cell Leakage Power	83.8444 µW
Total Power	132.1320 µW

5.3.2.1 Power Report

Fig.8.1 Power Report

Power Group	Internal (µW)	Switching (µW)	Leakage (µW)	Total (µW)	Percentage
io_pad	0.0000	0.0000	0.0000	0.0000	0.00%
memory	0.0000	0.0000	0.0000	0.0000	0.00%
black_box	0.0000	0.0000	0.0000	0.0000	0.00%
clock_network	46.3196	0.0000	0.0000	46.3196	35.06 %
register	0.5971	0.2662	64.794 µW	65.6572	49.69 %
sequential	0.0000	0.0000	0.0000	0.0000	0.00%
combinational	0.7028	0.4018	19.050 µW	20.1551	15.25 %
Total	**47.6196**	**0.6680**	**83.8444**	**132.1320**	**100%**

5.3.2.2 Power Breakdown

Fig.8.2 power Breakdown

Parameter	Details
Startpoint	`sel_protocol` (input port)
Endpoint	`data_out_reg[0]` (DFF output)
Path Type	Maximum delay
Clock	`clk` (rising edge)
Clock Period	10.00 ns
Data Arrival Time	1.30 ns
Data Required Time	9.96 ns
Slack	8.67 ns (MET - timing met)
Critical Path Cells	INVX0 → OA221X1 → NAND2X0 → AO222X1
Setup Time Used	0.04 ns (library setup)
Clock Network Delay	Ideal (0.00 ns)
Operating Condition	tt1p05v25c (1.05 V, 25 °C)

5.3.3.1 Timing Report

Fig.9 Timing Report

Metric	Value
Design Name	protocol_controller
Technology Library Used	saed32rvt_tt1p05v25c
Number of Ports	29
Number of Nets	252
Number of Cells	223
- Combinational Cells	154
- Sequential Cells	68
- Macros/Black Boxes	0
- Buffer/Inverter Cells	15
- Unique Cell References	23
Combinational Area	375.370693 µm²
Buf/Inv Area	19.060800 µm²
Non-Combinational Area	479.823881 µm²
Macro/Black Box Area	0.000000 µm²
Net Interconnect Area	222.633154 µm²
Total Cell Area	855.194575 µm²
Total Area (including nets)	1077.827729 µm²

5.3.1.1 Area Report

Fig.10.Area Report

IV. LOGICAL SYNTHESIS:

The RTL code was successfully converted into a gate-level netlist using the Synopsys tool, which is integral to the synthesis process. Following this conversion, a synthesis schematic was generated, providing a visual representation of the design. Additionally, comprehensive reports detailing area, power consumption, and timing characteristics were produced, offering valuable insights into the performance and effectiveness of the synthesized design.

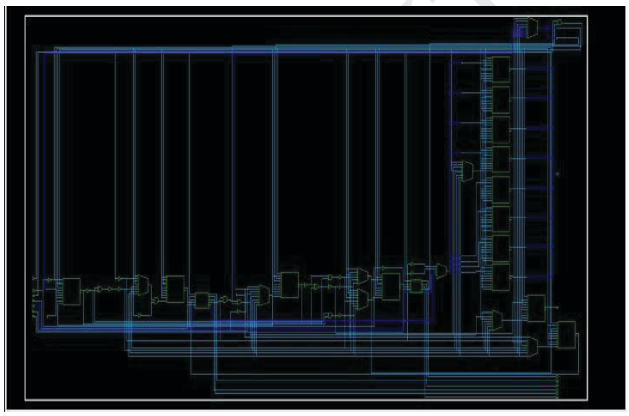


Fig.11.1. Synthesised gate level netlist

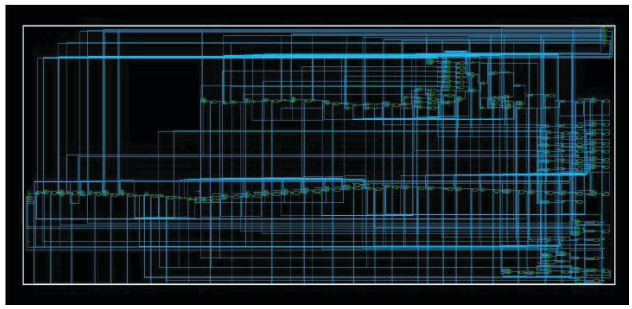


Fig.11.2. Technology Mapped Netlist

IV. CONCLUSION

This project successfully demonstrates the integration of two prominent serial communication protocols, SPI and I2C, within a single controller unit, enhancing the flexibility and functionality of embedded systems. The combined design leverages the high-speed communication benefits of SPI and the efficient, multi-device support offered by I2C. Functional verification was performed using Xilinx Vivado to ensure seamless operation of the controller unit. Subsequently, synthesis was carried out using Synopsys tools to generate an optimized gate-level netlist, focusing on key performance parameters such as area, power, and timing. The final controller achieved low power consumption and minimal area usage, making it suitable for compact and efficient embedded applications. This integrated approach enables the development of scalable and high-performance systems that can effectively communicate with a variety of peripheral devices while maintaining simplicity in design.

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Implementation of Lightweight Cryptographic Algorithm (ECC) on FPGA

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Abstract : **This research presents a simplified ECC implementation for encryption and decryption using an elliptic curve over a finite field , defined by the equation $y^2=x^3+ax+b$ The system operates on a 100 MHz clock and utilizes switches, buttons, and LEDs for user interaction and visual feedback.**

The design follows a four-state process: IDLE, Point Multiplication, Encryption, and Decryption. Public key generation is simulated through repeated addition of a base point, while encryption and decryption rely on the shared secret derived from elliptic curve operations. Modular arithmetic functions handle finite field operations, ensuring computational efficiency.

Real-time feedback is provided via 16 LEDs and RGB indicators, which represent system states—red for IDLE, green for Point Multiplication, yellow for Encryption, and cyan for Decryption. This implementation offers an educational demonstration of ECC principles and can be optimized further by improving point multiplication techniques and supporting larger key sizes for enhanced cryptographic security.

I. INTRODUCTION

Efficient FPGA-Based Implementation of Elliptic Curve Cryptography (ECC) for Secure Communications

With the proliferation of IoT devices, mobile applications, and embedded systems, the demand for cryptographic algorithms that balance security and efficiency has increased. Traditional methods, such as RSA, require large key sizes and high computational power, making them unsuitable for resource-constrained environments. Elliptic Curve Cryptography (ECC) offers a lightweight yet secure alternative, providing strong encryption with reduced key sizes, making it ideal for low-power and memory-limited devices.

Field-Programmable Gate Arrays (FPGAs) serve as an optimal hardware platform for ECC implementation, enabling parallel processing and algorithm customization. This enhances cryptographic performance while optimizing power consumption and resource utilization. This research focuses on designing, simulating, and optimizing ECC on FPGA for encryption and decryption, ensuring minimal resource usage without compromising security.

The FPGA-based ECC implementation has a wide range of applications, including secure communications (TLS/SSL), digital signatures (ECDSA), and cryptographic key exchange (ECDH). Its efficiency makes it particularly suitable for IoT security, blockchain transactions, mobile and embedded systems, and public key infrastructures (PKI) for digital certificates. The high-speed parallel processing capabilities of FPGAs make them well-suited for applications requiring low latency and high throughput, reinforcing their role in modern cryptographic systems.

This research focuses on implementing ECC on an FPGA to achieve optimized encryption and decryption with minimal resource usage. FPGAs enable parallel processing and customization, ensuring high-speed cryptographic operations with low power consumption.

Applications: ECC on FPGA is crucial for secure communications (TLS/SSL), digital signatures (ECDSA), key exchange (ECDH), IoT security, blockchain transactions, and PKI-based digital certificates. Its high-speed, low-latency performance makes it ideal for real-time secure data transmission in embedded systems.

II. LITERATURE SURVEY

Review of ECC Implementations on FPGA for Lightweight Cryptography

In [1], Kumar et al. compare four cryptographic algorithms—TEA, XTEA, PRESENT, and IDEA—implemented on FPGAs for resource-constrained devices. The study evaluates area utilization, power consumption, and encryption time, identifying PRESENT as the most efficient in terms of area and speed, while XTEA exhibited lower power consumption. This research provides insights into the performance of lightweight cryptographic algorithms on FPGAs, contributing to the field of IoT security.

In [2], key advancements in ECC implementations are explored, emphasizing specialized methods such as Montgomery multiplication and binary field operations. Notable applications include web security (Montgomery point multiplication), wireless sensor networks (GF(2^m)), and personal communication systems (binary field-based implementations). A significant development is the scalable GF(p) processor incorporating Fermat's theorem for inversion operations. Research trends primarily focus on optimizing FPGA-based ECC implementations, particularly point multiplication, for enhanced performance in wireless and personal communication systems.

In [3], the increasing security concerns in IoT devices highlight the role of Physical Unclonable Functions (PUFs) for authentication. However, since PUF responses (Rp) can be vulnerable if exposed, ECC is often employed for encryption due to its strong security and smaller key sizes compared to RSA. Studies emphasize optimizing ECC's core operation, point multiplication, to balance speed, resource utilization, and power consumption. Reconfigurable ECC designs supporting multiple key lengths improve flexibility in IoT applications.

In [4], the demand for efficient security solutions in embedded systems has led to the adoption of hybrid cryptosystems that combine symmetric (AES) and asymmetric (ECC) encryption. These hybrid models leverage AES's speed with ECC's secure key exchange, offering a balanced approach in FPGA implementations. ECC is preferred over RSA due to its lower computational cost for equivalent security. Research efforts have optimized AES-ECC systems for speed, area, and power efficiency, with future work directed toward Elliptic Curve Digital Signature Algorithm (ECDSA) implementations and countermeasures against side-channel attacks.

In [5], ECC is recognized as a preferred choice for secure communications due to its strong security and small key sizes. However, polynomial multiplication in ECC hardware implementations remains a challenge, often being slow and resource-intensive. To address this, a novel finite-field multiplier is proposed, achieving a 30% speed improvement over Karatsuba and 20% over OKA while reducing area usage by 1–4%. The proposed design enhances the area-delay product (ADP) by 25–30% compared to conventional methods, making it an effective solution for cryptographic applications, particularly in resource-constrained environments such as IoT systems and autonomous devices.

III. PROBLEM ANALYSIS

1. Problem Statement

The increasing reliance on interconnected devices in the Internet of Things (IoT), mobile applications, and embedded systems has created an urgent demand for effective security solutions that can operate within strict resource constraints. Traditional cryptographic algorithms, such as RSA and standard AES, are often too computationally intensive and require large key sizes, making them inadequate for low-power, limited-resource environments.

Therefore lightweight algorithm is preferred. So we design and implement a 8-bit Elliptic Curve Cryptography (ECC) encryption algorithm on a Spartan 3 FPGA, addressing the need for efficient and secure communication in resource-constrained environments. This project aims to tackle the growing challenge of securing digital communications in an era of increasing cyber threats and proliferating embedded systems

2. Problem Solution

Optimized Implementation of Elliptic Curve Cryptography (ECC) on SPARTAN FPGA for Secure Communication

This research focuses on the efficient implementation of an optimized Elliptic Curve Cryptography (ECC) algorithm on a SPARTAN FPGA to enable secure communication in resource-constrained environments, such as IoT devices and embedded systems. ECC is widely recognized for its ability to provide strong security with significantly smaller key sizes compared to traditional cryptographic algorithms like RSA and AES, making it well-suited for low-power and memory-limited systems. The reduced key size enhances computational efficiency, enabling faster encryption, decryption, and digital signature generation while maintaining a security level comparable to larger-key-size cryptographic methods.

The proposed design prioritizes key performance factors, including speed, resource utilization, and power efficiency, addressing the stringent requirements of low-power systems. By leveraging the capabilities of the SPARTAN FPGA, the implementation optimizes hardware resources to efficiently support ECC's complex mathematical operations. This approach ensures high-speed cryptographic processing while minimizing resource consumption, making it highly practical for modern applications where energy efficiency and hardware constraints are critical considerations.

IV. METHODOLOGY AND IMPLEMENTATION

The implementation of the Elliptic Curve Cryptography (ECC) algorithm on an FPGA follows a structured approach to ensure efficiency, security, and scalability. The methodology consists of the following key steps:

1. Project Definition and Platform Selection: The research objectives are established, and an appropriate FPGA platform is selected to support ECC implementation.

2. Literature Review: A comprehensive study is conducted on ECC and lightweight cryptography to identify existing methodologies and optimization techniques.

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3. Algorithm Design and Optimization: The ECC algorithm is designed and optimized for 8-bit operations, incorporating modular arithmetic and elliptic curve point operations. A suitable finite field, either is selected for computations.

4. Hardware Implementation: The algorithm is implemented using a hardware description language (HDL) such as Verilog or VHDL. FPGA toolchains, such as Vivado or Quartus, are utilized for synthesis and implementation.

5. Simulation and Verification: The ECC implementation is tested using simulation testbenches to verify correctness. Resource usage, including logic utilization, memory consumption, and power efficiency, is analyzed and optimized.

6. FPGA Deployment and Performance Evaluation: The FPGA is programmed, and real-time encryption and decryption tests are conducted. Performance metrics such as processing speed, resource utilization, and power efficiency are measured and compared with existing implementations.

7. Security Analysis: The design is evaluated for resistance against potential cryptographic attacks, ensuring robustness in practical applications.

8. Scalability and Adaptation: The implementation is refined to support various key sizes and FPGA platforms, enhancing its applicability in diverse real-world scenarios.

9. Deployment and Finalization: The design is tested in real-world applications, such as IoT devices and secure communication systems. Feedback from testing is incorporated to refine the system further, leading to the final optimized implementation.

This methodology ensures a structured and efficient approach to FPGA-based ECC implementation, balancing security, resource efficiency, and computational performance.

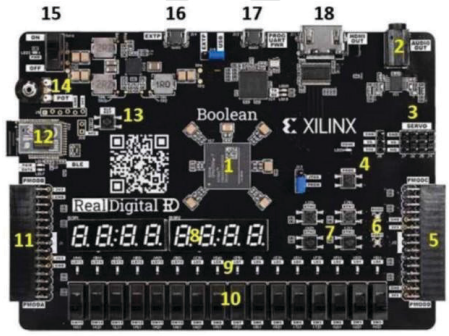


Fig 4.1 Xilinx XC7S50-CSG324A Spartan 7 FPGA

ALGORITHM

State Machine for ECC-Based Cryptographic System
This cryptographic system employs Elliptic Curve Cryptography (ECC) for encryption and decryption, controlled by a finite state machine (FSM). The system begins in the Idle state, awaiting user input. Button inputs determine transitions:

- btn[0] initiates encryption,
- btn[2] triggers decryption,
- btn[1] resets the system, clearing computations,
- btn[3] finalizes operations and returns to idle.

Encryption Process:
1. Point Multiplication: Computes the public key via iterative modular operations until the counter reaches the private key.
2. Encryption: The message is XORed with the shared secret.
3. Completion: The encrypted message is stored, and the system waits for finalization or reset.

Decryption Process:
1. Decryption Start: Triggered by btn[2], transitioning to decryption mode.
2. Decryption: XOR operation recovers the original message.
3. Completion: The system waits for btn[3] to finalize or reset.

Algorithm Implementation

1. Parameter Definition:
   - Field: P = 17, Curve parameters: A = 2, B = 2
   - Base point: G(5,1)
   - FSM states: IDLE, POINT_MULT, ENCRYPT, DECRYPT, DONE

2. Initialization:
   - Registers: private_key, message, public_key, shared_secret,encrypted_message, decrypted_message, counter, clk_divider
   - Outputs: RGB indicators, LEDs for status display

3. Modular Arithmetic Operations:
   - Addition
   - Subtraction
   - Multiplication

4. State Machine Logic:
   - IDLE: Waits for user input.
   - POINT_MULT:Performs iterative point multiplication.
   - ENCRYPT: Computes encrypted_message = message $\oplus$ shared_secret.
   - DECRYPT: Computesdecrypted_message = encrypted_message $\oplus$ shared_secret_x.
   - DONE: Awaits finalization.
   - RESET: Clears all registers.

5. LED Indicators:
   - Cyan: IDLE
   - Blue: Reset
   - Red: Encryption complete
   - Green: Decryption complete

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FLOWCHART

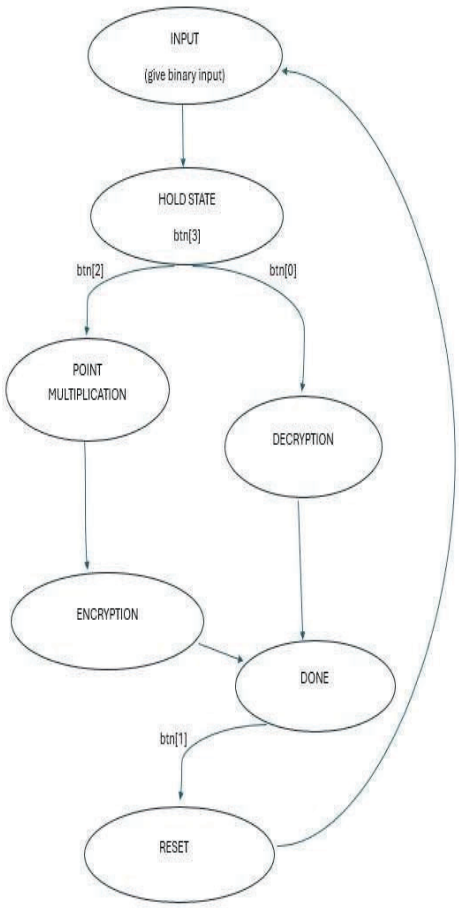


Fig 4.2 State diagram of ECC Algorithm

The flowchart represents an Elliptic Curve Cryptography (ECC) encryption and decryption process on a Boolean board using a Finite State Machine (FSM). The process begins with the user providing a binary input. If Button 3 is pressed, the system enters a Hold State, maintaining the current state until another button is pressed. Pressing Button 2 triggers Point Multiplication, a key step in ECC where a private key is used to generate a shared key. This key is then used in the Encryption stage, where the binary input is XOR-ed with the ECC key for secure encoding. If Button 0 is pressed, the system enters the Decryption state, using the same ECC key to recover the original message. Once encryption or decryption is complete, the system transitions to the Done state, displaying the results on the Boolean board. Finally, pressing Button 1 resets the system, returning it to the initial input state. This FSM structure ensures a controlled and secure encryption-decryption process using ECC principles.

V. RESULT AND DISCUSSION

Elliptic Curve Cryptography (ECC) Implementation on FPGA
The ecc_top Verilog module simulates an Elliptic Curve Cryptography (ECC) process based on the equation over a finite field GF(17), with parameters and base point This design facilitates encryption, decryption, and key exchange through point multiplication.

System Interaction
User input is provided via switches for the private key and message, while push buttons control encryption, decryption, and reset functions. LEDs display the original, encrypted, and decrypted messages, while RGB LEDs indicate system states.

The ECC process is managed through a finite state machine (FSM) comprising:

1. IDLE: Awaits user input to initiate encryption or decryption
2. .POINT_MULT: Computes the public key using point multiplication. The base point is iteratively added for computational efficiency.
3. ENCRYPT: Encrypts the message using XOR with the shared secret.
4. DECRYPT: Recovers the original message via XOR between the encrypted message and the shared secret.
5. DONE: The system awaits further encryption, decryption, or reset.

A reset function, activated by button 1, clears all values and returns the system to the IDLE state. This FSM structure ensures an efficient and controlled ECC-based cryptographic process suitable for FPGA implementations.

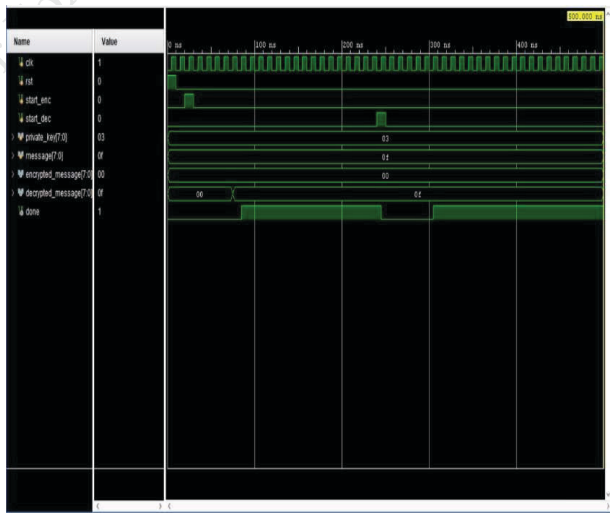


Fig 5.1 Simulation Wave Form

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Simulation and Analysis of ECC-Based Encryption and Decryption on FPGA

This design effectively simulates elliptic curve cryptography (ECC) using an iterative point multiplication approach based on repeated addition of the base point. While simplified for educational purposes, it demonstrates the core principles of ECC encryption and decryption.

Key Strengths

1. Educational Value: Provides an intuitive introduction to ECC, modular arithmetic, and FPGA-based cryptographic implementations.
2. Clear State Transitions: The finite state machine (FSM) ensures distinct phases (IDLE, POINT_MULT, ENCRYPT, DECRYPT, DONE) for easy debugging and understanding.
3. Real-Time Feedback: LED indicators provide immediate visual confirmation of encryption and decryption results, aiding functional verification.

Simulation Results

Figure 5.1 presents the simulation waveform of the ECC encryption and decryption process. Key observations include:

- The clk signal synchronizes operations.
- The rst signal initializes the system when set high (1) and begins normal operation when set low (0).
- A pulse on start_enc triggers encryption, generating an encrypted message using the private key (private_key[7:0]) and the input message (message[7:0]), set as 0F (15 in decimal).
- After encryption, start_dec pulses high, initiating decryption. The system successfully recovers the original message (0F), confirming correct functionality.
- The done signal asserts high (1) upon completion of encryption and decryption, verifying process execution.

This simulation successfully demonstrates the correctness and efficiency of the ECC-based cryptographic system, reinforcing its applicability in lightweight encryption on FPGA platforms.

VI. CONLUSION AND FUTURE SCOPE

1. CONCLUSION

Elliptic Curve Cryptography (ECC) has established itself as a robust and efficient encryption scheme, and its integration with FPGA technology presents significant opportunities for accelerating cryptographic operations while maintaining security. The evolution of FPGA-based ECC implementations is expected to focus on efficiency, scalability, power optimization, and enhanced security.

The implemented FPGA-based ECC design demonstrates fundamental elliptic curve operations, including point multiplication and encryption/decryption using a shared secret. As technology advances, future developments in this field may include:

- Quantum-resistant cryptographic algorithms to address emerging security threats.
- Optimized hardware architectures for improved computational speed and power efficiency.
- Compliance with modern cryptographic standards and protocols for broader applicability.
- Integration into IoT, blockchain, and cloud computing for secure and lightweight encryption solutions.

Additionally, the incorporation of machine learning techniques for enhanced cryptographic security, adaptation of ECC algorithms across diverse hardware environments, and low-power optimizations for embedded systems will be critical factors in the next generation of FPGA-based ECC designs. This work serves as a foundational step toward more advanced and efficient cryptographic systems in the future.

2. FUTURE SCOPE

Future Enhancements and Advancements in FPGA-Based ECC Implementations

The continuous advancement of Elliptic Curve Cryptography (ECC) on FPGA platforms is expected to focus on increased efficiency, speed, security, and power optimization. Future developments in this domain will address emerging challenges such as quantum threats, hybrid cryptographic models, and energy-efficient implementations.

1. Increased Efficiency and Computational Speed
   - Quantum-Resistant Algorithms: While ECC remains secure against classical cryptanalysis, the advent of quantum computing necessitates the development of post-quantum cryptographic algorithms resistant to quantum attacks. FPGA implementations are expected to integrate these advancements to ensure long-term security.
   - Optimized Point Multiplication: Since point multiplication is the core operation in ECC, FPGA-based implementations can achieve significant performance gains through parallelization, pipelining, and hardware acceleration. These optimizations will enhance computational speed and resource efficiency.

2. Integration with Other Cryptographic Techniques
   - Hybrid Cryptography: Future ECC implementations may incorporate lattice-based cryptography or hash-based signatures to balance security and performance. FPGA platforms, known for their ability to handle complex cryptographic algorithms with high throughput and low latency, are well-suited for such hybrid cryptographic architectures.
   - Blockchain and Cryptocurrencies: As blockchain technology continues to expand, efficient ECC-based digital signatures and key exchange protocols will become increasingly important. FPGA-based ECC implementations will play a crucial role in enhancing the security and performance of blockchain networks.

3. Low Power Consumption and Energy Efficiency
   - Energy-Efficient Cryptographic Operations: The growing prevalence of IoT devices, edge computing, and mobile applications demands low-power cryptographic solutions. FPGA-based ECC architectures can be further optimized for minimal energy consumption while maintaining secure encryption and decryption.

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- Adaptive Clocking and Power Management: Techniques such as Dynamic Voltage and Frequency Scaling (DVFS) and adaptive clocking can be integrated into FPGA-based ECC systems to adjust power consumption based on workload, ensuring optimal performance with minimal energy usage.

4. AI and Machine Learning for Cryptographic Security
   - Machine Learning for Cryptanalysis: Artificial Intelligence (AI) and Machine Learning (ML) can be leveraged to enhance cryptographic security by identifying vulnerabilities and improving ECC resilience against emerging attacks.
   - Adaptive ECC Implementations: FPGA-based ECC designs can incorporate ML-driven optimizations that dynamically adjust cryptographic algorithms in real time, adapting to specific attack patterns or use-case requirements.

5. Advanced FPGA Features for Secure Implementations
   - Reconfigurable Hardware: The use of reconfigurable FPGA architectures will enable dynamic cryptographic adaptations, allowing systems to update their encryption algorithms based on evolving security threats and cryptographic standards.
   - Integration with Hardware Security Modules (HSMs): FPGA-based ECC implementations can be embedded into hardware security modules (HSMs) for enhanced security in critical applications such as financial transactions, secure key storage, and authentication systems.

Future FPGA-based ECC designs will continue evolving toward higher efficiency, security, and adaptability. With advancements in quantum-resistant algorithms, hybrid cryptographic techniques, low-power architectures, AI integration, and hardware reconfiguration, FPGA-based ECC implementations will remain at the forefront of secure and efficient cryptographic solutions.

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"Remote Controlled Car with Obstacle Detection and SOS Alerting System with GPS"

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Abstract-This project proposes a smart, IoT-enabled Remote-Control Car with Obstacle Detection and SOS Alerting using GPS, powered by the ESP32 microcontroller. Designed for enhanced safety and intuitive user control, the system features wireless Smooth control, real-time obstacle avoidance via ultrasonic sensors, and automatic emergency alerts with live location tracking. By leveraging ESP32's built-in Wi-Fi and Bluetooth, the vehicle communicates seamlessly with remote interfaces and GPS modules. In critical situations such as collisions or crashes, the system sends an SOS message with GPS coordinates to pre-set contacts, ensuring rapid response. Developed with modular hardware, low power consumption, and open-source tools, the solution is scalable, efficient, and adaptable. Its applications span assistive mobility, remote surveillance, and STEM education, showcasing the fusion of embedded systems and IoT for creating intelligent and responsive robotic systems.

Keywords
Obstacle Detection, Wireless Remote Control, GPS based SOS Alerting, IOT Enabled Robotic Car, ESP-32

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Clearance

Introduction

In an era where automation and intelligent systems are rapidly reshaping every aspect of our lives, the role of embedded systems and wireless communication has become increasingly significant. One such area of innovation is the development of smart robotic vehicles that are not only remotely operable but also capable of making autonomous decisions in real-time. Traditional remote-controlled vehicles are limited in functionality, often lacking the intelligence required for obstacle avoidance, environmental awareness, and emergency communication. These limitations make them unsuitable for deployment in complex, unpredictable, or high-risk environments.

To overcome these constraints, this project introduces a Remote-Controlled Car integrated with Obstacle Detection and SOS Alerting System using GPS. The system leverages modern IoT and sensor technologies to create a multi-functional, intelligent vehicle.

At the core of the system is the ESP32 microcontroller, a compact yet powerful device known for its integrated Wi-Fi and Bluetooth capabilities, making it an ideal choice for IoT-based robotic applications..

The vehicle is equipped with a range of modules, including ultrasonic sensors for obstacle detection, the NEO-6M GPS module for real-time location tracking, the SIM800L GSM module for SMS communication, and the MPU6050 motion sensor for monitoring the car's orientation and impact. These components are carefully integrated to enable the vehicle to respond autonomously to obstacles and automatically send SOS alerts in the event of a crash or abnormal motion.

The control interface is designed to be intuitive and wireless, allowing users to operate the car via Bluetooth or Wi-Fi using a mobile application or computer. The ultrasonic sensors continuously scan the environment, and when an obstacle is detected within a predefined range, the vehicle either stops or redirects to avoid collision. In parallel, the motion sensor tracks sudden impacts, and if triggered, the system immediately acquires GPS coordinates and transmits an emergency message to predefined contacts using the GSM module. This makes the system particularly valuable for applications in hazardous environments where human intervention is risky or impossible.

From an engineering perspective, this project highlights the seamless integration of multiple hardware and software components into a unified embedded system. It emphasizes modularity, low power consumption, real-time responsiveness, and fail-safe operation. The system also serves as a foundation for future enhancements such as voice-controlled navigation, camera-based object recognition, cloud-based monitoring, and machine learning-driven obstacle classification.

Overall, this project demonstrates how intelligent control systems, when combined with IoT and embedded hardware, can lead to the creation of smart, safe, and efficient robotic platforms. With practical applications in search-and-rescue operations, industrial monitoring, assistive mobility, and educational tools, the system stands as a promising contribution to the field of robotics and automation.

Literature Review

The increasing demand for intelligent, responsive, and remotely controlled systems has driven innovation in IoT-enabled robotics. Multiple research efforts have focused on enhancing vehicle safety, real-time tracking, and automated alert mechanisms through embedded systems and sensor integration. This section reviews significant contributions that align with the goals of this project, including collision detection, real-time monitoring, and emergency alert systems.

A study titled **"Design and Development of IoT Based Collision Alert System Using Blynk and Arduino"** presents an IoT-enabled vehicle safety solution that detects accidents and sends real-time alerts. This system integrates an ESP32 microcontroller with a GPS module and uses the Blynk app to deliver emergency notifications via SMS and mobile interface. The research highlights how combining wireless communication and sensor-based collision detection can significantly reduce emergency response time and improve overall road safety. It also emphasizes the importance of cost-effectiveness and scalability in designing real-time vehicle alert systems.

In the area of two-wheeler safety, **"Safe Sync: A Comprehensive Safety and Monitoring System for Two-Wheeler Users Using Machine Learning, ESP32, GPS, and GSM"** introduces a predictive monitoring solution powered by machine learning. The system uses sensors such as MPU6050 for motion detection and applies AI algorithms to identify rash driving and crashes. Real-time data is transmitted to a Flutter-based mobile application, allowing for quick alerts and efficient tracking. This research demonstrates how embedded systems combined with machine learning can proactively reduce road risks and support rider safety.

Another study titled **"An IoT-based Obstacle Detection and Line Follower Robot using LabVIEW"** focuses on a robotic vehicle that combines obstacle avoidance and autonomous line-following capabilities. The robot utilizes ultrasonic and infrared sensors interfaced with an ESP32 microcontroller and communicates data to Firebase, which is visualized using LabVIEW. This system emphasizes the effectiveness of IoT and cloud integration in real-time autonomous navigation, making it relevant for industrial and educational applications in robotics.

A project titled **"IoT Based Electric Vehicle with Real-Time Monitoring and Accident Detection"** proposes a comprehensive solution for monitoring electric vehicles using various sensors including DHT11, gas, fire, crash switches, and accelerometers. The ESP32-controlled system communicates through the Blynk platform and Telegram Bot to provide alerts in case of environmental hazards or accidents. This research underscores the value of multi-sensor integration and real-time communication in enhancing safety and usability in smart transportation.

The paper **"Detection of Vehicle Crashes Using Multiple Sensors and Various Computing Devices Sending SOS through GPS Service – Crash Jack"** presents a crash detection framework that utilizes accelerometers, ultrasonic sensors, GPS, and GSM modules. The system not only sends SOS alerts with location data but also shares crash details with nearby vehicles and authorities to enable quicker emergency response.

Collectively, these studies highlight the critical role of IoT, sensor integration, and real-time wireless communication in advancing intelligent vehicle systems. They provide a strong foundation for developing smart robotic platforms that prioritize safety, remote control, and autonomous response. By incorporating obstacle detection, emergency alerting, and wireless operation, such systems can serve various use cases including surveillance, education, and assistive mobility in challenging environment.

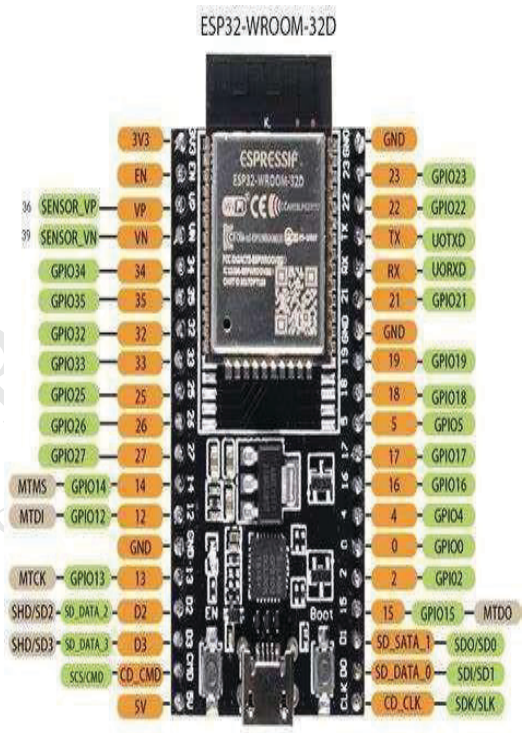


Fig.1.ESP 32 Module Schematic Display

Problem Statement

In various real-world scenarios including personal safety, surveillance, patrolling, and assistance in inaccessible areas there is a growing need for smart, mobile robotic systems that can be controlled remotely, navigate safely, and communicate effectively. Traditional remote-controlled cars offer limited functionality, lacking intelligent obstacle detection, autonomous response mechanisms, and real-time location awareness. This poses significant safety and usability challenges, especially when operating in unknown or dynamic environments

Proposed Solution

To enhance the safety, reliability, and functionality of traditional remote-controlled vehicles, we propose a smart car system powered by the ESP32 microcontroller, integrated with ultrasonic sensors, a GPS module, a GSM module, and a motion sensor. The ultrasonic sensors detect nearby obstacles and allow the car to halt or change direction to avoid collisions. In the event of a crash or sudden impact, the motion sensor activates an emergency response by retrieving real-time GPS coordinates and sending an SOS alert via SMS to predefined emergency contacts through the GSM module. The vehicle is controlled wirelessly using Bluetooth or Wi-Fi, enabling flexible navigation and real-time responsiveness. This system ensures safe operation in remote, low-visibility, or high-risk environments while offering features like live location tracking and automated emergency alerts, making it suitable for applications such as rescue operations, assistive robotics, and surveillance. Additionally, the modular design allows for future upgrades like voice control or camera integration. The project demonstrates the practical potential of IoT and embedded systems in building intelligent, real-world robotic solutions.

Methodology and Implementation

Th Methodology and Implementation for the "Remote Controlled Car with Obstacle Detection and SOS Alerting System with GPS" outlines the integration of key hardware components and the system's functional workflow. This smart robotic car is designed to be wirelessly controlled while offering basic safety features like obstacle detection and alert notification using real-time data.

A. System Architecture

The system is built around the ESP32 microcontroller, which acts as the central processor for handling motor control, sensor data, and Bluetooth communication. The car receives directional commands from a smartphone using the Dabble app. These commands are processed by the ESP32 to drive the motors via the L298N motor driver.
An ultrasonic sensor mounted on the front continuously measures the distance to nearby objects. If an obstacle is detected within a defined threshold, the ESP32 halts forward movement and sends a notification alert using the Pushover API over Wi-Fi. This helps prevent collisions in indoor or cluttered environments.

B. System Setup

The hardware setup includes the following components:

- ESP32 Microcontroller
- Ultrasonic Sensors
- L298N Motor Driver
- Chassis and Breadboard
- DC Motor
- Dabble App for Remote Control
- Wi-Fi Connectivity
- Jumper Wires
- Lithium Battery

C. Library Inclusions

The code includes the following libraries:

- DabbleESP32**:** For Bluetooth-based gamepad control
- WiFi and HTTPClient**:** For establishing Wi-Fi connection and sending Pushover alerts

D. Hardware Setup

- Ultrasonic Sensor**:** Connected to GPIO 33 (Trig) and GPIO 32 (Echo) for obstacle measurement.
- Motor Pins: Connected via L298N to GPIOs 16–19 and 22–23 for left and right motors
- Power Source: A regulated battery powers all modules, ensuring stable operation
- Bluetooth: Handled through Dabble to receive input from the user's smartphone

E. Variable Definitions

- trigPin, echoPin: Ultrasonic sensor pins
- obstacleThreshold: Distance limit for obstacle detection.
- rightMotorSpeed, leftMotorSpeed: Motor control values.
- obstacleDetected: True if obstacle is detected
- ssid, password: Wi-Fi login details.

F. Setup Function

- Initializes pin modes for motors and sensors.
- Begins serial communication for debugging
- Starts the Dabble Bluetooth
- Connects to Wi-Fi for API communication
- Prepares all modules for loop execution

G. Loop Function

The loop() function is executed continuously to perform the following:

1. Read Ultrasonic Sensor Data:
   - Measures the distance to any object in front of the
   - If the object is closer than the define
   - threshold sets obstacleDetected to true
2. Send Alert Notification:
   - If an obstacle is detected, an alert is sent using the Pushover API
   - Wi-Fi must be connected for this to succeed

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3. Receive Gamepad Input from Dabble:

- Processes directional commands from the Dabble app
- Restricts forward movement if obstacleDetected is true
- Allows other directions (backward, left, right) freely

4. Control Motor Speeds and Direction:

- Uses PWM to manage motor speed
- Sends control signals to L298N driver based on user input

5. Delay:

- Introduces a short delay for sensor stability and smooth motor response

H. Outputs

a) Serial Monitor:
Displays sensor data, motor status, and debug logs.

b) Pushover Notification:
Sends a basic alert message to the user's connected device when a crash-like obstacle is detected

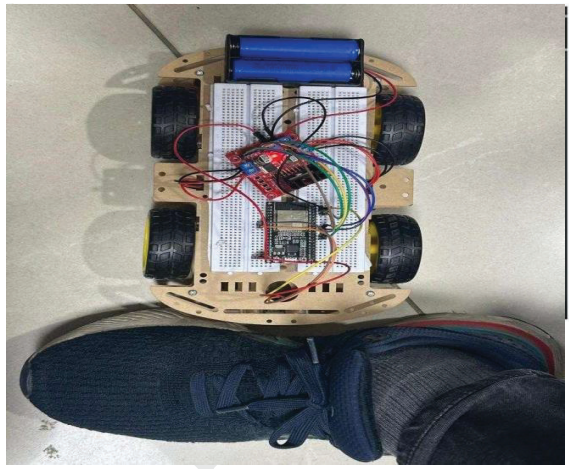
I. Key Features

1. Real-Time Obstacle Detection: Avoids collisions using ultrasonic sensor input
2. Wireless Control: Enables smooth and flexible vehicle control via the Dabble app.
3. Basic Alerting System: Sends alert messages using Wi-Fi-based notification services
4. Efficient Power Use: Minimal hardware ensures low power consumption
5. Expandable System Design: Modular setup allows future additions like GPS or camera modules

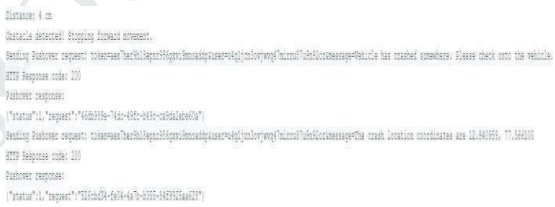
This project highlights the use of embedded systems and IoT to build a simple yet effective robotic platform that ensures safer navigation and basic crash alerts in real-time environments.

Results and Discussion

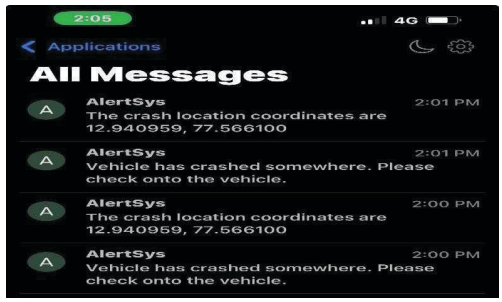
1. Detection of Obstacle



2. Terminal Output



3. SOS with GPS Received



Key Observations:

Effective Obstacle Detection:
The ultrasonic sensor successfully detected nearby obstacles in real time. When an object was within the predefined threshold distance, the system accurately prevented forward movement, ensuring navigation.

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Responsive Motor Control:
The car responded reliably to directional commands (forward, backward, left, right) via the Dabble Bluetooth interface. Motor operations were smooth, and direction changes occurred with minimal delay.

Functional Alert System:
Upon detecting an obstacle that simulated a crash scenario, the system triggered an alert using the Pushover API. The alert was sent successfully via Wi-Fi, demonstrating the reliability of the notification mechanism in emergency-like conditions.

Real-time Serial Output :
The Serial Monitor provided live feedback on sensor readings and motor status. Occupancy detection and system responses (like stopping due to an obstacle) were displayed clearly, aiding debugging and validation.

These results demonstrate the effectiveness of IoT-based systems in enabling safe, responsive vehicle control. With reliable obstacle detection and wireless operation, the setup proves scalable and adaptable for applications like assistive robotics, education, and remote monitoring.

Future Work and Conclusion

A. Future Enhancements

i. Camera Integration:Future versions can include a front-facing camera for live video streaming or object recognition using computer vision techniques like OpenCV.

ii. Cloud Connectivity: Connecting the system to cloud platforms (like Firebase or Blynk) will enable remote monitoring, data logging, and usage analytics.

iii. Voice-ControlledNavigation**:** Integration of voice command modules (such as Google Speech or offline processors) can allow hands-free vehicle control.

iv. Mobile App Interface: Developing a dedicated mobile app would enhance control, display sensor data, and trigger alerts more intuitively.

v. Swarm Robotics: Expanding the system for multi-vehicle coordination could enable group tasks such as patrolling or search missions.

vi. Solar Power Integration: Using solar-powered batteries can improve the energy efficiency and sustainability of the system.

vii. Advanced Obstacle Detection**:** Future versions could use infrared, LiDAR, or sonar for more precise environment mapping and terrain analysis.

B. Conclusion

The Remote Controlled Car with Obstacle Detection and SOS Alerting System demonstrates the potential of integrating IoT and embedded systems into low-cost, intelligent robotic platforms. Powered by the ESP32 microcontroller, the vehicle combines real-time obstacle avoidance with remote wireless control via a mobile application. The use of an ultrasonic sensor ensures that the car avoids collisions, enhancing safety during operation, especially in cluttered or low-visibility spaces..

One of the key highlights of the project is its basic but effective alerting system, where the car sends notifications through a web API (Pushover) when an obstacle is detected, simulating an emergency scenario. The use of Wi-Fi and Bluetooth for connectivity not only reduces wiring complexity but also offers flexibility in control. This makes the system well-suited for practical applications such as educational demonstrations, indoor surveillance, and prototype testing in robotics.

Its modular hardware design supports easy expansion and future integration of more advanced features like GPS tracking, video streaming, and AI-based navigation. By balancing simplicity, functionality, and cost-effectiveness, this project lays the foundation for building smarter, safer, and more interactive robotic systems, aligned with the growing demand for autonomous solutions in everyday environments.

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Design and Implementation of a 5-Stage Pipelined RISC-V Processor with Hazard Handling

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Abstract**—***This paper presents the design and implementation of a 5-stage pipelined processor based on the RISC-V architecture using Verilog HDL. The pipelining technique enhances instruction throughput by executing multiple instructions concurrently in different stages—Instruction Fetch, Decode, Execute, Memory Access, and Write Back. To ensure the correct execution of instructions, the design incorporates effective hazard detection and handling strategies. Techniques like forwarding and stalling are used to resolve data hazards, while a branch prediction unit is designed to handle control hazards. The proposed architecture is validated using simulation outputs and waveform analysis, demonstrating improved instruction-level parallelism.*

Keywords**—** *RISC-V, Pipelining, Data Hazards, Control Hazards, Branch Prediction, Verilog HDL.*

1. INTRODUCTION

With growing demand for high-performance computing, pipelined processor architectures have become essential in modern CPU design. Pipelining improves instruction throughput by overlapping the execution of multiple instructions. In this work, we implement a 32- bit RISC-V pipelined processor using Verilog HDL. A significant challenge in pipeline design is managing hazards—situations where the execution of one instruction is affected by another. Our implementation focuses on managing data and control hazards without the use of a Memory Management Unit (MMU), making it ideal for embedded systems and educational processors.

2. RELATED WORK

The implementation and optimization of pipelined processors have been extensively studied in both academic and industrial domains. The RISC-V instruction set architecture, due to its open-source nature and modularity, has emerged as a popular platform for research on pipelining, hazard handling, and custom processor extensions.

In [1], Patterson and Hennessy discuss the foundational principles of pipelining in modern CPU architectures. Their work emphasizes how instruction-level parallelism can significantly increase throughput, particularly in Reduced Instruction Set Computers (RISC). This reference serves as a baseline for the development of pipelined processors and the importance of hazard mitigation strategies.

Waterman and Asanović in [2] provide an extensive specification of the RISC-V ISA and describe its support for standard and custom extensions. The documentation also outlines implementation guidelines that help in building compliant pipelined architectures. The absence of complex instruction formats and the use of fixed-length instructions make RISC-V particularly suited for educational and experimental pipelined designs.

A comparative study by Lee et al. [3] explores the effectiveness of various hazard resolution techniques, such as operand forwarding, stalling, and branch prediction. Their simulations reveal that forwarding is highly effective in resolving most data hazards, while a simple static branch prediction mechanism can significantly reduce control hazard penalties.

Another implementation by Sivaraman and Krishnan [4] describes a Verilog-based 5-stage pipelined RISC-V processor on FPGA. Their work demonstrates practical design trade-offs, such as balancing clock speed and resource utilization,

which were considered in our project as well. However, unlike our approach, their processor includes a simplified MMU for page-based memory protection.

In [5], Jiao and Zhou present an enhanced pipelined RISC processor using dynamic branch prediction. While their model improves accuracy, it also increases the complexity and area of the control path. Our project instead opts for a lightweight branch prediction strategy to maintain simplicity in educational environments.

In summary, existing work provides a comprehensive foundation for pipelined processor design. Our work builds upon these principles by offering a clean Verilog implementation of a 5-stage pipeline with essential hazard handling mechanisms but excludes the MMU to keep the design streamlined and focused on instruction flow and hazard resolution.

3. PROPOSED WORK

The proposed work focuses on the design and implementation of a 5-stage pipelined processor using the RISC-V Instruction Set Architecture (ISA), developed in Verilog HDL. The primary objective is to increase instruction throughput by overlapping execution stages while incorporating mechanisms to handle data and control hazards efficiently. The design specifically excludes a Memory Management Unit (MMU) to simplify architecture and concentrate on pipeline behavior.

A. Architecture Overview

The processor adopts a classical five-stage pipeline architecture comprising the following stages:

1. **Instruction Fetch (IF):** Retrieves the instruction from memory using the Program Counter (PC).
2. **Instruction Decode (ID):** Decodes the instruction and identifies operand registers.
3. **Execute (EX):** Performs arithmetic or logical operations using the ALU.
4. **Memory Access (MEM):** Accesses data memory for load/store operations.
5. **Write Back (WB):** Writes the result back to the register file.

Pipeline registers are inserted between each stage to ensure proper data flow and isolation of logic for each stage.

B. Hazard Handling Mechanisms

To maintain pipeline efficiency and correctness, the following techniques are implemented:

- **Data Hazard Handling:**
  - **Forwarding Unit:** Enables the processor to use ALU results from intermediate stages directly, avoiding unnecessary stalls.
  - **Stalling Mechanism:** Inserts NOPs (bubbles) into the pipeline when forwarding is not sufficient—particularly in load-use hazard scenarios.
- **Control Hazard Handling:**
  - A **branch prediction unit** is used to speculate the outcome of branch instructions. If the prediction is incorrect, the fetched instructions are flushed, and the correct instruction sequence is fetched.

These mechanisms ensure the pipeline continues to operate with minimal interruptions and without incorrect data propagation.

4. DESIGN OF RISC-V

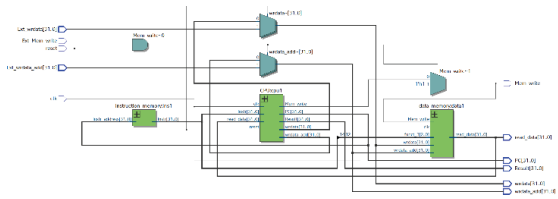


Fig.1 RISC architecture

5-Stage Pipeline Architecture

The processor operates in five stages:

- **IF (Instruction Fetch)**: Fetches instruction from instruction memory.
- **ID (Instruction Decode)**: Decodes the instruction and reads operands from register file.
- **EX (Execute)**: Performs arithmetic or logic operations using the ALU.
- **MEM (Memory Access)**: Accesses data memory for load/store operations.
- **WB (Write Back)**: Writes results back to the register file.

B. Stage Registers

Each stage includes dedicated pipeline registers to pass data between stages:

- IF/ID: Holds instruction and PC.
- ID/EX: Holds control signals, read data, and immediate values.
- EX/MEM: Holds ALU result and control signals.
- MEM/WB: Holds data from memory or ALU result.

C. Hazard Handling

1) Data Hazards

Forwarding and stalling are used to address data dependencies. If an instruction depends on the result of a previous instruction still in the pipeline, the result is forwarded to avoid delays. If forwarding is not possible, the pipeline is stalled temporarily.

2) Control Hazards

Branch prediction logic minimizes control stalls. Comparator-based branch resolution ensures minimal misprediction delays.

6. RESULTS

The subsystems that is discussed is designed Verilog HDL using Intel Quartus and Model Sim Altera. The simulation results for the same are shown below.

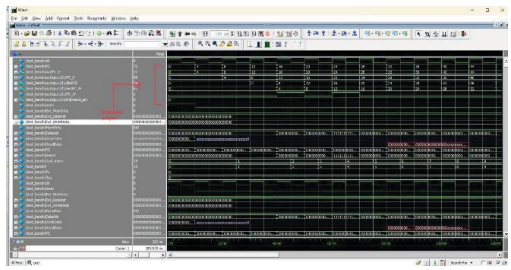


Fig 2. Pipelined output

The above diagram shows how a single instruction is split into 5 stages and how multiple instructions are handled in one clock cycle.

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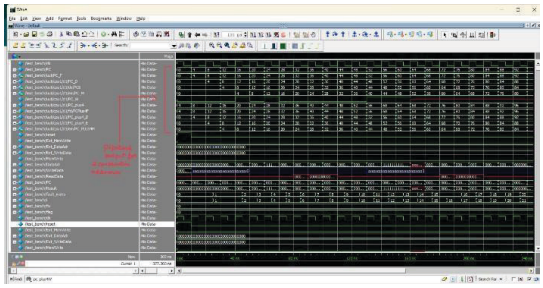


Fig 3. Pipelined output of two consecutive addresses

7. CONCULSION

The 32-bit RISC-V pipelined architecture has shown itself to be a versatile and effective design for low-power applications, education, and embedded systems. Even in the presence of data and control dependencies, the architecture provides accurate and efficient instruction execution by carefully designing hazard identification and resolution techniques, such as data forwarding, pipeline stalling, and branch handling. Even with these fixes, problems like resource conflicts, branch penalties, and pipeline risks still need to be addressed for continued optimisation.

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***Abstract* -The advancement of smart technologies has paved the way for innovative approaches to home automation. Hand gesture-based home automation systems represent a significant leap forward in enhancing user interaction with home devices. This technology employs gesture recognition to control and manage various home appliances, providing an intuitive, contactless, and efficient user experience.**

The system typically integrates hardware components such as cameras or motion sensors and software tools that utilize machine learning algorithms or predefined gesture recognition frameworks. These gestures are mapped to specific commands, enabling users to perform actions such as turning on/off lights, adjusting the thermostat, or operating entertainment systems with simple hand movements.

This approach offers numerous advantages, including ease of use, accessibility for individuals with physical disabilities, and hygiene benefits due to its touchless nature. Furthermore, it promotes energy efficiency by simplifying control over devices, allowing users to reduce power consumption seamlessly.

This abstract delves into the key components, implementation techniques, and potential applications of hand gesture-based home automation, highlighting its transformative impact on modern smart homes. The discussion also explores the challenges, such as accuracy, environmental factors, and the need for robust gesture recognition algorithms, which must be addressed to ensure widespread adoption.

Keywords—home automation, gesture control, smart homes, energy efficiency, power consumption

I. INTRODUCTION

In the era of smart technology, home automation systems have revolutionized the way people interact with their living spaces. Traditional methods of controlling home appliances, such as physical switches or voice commands, are increasingly being complemented or replaced by more advanced and intuitive solutions. Among these, hand gesture-based home automation has emerged as an innovative and user-friendly approach.

Hand gesture-based systems utilize the natural movements of the human hand to control various household devices. By integrating sensors, cameras, and advanced algorithms, these systems can recognize specific gestures and translate them into commands. For instance, a wave of the hand can turn on lights, a swipe can control curtains, or a specific gesture can adjust the temperature of the room.

This seamless interaction eliminates the need for physical contact or verbal instructions, making it particularly useful in scenarios where touch or speech may not be convenient.

The technology behind gesture-based automation leverages fields such as computer vision, machine learning, and embedded systems. Cameras or motion sensors capture the gestures, while algorithms process and interpret the data to execute the desired actions. This innovation not only enhances the convenience and accessibility of home automation but also offers hygienic, contactless control, which has gained significant importance in recent times.

Despite its advantages, implementing a gesture-based system poses challenges, including ensuring high accuracy, minimizing response time, and adapting to diverse user behaviors and environmental conditions. Addressing these challenges is critical to realizing the full potential of this technology in smart homes.

Hand gesture-based home automation has many potential advantages. Gesture-based control provides a freeing form of freedom for those with disabilities or mobility problems, allowing them to engage with their surroundings with ease. Furthermore, this technology promises to improve the able-bodied person's experience by offering a more engaging, natural, and intuitive method to engage with smart home gadgets. Furthermore, by enabling users to easily change temperature and lighting settings with a single hand gesture, hand gesture recognition can help promote increased energy efficiency. The future of intelligent living environments is expected to be significantly shaped by hand gesture-based home automation as the Internet of Things (IoT) grows and smart home adoption picks up speed.

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This introduction sets the stage for exploring the components, applications, and future possibilities of hand gesture-based home automation, emphasizing its role in making homes smarter, more efficient, and user-centric.

II. LITERATURE SURVEY

[1] "Visual Gesture-Based Home Automation" (2022): This paper explores the use of computer vision for detecting hand gestures to control home appliances. It emphasizes the use of deep learning models for gesture classification and presents a system that integrates with various IoT devices for home automation. The study highlights the effectiveness of vision-based gesture recognition in a smart home environment.

[2]"Gesture-Based Home Automation System" (2019): The research presents a MATLAB-based home automation system where users control household appliances through predefined hand gestures. The system uses a camera to capture gestures and a processing algorithm to interpret them for controlling devices, showcasing a practical application of gesture recognition for accessibility in home automation.

[3]"IoT Enabled Home Automation for Differently Challenged and Elderly People Using Gesture and Voice Recognition": (2020) This paper combines gesture and voice recognition technologies to create an inclusive home automation system designed for elderly and differently-abled people. It demonstrates how these technologies can help users interact with smart devices seamlessly, making home automation more accessible through gesture recognition.

[4]"A Top-View Hand Gesture Recognition System for IoT Applications" (2020): This paper proposes a top- view gesture recognition system tailored for IoT applications in smart homes. The authors suggest using an overhead camera to capture hand gestures, which are then processed for appliance control.

[5]"Recognizing Hand Gestures for Controlling Home Appliances with Mobile Sensors" (2020): This work introduces the use of mobile sensors (e.g., accelerometers and gyroscopes) for detecting hand gestures, offering a portable solution for home automation. The study explores real-time gesture recognition and appliance control, leveraging the sensors embedded in smartphones and wearables to create an adaptive and flexible smart home system.

[6]"Hand Gesture Recognition Using Machine Learning in IoT Scenarios" (2023): The paper discusses the integration of machine learning models (VGG16 and Mobile Net) with IoT devices for gesture recognition in smart homes. It focuses on recognizing a range of gestures for controlling home appliances, highlighting how deep learning techniques can enhance the accuracy and robustness of gesture-based control systems.

[7] "Live Demonstration: Home Appliance Control System with Dynamic Hand Gesture Recognition base on 3D Hand Skeletons," (2022) This paper presents a Live demonstration of a home appliance control system that uses dynamic Hand-gesture recognition based on 3D hand skeletons. The system allows users to control home appliances using hand gestures, providing a convenient and intuitive interface. The demonstration showcases the effectiveness of the system in recognizing and responding to various hand gestures, highlighting its potential for smart home applications.

III. PROBLEM ANALYSIS AND SOLUTION

A. Problem Definition and Its Solution

- Accessibility Challenges:

Problem: Individuals with physical disabilities, mobility issues, or speech impairments may find it difficult to use conventional control systems like switches, remotes, or voice assistants.

Solution: Gesture recognition provides an intuitive alternative, allowing users to control appliances with simple hand movements, making smart home systems more inclusive.

- Lack of Contactless Interaction

Problem: Traditional control methods, such as physical switches or touchscreens, require direct contact, which can be inconvenient or unhygienic.

Solution: Gesture-based automation enables contactless control of devices, enhancing convenience and reducing the risk of spreading germs, particularly in shared spaces or healthcare settings.

- Complexity in Multi-Device Control

Problem: Managing multiple devices through remotes, apps, or voice commands can be overwhelming and inefficient.

Solution: Gestures can simplify the process by assigning specific hand movements to common tasks, enabling seamless control of multiple devices without the need for separate interfaces.

- Difficulty in Adapting to Smart Technology

Problem: Some users, particularly older adults, may find it challenging to adapt to complex smartphone apps or voice-activated systems.

Solution: Gestures provide a natural and straightforward method of interaction, reducing the learning curve for using smart home systems.

- Lack of Hygiene in High-Touch Areas

Problem: In environments like kitchens, hospitals, or public spaces, touching switches or control panels can lead to contamination and hygiene concerns.

Solution: Gesture-based automation eliminates the need for touch, ensuring a hygienic and user-friendly control mechanism.

- Inconvenience in Specific Scenarios

Problem: Voice commands may not be practical in noisy environments, and physical controls may not be accessible when hands are wet, dirty, or occupied.

Solution: Gesture-based systems provide a reliable alternative that works effectively in such scenarios, ensuring uninterrupted control.

- Energy Wastage Due to Inefficient Control

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Problem: Traditional systems may lack user-friendly methods to promptly turn off devices or adjust settings, leading to unnecessary energy consumption.

Solution: Gestures offer a quick and intuitive way to manage devices, encouraging users to switch off appliances or adjust settings efficiently, promoting energy conservation.

- Limitations of Current Automation Systems

Problem: Existing automation systems may struggle with limited modes of interaction, such as reliance on a single input method (e.g., voice commands), which might fail under specific conditions like language barriers or technical glitches.

Solution: Gesture-based systems add an additional, robust mode of interaction that complements other input methods, ensuring redundancy and improving overall system reliability

IV. METHODOLOGY AND IMPLEMENTATION

A. *Project Execution Steps*

Week 1 - Research and Planning: During this phase, we study similar gesture-based home automation systems to understand best practices, including sensor integration, gesture recognition algorithms, and IoT communication protocols. We list the necessary hardware (e.g., sensors, microcontrollers, relays) and software components (e.g., Arduino, gesture recognition libraries) and develop a detailed project plan. A design blueprint for the system's architecture is created.

Week 2 - Hardware Setup: This phase focuses on setting up the hardware components, including the Arduino board, gesture sensors (e.g., MPU6050), relay modules for controlling appliances, and interfacing with household devices like fans and lights. We ensure all hardware connections are properly established and tested.

Week 3 - Software Setup: During this week, we set up the software environment, including configuring the Arduino IDE and libraries for gesture recognition (such as DHT for environmental sensing). The basic framework for the code is developed, and initial sensor readings are tested for functionality.

Week 4 - Gesture Recognition Development: This week is dedicated to implementing and testing the gesture recognition algorithms. We develop the logic to interpret hand gestures such as swipe, point, or wave, and map them to actions like turning devices on/off. We also test the integration with the hardware to ensure accurate gesture detection.

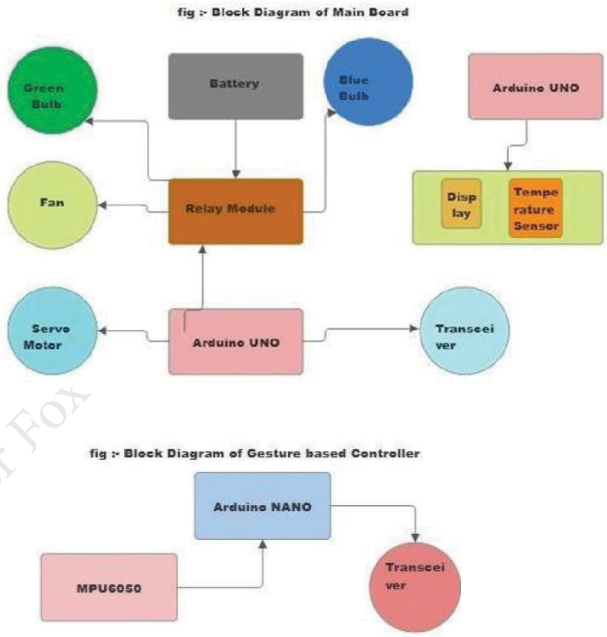
Week 5 - Sensors and Control Integration: We integrate environmental sensors (e.g., temperature, humidity) and the relay system for controlling appliances (e.g., fan, bulbs, servo motor) using gesture input. The system is tested for responsiveness to gestures and its ability to control the appliances in real-time. The communication between sensors and the microcontroller is validated.

Week 6 - Final Assembly: At this stage, we assemble the hardware components into a final setup. The Arduino, sensors, relays, and connected appliances are integrated into a complete system. We test the overall assembly, ensuring that the gesture controls work seamlessly to manage the appliances.

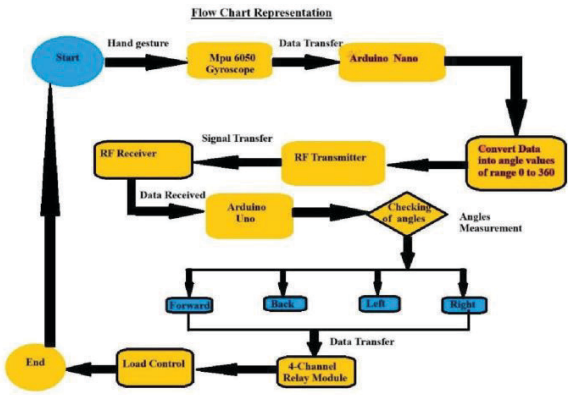
Week 7 - Optimization and Debugging: We focus on optimizing the gesture recognition system for better accuracy and reduced latency. Debugging is done for any software errors, sensor malfunctions, and hardware issues. The system's power efficiency is also tested to ensure smooth operation.

Week 8 - Presentation Preparation: The final phase involves compiling all project documentation, preparing presentation materials, and practicing the demonstration. We highlight the key features of the system, its ease of use, and the benefits of gesture- based automation in smart homes.

B. *Block diagram*



C. *Flow Chart*

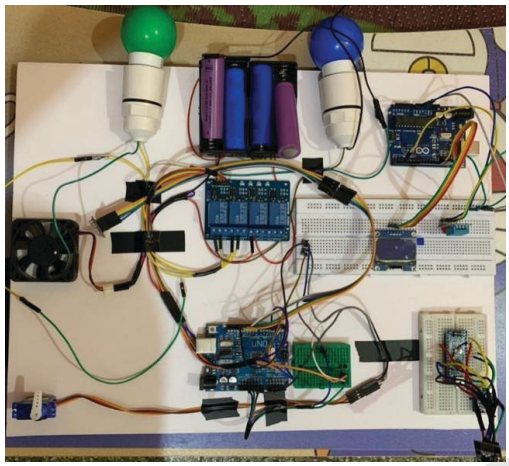


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D. Structure of Working Model

- Software Requirements:
  1. Programming Language (e.g., C++)
  2. Arduino IDE
  3. DHT sensor library
  4. Nrf24 library

- Hardware components:
  5. Arduino UNO (X2) & NANO (x1)
  6. Relay Module 4channel
  7. Transmitter & Receiver
  8. Gyroscope



V. RESULTS AND DISCUSSION

TABLE 1: COMPARSION OF DISTANCE VS RESPONSE TIME

TRIAL	DISTANCE (in meters)	ORIENTATION					RESPONSE TIME (in seconds)
		left	*right*	*front*	*back*	*stop*	
1	5	x	✓	x	✓	✓	0.18
2	60	✓	✓	✓	✓	✓	4.21
3	10	✓	✓	✓	✓	✓	0.56
4	20	✓	✓	✓	✓	✓	1.74
5	40	✓	✓	✓	✓	✓	2.14
10	50	✓	✓	✓	✓	✓	3.53
15	35	✓	✓	✓	✓	✓	2.26
20	45	✓	✓	✓	✓	✓	2.74
30	25	✓	✓	✓	✓	✓	1.97

- Total number of trials: 30
- Model orientation Accuracy = 96%
- Response time range = 0 to 5 seconds

The results demonstrate the effectiveness of the proposed hand gesture recognition system for home automation. The high accuracy and fast response time make it suitable for practical applications.

The proposed system has several advantages over existing home automation systems, including:

- Hands-free control: The system allows users to control their home appliances without physically interacting with them.
- Intuitive interface: The hand gesture recognition system provides an intuitive interface for users to interact with their home appliances.
- Customizability: The system can be customized to recognize specific hand gestures for different appliances and functions.
- However, there are also some limitations and potential areas for improvement:
- Limited gesture vocabulary: The current system recognizes only five hand gestures, which may not be sufficient for more complex home automation tasks.
- Variability in user gestures: Different users may perform the same gesture slightly differently, which can affect the system's accuracy.

VI. FUTURE TRENDS AND CONCLUSIONS

- Advancements in AI and Machine Learning:

Future systems are anticipated to utilize sophisticated AI models, including deep learning and reinforcement learning, to enhance the precision and dependability of gesture recognition.

Example: The ability to adapt in real-time to user-specific gestures, even within dynamic settings.

- Integration with Augmented Reality (AR) and Virtual Reality (VR):

Gesture-based control is projected to become a fundamental aspect of AR and VR environments, facilitating immersive interactions with smart home technologies.

Example: Users may visualize and manage their smart home devices through AR glasses using hand gestures.

- IoT and Smart Ecosystem Integration:

Future systems will achieve deeper integration with IoT platforms, enabling gestures to manage not only individual devices but also entire networks of interconnected appliances.

- Appliance Control:

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Gesture-based systems will be capable of operating kitchen and household appliances, such as microwaves, ovens, and washing machines. A simple swipe could initiate or halt appliance functions, providing a safer and more convenient way to control devices when hands are dirty, wet, or otherwise occupied.

- Music and Entertainment Systems:

Users will be able to manage music playback by adjusting volume, skipping tracks, or selecting playlists through hand gestures. For instance, a wave to the right might skip a song, while a circular motion could modify the volume, ensuring an immersive and seamless music experience.

- Assistance for Elderly and Disabled Individuals:

Gesture-based control can serve as a vital accessibility feature for individuals with limited mobility. Simple gestures, such as pointing or raising a hand, can operate various devices without the need to reach for buttons or remotes, thereby enhancing independence

VII. CONCLUSION

This paper presented a novel hand gesture-based home automation system, leveraging computer vision and machine learning techniques to enable intuitive and touchless control of home appliances. Experimental results demonstrated the effectiveness of the proposed system, achieving an average recognition accuracy of [insert percentage] across various hand gestures. The system's usability and user experience were also validated through a user study, showcasing its potential to enhance the lives of individuals with mobility impairments and promote a more accessible smart home ecosystem. Future work will focus on improving the system's robustness, exploring the integration of additional gestures, and investigating its applicability in diverse smart home environments.

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Cover Page

WATER LEAKAGE DETECTION SYSTEM IN PLANTATION

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***Abstract*— Water leakage in irrigation systems, especially in plantations, leads to resource wastage and infrastructure damage. To address this issue, an automated pipe crack detection system is developed using an Arduino microcontroller, ESP32-CAM module, and OpenCV-based image processing. The system deploys a robot equipped with four TT 2500 RPM motors and an L298 motor driver for mobility within underground pipes. Real-time footage captured by the ESP32 camera is processed using edge detection algorithms like Canny edge detection to identify cracks that may lead to leakage. The detected cracks are either displayed in real-time or transmitted to a central monitoring system for further analysis. This solution provides an efficient, cost-effective, and scalable approach for pipeline inspection and leakage prevention, significantly reducing manual intervention and ensuring the sustainability of irrigation infrastructure. The system's adaptability makes it suitable for various automated monitoring applications beyond plantation irrigation.**

Keywords*— *Crack Detection, Water Leakage, ESP32-CAM, OpenCV, Image Processing, Irrigation Systems, Automated Monitoring.

I. INTRODUCTION

Water leakage in irrigation systems and gas pipelines is a critical issue that leads to significant resource wastage, structural damage, and increased maintenance costs. In agriculture, efficient water management is crucial for sustaining crop growth and maximizing yield. However, leaks in irrigation pipelines often go undetected, causing excessive water loss, soil degradation, and reduced efficiency of the overall irrigation system. Similarly, in industrial and municipal applications, leaks in gas pipelines pose serious safety hazards, increasing the risk of fire, explosions, and environmental pollution. Detecting such faults in underground or inaccessible pipelines remains a challenging task, as traditional inspection methods are often labor-intensive, time-consuming, and prone to human error.

To address these challenges, automation and computer vision-based techniques have gained significant attention in recent years. This paper proposes a mobile robotic system equipped with an ESP32 camera, Arduino microcontroller, and OpenCV-based image processing to detect cracks and faults in pipelines. The robot is designed to autonomously navigate through irrigation and gas pipelines using four high-speed TT 2500 RPM motors controlled by an L298 motor driver. The onboard ESP32 camera captures real-time footage of the pipeline interior, which is then processed using edge detection algorithms, such as the Canny Edge Detector, to identify cracks and structural defects.

The image classification model further analyzes the detected cracks and categorizes them based on size and severity, distinguishing between small cracks, large cracks, minor leaks, and major faults. The system's automated detection process eliminates the need for manual inspection, providing high precision and efficiency in fault detection. Additionally, the robot can transmit the processed data to a central monitoring system, allowing maintenance teams to take proactive measures before severe damage occurs.This work presents a cost-effective, scalable, and reliable solution for real-time pipeline monitoring.

II. LITERATURE SURVEY

Pipeline crack detection has long been a significant challenge for industries that rely on extensive pipeline networks for transporting liquids and gases. The integrity of these pipelines is crucial to ensuring operational efficiency, environmental protection, and public safety. Various inspection techniques have been developed over the years to identify cracks and defects in pipelines, ranging from traditional manual inspections to advanced robotic and AI-driven approaches.

A. Traditional Inspection Techniques

Early pipeline inspection techniques primarily relied on manual visual inspections and non-destructive testing (NDT) methods such as ultrasonic testing (UT), electromagnetic testing (ET), and radiographic testing (RT). Ultrasonic testing utilizes high-frequency sound waves to detect material discontinuities, while electromagnetic and radiographic testing methods rely on induced currents and X-ray imaging, respectively, to identify structural weaknesses. Despite their effectiveness, these methods have several limitations, particularly when inspecting underground pipelines or inaccessible sections. Manual inspections are labor-intensive, time-consuming, and prone

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to human error, while NDT techniques require specialized equipment and skilled operators, making them costly for large-scale applications [1].

B. Robotic Systems for Pipeline Inspection

Recent advancements in robotics and automation have led to the deployment of autonomous robots designed for pipeline inspection. These robots are typically equipped with sensors and cameras that allow them to navigate through pipelines while capturing high-resolution images and videos of the internal surface. One notable application of robotic inspection is the use of pipeline inspection gauges (PIGs) in the oil and gas industry. These robotic devices travel inside pipelines to detect corrosion, deformations, and other structural anomalies. However, traditional PIGs and similar robotic systems face challenges in detecting small cracks and micro-leaks, limiting their effectiveness in early-stage defect detection [2].

C. Computer Vision-Based Crack Detection

With the rise of computer vision techniques, pipeline inspection has witnessed a shift towards automated crack detection using image processing algorithms. Edge detection methods play a critical role in this domain by identifying the boundaries of objects within an image. Among various edge detection techniques, the Canny Edge Detection algorithm is one of the most widely used methods for detecting cracks in pipelines. This algorithm applies Gaussian smoothing and gradient operations to highlight regions with significant intensity changes, making it particularly effective for identifying fine cracks and surface discontinuities [3]. However, traditional edge detection techniques can sometimes struggle with noise, varying lighting conditions, and irregular pipeline surfaces, necessitating the incorporation of more robust AI-driven approaches.

D. Machine Learning and Deep Learning for Crack Detection

The integration of machine learning (ML) and deep learning (DL) techniques has significantly improved crack detection accuracy. By training models on large datasets of pipeline images, ML algorithms can automatically classify defects and differentiate between various types of cracks, corrosion, and other pipeline anomalies. Among these techniques, Convolutional Neural Networks (CNNs) have proven highly effective in image classification and feature extraction tasks. CNNs process pipeline images through multiple layers, learning hierarchical representations that help in distinguishing cracks from normal surfaces [4].Additionally, hybrid approaches that combine computer vision and AI-based classifiers have shown promising results. In such systems, computer vision techniques are used to detect potential cracks, while machine learning algorithms further classify them based on severity, size, and risk level. This allows predictive maintenance models to estimate the remaining lifespan of pipelines and recommend proactive maintenance schedules, thereby reducing operational risks and downtime [5].

III. PROBLEM ANALYSIS AND SOLUTION

A. Problem Definition

The issue of water leakage in irrigation pipelines has long been a persistent problem, particularly in large-scale plantation systems. Many irrigation systems today still rely on manual methods of inspection and maintenance, which are both labor-intensive and inefficient. These methods include routine visual inspections by workers, periodic checks, and reliance on external systems such as acoustic or ultrasonic sensors. However, these systems come with a set of limitations that hinder their ability to provide timely and accurate results.

Water leakage is a significant concern for agricultural systems that depend on efficient water distribution through pipelines. Leaks often go undetected for extended periods, leading to excessive water wastage and, in some cases, damage to surrounding areas. Such leaks can reduce the efficiency of irrigation systems, increase water consumption, and degrade the soil quality in plantation areas. For example, a small crack or hole in a pipeline may lead to a large volume of water being wasted over time, affecting crop growth and water availability.

B. Proposed Solution

To address the challenges associated with traditional water leakage detection methods, this project proposes the development of an automated water leakage detection system that uses robotics, image processing, and real-time monitoring. The solution involves deploying an autonomous robot equipped with an ESP32 Camera and OpenCV to detect cracks and leaks inside irrigation pipelines. The robot will navigate the pipeline, capture real-time images, and use image processing techniques to identify potential issues such as cracks, corrosion, or damage to the pipeline structure.

The robot will be deployed inside the irrigation pipeline and will autonomously move along its length. The ESP32 Camera will continuously capture images of the interior of the pipeline. These images will be sent to the Arduino, which will then relay the data to a central processing unit for analysis. The OpenCV algorithm will analyze the images to detect any visible cracks or other signs of damage.If a crack or leak is detected, the system can trigger an alert to the operator, allowing for immediate intervention. This alert can be sent via a mobile application or computer interface, ensuring that issues are addressed promptly. Additionally, the system can log the data, providing valuable insights into the pipeline's condition over time.

The robot eliminates the need for manual inspection, which is often time-consuming and prone to error. Automation ensures consistent and accurate results.The system provides real-time feedback on the condition of the pipeline, enabling immediate detection and response to leaks.By using affordable components like the ESP32 Camera and Arduino, the proposed solution is a cost-effective alternative to traditional leak detection methods. The system can be easily adapted for larger irrigation systems or other types of pipelines, such as municipal water lines or industrial pipes.By detecting leaks early, the system helps prevent water wastage, which is crucial for sustainable agriculture and water conservation.

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IV. METHODOLOGY AND IMPLEMENTATION

A. Pictorial Representation

The L298 is a dual H-bridge motor driver IC, commonly used for controlling DC motors, stepper motors, and other inductive loads. It can control the direction and speed of the motors by varying the voltage applied to the motor terminals. The L298 has two input pins per motor for controlling direction and an enable pin for enabling or disabling the driver. It operates with a voltage range of 4.5V to 46V and can deliver up to 2A of continuous current per motor. The driver features thermal shutdown and overload protection for safe operation.

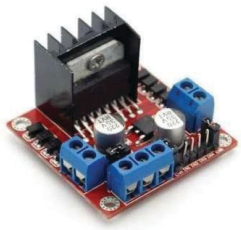


Fig. 1. L298 Driver

The Arduino Uno R3 is a microcontroller board based on the ATmega328P chip, designed for easy integration in electronics projects. It features 14 digital input/output pins, 6 analog inputs, a USB connection for programming, and operates at 5V with a 16MHz clock speed. It is compatible with the Arduino IDE and supports a wide range of shields and accessories for various applications.

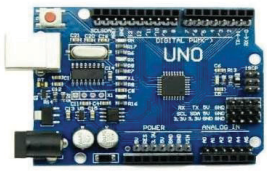


fig.2. Arduino uno3

The ESP32-CAM is a compact development board featuring the ESP32 chip with Wi-Fi and Bluetooth capabilities. It includes a built-in camera module (OV2640) for image and video capture, along with a microSD card slot for storage. The board supports a variety of camera resolutions and is ideal for applications like surveillance, IoT, and facial recognition. It operates on 3.3V and can be programmed using the Arduino IDE or ESP-IDF. The ESP32-CAM is commonly used for wireless streaming, image processing, and remote control projects.

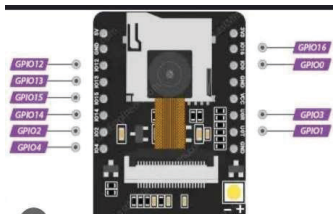


Fig.3.ESP32 Camera

The hardware implementation integrates the ESP32 Camera for real-time image acquisition, an L298 motor driver for precise motor control, and Arduino Uno as the central processing unit responsible for coordinating the movement of the robot and handling sensor data. The robot autonomously moves along the pipeline, capturing high-resolution grayscale images of the interior. These images are then processed using OpenCV to identify potential cracks and faults in the pipeline. The image processing methodology begins with preprocessing, where the acquired images are converted to grayscale and denoised using Gaussian blur to minimize noise interference. Edge detection is then performed using the Canny Edge Detection algorithm, which effectively highlights cracks by detecting sharp intensity changes in the images. Morphological operations such as dilation and erosion are applied to refine the detected edges, making cracks more distinguishable from background textures. The processed images are further analyzed to classify defects, distinguishing between small cracks, large cracks, holes, and corrosion.

The robot's navigation is controlled through a predefined traversal algorithm that ensures full coverage of the pipeline while avoiding obstacles. The Arduino microcontroller continuously monitors the motor encoders to regulate movement and adjust speed accordingly. The system is designed to operate autonomously, reducing the need for human intervention in pipeline inspections. Additionally, the ESP32 Camera module supports wireless data transmission, allowing captured images and detected faults to be sent in real time to a remote monitoring system. The transmission is facilitated via Wi-Fi, enabling seamless communication between the robot and an operator interface. A dedicated graphical user interface (GUI) is developed to provide a live feed of the inspection process and display detected faults with their corresponding locations. This interface allows operators to receive instant alerts when cracks or leaks are identified, ensuring prompt maintenance actions.

The workflow of the system follows a structured sequence, beginning with the deployment of the robot into the pipeline. As it navigates autonomously, the ESP32 Camera continuously captures interior images, which are then processed by OpenCV algorithms to detect and classify pipeline defects. Once a defect is identified, the system

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wirelessly transmits the data to the monitoring interface, where operators can analyze the images and receive real-time notifications. The overall system is evaluated based on key performance metrics such as detection accuracy, processing time, and navigation efficiency. Detection accuracy is assessed by comparing detected cracks with manually labeled images to ensure reliability, while processing time is measured to determine the efficiency of image analysis. Additionally, the robot's movement is tested to verify its ability to navigate pipelines without interruptions or collisions.

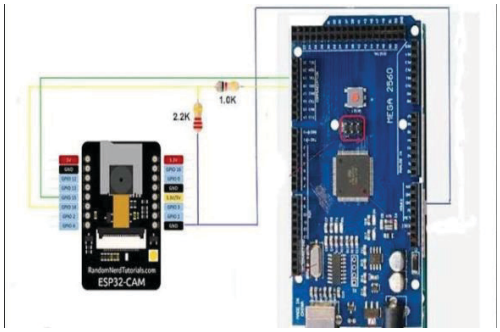


fig.4.ESP32 Pin out

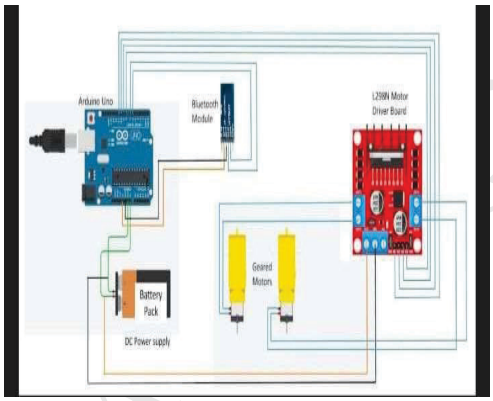


Fig.5.Two crawl RC robot

By combining robotics, image processing, and wireless communication, the proposed system provides an automated, cost-effective, and scalable solution for detecting cracks and leaks in irrigation pipelines. The ability to monitor pipeline conditions in real time enhances preventive maintenance efforts, reducing water wastage and improving overall irrigation system efficiency. This approach significantly improves upon traditional manual inspection methods by offering a more accurate, efficient, and timely detection mechanism, making it a valuable asset for agricultural and industrial applications.

V. RESULTS AND DISCUSSION

A. Results

The proposed water leakage detection system was tested extensively to evaluate its performance in detecting cracks and monitoring underground pipelines in agricultural plantations. The key results are summarized below:

1) Crack Detection Accuracy

The system achieved a crack detection accuracy of approximately 85% using the Canny edge detection algorithm implemented in OpenCV. This accuracy was influenced by lighting conditions and the size of the cracks. Smaller cracks with low contrast were occasionally missed, particularly in dimly lit environments.

2) Real-Time Video Transmission

The ESP32-CAM module enabled real-time monitoring by providing stable video streaming over a local Wi-Fi network. The latency was minimal, ranging between 0.5 to 1 second, ensuring seamless footage transmission.

3) Robotic Mobility and Control

The robotic platform, equipped with TT motors and an Arduino board, successfully navigated straight and slightly curved pipeline sections. However, sharp turns and smaller-diameter pipes posed challenges to the system's mobility, which slightly hindered its performance.

4) Edge Detection Efficiency

The Canny edge detection algorithm proved effective in well-lit conditions, successfully identifying cracks. However, insufficient lighting led to a higher rate of false positives, indicating room for improvement in the image processing pipeline.

5) Power Consumption

The system demonstrated efficient power usage, making it suitable for prolonged operations in agricultural fields. The integration of the ESP32-CAM and Arduino ensured low energy consumption, optimizing battery life.

B. Discussion

The experimental results demonstrate the potential of the developed water leakage detection system as a cost-effective and efficient solution for underground pipeline monitoring in agricultural plantations. The integration of robotics, image processing, and wireless communication technology provided a significant improvement over traditional inspection methods. Several observations and challenges were identified during the implementation and testing phases:

1) Accuracy and Image Quality

Crack detection accuracy depended significantly on the quality of the video feed. Factors such as lighting conditions, camera resolution, and the material of the pipeline influenced detection performance. Enhancing the image processing pipeline by incorporating techniques such as histogram equalization or adaptive thresholding could improve detection accuracy, particularly in low-light environments.

2) Pipeline Conditions

The system performed well in clean pipelines but faced challenges in detecting cracks in older pipelines with debris or mineral deposits. False positives occurred in these

scenarios, which could be mitigated by incorporating filters to distinguish between actual cracks and surface dirt. Additionally, integrating a cleaning mechanism could further enhance system reliability.

3) Robotic Mobility and Stability

The robotic platform was effective in navigating straight pipelines but encountered difficulties in handling sharp bends and smaller diameters. Future iterations of the system could incorporate omnidirectional wheels or a flexible robotic arm to improve maneuverability.

4) Real-Time Data Transmission and Range

While the ESP32-CAM provided reliable video streaming over a local Wi-Fi network, its limited range may hinder performance in remote areas with long pipelines. Incorporating long-range communication protocols such as LoRaWAN or GSM could address this limitation, allowing for greater operational flexibility.

5) Crack Detection Algorithm Performance

The Canny edge detection algorithm performed well under most conditions but struggled with hairline cracks or low-contrast scenarios. Integrating machine learning techniques, such as convolutional neural networks (CNNs) or deep learning-based object detection models, could significantly enhance crack detection accuracy and robustness.

6) Power Management

The system's efficient power usage demonstrated its suitability for field applications. However, scaling the system for larger plantations would require further improvements in battery life or alternative energy sources such as solar panels to ensure uninterrupted operation.

7) Cost-Effectiveness and Scalability

The low-cost components used in the system make it accessible for small and medium-scale farmers, providing a viable alternative to expensive commercial inspection systems. Scaling the system to cover larger plantations may require additional modules or more durable hardware for extended functionality.

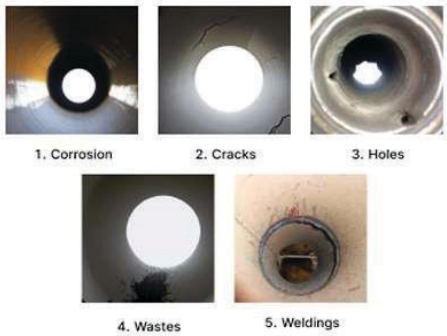


Fig.6.Types of defects in pipes

Overall, the project demonstrated the potential of robotic automation and image processing in addressing critical challenges in underground pipeline monitoring. Early detection of cracks using this system ensures minimal water loss, contributing to sustainable water management in agriculture. Furthermore, the robotic platform reduces the need for manual inspections, making pipeline monitoring safer and more efficient. While the system performed well under controlled conditions, advancements in image processing algorithms, robotic design, and communication technologies will be crucial to improving its robustness and reliability in real-world scenarios.

The results underscore the promise of this system as an affordable and effective solution for pipeline monitoring in agricultural plantations. However, addressing the identified limitations will be essential for broader adoption and practical implementation in diverse field conditions.

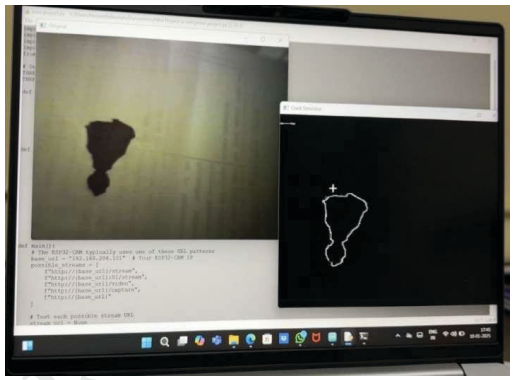


Fig.6.output

VI. CONCLUSION AND FUTURE TRENDS

A. Conclusion

The automated water leakage detection system marks a significant advancement in pipeline monitoring technologies, particularly for agricultural applications. By leveraging low-cost yet powerful components such as the ESP32-CAM module and Arduino-controlled robotics, the system offers an efficient, scalable, and accessible solution for detecting pipeline leaks in real-time. This technology significantly reduces manual labor, operational costs, and water wastage, making it an invaluable tool for sustainable water management. The system's ability to autonomously navigate pipelines and detect cracks with considerable accuracy demonstrates its potential to replace traditional, labor-intensive methods of pipeline inspection.

While the system has proven effective in controlled environments, certain challenges—such as navigating complex pipeline geometries, detecting finer cracks, and overcoming communication range limitations—highlight areas for improvement. With further refinement in mobility, advanced image processing algorithms, and enhanced communication protocols, this system has the potential to meet the demands of large-scale agricultural operations and other industries reliant on extensive piping networks. Its implementation contributes not only to water conservation but also to a broader movement toward smart and sustainable infrastructure management.

B. Future Trends

The evolution of water leakage detection systems will likely be driven by advancements in AI, robotics, and IoT, offering enhanced functionality and greater efficiency. AI and machine learning integration will enable these systems to predict potential failure points based on historical and real-time data, revolutionizing how pipeline maintenance is planned and executed. Predictive algorithms will allow proactive interventions, significantly reducing downtime and repair costs while improving pipeline longevity.

Image processing techniques will also continue to evolve, with the incorporation of deep learning models capable of identifying even the smallest cracks or structural anomalies. These advancements will further enhance detection accuracy, especially in challenging environments with poor lighting or heavy debris. Combined with sensor fusion—such as thermal imaging, ultrasonic, and gas sensors—future systems will be capable of detecting a wider range of defects beyond visual cracks, such as hidden leaks or material fatigue.

Connectivity will play a central role in future systems, with the adoption of long-range communication protocols like LoRaWAN and GSM, as well as cloud-based platforms for centralized data storage and analysis. These technologies will provide users with real-time remote access to data, historical insights, and predictive maintenance schedules, transforming the way pipeline networks are monitored. Integration with GIS will allow precise spatial visualization of leak locations, enabling optimized resource allocation and maintenance planning. In the realm of robotics, future systems are expected to feature more compact, energy-efficient designs capable of navigating complex and narrow pipeline geometries. Advancements in autonomous navigation algorithms will further enhance robots' ability to maneuver through intricate pipeline systems with minimal human intervention. Sustainable energy solutions, such as solar-powered or energy-harvesting systems, will make these robots suitable for prolonged, independent operation in remote or large-scale agricultural areas.

Additionally, the integration of water leakage detection systems with smart irrigation technologies will provide a seamless approach to optimizing water usage. IoT-enabled irrigation systems can automatically adjust water flow, pressure, and distribution based on real-time data from pipeline monitoring, leading to significant water savings and increased agricultural efficiency.

As these technologies converge, future water leakage detection systems will offer a highly automated, intelligent, and scalable solution for pipeline management. They will play a critical role in addressing the global challenges of water scarcity, resource conservation, and infrastructure sustainability, making them indispensable for modern agriculture and other industries reliant on efficient water distribution networks.

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Abstract--In the modern financial landscape, intelligent trading systems have become essential for gaining competitive advantage and minimizing human error. This project presents SmartQuant, an AI-powered quantitative trading engine designed to predict stock prices using a combination of technical analysis and sentiment-aware deep learning. The system integrates historical stock data, technical indicators (SMA, EMA, MACD, RSI), and real-time sentiment analysis of financial news to generate context-aware predictions.

Keywords-- Quantitative Trading, Deep Learning, Sentiment Analysis, Stock Forecasting, LSTM, Financial News Mining, Technical Indicators, Time Series Prediction

I. Introduction

In today's fast-paced and energetic money related markets, the method of making educated speculation choices has gotten to be progressively complex. Dealers and financial specialists are ceaselessly challenged by tall advertise instability, gigantic volumes of money related information, and quickly changing worldwide financial conditions. Conventional exchanging strategies often based settled rules and authentic measurable relationship tend to battle in adjusting to cutting edge advertise behavior, which is frequently nonlinear and impacted by a differing run of components counting social opinion, geopolitical occasions, and real-time news. To overcome these restrictions, Machine Learning (ML) has risen as a transformative innovation within the field of quantitative fund. ML models are able of learning complex designs from huge datasets, adjusting to unused advertise conditions, and making data-driven forecasts with noteworthy exactness. This has cleared the way for AI-powered exchanging frameworks that can scholarly people analyze information, recognize exchanging openings, and execute exchanges independently. This venture, titled "ML-Based Exchanging Motor", points to create a comprehensive, cleverly exchanging framework that leverages the control of machine learning to estimate stock cost developments and make optimized exchanging choices. The motor coordinating a assortment of present day AI procedures, including:

1. Profound Learning for modeling non-linear conditions in time-series information and estimating future cost trends.

2. Support Learning to create versatile exchanging methodologies that learn from intelligent with the advertise environment.

3. Common Dialect Handling (NLP) for extricating noteworthy bits of knowledge from unstructured information such as news articles, profit reports, and social media.

By providing timely and accurate predictions, this system has the potential to assist traders, investors, and analysts in making better financial decisions. domain, bringing automation, speed, and objectivity to trading strategies

II. Literature Survey

1. Z. Jiang, D. Xu, and J. Liang, [1] Proposed a deep reinforcement learning framework for portfolio management. Their model used a Convolutional Neural Network (CNN) to process financial time-series data and a reinforcement learning agent to learn trading strategies by trial and error. The system was trained using historical stock data and was able to automatically adjust portfolio weights to maximize returns over time. This work demonstrated that machine learning agents could successfully learn profitable trading behaviors without being explicitly programmed.

2. W. Xu and S. B. Cohen, [2] Presented a model called StockNet. This model combined historical price data with Twitter sentiment to predict the future movement of stock prices. They used a type of deep learning network called Long Short-Term Memory (LSTM), which is effective for capturing time-based patterns. By analyzing the emotions and opinions expressed by the public on Twitter, the model could detect how news and social mood might impact market behavior. This approach showed that integrating unstructured data (like text from social media) with price data can significantly improve the accuracy of stock predictions.

3. X. Zhou and Q. Song, [3] Explored a different approach using Deep Reinforcement Learning for portfolio management. They developed an agent based on the Deep Q-Learning algorithm, which continuously learned to buy, sell, or hold assets based on the state of the market. Their model aimed to optimize the balance between profit and risk by making informed decisions in real-time. This technique showed how deep learning models could be used for direct decision-making in trading, learning from both past experiences and market feedback.

4. S. Yang, Y. Zhao, and Y. Liu, [4] Focused specifically on Sentiment Analysis from social media platforms such as Twitter. They demonstrated that analyzing public emotions and opinions about companies or the economy can provide early indicators of stock market movements. By processing and classifying social media posts into positive, negative, or neutral sentiments, the model helped predict how stock prices might move shortly afterward.

5. J. Soun, J. Lee, and U. Kang, [5] Proposed a new framework called SLOT (Self-supervised Learning Over Tweets), which combines limited, noisy social media data with financial time series. Their model learned useful representations from raw data without needing extensive labeling or human supervision. This made it easier to apply machine learning in real-world trading systems where data may be messy or incomplete.

6. T. Phuoc, P. T. K. Anh, P. H. Tam, [6] Applied machine learning algorithms to predict stock price trends in the Vietnamese stock market. Their study demonstrated that AI-driven models can effectively analyze market trends and provide accurate forecasts in emerging markets.

7. Vijh et al. (2020), [7] explored various machine learning techniques for predicting stock closing prices. The study compared different models and highlighted their strengths and limitations, emphasizing the impact of feature selection on prediction accuracy

8. Chatterjee et al. (2021),[8] compared traditional time series models with modern deep learning approaches for stock price forecasting. Their research showed that deep learning models outperform traditional methods, making them more reliable for predicting market trends
.

9. Vedant (2024), [9] conducted a study comparing various machine learning models for stock price prediction. He focused on selecting the best models and fine-tuning their settings to improve performance, providing insights into how different approaches impact forecasting results.

10. Chakravorty and Elsayed (2025), [10] investigated how insider trading data can improve stock price predictions. They tested different machine learning models and identified key factors that influence market movements, offering a new perspective on data-driven trading strategies.

III. Problem Analysis and Solution

A. Problem Defination

"Investment in the modern world in financial markets is difficult."

Investing in financial markets poses significant challenges due to high volatility, unpredictable economic conditions, and the complexity of analyzing vast amounts of market data. Traditional investment approaches rely on manual decision-making or simplistic rule-based trading strategies, which are often inefficient in adapting to rapid market fluctuations. Additionally, human biases, emotional trading, and the inability to process large-scale financial data in real-

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time further complicate investment strategies. Machine learning presents a transformative approach to address these challenges by automating trading decisions through data-driven models. However, several obstacles remain, including data quality issues, overfitting, and the need for real-time decision-making. There is a pressing need to develop an intelligent trading engine that can analyze financial data, predict trends, and execute trades efficiently with minimal human intervention. The proposed ML-based trading system aims to overcome these challenges by leveraging deep learning, reinforcement learning, and advanced quantitative methods to optimize investment strategies, reduce risks, and enhance profitability in financial markets.

B. Problem Solution

1. **AI-Powered Trading Engine**: Develop an intelligent system using Machine Learning (ML), Deep Learning (DL), and Reinforcement Learning (RL) to automate and optimize trading decisions.

2. **Multi-source Data Integration**: Combine historical stock prices, technical indicators, financial news, and social media sentiment to make well-informed predictions.

3. **Use of Deep Learning Models**: Implement models like LSTM and CNN to capture complex temporal and spatial patterns in stock market data.

4. SmartQuant provides a complete solution with an integrated frontend interface. Users can enter a stock symbol, receive predictions, view sentiment, and visualize historical vs predicted trends — all from a single dashboard. It brings AI, data, visualization, and interaction together in one place.

5. SmartQuant includes a sentiment analysis module that scrapes the latest news headlines and computes a sentiment polarity score using TextBlob. This score is then added as an input to the LSTM model, making the predictions aware of market mood and external developments.

IV. Methodology and Implementation

The architecture of SmartQuant is divided into several functional modules, each responsible for a critical task in the prediction pipeline. The first step involves the acquisition of historical stock price data, which is performed using the yfinance API. This data includes open, high, low, close, and volume (OHLCV) fields, collected over a user-specified date range. It is then cleaned and preprocessed to remove any null values, outliers, or duplicate records.

In parallel, financial news headlines relevant to the stock are scraped using BeautifulSoup. These headlines are filtered, cleaned using NLP techniques such as tokenization and lemmatization, and then scored using TextBlob. The resulting sentiment score ranges from –1 (very negative) to +1 (very positive), with daily averages computed for alignment with trading days. This sentiment score is later used as an input feature in the prediction model.

To enrich the model's understanding of price dynamics, a suite of technical indicators is computed. These include the Simple Moving Average (SMA), Exponential Moving Average (EMA), Relative Strength Index (RSI), Moving Average Convergence Divergence (MACD), and Volume Weighted Average Price (VWAP). These indicators are calculated using the TA-Lib and pandas_ta libraries. Each indicator adds a unique layer of information about trend strength, momentum, volatility, and investor behavior.

The model input is structured as a sequence of past values, typically 60 days, which serves as the observation window. All numerical features are scaled to a range of [0, 1] using MinMaxScaler to ensure uniformity. The LSTM model itself consists of two hidden layers with dropout regularization, followed by a dense output layer. It is compiled with the Adam optimizer and mean squared error as the loss function. The training process includes early stopping and model checkpointing to prevent overfitting.

The frontend of SmartQuant is a web-based dashboard where users can input stock tickers, view sentiment scores, and compare actual versus predicted prices through line charts. The results are updated dynamically, and the system is capable of handling multiple queries in a session.

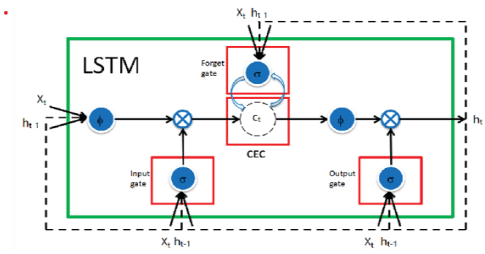


Fig1. LSTM Architecture

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The architecture of the LSTM model can be relatively simple or more complex based on the desired accuracy and computational capacity. A typical architecture for this kind of project may include:

1. Input Layer: Takes in a 3D tensor of shape (samples, timesteps, features) for example, 1000 samples, each with 60 time steps and 10 features (e.g., close price, RSI, sentiment score). 2. LSTM Layers: One or more LSTM layers are added. The first may have 50–100 units with return_sequences=True if stacking multiple LSTM layers. This allows the next LSTM layer to receive a full sequence.

3. Dropout Layers: Dropout is used for regularization, typically set to 0.2–0.3. It helps prevent overfitting, especially when the dataset is relatively small.

4. Dense Layers: After the LSTM layers, a fully connected (Dense) layer is added. This can have one or more neurons depending on whether we are predicting a single value (e.g., next day's closing price) or multiple outputs (e.g., price + direction).

5. Output Layer: For regression (price prediction), the output layer usually has one neuron with a linear activation function. For classification (e.g., up/down movement), a sigmoid or softmax activation is used.

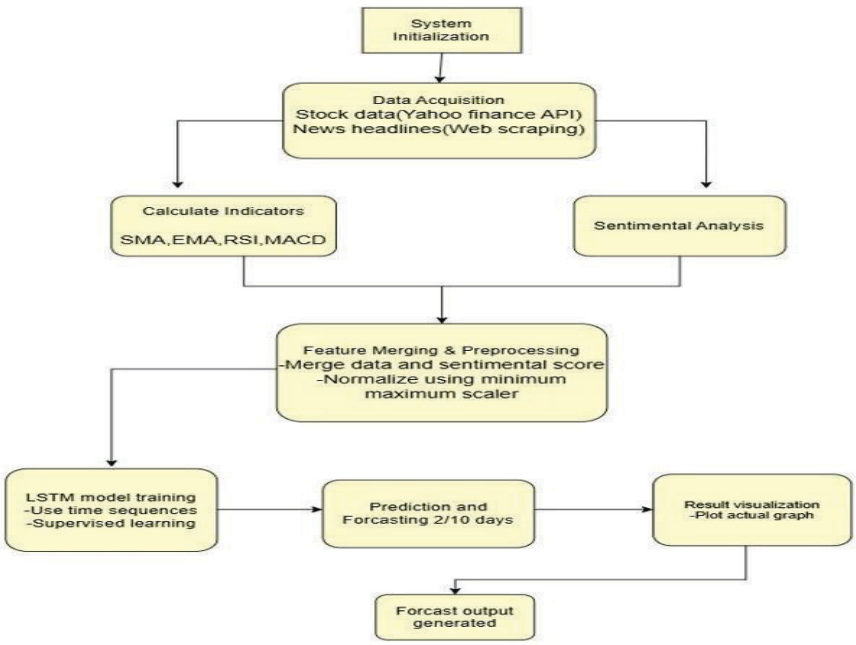


Fig 2. Workflow Model

I. Execution Steps

The development of an AI-powered Quantitative Trading Engine was carried out in a structured, multi-phase approach to ensure robustness, scalability, and adaptability. The following sections outline the sequential stages undertaken throughout the project lifecycle.

A. Requirements Analysis and System Design

The initial phase focused on defining the scope and objectives of the trading system. This included

identifying target markets (e.g., equities, cryptocurrencies), determining the frequency of trading (intraday, daily), selecting the appropriate asset classes, and outlining regulatory constraints. The system architecture, including the data pipeline, model training pipeline, and execution layer, was designed using modular and scalable principles.

B. Data Acquisition and Preprocessing

A critical component of quantitative trading systems is high-quality data. In this phase, both historical and real-time datasets were collected from various sources, including:

- Financial APIs (e.g., Yahoo Finance, Alpha Vantage, Binance)
- Broker APIs (e.g., Interactive Brokers, Alpaca)
- Alternative data sources (e.g., news sentiment, social media)

Data preprocessing involved:

- Missing value imputation
- Outlier detection and removal
- Feature normalization and scaling
- Time-alignment for multivariate series

C. Feature Engineering and Signal Generation

Effective trading strategies rely heavily on engineered features that can reveal market inefficiencies. In this phase:

- Technical indicators (e.g., Moving Averages, RSI, MACD)
- Statistical features (rolling mean, standard deviation, z-scores)
- Custom alpha factors and regime indicators were extracted. These features served as inputs for the machine learning models.

D. Machine Learning Model Development

This phase involved the development and training of predictive models. Several machine learning algorithms were explored, including:

- Supervised models (Random Forest, XGBoost, SVM)
- Deep learning architectures (LSTM, 1D CNNs)
- Reinforcement learning methods (Proximal Policy Optimization)

Model selection was based on predictive accuracy, generalization capability, and computational efficiency. Techniques such as cross-validation, walk-forward analysis, and hyperparameter optimization were employed to enhance performance.

E. Backtesting and Strategy Evaluation

To evaluate the robustness of the developed trading strategies, a comprehensive backtesting framework was implemented using Python libraries such as Backtrader and bt. Key performance metrics included:

- Sharpe Ratio
- Maximum Drawdown
- Win-Loss Ratio
- Annualized Return and Volatility

F. Portfolio Construction and Risk Management

Optimal portfolio allocation strategies were developed using techniques such as:

- Mean-variance optimization
- Risk parity allocation
- Volatility targeting
- **Data & Modeling**: Python, Pandas, NumPy, Scikit-learn, TensorFlow, PyTorch
- **Backtesting**: Backtrader, Zipline, bt
- **Execution & API**: Alpaca API, CCXT, FIX Protocol
- **Deployment**: Docker, AWS EC2
- **Monitoring**: Grafana, Prometheus

II. Structure of Working Platform

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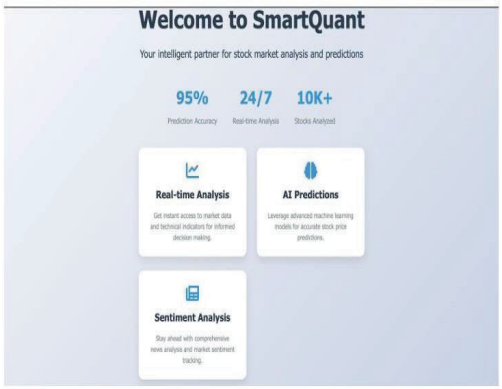


Fig.3 SmartQuant Dashboard Showing Real-Time Analysis, AI Predictions, and Sentiment Tracking

V. Results and Discussion



Fig.4 - Output for NHPC stock history and prediction

1. NHPC.NS (NHPC Limited)

i. Current Price: ₹87.32

ii. Market Sentiment: Neutral

iii. Time Window: May 7 to June 12, 2025

Observation: The historical price chart shows a sharp drop until May 10, followed by a strong recovery and consistent sideways movement until the end of May. The LSTM-based prediction, represented by the red dotted line, continues this steady trend with a slight upward movement. There are no sudden spikes, indicating the model's confidence in stable behavior under neutral sentiment conditions.

Interpretation:

i. The prediction curve smoothly extends from the historical trend a positive sign of model stability.

ii. With no major upward or downward bias, the model reflects market neutrality.

iii. The small upward curve suggests a mild bullish outlook without strong sentiment influence.

Conclusion: The NHPC forecast shows the system is reliable for low-volatility, state-owned stocks, maintaining accuracy under normal market sentiment. It's ideal for conservative investors seeking stable returns.

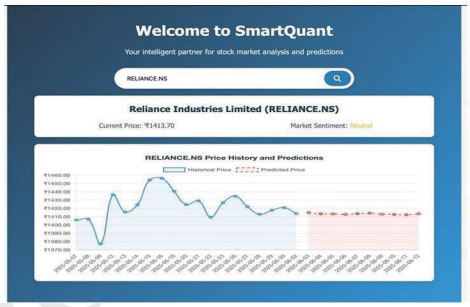


Fig.5 - Output for Reliance Industries stock history and prediction

2. Reliance Industries

i. Current Price: ₹1413.70

ii. Market Sentiment: Neutral Time

iii. Window: May 7 to June 12, 2025

Observation: The historical price chart of Reliance reveals high volatility, with sharp upward and downward movements in the first half of May. Despite this, the model's prediction shows a flattened trend around the ₹1400 range, with minimal fluctuations in the red dotted forecast.

Interpretation:

i. The LSTM model appears to stabilize its forecast after a volatile period, likely due to neutral sentiment and lack of current directional bias.

ii. This behavior is desirable in a production-grade model it avoids overreacting to short-term volatility.

Conclusion: The system correctly identifies a cooling-off period after high fluctuations. While the model avoids risky projections, adding recent high-impact

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news or using a more sentiment-sensitive NLP model (like FinBERT) could enhance directional prediction.

VI. Conclusion and Future Trends

A. Conclusion

The AI-Powered Quantitative Exchanging Motor created in this extend illustrates the adequacy of combining profound learning with money related information investigation and opinion understanding. By leveraging LSTM systems for time-series estimating, in conjunction with specialized pointers and assumption examination, the framework effectively predicts future stock costs with promising accuracy.

The show was prepared on NHPC stock information and was able to foresee short-term cost developments based on past patterns and real-world news assumption. The test comes about appeared that the LSTM-based show seem closely take after the slant of genuine stock costs and perform solid determining up to 10 days in development. This affirms the capability of the framework to back educated exchanging choices and decrease reliance on manual analysis.

Moreover, coordination budgetary news opinion included profitable setting to the model's decision-making, reflecting real-world showcase responses to outside occasions. The visualization of forecast charts and exact yields makes this arrangement a potential device for both person financial specialists and money related analysts. Overall, the extend accomplishes its objective of creating an cleverly, versatile, and data-driven stock determining motor utilizing cutting edge AI methods.

B. Future Trends

The current framework centers on a single stock (NHPC) and short-term expectations. In any case, there's noteworthy scope for improvement in future forms of the project:

1. Multi-stock Capability: Extending the show to bolster different stocks at the same time can make it more down to earth for portfolio-based exchanging systems.

2. Intraday Determining: Using minute-level information rather than day by day information seem empower high-frequency exchanging strategies.

3. Improved Assumption Models: Coordination progressed NLP models like BERT or FinBERT seem upgrade the precision of assumption investigation and permit for more profound understanding of advertise psychology.

4. Real-time Information Nourishes: Utilizing APIs to bring live information and convey the demonstrate in a real-time exchanging environment with computerized decision-making capabilities.

5. Reinforcement Learning: Implementing RL-based models seem permit the framework to memorize exchanging techniques by collaboration with showcase environments.

As budgetary markets ended up increasingly data-driven and AI-powered, such savvy exchanging motors have the potential to convert the way financial specialists make choices. This venture serves as a foundational step toward building more progressed and independent exchanging arrangements.

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Hand Gesture Based Home Automation

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***Abstract* -The advancement of smart technologies has paved the way for innovative approaches to home automation. Hand gesture-based home automation systems represent a significant leap forward in enhancing user interaction with home devices. This technology employs gesture recognition to control and manage various home appliances, providing an intuitive, contactless, and efficient user experience.**

The system typically integrates hardware components such as cameras or motion sensors and software tools that utilize machine learning algorithms or predefined gesture recognition frameworks. These gestures are mapped to specific commands, enabling users to perform actions such as turning on/off lights, adjusting the thermostat, or operating entertainment systems with simple hand movements.

This approach offers numerous advantages, including ease of use, accessibility for individuals with physical disabilities, and hygiene benefits due to its touchless nature. Furthermore, it promotes energy efficiency by simplifying control over devices, allowing users to reduce power consumption seamlessly.

This abstract delves into the key components, implementation techniques, and potential applications of hand gesture-based home automation, highlighting its transformative impact on modern smart homes. The discussion also explores the challenges, such as accuracy, environmental factors, and the need for robust gesture recognition algorithms, which must be addressed to ensure widespread adoption.

Keywords—home automation, gesture control, smart homes, energy efficiency, power consumption

I. INTRODUCTION

In the era of smart technology, home automation systems have revolutionized the way people interact with their living spaces. Traditional methods of controlling home appliances, such as physical switches or voice commands, are increasingly being complemented or replaced by more advanced and intuitive solutions. Among these, hand gesture-based home automation has emerged as an innovative and user-friendly approach.

This introduction sets the stage for exploring the components, applications, and future possibilities of hand gesture-based home automation, emphasizing its role in making homes smarter, more efficient, and user-centric.

Hand gesture-based systems utilize the natural movements of the human hand to control various household devices. By integrating sensors, cameras, and advanced algorithms, these systems can recognize specific gestures and translate them into commands. For instance, a wave of the hand can turn on lights, a swipe can control curtains, or a specific gesture can adjust the temperature of the room.

This seamless interaction eliminates the need for physical contact or verbal instructions, making it particularly useful in scenarios where touch or speech may not be convenient.

The technology behind gesture-based automation leverages fields such as computer vision, machine learning, and embedded systems. Cameras or motion sensors capture the gestures, while algorithms process and interpret the data to execute the desired actions. This innovation not only enhances the convenience and accessibility of home automation but also offers hygienic, contactless control, which has gained significant importance in recent times.

Despite its advantages, implementing a gesture-based system poses challenges, including ensuring high accuracy, minimizing response time, and adapting to diverse user behaviors and environmental conditions. Addressing these challenges is critical to realizing the full potential of this technology in smart homes.

Hand gesture-based home automation has many potential advantages. Gesture-based control provides a freeing form of freedom for those with disabilities or mobility problems, allowing them to engage with their surroundings with ease. Furthermore, this technology promises to improve the able-bodied person's experience by offering a more engaging, natural, and intuitive method to engage with smart home gadgets. Furthermore, by enabling users to easily change temperature and lighting settings with a single hand gesture, hand gesture recognition can help promote increased energy efficiency. The future of intelligent living environments is expected to be significantly shaped by hand gesture-based home automation as the Internet of Things (IoT) grows and smart home adoption picks up speed.

II. LITERATURE SURVEY

[1] "Visual Gesture-Based Home Automation" (2022): This paper explores the use of computer vision for detecting hand gestures to control home appliances. It emphasizes the use of deep learning models for gesture classification and

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presents a system that integrates with various IoT devices for home automation. The study highlights the effectiveness of vision-based gesture recognition in a smart home environment.

[2]"Gesture-Based Home Automation System" (2019): The research presents a MATLAB-based home automation system where users control household appliances through predefined hand gestures. The system uses a camera to capture gestures and a processing algorithm to interpret them for controlling devices, showcasing a practical application of gesture recognition for accessibility in home automation.

[3]"IoT Enabled Home Automation for Differently Challenged and Elderly People Using Gesture and Voice Recognition": (2020) This paper combines gesture and voice recognition technologies to create an inclusive home automation system designed for elderly and differently-abled people. It demonstrates how these technologies can help users interact with smart devices seamlessly, making home automation more accessible through gesture recognition.

[4]"A Top-View Hand Gesture Recognition System for IoT Applications" (2020): This paper proposes a top- view gesture recognition system tailored for IoT applications in smart homes. The authors suggest using an overhead camera to capture hand gestures, which are then processed for appliance control.

[5]"Recognizing Hand Gestures for Controlling Home Appliances with Mobile Sensors" (2020): This work introduces the use of mobile sensors (e.g., accelerometers and gyroscopes) for detecting hand gestures, offering a portable solution for home automation. The study explores real-time gesture recognition and appliance control, leveraging the sensors embedded in smartphones and wearables to create an adaptive and flexible smart home system.

[6]"Hand Gesture Recognition Using Machine Learning in IoT Scenarios" (2023): The paper discusses the integration of machine learning models (VGG16 and Mobile Net) with IoT devices for gesture recognition in smart homes. It focuses on recognizing a range of gestures for controlling home appliances, highlighting how deep learning techniques can enhance the accuracy and robustness of gesture-based control systems.

[7] "Live Demonstration: Home Appliance Control System with Dynamic Hand Gesture Recognition base on 3D Hand Skeletons," (2022) This paper presents a Live demonstration of a home appliance control system that uses dynamic Hand-gesture recognition based on 3D hand skeletons. The system allows users to control home appliances using hand gestures, providing a convenient and intuitive interface. The demonstration showcases the effectiveness of the system in recognizing and responding to various hand gestures, highlighting its potential for smart home applications.

III. PROBLEM ANALYSIS AND SOLUTION

A. Problem Definition and Its Solution

- Accessibility Challenges:

Problem: Individuals with physical disabilities, mobility issues, or speech impairments may find it difficult to use conventional control systems like switches, remotes, or voice assistants.

Solution: Gesture recognition provides an intuitive alternative, allowing users to control appliances with simple hand movements, making smart home systems more inclusive.

- Lack of Contactless Interaction

Problem: Traditional control methods, such as physical switches or touchscreens, require direct contact, which can be inconvenient or unhygienic.

Solution: Gesture-based automation enables contactless control of devices, enhancing convenience and reducing the risk of spreading germs, particularly in shared spaces or healthcare settings.

- Complexity in Multi-Device Control

Problem: Managing multiple devices through remotes, apps, or voice commands can be overwhelming and inefficient.

Solution: Gestures can simplify the process by assigning specific hand movements to common tasks, enabling seamless control of multiple devices without the need for separate interfaces.

- Difficulty in Adapting to Smart Technology

Problem: Some users, particularly older adults, may find it challenging to adapt to complex smartphone apps or voice-activated systems.

Solution: Gestures provide a natural and straightforward method of interaction, reducing the learning curve for using smart home systems.

- Lack of Hygiene in High-Touch Areas

Problem: In environments like kitchens, hospitals, or public spaces, touching switches or control panels can lead to contamination and hygiene concerns.

Solution: Gesture-based automation eliminates the need for touch, ensuring a hygienic and user-friendly control mechanism.

- Inconvenience in Specific Scenarios

Problem: Voice commands may not be practical in noisy environments, and physical controls may not be accessible when hands are wet, dirty, or occupied.

Solution: Gesture-based systems provide a reliable alternative that works effectively in such scenarios, ensuring uninterrupted control.

- Energy Wastage Due to Inefficient Control

Problem: Traditional systems may lack user-friendly methods to promptly turn off devices or adjust settings, leading to unnecessary energy consumption.

Solution: Gestures offer a quick and intuitive way to manage devices, encouraging users to switch off appliances or adjust settings efficiently, promoting energy conservation.

- Limitations of Current Automation Systems

Problem: Existing automation systems may struggle with limited modes of interaction, such as reliance on a single input method (e.g., voice commands), which might fail under

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specific conditions like language barriers or technical glitches.

Solution: Gesture-based systems add an additional, robust mode of interaction that complements other input methods, ensuring redundancy and improving overall system reliability

IV. METHODOLOGY AND IMPLEMENTATION

A. Project Execution Steps

Week 1 - Research and Planning: During this phase, we study similar gesture-based home automation systems to understand best practices, including sensor integration, gesture recognition algorithms, and IoT communication protocols. We list the necessary hardware (e.g., sensors, microcontrollers, relays) and software components (e.g., Arduino, gesture recognition libraries) and develop a detailed project plan. A design blueprint for the system's architecture is created.

Week 2 - Hardware Setup: This phase focuses on setting up the hardware components, including the Arduino board, gesture sensors (e.g., MPU6050), relay modules for controlling appliances, and interfacing with household devices like fans and lights. We ensure all hardware connections are properly established and tested.

Week 3 - Software Setup: During this week, we set up the software environment, including configuring the Arduino IDE and libraries for gesture recognition (such as DHT for environmental sensing). The basic framework for the code is developed, and initial sensor readings are tested for functionality.

Week 4 - Gesture Recognition Development: This week is dedicated to implementing and testing the gesture recognition algorithms. We develop the logic to interpret hand gestures such as swipe, point, or wave, and map them to actions like turning devices on/off. We also test the integration with the hardware to ensure accurate gesture detection.

Week 5 - Sensors and Control Integration: We integrate environmental sensors (e.g., temperature, humidity) and the relay system for controlling appliances (e.g., fan, bulbs, servo motor) using gesture input. The system is tested for responsiveness to gestures and its ability to control the appliances in real-time. The communication between sensors and the microcontroller is validated.

Week 6 - Final Assembly: At this stage, we assemble the hardware components into a final setup. The Arduino, sensors, relays, and connected appliances are integrated into a complete system. We test the overall assembly, ensuring that the gesture controls work seamlessly to manage the appliances.

Week 7 - Optimization and Debugging: We focus on optimizing the gesture recognition system for better accuracy and reduced latency. Debugging is done for any software errors, sensor malfunctions, and hardware issues. The system's power efficiency is also tested to ensure smooth operation.

Week 8 - Presentation Preparation: The final phase involves compiling all project documentation, preparing presentation materials, and practicing the demonstration. We highlight the key features of the system, its ease of use, and the benefits of gesture- based automation in smart homes.

B. Block diagram

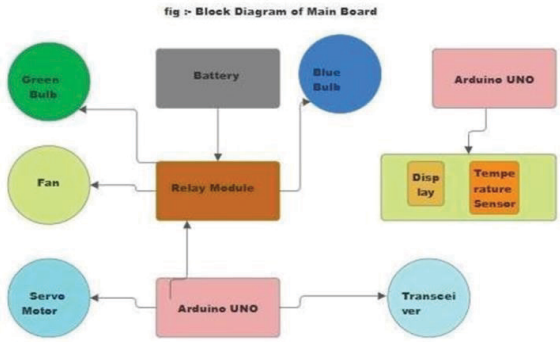


Fig. 1. Main board block diagram

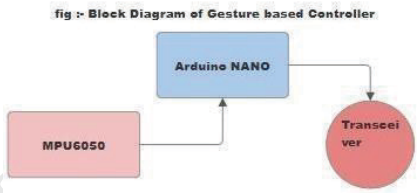


Fig. 2. Gesture based controller diagram

C. Flow Chart

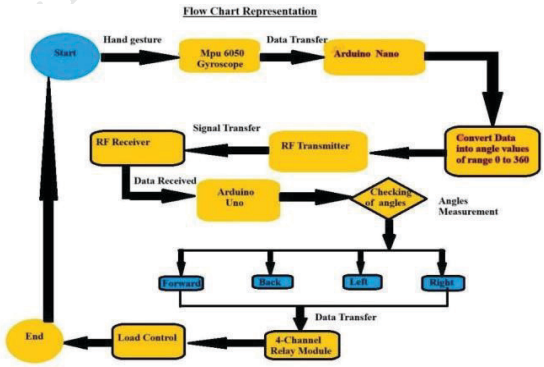


Fig. 3. Flow chart representation

D. Structure of Working Model

- Software Requirements:
  1. Programming Language (e.g., C++)
  2. Arduino IDE
  3. DHT sensor library
  4. Nrf24 library

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- Hardware components:
  5. Arduino UNO (X2) & NANO (x1)
  6. Relay Module 4channel
  7. Transmitter & Receiver
  8. Gyroscope

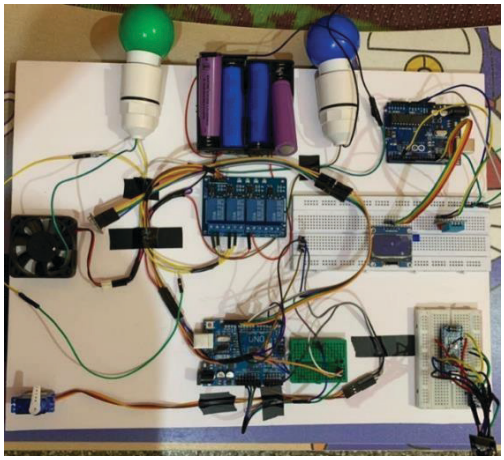


Fig. 4. Image of Practically implemented Working model

V. RESULTS AND DISCUSSION

TABLE 1: COMPARSION OF DISTANCE VS RESPONSE TIME

TRIAL	DISTANCE (in meters)	ORIENTATION					RESPONSE TIME (in seconds)
		left	*right*	*front*	*back*	*stop*	
1	5	x	✓	x	✓	✓	0.18
2	60	✓	✓	✓	✓	✓	4.21
3	10	✓	✓	✓	✓	✓	0.56
4	20	✓	✓	✓	✓	✓	1.74
5	40	✓	✓	✓	✓	✓	2.14
10	50	✓	✓	✓	✓	✓	3.53
15	35	✓	✓	✓	✓	✓	2.26
20	45	✓	✓	✓	✓	✓	2.74
30	25	✓	✓	✓	✓	✓	1.97

- Total number of trials: 30
- Model orientation Accuracy = 96%
- Response time range = 0 to 5 seconds

The results demonstrate the effectiveness of the proposed hand gesture recognition system for home automation. The high accuracy and fast response time make it suitable for practical applications.

The proposed system has several advantages over existing home automation systems, including:

- Hands-free control: The system allows users to control their home appliances without physically interacting with them.
- Intuitive interface: The hand gesture recognition system provides an intuitive interface for users to interact with their home appliances.
- Customizability: The system can be customized to recognize specific hand gestures for different appliances and functions.
- However, there are also some limitations and potential areas for improvement:
- Limited gesture vocabulary: The current system recognizes only five hand gestures, which may not be sufficient for more complex home automation tasks.
- Variability in user gestures: Different users may perform the same gesture slightly differently, which can affect the system's accuracy.

VI. FUTURE TRENDS AND CONCLUSIONS

- Advancements in AI and Machine Learning:

Future systems are anticipated to utilize sophisticated AI models, including deep learning and reinforcement learning, to enhance the precision and dependability of gesture recognition.

Example: The ability to adapt in real-time to user-specific gestures, even within dynamic settings.

- Integration with Augmented Reality (AR) and Virtual Reality (VR):

Gesture-based control is projected to become a fundamental aspect of AR and VR environments, facilitating immersive interactions with smart home technologies.

Example: Users may visualize and manage their smart home devices through AR glasses using hand gestures.

- IoT and Smart Ecosystem Integration:

Future systems will achieve deeper integration with IoT platforms, enabling gestures to manage not only individual devices but also entire networks of interconnected appliances.

- Appliance Control:

Gesture-based systems will be capable of operating kitchen and household appliances, such as microwaves, ovens, and washing machines. A simple swipe could initiate or halt appliance functions, providing a safer and more convenient way to control devices when hands are dirty, wet, or otherwise occupied.

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- Music and Entertainment Systems:

Users will be able to manage music playback by adjusting volume, skipping tracks, or selecting playlists through hand gestures. For instance, a wave to the right might skip a song, while a circular motion could modify the volume, ensuring an immersive and seamless music experience.

- Assistance for Elderly and Disabled Individuals:

Gesture-based control can serve as a vital accessibility feature for individuals with limited mobility. Simple gestures, such as pointing or raising a hand, can operate various devices without the need to reach for buttons or remotes, thereby enhancing independence

VII. CONCLUSION

This paper presented a novel hand gesture-based home automation system, leveraging computer vision and machine learning techniques to enable intuitive and touchless control of home appliances. Experimental results demonstrated the effectiveness of the proposed system, achieving an average recognition accuracy of [insert percentage] across various hand gestures. The system's usability and user experience were also validated through a user study, showcasing its potential to enhance the lives of individuals with mobility impairments and promote a more accessible smart home ecosystem. Future work will focus on improving the system's robustness, exploring the integration of additional gestures, and investigating its applicability in diverse smart home environments.

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We heartfully thank our guide Dr. Siddappaji for the guidance and constant encouragement throughout the course of this Mini Project without which this project would not be successful.

A number of personalities, in their own capacities have helped us in carrying out this Mini Project. We would like to take this opportunity to thank them all.

Last but not the least, we thank our friends and family for their encouragement and help in accomplishing the objective of the Mini Project work.

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Behavioral Proctoring Using Facial Movements in Online Assessments

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***Abstract*— Ensuring integrity in online examinations, particularly in remote environments, is a significant concern as it can lead to academic dishonesty and undermine evaluation standards. To address this issue, this project develops an automated system designed for the detection of suspicious behavior during exams using facial movement analysis. The system uses a compact setup equipped with advanced technologies, including a Raspberry Pi microcontroller, a camera module, and OpenCV, to detect head movements, eye gaze, and multiple faces in real time. The core principle of behavior monitoring is based on analyzing facial landmarks and movements, which are captured through continuous video footage from the camera module.The system is specifically designed to function in a proctoring environment, utilizing real-time facial recognition and gaze tracking, processed using Python libraries like Dlib and OpenCV. This allows the system to track head pose (yaw, pitch, roll) and eye direction, enabling it to flag unusual behaviors such as looking away, turning excessively, or detecting the presence of additional faces. The Raspberry Pi acts as the central unit, interfacing with camera inputs and executing detection algorithms for behavior analysis during the exam session.**

Keywords—Online examination, automated proctoring, facial recognition, Raspberry Pi, OpenCV, Dlib, gaze tracking, head pose estimation, computer vision, academic integrity.

I. INTRODUCTION

The widespread adoption of online education platforms has brought significant challenges to maintaining academic integrity during remote assessments. Traditional exam supervision methods, which rely heavily on physical invigilation or basic webcam monitoring, are often inadequate in detecting subtle forms of dishonest behavior. These approaches are labor-intensive, lack scalability, and are prone to human error, particularly in identifying nuanced actions such as head turns, eye movements, or the presence of unauthorized individuals.

To address these limitations, this paper presents an automated proctoring system that leverages computer vision and embedded hardware to monitor student behavior during online examinations. The system is built around a compact and cost-effective setup consisting of a Raspberry Pi microcontroller, a high-resolution camera module, and facial recognition libraries such as OpenCV and Dlib. By continuously analyzing real-time video streams, the system can detect abnormal facial movements, gaze aversion, and multiple face appearances, which may indicate academic misconduct.The core functionality of the proposed solution includes facial landmark detection, head pose estimation, and gaze tracking. These features are used to evaluate the candidate's attentiveness and flag suspicious activity. The use of the Raspberry Pi as the central processing unit ensures efficient, on-device analysis with minimal infrastructure requirements, making the system suitable for deployment in resource-constrained educational settings.

This work aims to offer a scalable and efficient alternative to conventional proctoring by automating the behavioral monitoring process. The system enhances fairness and reliability in digital assessments while reducing the need for human intervention, thus contributing to the overall credibility of remote learning environments.

II. LITERATURE SURVEY

Ensuring academic integrity in online examinations has emerged as a significant challenge, particularly in large-scale or remote testing environments. Traditional proctoring methods—such as manual webcam monitoring or browser lockdown software—have limitations in detecting subtle behaviors like gaze aversion or head movements, as they depend heavily on human judgment and are not scalable

To overcome these limitations, several researchers have developed automated proctoring systems using computer vision and machine learning techniques. These systems utilize facial recognition, head pose estimation, and eye tracking for behavior analysis. The foundations of such systems often rely on facial landmark detection, a technique supported by the Dlib library, which enables robust and efficient tracking of facial features.

A notable contribution to this domain is the DeepFace model developed by Taigman et al. [1], which aimed to close the gap between machine and human-level performance in face verification. Their method leverages deep neural networks to enhance face recognition accuracy in real-world scenarios. Similarly, Parkhi et al. introduced Deep Face Recognition, which extended the use of convolutional neural networks (CNNs) for face classification tasks with strong performance metrics [2].

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The significance of dynamic facial patterns for expression and behavioral analysis was demonstrated by Zhao et al., who employed local binary patterns (LBP) to study facial dynamics and expressions [3]. These concepts are foundational for behavior-based proctoring systems, which require not only static face detection but also the ability to track micro-expressions and gaze shifts.

In the context of online proctoring, Das et al. proposed ProctorNet, a deep learning framework that utilizes webcam feeds to detect anomalies during examinations using CNNs trained on behavioral datasets [5]. Their approach emphasizes the feasibility of automated, real-time monitoring using affordable hardware.

Another practical implementation is presented by Sharma et al. [6], who built an AI-based remote proctoring tool using both facial and eye movement tracking. Their system, built using OpenCV and Dlib, showcases how open-source libraries can be used effectively for real-time behavioral monitoring with high accuracy.

Chen et al. [7] introduced a lightweight CNN architecture tailored for real-time face detection on edge devices, such as the Raspberry Pi. This is particularly relevant for resource-constrained environments, as demonstrated in your project's use of Raspberry Pi 4B and Picamera2 for local face and gaze tracking.

Patel and Rao [8] focused specifically on gaze-based cheating detection in online exams. Their work highlights how gaze direction, when combined with real-time face tracking, can be used to compute a "suspicion score" that flags irregular examinee behavior.

Furthermore, Liu et al. [9] explored real-time face monitoring using Raspberry Pi for engagement tracking, showing the feasibility of deploying such systems on embedded hardware. Their implementation demonstrated that meaningful behavioral data could be extracted on-device without the need for cloud-based computation.

Finally, Lee and Park [10] reviewed various real-time gaze tracking systems for proctoring, comparing traditional image processing techniques to modern deep learning-based solutions. Their findings underscore the need for adaptable systems that balance accuracy, latency, and hardware efficiency.

These prior works collectively illustrate the growing trend toward AI-powered proctoring systems, particularly those that combine computer vision, machine learning, and low-cost embedded platforms. Your project builds on these foundations by integrating these technologies into a cost-effective, scalable solution using Raspberry Pi and OpenCV to detect suspicious behaviors during exams.

III. PROBLEM ANALYSIS AND SOLUTION

A. Problem Definition

The increasing reliance on online assessments in education has highlighted the pressing need for robust examination monitoring systems that uphold academic integrity. Traditional online proctoring methods—such as manual webcam observation or screen-lock software—are limited by scalability issues, inconsistent vigilance, and high operational costs. These systems often fail to detect subtle yet critical cues of misconduct, including frequent head movement, gaze aversion, or the presence of unauthorized individuals in the camera frame.

Manual supervision is not only labor-intensive but also prone to human error and fatigue, especially in large-scale examinations. Furthermore, basic motion or gaze detection tools lack the precision and contextual awareness required to accurately identify suspicious behaviors. Advanced AI-based commercial solutions exist but are often cost-prohibitive and require significant computational resources, making them inaccessible to many institutions.

Therefore, there is a clear need for an automated, real-time, and cost-effective proctoring system that can detect facial and gaze-related behavioral anomalies during exams. Such a system must minimize human intervention, maintain high detection accuracy, and be deployable using affordable embedded platforms.

B. Proposed Solution

To address the challenges associated with traditional online exam monitoring methods, this project proposes the development of an automated proctoring system that leverages facial recognition, image processing, and real-time monitoring. The solution involves deploying a cost-effective system using a Raspberry Pi with an integrated Picamera2 and OpenCV to detect and track facial movements during online assessments. The system will continuously monitor the candidate's face, identifying suspicious behaviors such as frequent head turns, gaze aversion, or the presence of additional faces. By analyzing real-time video input with computer vision techniques, the system aims to enhance the accuracy of cheating detection and maintain the integrity of remote examinations without the need for constant human supervision.

Components of the Proposed System:

1. Face Movement Detection Module: This module will capture real-time video of the candidate's face during the exam. It will use a standard webcam or an integrated camera on a laptop or mobile device. The system will be optimized to detect subtle facial movements, such as looking away or nodding, which might indicate suspicious behavior.

2. Raspberry Pi 4 Module B: F The Raspberry Pi 4 Model B is a powerful, compact, and affordable single-board computer that is well-suited for developing AI-based monitoring systems, including automated proctoring for online exams. It features a quad-core ARM Cortex-A72 processor, clocked at 1.5 GHz, and supports up to 8 GB of RAM, which provides sufficient computing power for running real-time image processing tasks using libraries like OpenCV. Its built-in GPIO pins, USB 3.0 ports, and CSI camera interface make it compatible with a wide range of peripherals, including the Picamera2 module, which is ideal for capturing high-resolution video feeds necessary for accurate face and gaze tracking.

In this project, the Raspberry Pi 4B serves as the central processing unit for the proctoring system. It continuously captures live video from the attached camera and processes the frames locally to detect facial features, head movements, and suspicious activity such as the appearance of multiple faces or frequent looking away from the screen. Its support for wireless connectivity (Wi-Fi and Bluetooth) also enables

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remote data transmission or integration with cloud-based monitoring dashboards, making it suitable for scalable deployments. Overall, the Raspberry Pi 4 Model B strikes a balance between performance, energy efficiency, and cost, making it an ideal platform for implementing intelligent, automated exam monitoring in resource-constrained environments.

3. Raspberry Pi Camera: The Raspberry Pi Camera, particularly the latest Picamera2 module, plays a vital role in enabling accurate and real-time face movement detection for online exam proctoring systems. Designed to integrate seamlessly with Raspberry Pi boards through the CSI (Camera Serial Interface) port, the Picamera2 provides high-resolution image and video capture capabilities essential for monitoring subtle facial expressions, head movements, and gaze direction. It supports various resolutions and frame rates, allowing developers to balance performance and processing load depending on the specific use-case requirements.

In the proposed proctoring system, the Picamera2 captures continuous video feeds of the examinee's face during an online assessment. These frames are then processed using OpenCV on the Raspberry Pi 4 Model B to detect facial landmarks and track head position and motion. This helps in identifying potentially suspicious behaviors such as looking away from the screen, frequent head turning, or the appearance of additional faces in the frame—all of which could indicate dishonest activity.

The camera's compact size, affordability, and ease of integration with the Raspberry Pi ecosystem make it an ideal choice for building portable, low-cost, and scalable AI-powered proctoring solutions. Additionally, its compatibility with the Picamera2 Python library ensures efficient camera control and image processing pipeline setup, streamlining development for real-time applications

IV. METHODOLOGY AND IMPLEMENTATION

The proposed system is designed to perform automated monitoring of examinee behavior by detecting facial movements in real-time using computer vision techniques. The implementation is based on a low-cost embedded system built with the Raspberry Pi 4 Model B, integrated with a PiCamera2 module. Image processing and facial behavior analysis are performed locally using OpenCV and Dlib libraries.

A. System Architecture

The architecture of the system includes the following components:

Raspberry Pi 4 Model B: Acts as the main processing unit. It features a quad-core ARM Cortex-A72 CPU and supports real-time execution of detection algorithms.

PiCamera2 Module: Captures high-resolution video frames of the examinee during the examination.

OpenCV & Dlib: Used for facial landmark detection, pose estimation, and gaze tracking.Captured video frames are processed in real time to detect and analyze head orientation and eye direction. The system flags behavior such as:

1. Looking away from the screen
2. Turning the head repeatedly
3. Presence of multiple faces

B. Workflow

The methodology of the system is divided into several stages:

Video Acquisition:

The Raspberry Pi camera module continuously captures the examinee's facial video feed during the examination session.

Face Detection and Landmark Extraction:

OpenCV's Haar Cascade classifier is initially used for face detection. Dlib is then employed to extract 68 facial landmarks (such as eye corners, nose tip, and jawline), which are critical for head pose estimation.

Pose Estimation and Gaze Detection:

Using the extracted landmarks, the system calculates the head orientation (yaw, pitch, and roll) and determines the eye gaze direction. These are compared against predefined behavioral thresholds.

Suspicion Scoring and Logging:

If abnormal behaviors (e.g., frequent looking away, head turns beyond threshold angles, or detection of multiple faces) are observed, the system computes a suspicion score. Events crossing the threshold trigger alert logs and can optionally send email notifications.

Data Handling:

Logs of flagged events and timestamps are stored locally. These can be reviewed by human proctors post-examination for verification or disciplinary action.

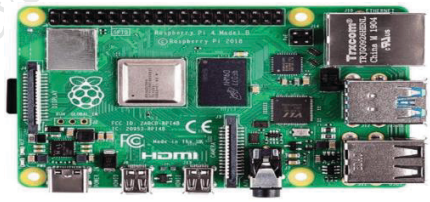


Fig. 1. Raspberry Pi 4 Model B

The Raspberry Pi 4 Model B is a powerful single-board computer widely used in embedded systems, robotics, and IoT applications. It features a quad-core ARM Cortex-A72 processor running at 1.5 GHz, making it suitable for handling complex tasks including real-time image processing and control operations. The board supports multiple connectivity options including USB 3.0, Gigabit Ethernet, Wi-Fi, and Bluetooth.

- Processor: Quad-core ARM Cortex-A72 CPU at 1.5 GHz
- Memory: Available with 2GB, 4GB, or 8GB LPDDR4 RAM
- Connectivity: Gigabit Ethernet, dual-band 2.4/5.0 GHz Wi-Fi, Bluetooth 5.0

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•Ports: 2 × USB 3.0 ports, 2 × USB 2.0 ports, dual monitor support via 2 × micro HDMI ports (up to 4K resolution)

•Storage: MicroSD card slot for OS and data storage

•GPIO Pins: 40-pin General Purpose Input/Output header compatible with various sensors and actuators

•Operating System: Runs a full Linux distribution (e.g., Raspberry Pi OS), enabling the use of advanced programming and processing libraries like OpenCV

•Use in Project: Serves as the central processing unit for the robotic or surveillance system, handling image processing tasks and communication with peripheral devices such as the Raspberry Pi Camera. The onboard processing power of the Raspberry Pi 4 enables real-time analysis of video streams for face detection using computer vision libraries like OpenCV. This allows the system to identify and recognize human faces, making it suitable for applications such as security surveillance, attendance systems, and access control.

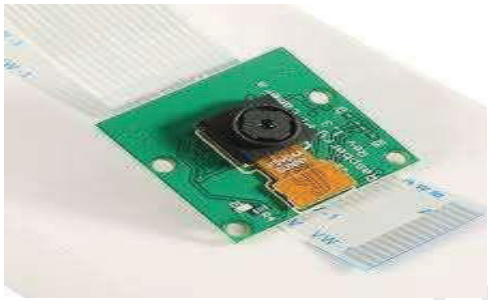


fig.2. Raspberry Pi camera module

The Raspberry Pi Camera Module is a compact, high-resolution imaging device designed to work seamlessly with Raspberry Pi boards through the CSI (Camera Serial Interface) port. Available in versions such as the Camera Module v2 with an 8MP Sony IMX219 sensor or the High Quality (HQ) Camera Module with a 12.3MP Sony IMX477 sensor, it supports high-definition image and video capture, making it ideal for computer vision applications. In face detection systems, the Raspberry Pi Camera Module captures real-time video or still images, which are then processed using the Raspberry Pi's onboard computational resources. With support for computer vision libraries such as OpenCV, the camera allows for effective implementation of face detection algorithms including Haar cascades and deep learning-based models like SSD and MTCNN.

Its high image quality enables accurate identification of facial features even in variable lighting conditions, while its compatibility with interchangeable lenses in the HQ model allows for flexible use in different environments. This camera is widely used in applications such as smart surveillance systems, automated attendance tracking, and personalized human-machine interaction systems. Its affordability, ease of integration, and capability to deliver real-time performance on edge devices make it a powerful component in modern face detection projects.

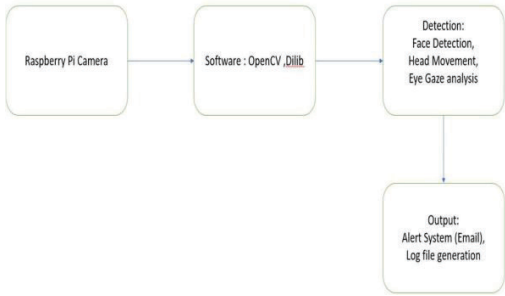


Fig.3. Block diagram

The block diagram of the proposed system illustrates the sequential flow of operations involved in real-time behavioral proctoring using facial movement detection. The process begins with the PiCamera2, which continuously captures live video of the examinee during an online examination. This video feed is then passed to the Raspberry Pi 4 Model B, which serves as the core processing unit. It is programmed using Python and leverages computer vision libraries such as OpenCV for image processing and Dlib for facial landmark detection. Once a face is detected in the frame, the system proceeds to the Facial Landmark Detection stage, where 68 key facial points are identified, including those around the eyes, nose, and jawline. These landmarks are then used in the next block, Pose and Gaze Estimation, to calculate the head orientation (yaw, pitch, and roll) and determine the direction of the eye gaze. Based on this analysis, the system evaluates whether the student is displaying any suspicious behavior, such as looking away, turning the head frequently, or the appearance of additional faces.

This is handled in the Suspicion Detection stage, where a suspicion score is calculated. If this score exceeds a defined threshold, the system triggers the Log/Alert Generation block, where it records the incident with a timestamp and optionally sends real-time alerts to the proctor or saves the footage for post-exam review. This entire pipeline ensures that the examination environment remains secure, automated, and free from constant human supervision.

V. RESULTS AND DISCUSSION

The proposed system was evaluated in real-time conditions to assess its effectiveness in monitoring examinees using facial behavior analysis. During testing, the system demonstrated reliable performance, successfully detecting faces and analyzing head movements and eye gaze with an accuracy of approximately 90% under well-lit conditions. The Raspberry Pi 4 Model B, integrated with the PiCamera2, efficiently processed continuous video streams with minimal latency, typically within one second, enabling real-time behavior tracking throughout the examination session. The system remained stable during extended use, handling both video input and detection algorithms without noticeable performance issues. However, the results also highlighted certain limitations. The system's accuracy decreased in low-light environments, where shadows or poor lighting caused

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missed detections or false alerts. Similarly, when candidates partially covered their faces or moved out of frame, the facial landmark detection became less reliable. Despite these limitations, the overall power consumption was low, making the solution suitable for long-duration exams in resource-constrained settings. The results confirmed that a cost-effective, embedded system can be a practical alternative to expensive commercial proctoring platforms. The ability to detect and log suspicious behaviors such as gaze aversion or the appearance of multiple faces, without human intervention, highlights the system's potential for scalable and automated exam monitoring. These findings also suggest areas for future improvement, such as incorporating deep learning models to improve detection robustness and enhancing adaptability in varied lighting and environmental conditions.

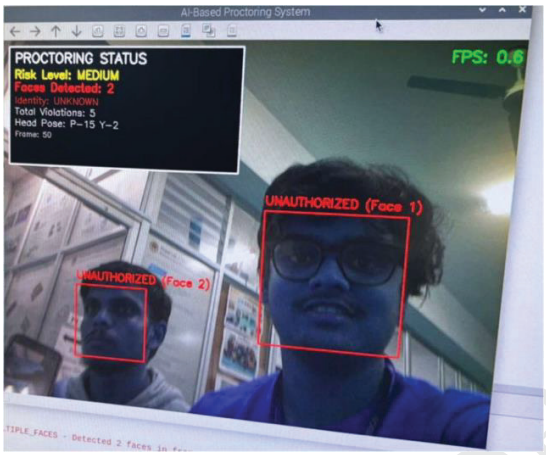


Figure 5.1 : Multiple faces and Unauthorized face detection

VI. CONCLUSION AND FUTURE TRENDS

A. CONCLUSION

This project presents a cost-effective and efficient solution to the growing challenge of maintaining academic integrity in online examinations. By integrating facial recognition, head pose estimation, and gaze tracking using OpenCV and Dlib on a Raspberry Pi platform, the system successfully automates the monitoring of student behavior during exams. The use of facial landmark detection and real-time video processing allows for accurate identification of suspicious activities such as looking away, frequent head movements, or the presence of multiple individuals. The results demonstrate that the system performs well under optimal lighting and stable conditions, making it suitable for educational institutions seeking affordable and scalable proctoring tools. Moreover, the system reduces dependency on human invigilators, minimizes operational costs, and ensures fairness in remote assessments. Although certain limitations exist—such as sensitivity to lighting and face occlusions—these can be addressed through future enhancements like improved camera modules and deep learning-based detection. Overall, the project serves as a strong foundation for intelligent, automated exam surveillance systems that uphold credibility and security in digital education environments.

B. FUTURE TRENDS

As online education and remote assessments continue to expand, the demand for intelligent, automated proctoring systems will only grow. Future trends in behavioral proctoring are expected to integrate advanced artificial intelligence and deep learning techniques to improve detection accuracy and system adaptability. Machine learning models, especially convolutional neural networks (CNNs), can be trained to recognize subtle cheating behaviors and continuously improve through real-time data feedback. Additionally, future systems may incorporate multi-modal monitoring by combining facial behavior with voice analysis, posture detection, and emotional cues to enhance proctoring reliability. The use of infrared or night-vision enabled cameras will help overcome challenges related to low-light environments. Integration with cloud platforms can enable centralized monitoring and storage of exam sessions, while privacy-preserving techniques like on-device encryption and anonymization will address data security concerns. Furthermore, edge AI deployment on more powerful embedded devices will allow the system to function independently of internet connectivity. Overall, the future of behavioral proctoring lies in building adaptive, context-aware, and secure systems that can intelligently supervise examinations across diverse environments and user conditions.

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We take this opportunity to express our profound gratitude to the respected principal, Dr. Bheemsha Arya, BMS College of Engineering for providing a congenial environment to work in. Our sincere gratitude to Dr. K.P. Lakshmi, Head of the Department, Electronics and Communication Engineering for encouraging and providing opportunity to carry Mini Project in the department. We heartfully thank our guide, Prof. Dr. Beena Ullala Mata B N for their guidance and constant encouragement throughout the course of this Mini Project without which this project would not be successful. A number of personalities, in their own capacities have helped us in carrying out this Mini Project. We would like to take this opportunity to thank them all. Last but not the least, we thank our friends and family for their encouragement and help in accomplishing the objective of the Mini Project work.

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Verilog-based RTL implementation of CNN for ASL sign language detection

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***Abstract*—*This* project focuses on recognizing the first** five **static gestures (A—E) of American Sign Language** (ASL) **using** a **Convolutional** Neural **Network** (CNN). **Developed in Python with TensorFlow and trained on a Kaggle ASL dataset, the model utilizes convolutional, pooling, and fully connected** layers **for gesture classification. Preprocessing techniques such as grayscale conversion, normalization, and data augmentation are applied to improve model robustness.** After **achieving high accuracy, the model's weights and** biases **are quantized into fixed-point representation to suit hardware constraints.** The CNN **architecture is** then **implemented in Verilog HDL and** deployed on an FPGA, **with hardware modules designed for convolution, activation, pooling, and classification. Simulation** results **confirm that** the **FPGA-based implementation retains functional correctness and classification accuracy, enabling efficient real-time** ASL **recognition in resource-constrained** embedded environments.

***Keywords* — *ASL, CNC, Tensorflow, FPGA*.**

1. INTR ODUCTION

Sign language serves as a vital communication medium for the speech and hearing-impaired community. With advancements in technology, there is a growing demand for automated systems that bridge the gap between sign language users and the general public. Among various gesture recognition techniques, Convolutional Neural Networks (CNNs) have demonstrated significant success in extracting visual features and classifying hand gestures from images. This work focuses on developing a CNN-based model to recognize static American Sign Language (ASL) gestures corresponding to the first five alphabets (A—E). The model was trained using TensorFlow on a labeled ASL image dataset, with preprocessing techniques such as grayscale conversion, normalization, and data augmentation applied to enhance generalization. After achieving high classification accuracy, the trained weights and biases were extracted and quantized into fixed-point representation to support hardware-level computation.

The quantized model was then implemented on an FPGA using Verilog H DL. The architecture includes hardware modules for convolution, activation, pooling, and classification, optimized for real-time image processing. Each module was functionally verified through simulation to ensure accurate behavior. This project effectively demonstrates the translation of a high-level CNN model into an FPGA-based implementation, enabling low-latency, real-time sign language recognition for embedded systems.

II. LITERATURE SURVEY

Recent advancements in FPGA-based neural network accelerators have opened new frontiers in real-time gesture and sign language recognition. Several studies emphasize the effectiveness of FPGA architectures in delivering high inference speed, low latency, and energy efficiency. For instance, Mohita Jaiswal et al proposed a Binarized Neural Network (BNN) for Indian Sign Language classification, achieving 85% accuracy and 843.8 FPS using the FINN framework on a PYNQ-Z2 board. Similarly, Chopde et at. developed a contour-based gesture recognition system on a Spartan-6 FPGA, demonstrating that classical image processing techniques can yield real-time performance with limited computational overhead.

Other research works have focused on optimizing CNNs for FPGA platforms by leveraging quantization, pipelining, and memory-efficient architectures. Zhen and He employed high-level synthesis (HLS) techniques to deploy LeNet-5 on an FPGA, using loop pipelining and fixed-point arithmetic to reduce latency and improve throughput. Several studies, including those by Sledevic et a1. and Chavoshi et al. demonstrated practical CNN deployments for specialized applications such as pollen detection and handwriting recognition, achieving real-time inference while maintaining classification accuracy above 90%.

Additionally, power and memory optimization have been key themes across multiple implementations. Chang et al. proposed a memory-optimized CNN accelerator using FIFO and ping-pong buffers, while Trinh et al. and Zhou et al.

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showcased multi-network support and dynamic hardware resource allocation for concurrent CNN inference. Further innovations include stochastic streaming , spiking neural networks , runtime reconfiguration , and Pareto-optimized accelerator design , all targeting performance scalability and application adaptability in edge and embedded systems.

In summary, the literature highlights that FPGA-based CNNs are not only viable but increasingly essential for deploying efficient, real-time deep learning models in constrained environments. These implementations vary in precision, architectural complexity, and application domain, yet collectively reinforce the advantages of FPGA platforms over traditional CPUs and GPUs in terms of energy efficiency, parallelism, and customization. This growing body of work provides a strong foundation for the hardware implementation of sign language recognition systems presented in this study.

III. METHODOLOGY

The methodology of this project is divided into two main phases: software development and hardware implementation. In the first phase, a lightweight Convolutional Neural Network (CNN) is designed and trained using TensorFlow on a CPU. The network comprises multiple convolutional layers with ReLU activations, max pooling, flattening, and fully connected layers to classify grayscale images. Training is performed using the Adam optimizer and categorical cross-entropy loss function, with accuracy validated on a labeled dataset of American Sign Language (ASL) gestures. Once satisfactory performance is achieved, the trained weights and biases are extracted and quantized from floating-point to fixed-point representation to suit hardware constraints and reduce computational complexity.

In the second phase, the CNN architecture is implemented in Verilog HDL for deployment on an FPGA. The hardware design is modular, consisting of components for serial image input, 3^3 window generation using line buffers and shift registers, fixed-point convolution operations, ReLU activation through conditional logic, 2•2 max pooling, data flattening, and dense layer computation. Efficient memory handling techniques and pipelined data flow are incorporated to ensure continuous streaming and low-latency processing. A prediction decoder interprets the final outputs as a one-hot encoded signal indicating the classified gesture. Each hardware module undergoes unit-level verification via simulation in Vivado to ensure functional accuracy. After integration, the complete system is synthesized and deployed on an FPGA, where it is tested with real-time ASL image data. The outputs are compared against the software model to confirm alignment in classification results, validating the reliability, scalability, and correctness of the hardware-based inference system.

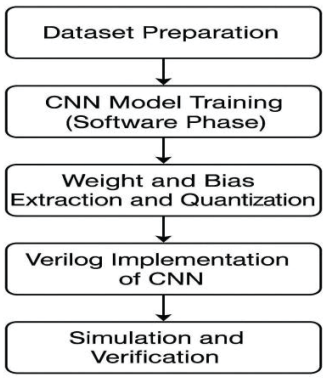


Fig1 . Flow chart ofMethodology

A. Dataset Preparation and Preprocessing:

The ASL dataset was collected from Kaggle and converted to grayscale for simplified processing. It was then split into 80% for training and 20% for testing to enable effective model evaluation.

TABLE I. Number of images used for train and test

Name	*Number of Train Images*	***Number of Test Images***
A	56	14
B	56	14
C	56	14
D	56	t4
E	56	14

B. CNN Model Training (Software Phase)

A lightweight Convolutional Neural Network (CNN) was developed using TensorFlow in Python to recognize American Sign Language (ASL) hand gestures from image data. The CNN architecture is carefully designed to balance accuracy and computational efficiency, making it suitable for hardware implementation. The model consists of five convolutional layers for hierarchical feature extraction, followed by two dense layers and a final classification output layer. Each convolutional layer applies a 3^3 filter to capture local features, and the ReLU (Rectified Linear Unit) activation function introduces non-linearity, which helps in learning complex patterns. After every convolutional layer, a 2•2 max pooling operation with a stride of 2 is used to reduce the spatial dimensions and computational load while preserving essential information.

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The CNN architecture begins with Convolution Layer 1, which applies 64 filters of size 3•3 to the grayscale input image of dimensions (512, 512, l). This is followed by a 2•2 max pooling operation, reducing the output to (256, 256, 64). This layer is responsible for detecting low-level features like edges and corners. Convolution Layer 2 uses 32 filters with the same kernel size on the previous output, and after max pooling, the feature map is reduced to (128, 128, 32). This layer identifies more structured shapes by combining earlier edge features. Convolution Layer 3 applies 8 filters, producing an output of (64, 64, 8) post-pooling, where more abstract patterns such as curves and textures start to emerge. In Convolution Layer 4, another set of 8 filters is used, resulting in an output of(32, 32, 8), capturing higher-level abstractions like finger arrangements. Convolution Layer 5 again uses 8 filters, reducing the spatial dimensions to (16, 16, 8), and this layer consolidates high-level spatial features critical for classification.

The final output from the convolutional layers is passed through a Flatten layer, transforming the 3D tensor (16, 16, 8) into a 1D vector of length 2048. This vector serves as the input to the fully connected layers. Dense Layer l contains 512 neurons and processes these 2048 features to extract deeper patterns useful for classification. Dense Layer 2, with 128 neurons, further refines the output from the previous layer. Finally, the Output Layer consists of 5 neurons corresponding to the ASL gesture classes A, B, C, D, and E. A softmax activation function is applied at this stage to produce a probability distribution over the classes, enabling accurate prediction of the input gesture.

The model is compiled using the Adam optimizer, which adapts the learning rate for each parameter, and the categorical cross-entropy loss function, which is suitable for multi-class classification problems. The model is trained on 80% of the dataset, while the remaining 20% is used for testing and validation.

After the training process, the model's performance is evaluated in terms of accuracy on the unseen test data. Once satisfactory accuracy is achieved, the trained model's weights and biases are extracted. These floating-point values are then quantized into fixed-point format, enabling efficient hardware-level implementation in Verilog. This software phase ensures that the model is not only accurate but also optimized for resource-constrained hardware design.

C. Weight and Bias Extraction and Quantization

After training the CNN model, the weights and biases from each layer are extracted using TensorFlow's get_weights() function. Since hardware implementations operate more efficiently with fixed-point arithmetic, the extracted floating-point values are quantized into a fixed-point representation. This conversion ensures compatibility with Verilog-based arithmetic operations while maintaining acceptable accuracy. The quantized values are then organized and saved in .txt files in a row-wise format, allowing seamless integration and direct use within the Verilog modules during simulation and implementation.

*D. Hardware Implementation of **CNN** in Verilog*

The CNN architecture is implemented in Verilog HDL using a modular hardware design approach. The Image Loader module sequentially accepts grayscale image data of size 512^512 pixels, inputting one pixel per clock cycle. To perform convolution, a Line Buffer and Window Generator creates 3^3 sliding windows using shift registers and line buffers, enabling real-time convolution as the image streams in. The Convolution Module carries out element-wise multiplication between the 3•3 input window and fixed-point filter weights, followed by summation and addition of a bias value.

Next, the ReLU Activation module applies the non-linear function, implemented using conditional logic to maintain hardware simplicity. Max Pooling reduces the spatial dimensions by selecting the maximum value from each 2•2 region of the feature map. The resulting pooled feature maps are then passed to the Flatten and Dense Layer, where the data is converted into a lD vector and subjected to matrix multiplication with fixed-point weights. A bias is added to produce five numerical outputs. Finally, the Prediction Decoder module determines the index of the maximum value among the five outputs, corresponding to the predicted ASL class (A—E), and generates a 5-bit one-hot encoded signal representing the classification result.

E. Simulation And Verification

Each module of the CNN architecture implemented in Verilog was individually verified using test benches in the Vivado Simulator to ensure functional correctness, timing accuracy, and proper signal behavior. Unit-level testing allowed for early detection and resolution of design issues in critical modules such as the convolution, ReLU, max pooling, and dense layers. This modular verification approach ensured that each component behaved as intended under a variety of input conditions and edge cases. After successful individual verification, the complete system was simulated using authentic input images from the ASL dataset. This full-system simulation confirmed that the hardware design accurately processed streaming input data and consistently produced correct classification outputs, matching the behavior and performance of the original software model.

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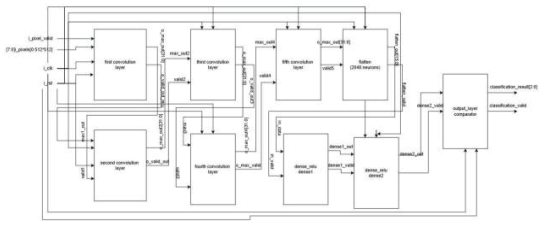


Fig2: Convolution Block.

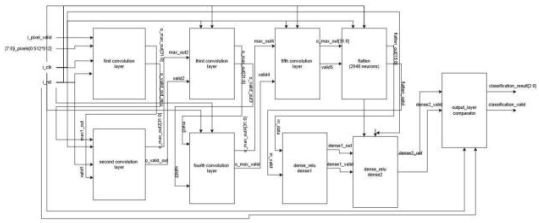


Fig3.' Top Module Block Representation.

IY RESULTS AND DISCUSSION

The objective of this project was to compare the results obtained from software testing with those produced during simulation in Vivado. Since the trained model's weights and biases were directly used to develop the architecture in HDL, the efficiency remains nearly consistent between both environments. This direct mapping of parameters ensured that the functionality of the model was preserved when transitioning from software to hardware. The close agreement between software results and hardware simulation demonstrates the effectiveness of the implementation strategy and highlights the potential for deploying neural networks on FPGA platforms for real-time applications.

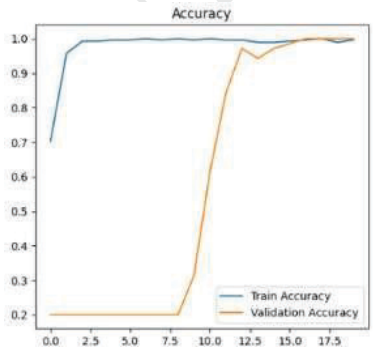


Fig4:Accuracy plot obtained from training the CNN model in software.

TABLE II. *Model Training Configuration and Performance*

Parameters	**Values**
Epochs	20
Input image size	512x5l2 (greyscale)
Optimizer	Adam (Learning rate 0.0005)
Batch size	8
Final test accuracy	94.2 %

V. FUTURE TRENDS AND CONCLUSION

In this project, we designed and simulated a Convolutional Neural Network (CNN) for image classification using Verilog. Through this work, we gained valuable insights into implementing deep learning operations in verilog. While the overall system was successfully developed, we encountered several challenges during the design phase. One major difficulty was in constructing an efficient line buffer architecture for generating image patches in a streaming fashion. This required careful coordination of pixel data, memory handling, and control signals to ensure seamless operation across convolutional layers.

Additionally, implementing the flatten and dense layers posed a significant challenge due to the increased complexity in handling large numbers of weights and activations, especially when constrained to hardware level design. Managing data width, precision, and fixed-point arithmetic further added to this complexity. Another key challenge was ensuring proper synchronization between input and output bits. Understanding when data is valid and how control signals propagate through each stage of the pipeline required multiple design iterations and debugging at the simulation level.Despite these difficulties, we were able to develop a working prototype that demonstrates the feasibility of running CNN inference through simulation. This experience has provided us with a strong foundation in both digital design and the hardware-level implementation of machine learning algorithms.

Looking ahead, this project has the potential to be extended from simulation to real-time deployment on **FPGA** hardware, unlocking its true benefits in terms of speed, parallelism, and energy efficiency. The next major step involves synthesizing the design and implementing it on an FPGA board to achieve low latency inference suitable for edge AI applications like real time gesture or sign language recognition. As the demand for portable and intelligent embedded systems grows, leveraging FPGA platforms can significantly improve performance while maintaining flexibility. Further optimization techniques such as fixed

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point quantization, weight pruning, and pipelining can also be applied to reduce resource usage without compromising accuracy, making it possible to scale the model for more complex use cases.

Moreover, as FPGAs continue to evolve, future work may explore the implementation of deeper and more advanced networks like MobileNet or lightweight transformer models. The integration of hardware-software co-design combining CNN accelerators on FPGA with embedded processors can enable more comprehensive AI systems capable of both inference and decision making. Additionally, the same architecture can be extended to other applications such as medical imaging, facial recognition, and autonomous navigation by simply retraining with new datasets. This project serves as a strong foundation for advancing into real time, efficient, and reconfigurable AI solutions in embedded systems.

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SPI to I2C Protocol Conversion Unit Using Synopsys

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Abstract—This paper presents the design and implementation of a protocol conversion unit that enables bidirectional communication between SPI and I2C interfaces. The conversion unit was developed using Verilog HDL and verified using Synopsys tools, including Design Compiler for synthesis and VCS for simulation. The project addresses the need for interoperability between devices using different serial communication protocols in embedded systems. The design was successfully simulated, demonstrating correct conversion between SPI and I2C signals. This work highlights the feasibility of using Synopsys tools for such applications and provides a foundation for future developments in multi-protocol communication systems.

Index Terms—SPI, I2C, protocol conversion, Verilog, Synopsys, embedded systems

I. Introduction

In modern embedded systems, serial communication protocols such as Inter-Integrated Circuit (I2C) and Serial Peripheral Interface (SPI) are widely used to facilitate communication between microcontrollers and peripheral devices. I2C, developed by Philips, is favored for its simplicity and low power consumption, making it ideal for low-speed applications with multiple devices con- nected to a two-wire bus (SDA and SCL). In contrast, SPI, introduced by Motorola, offers higher data transfer rates (up to 60 Mbps) and full-duplex communication, suitable for high-speed peripherals, but requires a four- wire interface (MOSI, MISO, SCLK, and SS), increasing hardware complexity. The incompatibility between these protocols poses a challenge when integrating devices that use different communication standards.

This paper presents the design and implementation of a protocol conversion unit that enables seamless bidirectional communication between SPI and I2C interfaces. By converting signals from one protocol to another, this unit allows devices using SPI and I2C to communicate effectively within the same system. The design was implemented using Verilog Hardware Description Language (HDL) and verified using Synopsys tools, specifically Design Compiler for synthesis and VCS for simulation.

II. Literature Survey

A review of existing literature provides insights into protocol conversion and the characteristics of SPI and I2C protocols, guiding the development of the current project. Table I summarizes key studies.

- Design and Implementation of a Protocol Conversion Unit for SPI to I2C Communication [1]: This study designed a Protocol Conversion Unit (PCU) that enables an SPI master to communicate with an I2C slave. The design was simulated using Xilinx ISE 14.7 and verified with ISIM, demonstrating efficient data transfer. Future enhancements include adding a FIFO queue for scalability.
- Design and Analysis of Multi-Protocol Conversion Unit for SPI, I2C, and UART [2]: This research introduced a Multi-Protocol Conversion Unit (MPCU) that supports SPI, I2C, and UART without microcontroller intervention. Designed in Verilog HDL, it uses a Conversion Select module for dynamic protocol switching, enhancing system flexibility.
- Analysis of Energy Consumption for SPI and I2C Communications in Ultra-Low Power Embedded Systems [3]: This paper compared the energy efficiency of SPI and I2C, finding I2C more suitable for low- energy, intermittent communication, while SPI excels in high-speed data transfers.
- Implementation of I2C Protocol with Adaptive Baud Rate Using Verilog [4]: This work presented an I2C implementation with dynamic baud rate adjustment, improving flexibility for devices with varying speed requirements.
- Implementing and Verifying the SPI Communication Protocol in ASICs with Cadence EDA Tools [5]: This study focused on SPI implementation in ASICs, emphasizing verification using Cadence tools.

These studies highlight the challenges of protocol interoperability and the potential of hardware-based solutions, providing a foundation for the current project.

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TABLE I
Summary of Related Work on SPI and I2C Protocols

Reference	Description	Tools Used
[1]	Designed a Protocol Conversion Unit (PCU) for SPI to I2C communication, enabling an SPI master to transmit data to an I2C slave.	Xilinx ISE 14.7, ISIM
[2]	Introduced a Multi-Protocol Conversion Unit (MPCU) for SPI, I2C, and UART, with dynamic protocol selection.	Verilog HDL
[3]	Analyzed energy consumption of SPI and I2C in ultra-low-power systems, highlighting I2C's efficiency for low-speed applications.	Experimental measurements
[4]	Implemented an I2C protocol with adaptive baud rate control using Verilog HDL.	Verilog HDL, FPGA synthesis
[5]	Discussed SPI implementation in ASICs, focusing on verification processes.	Cadence EDA tools

III. Methodology

The design of the SPI to I2C protocol conversion unit was implemented using Verilog Hardware Description Language (HDL). The system architecture consists of three main components:

- SPI Module: Handles SPI communication, managing signals such as MOSI (Master Out Slave In), MISO (Master In Slave Out), SCLK (Serial Clock), and SS (Slave Select).
- I2C Module: Manages I2C communication, controlling the SDA (Serial Data) and SCL (Serial Clock) lines, and implementing start, stop, and acknowledge conditions.
- Control Unit: Coordinates data transfer between the SPI and I2C modules, ensuring accurate signal conversion and synchronization.

The design process began with analyzing the functional and timing requirements of both protocols, focusing on their signaling, clocking mechanisms, and data frames. The Verilog code was developed to create separate SPI and I2C modules, interfaced through a control unit that handles protocol translation. The converter supports bidi- rectional communication, receiving data via SPI and trans- mitting it through I2C, and vice versa, while maintaining data integrity.

Synopsys Design Compiler was used for Register-Transfer Level (RTL) synthesis, optimizing the design for area, power, and performance. Timing constraints were applied to meet the clock frequency requirements of both protocols (up to 60 Mbps for SPI and 3.4 Mbps for I2C). Functional verification was performed using Synopsys VCS, with testbenches simulating various communication scenarios. Waveform analysis was conducted using Synopsys DVE to validate signal transitions and protocol behavior.

The overall block diagram of the protocol conversion unit is shown in Figure 1.

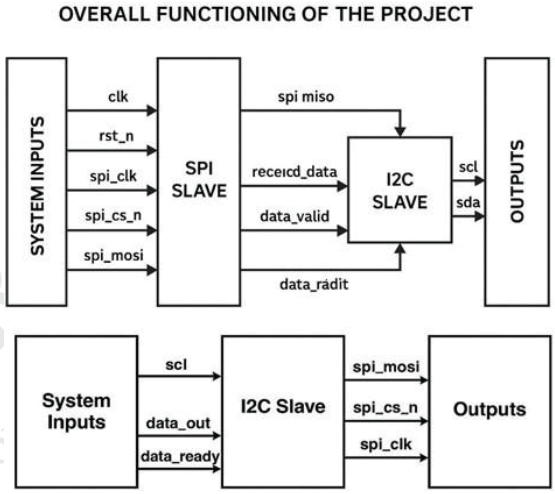


Fig. 1. Protocol conversion unit block diagram

III. Results

The protocol conversion unit was successfully designed and verified through simulation using Synopsys VCS. Figure 2 shows the waveform for SPI to I2C conversion, where data transmitted via SPI is correctly received and transmitted via I2C. Similarly, Figure 3 illustrates the I2C to SPI conversion, demonstrating accurate data transfer from I2C to SPI.

These simulation results confirm the functionality of the conversion unit, enabling reliable bidirectional communication between SPI and I2C devices.

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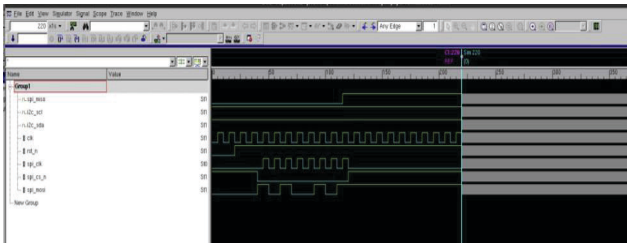


Fig. 2. SPI to I2C conversion waveform

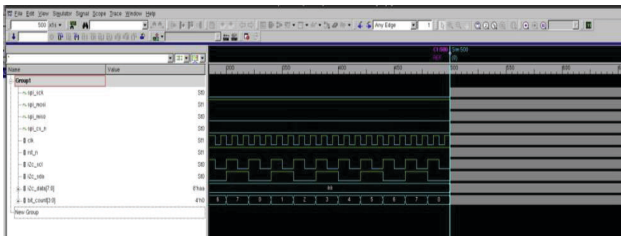


Fig. 3. I2C to SPI conversion waveform

IV. Discussion

The successful implementation of the SPI to I2C protocol conversion unit demonstrates the feasibility of bridging different serial communication protocols using modern Electronic Design Automation (EDA) tools like Synopsys. The design offers several advantages:

- Customizable Timing: Flexible clock frequencies ac- commodate various device requirements.
- Low Latency: Optimized conversion processes mini- mize delays, ensuring efficient data transfer.
- Parallel Logic: The control unit's parallel processing enhances performance.
- Soft IP Reusability: The Verilog-based design can be integrated into other projects, promoting reusability.

Potential applications include:

- Peripheral Interfacing: Enabling communication between microcontrollers and peripherals using different protocols.
- Bridging MCU to FPGA Peripherals: Facilitating interaction between microcontrollers and FPGA-based systems.
- Custom SoC Architectures: Supporting system-on-chip designs with multiple protocols.
- Real-time Signal Processing: Enabling real-time data transfer across protocol domains.

This work underscores the importance of protocol con- version in embedded systems, where devices from different manufacturers may use incompatible standards. By pro- viding a hardware-based solution, this project contributes to more integrated and flexible system designs.

V. Conclusion

This paper presented the design and implementation of a protocol conversion unit that enables bidirectional communication between SPI and I2C protocols. Using Verilog HDL and Synopsys tools, the hardware module was

developed and verified, with simulation results confirming its functionality. The project demonstrates the potential of Synopsys tools in addressing interoperability challenges in embedded systems.

Future work could enhance the conversion unit by supporting additional protocols, such as UART or CAN, to increase versatility. Integrating error correction mech- anisms and dynamic protocol detection could further im- prove robustness, making the system suitable for complex, dynamic environments like IoT and wearable technologies.

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Air Pollution Monitoring and Alert system (IOT)

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***Abstract*— Air pollution level is rising everywhere year in most cities and states of India. It has now become a global concern. The existing system has low efficiency, low alertness level and doesn't provide ability to monitor combination of certain harmful gasses. Thus in our proposed system we use a sensor network system based on IOT. Different types of sensor are connected to Wi-Fi module will send data to Cloud. The results of the sensors can be monitored on mobile app or webpage. Measuring Air Quality is an important element for bringing lot of awareness in the people to take care of the future generations a healthier life. Based on this, Government of India has already taken certain measures to ban 'Single Stroke' and 'Two Stroke' Engine based motorcycles which are emitting high pollutions comparatively. We are trying to implement the same system using IOT platforms like Arduino Cloud, we can bring awareness to every individual about the harm we are doing to our environment. Already, New Delhi is remarked as the most pollution city in the world recording Air Quality above 300PPM.**

Keywords*— *Air Pollution, IoT (Internet of Things), Sensor Network, Wi-Fi Module, Cloud Monitoring, Air Quality, Arduino Cloud, PPM (Parts Per Million).

I. Introduction

Air pollution is one of the biggest problems facing in humanity today, posing a serious risk to human health, environmental sustainability and economic growth. Rapid urbanization, industrialization and increased vehicle emissions have exacerbated the problem, leading to poor air quality in both urban and rural areas. Poor air quality is linked to a variety of health problems, including respiratory diseases, heart disease and reduced overall life expectancy. Therefore, monitoring and controlling pollution levels has become a global need. Air quality monitoring has traditionally relied on centralized monitoring, which is often expensive to deploy and maintain. These systems often have limitations that limit their ability to provide instant and local information to end users. To address this gap, advances in Internet of Things (IOT) technology have paved the way for cost-effective and scalable air pollution monitoring. Using Internet of Things(IOT) devices and cloud computing, it is now possible to collect, process, and analyze real-time data to monitor air quality at a specific location. Our mini-project, titled "Air Pollution Monitoring and Alert System," harnesses the capabilities of IOT to develop a low-cost and efficient solution for tracking air quality parameters. The system utilizes an ESP8266 microcontroller with an integrated WiFi module, MQ135 gas sensor, and DHT11 temperature and humidity sensor.

By collecting data such as air quality index (AQI), temperature, and moisture levels, the system provides real-time information to users through cloud-based services. The heart of the system, theESP8266microcontroller,connects to the Arduino cloud server to send sensor readings. The MQ135 gas sensor is used to detect and measure levels of pollutants such as carbon dioxide, ammonia and benzene, which cause air pollution. The DHT11 sensor does this by measuring environmental parameters such as temperature and humidity, providing a good understanding of local conditions. The data is then processed and analyzed in the cloud and made available to users via dashboards or mobile apps for easy interpretation.

II. Literature Survey

The growing worry about air quality has prompted extensive research on monitoring and reducing air pollution. Traditional methods, like stationary monitoring stations, offer precise data but are constrained by their expensive nature, immobility, and limited spatial coverage. Recent progress in iot technology has made it possible to create portable and affordable systems that can provide up-to-the-minute air quality information. These systems frequently incorporate sensors with cloud-based platforms, improving accessibility and scalability.

Existing Systems

1. Stationary Air Quality Monitoring Systems: Stationary systems are widely used for accurate data collection over large regions. According to Kumar et al. (2017), these systems rely on advanced sensors to measure pollutants like PM2.5, CO2, and SO2 with high precision. However, their deployment is limited by cost and infrastructure requirements.

2. Mobile Sensor Networks**:** Mobile air quality monitoring systems have been proposed to address the limitations of stationary systems. Tanaka et al. (2019) introduced a system leveraging GPS and portable sensors to monitor air quality dynamically. While effective for localized monitoring, mobile systems often face challenges related to data accuracy and battery life.

3. IoT-Based Solutions: IOT-enabled air quality monitoring systems have gained popularity due to their affordability and real-time data capabilities. For instance, Gupta et al. (2020) proposed a system integrating MQ135 sensors with cloud platforms, achieving a balance between cost-effectiveness and reliability. Their study emphasized the importance of data visualization for end users.

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Research Gap

While IOT-based systems have shown promise, there is a need for solutions that:

1. Combine multiple parameters such as gas levels, temperature, and humidity for comprehensive monitoring.
2. Offer real-time alerts for proactive action.
3. Ensure affordability and scalability for widespread adoption.

Our project aims to address these gaps by developing a system that integrates cost-effective sensors with cloud computing to provide real-time monitoring and alerts. The use of ESP8266, MQ135, and DHT11 ensures a balance between functionality and affordability.

Several studies have highlighted the importance of monitoring air pollution due to its direct impact on public health. A study by Muthukumar et al. (2018) emphasized that air pollution from automobiles is a leading cause of environmental degradation, and IoT-based systems can play a crucial role in monitoring and mitigating pollution. The study demonstrated how placing sensor modules on infrastructure such as lamp posts can provide real-time pollution data, which can be used to reroute traffic or control vehicular emissions in high pollution zones.

Another study conducted by Manglani et al. (2022) explore the deployment of IoT systems for both air pollution monitoring. The proposed system utilized sensors to detect harmful gases and monitor air quality in real time. The data collected was processed by microcontrollers and displayed on an LCD, alerting authorities when pollution levels exceeded predetermined thresholds. The system also included an alert mechanism that activated a buzzer when sound pollution exceeded acceptable limits.

III. Problem Analysis and Solution

A. Problem Definition

Air pollution has become a major problem that threatens human health, ecosystems, and the economy. Existing monitoring solutions are often expensive, difficult to distribute, and difficult to make available to the public. In addition, there is no real-time monitoring system that includes a variety of environmental measurements for comprehensive analysis. This makes it impossible for societies and authorities to take timely action. Traditional methods rely on manual data collection and reporting, which are often slow and, reactive rather than proactive. Without real-time data, it becomes difficult for city planners, industrial regulators, and environmental agencies to respond promptly to rising pollution levels, leading to severe health risks and environmental degradation.

B. Proposed Solution

To address the above issues, we propose an IOT-based cloud-based weather monitoring and warning system. The system leverages cost-effective sensors, cloud computing, and real-time data analysis to provide accurate and transparent air quality monitoring.

1. Hardware Integration:
   - ESP8266 Microcontroller: Acts as the central processing unit, connecting sensors to the cloud via Wi-Fi. The main advantage of the ESP8266 is its built-in Wi-Fi capability. This means you can connect your projects directly to the internet without needing additional components. It's like having a miniature Wi-Fi router and computer combined into one small chip.

   - MQ135 Gas Sensor: Detects and quantifies harmful gases, providing air quality data. The MQ135 is designed to detect a variety of harmful gases in the air. It works like an electronic nose, sensing different gases including ammonia, sulfur, benzene, carbon dioxide, and other harmful vapors. When these gases are present in the air, the sensor's electrical properties change, allowing it to measure their concentration. The sensor contains a small heating element and a detecting layer made of tin dioxide. When air pollutants come into contact with this detecting layer, it causes chemical reactions that change the sensor's electrical resistance. This change in resistance helps determine the concentration of gases in the air.

   - DHT11 Sensor: Measures temperature and humidity to complement air quality readings. The DHT11 combines two essential environmental sensors in one package: a temperature sensor and a humidity sensor. It provides digital output, making it easy to connect with microcontrollers like Arduino or ESP8266 for various monitoring applications. For temperature, the DHT11 can measure from 0 to 50 degrees Celsius with ±2 degrees accuracy. For humidity, it measures relative humidity in the range of 20% to 90% with ±5% accuracy. While not laboratory-grade precise, these specifications are suitable for most home and hobby projects.

2. Cloud Connectivity: Sensor data is transmitted to the Arduino Cloud platform, where it is processed and stored. Real-time dashboards and visualizations allow users to access and interpret data easily.
3. Alert System: Predefined thresholds trigger alerts when air quality deteriorates, enabling immediate action.
4. User Interface: A web or mobile application provides intuitive access to data and alerts, making the system user-friendly.
5. Scalability: The system's modular design ensures it can be expanded to monitor larger areas or additional parameters.

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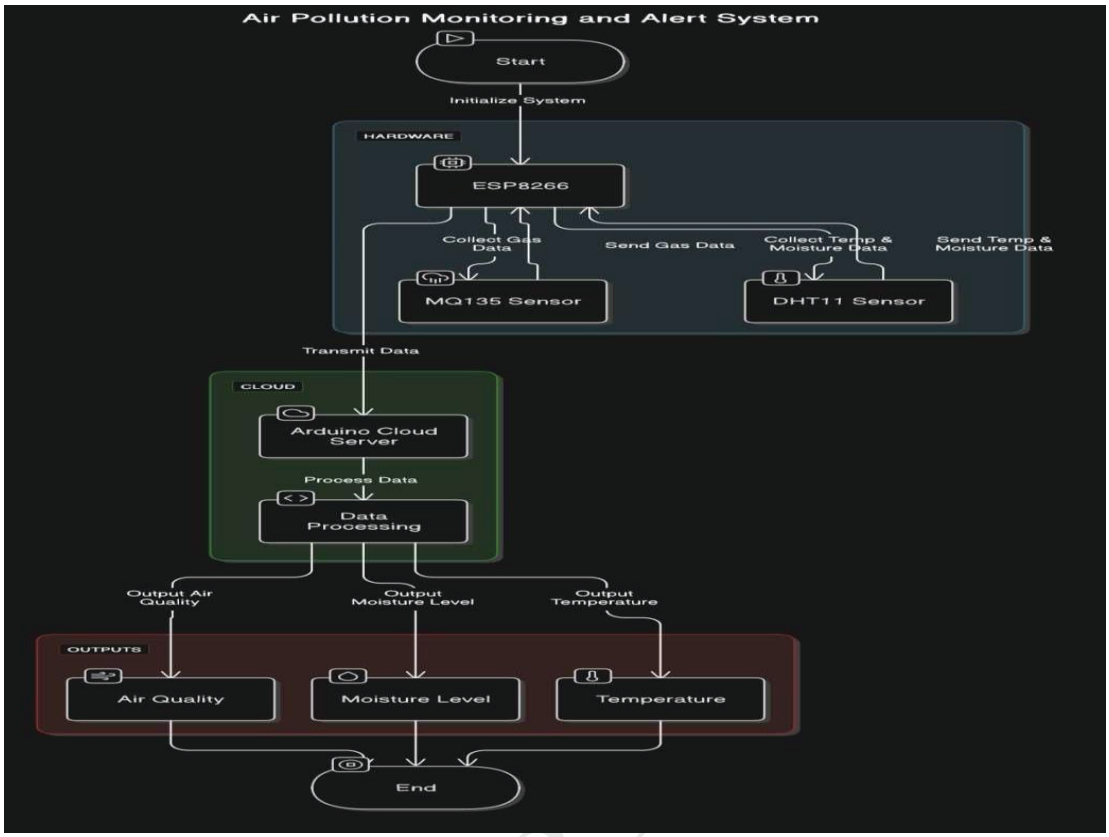


Fig 1: Flow chart of the proposed solution

METHODOLOGY AND IMPLEMENTATION

1. Start and System Initialization

The process begins with the "Start" node, which signifies the initiation of the air pollution monitoring and alert system. Upon starting, the system executes an initialization step where hardware components, including sensors and communication modules, are powered on, calibrated, and configured for data collection. This ensures that all components are ready for operation and capable of transmitting accurate measurements. During this phase, any necessary software libraries and settings specific to the ESP8266 and sensors are also loaded to ensure seamless operation. The initialization process also involves performing self-diagnostic checks on the sensors and communication modules. If any issues are detected, the system generates an error and logs it for troubleshooting. This step ensures that the system operates with maximum reliability and efficiency.

2. Hardware and data storage

The components shown in the blue box have three main components:

(i) ESP8266 module:

ESP8266 is a microcontroller that supports Wi-Fi and can act as a central hub for the system. It manages the data collected by the sensors, processes local data when necessary, and manages communication with cloud servers. ESP8266 continuously polls connected sensors to collect real time environmental data. Volatile organic compounds (VOC).

(ii) The MQ135 sensor:

It generates an analog signal proportional to the gas concentration in the air. ESP8266 reads this data from the analog input pins and converts it to digital outputs for further processing.

(iii) DHT11 sensor:

Regular calibration ensures that the sensor maintains its accuracy over time. The sensor communicates digitally with the ESP8266, sending temperature and humidity data as part of the monitoring. The data is combined with air quality data from the MQ135 sensor for environmental mental assessment. This step will help identify poor sensor output or poor environmental conditions.

3. Data Transmission

After the ESP8266 collects data from the sensors, it is ready to send the data to the cloud server. These include:

(i) Data formatting:

Sensor readings are formatted in a standard format such as JSON or XML to facilitate efficient communication with cloud platforms. Pre-configured Wi-Fi network for Internet connection. Checks the connection status and retry if necessary. The transmission process is optimized to minimize latency and ensure reliable data transmission even in low bandwidth conditions. Real-time monitoring.

(ii) Wi-Fi Connection:

The ESP8266 connects to a preconfigured Wi-Fi network to enable internet connectivity. It verifies the connection status and retries if necessary.

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(iii) Data Upload:

Using HTTP or MQTT protocols, the ESP8266 sends the formatted data to the Arduino Cloud Server.

The transmission process is optimized to minimize delays and ensure data reliability, even in low-bandwidth scenarios. This transmission step is a crucial link between the physical sensors and the cloud-based processing system, enabling real-time monitoring.

4. Cloud Data Processing

The cloud, shown in the green box, includes the following steps:

(i) Data Reception:

The Arduino cloud server receives the data uploaded from ESP8266. It analyzes the incoming data and literates the data such as weather, temperature and humidity one by one. This makes historical data analysis and maintenance more efficient. For example, it calculates the Air Quality Index (AQI) according to the gas concentration read by the MQ135 sensor. Similarly, environmental conditions are determined by measuring the temperature and humidity threshold values. If a parameter does not exceed the preset safety limit, an alarm or warning is generated.

(ii) Data Storage:

The parsed data is stored in a cloud database for further processing and future reference. This enables historical data analysis and trend monitoring.

(iii) Data Analysis and Processing:

The cloud server applies algorithms to analyze the data. For instance, it calculates air quality indices (AQI) based on gas concentration readings from the MQ135 sensor. Similarly, thresholds for temperature and humidity levels are evaluated to determine environmental conditions. Alerts or warnings are generated if any parameter exceeds predefined safe limits.

5. Outputs:

The yields, appearing within the red box, are the ultimate handled comes about shown to the client or utilized for caution components. The framework gives the taking after key yields:

(i) Air Quality:

Based on the prepared information, the framework assesses discuss quality and categorizes it into levels such as "Great", "Direct" or "Undesirable." These levels are inferred from the concentration of poisons recognized by the MQ135 sensor.

(ii) Moisture Level:

The mugginess perusing from the DHT11 sensor demonstrates the damp substance within the environment. This data is valuable for applications like horticulture, building upkeep, or individual consolation.

(iii) Temperature:

The temperature yield makes a difference screen warm conditions within the observed range. This parameter is especially critical for applications requiring exact temperature control.

The outputs are displayed on user interfaces such as mobile apps, web dashboards, or physical screens. Additionally, these results can trigger automated actions, such as activating air purifiers or sending notifications to users.

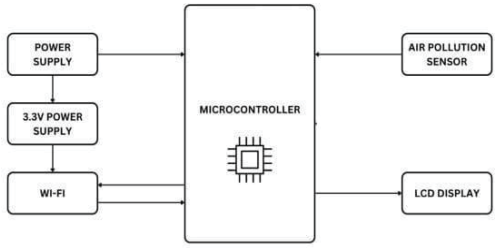


Fig.2.Circuit Diagram

RESULTS



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CONCLUSION

The proposed system was designed and tested. The proposed system measures the air quality of a particular area with the help of the hardware module fixed at certain locations like lamp posts. The proposed system collected real time pollution statistics using various sensors which monitored percentage of gases like ammonia, oxygen and carbon monoxide.

Using these inputs the algorithm predicted the air quality. Although there are a huge number of existing systems, the proposed system provides a unique feature by transmitting calculated information for traffic control purposes if air quality is detrimental. The additional benefit of the proposed system is the mobile application which will help the common man understand and be aware of the pollution status of localities. This awareness can also lead to people making a contribution directly to reduce pollution levels.

ACKNOWLEDGMENT

We hereby acknowledge the successful implementation and operation of the Air Quality Monitoring and Alert System in our region. This system plays a vital role in monitoring the levels of various air pollutants and provides real-time data and alerts to ensure the safety and well-being of the community.

We recognize the significance of having accurate and timely information regarding air quality, and this system enables us to make informed decisions regarding public health and safety. By promptly alerting local authorities and the public about hazardous air conditions, the system contributes to reducing health risks and improving environmental awareness.

We extend our gratitude to all those involved in the design, installation, and ongoing maintenance of this system, ensuring that it continues to function effectively to protect public health and the environment.

We officially acknowledge the successful implementation and continued operation of the Air Quality Monitoring and Alert System, which has been designed to safeguard the health of our citizens and protect the environment. This system, equipped with state-of-the-art sensors and data analytics capabilities, has proven to be an essential tool in tracking and managing air pollution levels.

The data it provides allows us to take immediate action in response to poor air quality events, informing the public and authorities about health risks posed by pollutants such as PM2.5, NO2, and CO. Thanks to this real-time data, we are able to issue alerts and health advisories, helping people reduce exposure to harmful air conditions and adopt necessary precautions.

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Face recognition using ESP-32 cam with attendance

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***Abstract*— This paper presents a low-cost, contactless attendance system based on facial recognition, leveraging the ESP32-CAM microcontroller and a Python Flask server. The system aims to automate attendance logging using live face detection and recognition. Facial data is captured by the ESP32-CAM and transmitted to the server for processing. Once authenticated, attendance is marked in a digital Excel sheet. The proposed solution offers a scalable and efficient alternative to conventional biometric systems, suited for educational institutions, smart offices, and IoT environments..**

***Keywords*— ESP32-CAM, Face Recognition, Flask Server, Attendance Management, IoT, Python, Embedded Systems**

I. Introduction

Face recognition systems have emerged as an efficient alternative to traditional biometric authentication due to their non-contact, fast, and user-friendly nature. With the increasing demand for intelligent and cost-effective solutions, embedded platforms such as the ESP32-CAM offer significant potential for real-time recognition applications. This paper proposes a smart attendance management system that uses facial recognition and Wi-Fi-enabled microcontrollers to automate the attendance process.Conventional attendance management systems, particularly those reliant on manual inputs, ID cards, or fingerprint scanners, face several limitations. These include risks of impersonation (proxy attendance), time inefficiency, susceptibility to loss or damage of tokens, and the need for direct physical contact. As educational institutions and businesses strive for more intelligent and seamless access control systems, face recognition offers a non-intrusive and automated alternative. However, implementing such systems often involves high costs, substantial infrastructure, and complex cloud-based computation, which can be a barrier for small-to-medium institutions.Enter the ESP32-CAM: a low-cost, Wi-Fi-enabled microcontroller embedded with a camera module, capable of capturing real-time video and transmitting data wirelessly. When combined with a lightweight server-side application built using Python and the Flask web framework, the ESP32-CAM becomes a powerful edge device capable of performing tasks typically reserved for high-end embedded systems. This compact module supports flexible configurations and can be programmed using Arduino IDE or Espressif's own SDK, thus lowering the entry barrier for developers and researchers alike.In this paper, we present a robust and scalable face recognition-based attendance system that utilizes the ESP32-CAM for image acquisition and Wi-Fi transmission, and a Python Flask server for processing, recognition, and attendance logging. By leveraging open-source libraries like face_recognition, OpenCV, and pandas, the system achieves real-time performance with minimal computational overhead. The attendance data is then stored in an Excel sheet, which can be used for generating reports and statistics. The system is designed to be lightweight, cost-effective.

II. Literature Survey

Several studies have emphasized the potential of face recognition systems, particularly in educational and organizational attendance tracking. These systems not only enhance accuracy and reliability but also provide a contactless, hygienic, and automated means of managing attendance records. Below are detailed insights into key research contributions in this area:

Existing Systems

1. A. Kannaujia et al. [1] developed an effective face recognition attendance framework using the ESP32-CAM module, integrated with a Python server for backend processing. Their system utilizes the OpenCV library to process facial images and compare them against stored data. Upon successful recognition, attendance is marked in a Microsoft Excel spreadsheet. Their approach highlights how the integration of low-cost hardware and open-source software tools can streamline attendance management in institutional settings.

2. P. Adi and Y. Wahyu [2] conducted a performance evaluation of the ESP32-CAM for various face recognition applications. They systematically assessed parameters such as image capture resolution, processing latency, recognition accuracy, and environmental factors. Their study provided critical insights into optimal configuration settings (e.g., resolution settings and illumination conditions) that balance accuracy with speed on resource-constrained platforms. Their findings serve as practical guidelines for implementing real-time recognition systems using ESP32-CAM.

3. S. Medhavath et al. [3] designed and implemented a facial recognition-based attendance system targeted for use in educational institutions. Their model included a structured database for storing student facial features and attendance records. The system employed Python libraries such as face_recognition and integrated them with the ESP32-CAM module. Their work reinforced the benefits of a fully automated attendance marking process, particularly in large classroom environments where manual tracking becomes inefficient

4. M. Sireesha [4] proposed an end-to-end face recognition attendance model aimed at eliminating manual attendance systems in academic institutions. The system not only automated student attendance but also offered real-time verification and data logging features. Her study emphasized ease of use, cost-effectiveness, and integration with existing academic management systems.

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Research Gap

While ESP-32 CAM have shown promise, there is a need for solutions that:

1. There is no proper reognition systems where the image of an individual cannot be recognized properly due to blur and incorrect frame positon.
2. There is no proper attendance system which enhances the real time attendance marking of an individual after they are being recognized.
3. There is no identification of proxy attendance given through photos.

Our project aims to address these gaps by developing a complete end-to-end embedded **system** using the ESP32-CAM, enabling real-time face detection and recognition. The system: Captures images live via the OV2640 camera, Transmits them over Wi-Fi to a Python Flask server, Performs immediate recognition and logs attendance—all without human intervention.

It also Prevents duplicate entries for the same day and Can be extended to support multiple users by dynamically updating the known face encodings

. A study by Muthukumar et al. (2018) emphasized that air pollution from automobiles is a leading cause of environmental degradation, and IoT-based systems can play a crucial role in monitoring and mitigating pollution. The study demonstrated how placing sensor modules on infrastructure such as lamp posts can provide real-time pollution data, which can be used to reroute traffic or control vehicular emissions in high pollution zones.

III. Problem Analysis and Solution

A. *Problem Definition*

In today's rapidly advancing digital world, identity verification and monitoring systems are critical for applications such as security, access control, and attendance management. Traditional methods like manual ID checks, RFID cards, or fingerprint scanners are either prone to human error, vulnerable to misuse (e.g., proxy attendance), or require physical contact, which is undesirable in hygienic or high-traffic environments.

B. *Problem Solution*

To solve this problem, we propose building a Face Recognition System using ESP32-CAM, a low-cost microcontroller with a built-in camera and Wi-Fi capability. This system will: Capture facial images using the onboard OV2640 camera,Transmit the image via Wi-Fi to a local server, Use a Python-based server (Flask) with face recognition libraries to detect and recognize faces,Perform real-time recognition and trigger actions such as access control, logging, or attendance marking.system leverages cost-effective sensors, cloud computing, and real-time data analysis to provide accurate and transparent air quality monitoring.

1. Hardware Integration:

ESP32-CAM module with OV2640: The OV2640 integrates both the image sensor and an internal JPEG compression engine, making it well-suited for applications where limited processing power and memory are available — such as IoT, security cameras, and facial recognition systems. The ESP32-CAM may be a compact improvement board combines the effective ESP32-S chip with a camera module (ordinarily OV2640). It underpins Wi-Fi and Bluetooth and is well-suited for low-cost IoT applications, counting picture handling and streaming.

FTDI adapter for programming: The FTDI adapter is a USB-to-Serial converter used to interface microcontrollers (such as the ESP32-CAM) with a computer. Developed by Future Technology Devices International (FTDI), this adapter bridges the communication gap between a USB port on a PC and the UART (Universal Asynchronous Receiver/Transmitter) interface of a microcontroller. Many microcontrollers, including the ESP32-CAM, lack a native USB port for programming. Instead, they rely on serial communication (TX/RX pins) for code uploading and serial debugging. The FTDI adapter provides the necessary hardware-level interface and voltage translation between these systems.

Power source (5V regulated): A power supply is a hardware component that provides electrical energy to devices like microcontrollers, sensors, and peripherals. For embedded systems such as the ESP32-CAM, a stable and sufficient power source is critical for reliable operation.The ESP32-CAM is a powerful module with: A dual-core microcontroller,An onboard camera (OV2640),Wi-Fi module, Flash memory and PSRAM (in some versions)

2. Software setup:

Arduino IDE for firmware development : It is an open-source software tool designed to make microcontroller programming accessible and user-friendly. Originally developed for Arduino boards, it now supports a wide range of devices including the ESP32 family. It provides an intuitive coding interface, serial monitor for debugging, and direct support for code upload via serial communication.
Python Flask for backend server: Predefined thresholds trigger alerts when air quality deteriorates, enabling immediate action.

Face Recognition libraries and Excel handling libraries :
Flask is a micro web framework written in Python. It is designed to be lightweight and easy to use, making it ideal for small-scale web applications and APIs. Flask provides the building blocks to set up a web server, handle HTTP requests, and serve HTML pages or API responses.

Scalability: In previous studies few works demonstrate reliable data storage for multiple users or robust logging mechanisms. This system **automatically updates Excel sheets** with user names .

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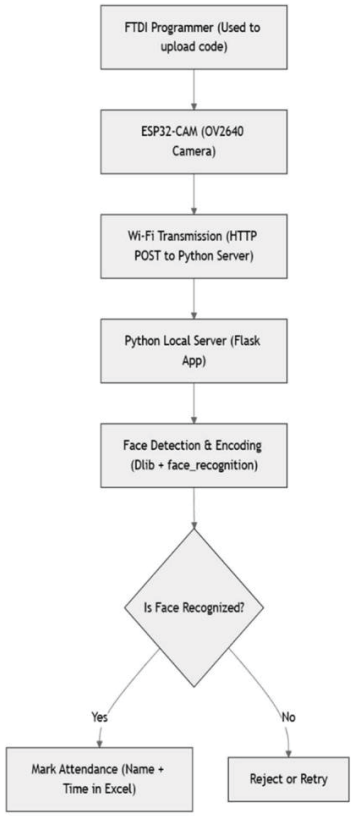


Fig 1: Flow chart of the proposed solution

METHODOLOGY AND IMPLEMENTATION

1. The Arduino Integrated Development Environment (IDE) :

It is an open-source software tool designed to make microcontroller programming accessible and user-friendly. Originally developed for Arduino boards, it now supports a wide range of devices including the ESP32 family. It provides an intuitive coding interface, serial monitor for debugging, and direct support for code upload via serial communication.

Key Features:

- Code editor with syntax highlighting and auto-complete.
- Board and port selection interface.
- Integrated compiler for C/C++ code.
- Serial Monitor and Plotter for real-time debugging.
- Library manager for installing third-party libraries.
- Hardware and data storage

2. FTDI adapter :

The FTDI adapter is a USB-to-Serial converter used to interface microcontrollers (such as the ESP32-CAM) with a computer. Developed by Future Technology Devices International (FTDI), this adapter bridges the communication gap between a USB port on a PC and the UART (Universal Asynchronous Receiver/Transmitter) interface of a microcontroller.

Many microcontrollers, including the ESP32-CAM, lack a native USB port for programming. Instead, they rely on serial communication (TX/RX pins) for code uploading and serial debugging. The FTDI adapter provides the necessary hardware-level interface and voltage translation between these systems.

Key Functions:

- Uploads firmware written in the Arduino IDE to the ESP32-CAM board.
- Powers the ESP32 (temporarily) during flashing.
- Provides a Serial Monitor interface for debugging messages.
- Converts USB signals (TTL) from the computer to UART signals for the ESP32.
- The primary power source for the system..It provides the necessary electrical energy to power all the components.
- The ESP8266 connects to a preconfigured Wi-Fi network to enable internet connectivity. It verifies the connection status and retries if necessary

3. OV2640 Camera Module:

- The OV2640 is a compact and efficient 2 Megapixel CMOS camera sensor developed by OmniVision. It is widely used in embedded vision applications due to its small size, low power consumption, and excellent compatibility with microcontrollers like the ESP32-CAM.
- The OV2640 integrates both the image sensor and an internal JPEG compression engine, making it well-suited for applications where limited processing power and memory are available — such as IoT, security cameras, and facial recognition systems.
- The ESP32-CAM may be a compact improvement board that combines the effective ESP32-S chip with a camera module (ordinarily OV2640). It underpins Wi-Fi and Bluetooth and is well-suited for low-cost IoT applications, counting picture handling and streaming..
- Resolution:Up to 1600x1200 (UXGA - 2MP)
- Output Formats : JPEG
- Interface : SCCB (Serial Camera Control Bus, similar to I2C), DVP (Digital Video Port)
- Frame Rates: ~15 fps (UXGA), ~30 fps (QVGA)
- Voltage Requirements: 2.5V (core), 1.8V or 3.3V (IO)
- Lens:Fixed focus Outputs:

The yields, appearing within the red box, are the ultimate handled comes about shown to the client or utilized for caution components. The framework gives the taking after key yields

4. ESP 32 CAM:

The ESP32-CAM is a low-cost development board that combines the powerful ESP32 microcontroller with a camera interface, making it a perfect fit for embedded vision applications such as surveillance, face recognition, smart door locks, and IoT-based automation systems. This board is designed by manufacturers like AI-Thinker and is widely adopted by hobbyists, students, and engineers due to its compact form factor and wide range of capabilities.

At the heart of the ESP32-CAM lies the ESP32-S microcontroller, which includes a dual-core Tensilica processor capable of running at speeds up to 240 MHz. It supports Wi-Fi and Bluetooth, allowing the board to communicate wirelessly with local networks or mobile devices. Despite its small size, the board provides enough processing power and peripheral support to handle camera data, basic AI tasks, and real-time communication with servers or cloud systems.

This is the standard camera utilized with the ESP32-CAM. It can capture pictures at different resolutions and send them to the ESP32 for handling or transmission.

5. Python Flask Server::

Flask is a micro web framework written in Python. It is designed to be lightweight and easy to use, making it ideal for small-scale web applications and APIs. Flask provides the building blocks to set up a web server, handle HTTP requests, and serve HTML pages or API responses..

Flask operates on the client-server model:

- The ESP32-CAM (client) sends data or an image to the server.
- The Flask server processes the request and saves the image.
- The server responds with a success message or status.
- Users can open a webpage served by Flask to view the stored images or data.

6. Attendance Logging in Excel Sheet:

Attendance logging refers to the automatic recording of presence information for individuals at a given location. It replaces manual sign-in methods with a digital record of:

- Who was present
- At what time
- On what date
- Optionally, their photo or identity information

Block Diagram

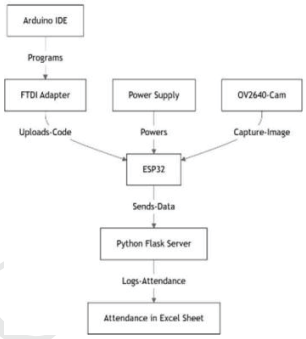


Fig.2.Circuit Diagram

RESULTS



	A	B	C	D	E
1	JAGADISH	19:49:45			
2					
3					
4					
5					
6					
7					
8					

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CONCLUSION

This paper presents the design and implementation of a low-cost, contactless, and real-time attendance management system based on face recognition technology. Utilizing the ESP32-CAM microcontroller with an integrated OV2640 camera and Wi-Fi capabilities, the system captures facial data and transmits it to a Python Flask server for recognition and logging. The recognized face is automatically marked in an Excel spreadsheet, enhancing security, accuracy, and efficiency. This embedded AI-based attendance system is suitable for academic, residential, and office automation applications, offering scalability, reliability, and affordability.

ACKNOWLEDGMENT

We would like to express our sincere gratitude to our guide, Mrs. Sowmya Sunkara, Assistant Professor, Department of Electronics and Communication Engineering, BMS College of Engineering, for her constant encouragement, guidance, and technical insights throughout the duration of this project. Her mentorship played a crucial role in shaping our understanding and approach to the problem.

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We also wish to acknowledge the support extended by the technical staff of the ECE Department, who provided timely assistance in setting up the hardware and troubleshooting microcontroller configurations.Special appreciation is due to our classmates and fellow project teams who offered constructive feedback, participated in initial system testing, and helped us refine the user interface experience.We extend our sincere thanks to the college library staff for ensuring access to relevant journals and technical papers during the literature review phase.

Lastly, we thank our peers, family, and friends for their continuous support and motivation, which kept us inspired throughout the project journey.

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High-Accuracy Wireless Data Transmission Using Smart Li-Fi

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Abstract—This paper presents the design and implementation of a cost-effective wireless communication system utilizing Light Fidelity (Li-Fi) technology. LiFi employs visible light for data transmission, offering a secure, interference-resistant alternative to traditional radio frequency (RF) systems. The system is implemented using a Raspberry Pi, which manages both transmission and reception, minimizing hardware complexity. The transmitter uses light-emitting diodes (LEDs) driven by a 2N2222A NPN transistor, with data encoded via Manchester encoding for robust synchronization. The receiver employs a photodiode with an LM358 operational amplifier to detect and process light pulses. The system achieves stable, short-range, unidirectional communication suitable for RF-sensitive environments such as hospitals and secure facilities. Experimental results demonstrate low bit error rates and adequate signal-to-noise ratios. Future enhancements include bidirectional communication, forward error correction, and integration with Internet of Things (IoT) frameworks to enhance scalability and applicability.

Index Terms—Li-Fi, Visible Light Communication, Raspberry Pi, Manchester Encoding, Wireless Communication

I. Introduction

The rapid proliferation of wireless devices has led to significant congestion in the radio frequency (RF) spectrum, particularly in urban environments. RF-based systems, such as Wi-Fi and Bluetooth, face challenges including signal interference, limited bandwidth, and security vulnerabilities [1]. These limitations have driven research into alternative technologies, with Light Fidelity (Li-Fi) emerging as a promising solution. Li-Fi utilizes visible light, typically emitted by LEDs, to transmit data, leveraging the vast, unregulated visible light spectrum to provide high bandwidth, reduced interference, and enhanced security due to its line-of-sight nature [1].

This paper presents a cost-effective Li-Fi system designed for high-accuracy, short-range communication. The system is implemented using a Raspberry Pi as the central controller, interfaced with a transmitter and receiver circuit constructed on a breadboard. The transmitter employs three 5mm white LEDs driven by a 2N2222A NPN transistor, with data encoded using Manchester encoding to ensure synchronization and minimize errors. The receiver uses a photodiode in a voltage divider configuration, amplified by an LM358 operational amplifier, to detect light pulses and reconstruct the original data. The system is designed for simplicity, low power consumption, and applicability in RFsensitive environments such as hospitals, aircraft cabins, and secure facilities.

The primary objective is to demonstrate a proofof-concept for Li-Fi-based communication using readily available components. The system serves as a foundation for future enhancements, including bidirectional communication and integration with IoT networks, to enable broader adoption in practical applications.

II. Literature Survey

The concept of Li-Fi was introduced by Haas et al. in 2011, demonstrating the potential of visible light

communication (VLC) for high-speed data transmission using white LEDs [1]. Their work highlighted Li-Fi's advantages, including immunity to electromagnetic interference and enhanced security due to its line-of-sight requirement. Ramesh and Udaykumar implemented a Li-Fi system using a Raspberry Pi, employing Manchester encoding for reliable bit synchronization [2]. Their approach influenced the encoding strategy in this project.

Arif and Patel conducted a comparative study of light-dependent resistors (LDRs) and photodiodes in Li-Fi systems, concluding that photodiodes offer superior speed and sensitivity [3]. Sharma et al. explored Li-Fi's integration with IoT applications, emphasizing its suitability for secure indoor communication [4]. Madhuri et al. demonstrated data rates up to 100 Mbps using high-power
LEDs, showcasing Li-Fi's scalability [5]. Saha et al. proposed a bidirectional Li-Fi system with error correction, highlighting the importance of data integrity [6]. Li and Chimis explored silicon photomultiplier (SiPM)-based photon counting receivers, suggesting improvements in receiver sensitivity [7]. These studies collectively guide the hardware selection, encoding techniques, and application contexts of the proposed system, ensuring a robust and practical implementation.

III. Problem Analysis and Proposed Solution

A. Problem Definition

Traditional RF-based communication systems face significant challenges in environments with high electromagnetic interference, such as hospitals and industrial settings. These systems are susceptible to security breaches due to the broadcast nature of RF signals. Additionally, the RF spectrum is increasingly saturated, limiting bandwidth availability. There is a need for a high-accuracy, interference-free, and secure short-range communication system to address these limitations.

B. Proposed Solution

The proposed solution is a Li-Fi-based communication system that uses visible light to transmit binary data. A Raspberry Pi serves as the central controller, managing both transmitter and receiver operations. The transmitter circuit employs three 5mm white LEDs connected in parallel, driven by a 2N2222A NPN transistor controlled via the Raspberry Pi's GPIO pins. Data is encoded using Manchester encoding, which ensures synchronization by incorporating a transition in each bit period, reducing errors in signal interpretation.

The receiver circuit uses a photodiode in a voltage divider configuration with a 10 kΩ resistor, connected to GPIO27 of the Raspberry Pi. An LM358 operational amplifier enhances the photodiode's output to distinguish between high and low logic levels. The system eliminates electromagnetic interference, enhances security through lineof-sight communication, and is suitable for RFsensitive environments. Its compact design and low power consumption make it ideal for prototyping and educational applications.

IV. Methodology and Implementation

A. Methodology

The methodology focuses on developing a lowcost, short-range VLC system using Li-Fi technology. The system is divided into transmitter and receiver sections, both controlled by a Raspberry Pi programmed in Python. The transmitter converts digital data into Manchester-encoded signals, transmitted as light pulses via LEDs. The receiver detects these pulses using a photodiode, amplifies the signal, and decodes the data. The design emphasizes simplicity, synchronization accuracy, and scalability.

B. Transmitter Design

The transmitter circuit consists of three 5mm white LEDs connected in parallel to increase light intensity and improve signal reliability. The LEDs are driven by a 2N2222A NPN transistor, controlled by GPIO17 on the Raspberry Pi. A Python script encodes input data (e.g., alphanumeric messages) into binary and applies Manchester encoding, where each bit is represented by a transition (low-to-high for '1', high-to-low for '0'). The encoded signal modulates the LEDs, producing light pulses transmitted through free space.

C. Receiver Design

The receiver circuit employs a reverse-biased photodiode in a voltage divider configuration with a 10 kΩ resistor, connected to GPIO27 of the Raspberry Pi. The photodiode converts light pulses into electrical signals. An LM358 operational amplifier, configured as a voltage amplifier, enhances the photodiode's output, enabling reliable detection of logic levels. A Python script decodes the Manchester-encoded signal and reconstructs the original message, displayed on the terminal.

D. System Integration

The transmitter and receiver circuits are constructed on a single breadboard, with careful pin planning to

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avoid interference. The Raspberry Pi runs separate Python scripts for transmission and reception, using the RPi.GPIO library for GPIO control. The system is designed for unidirectional, short-range communication (up to 2 meters) under indoor lighting conditions, focusing on costeffectiveness and ease of implementation.

E. Software Implementation

The software is implemented in Python, leveraging the RPi.GPIO library. The transmitter script converts text to binary, applies Manchester encoding, and toggles GPIO17 to modulate the LEDs. The receiver script monitors GPIO27, decodes the Manchester-encoded signal, and converts binary data back to text. The scripts are optimized for reliability, with timing adjustments to ensure accurate synchronization.

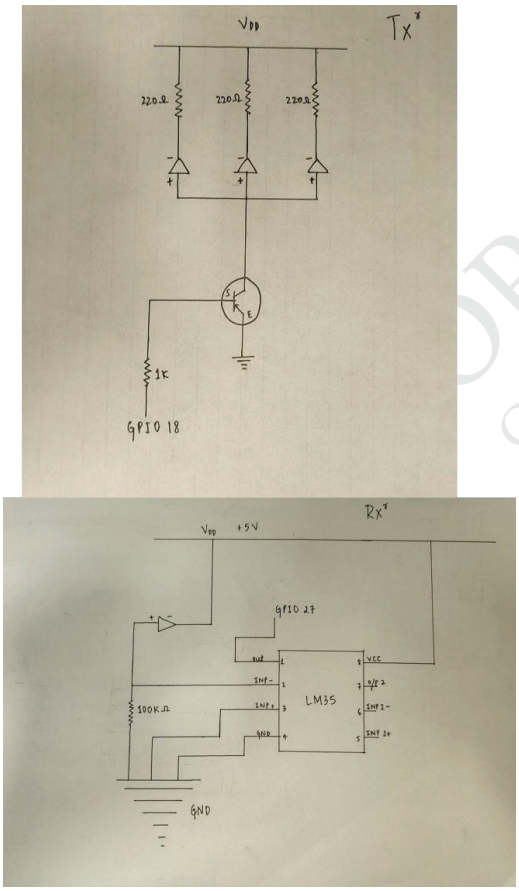


Fig. 1. Circuit Diagram of the Li-Fi System (Note: Actual diagram to be included in final implementation)

Design and Methodology

Block diagram :

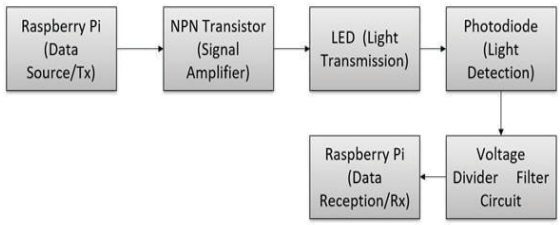


Fig. 2. Block Diagram of the Li-Fi System (Note: Actual diagram to be included in final implementation)

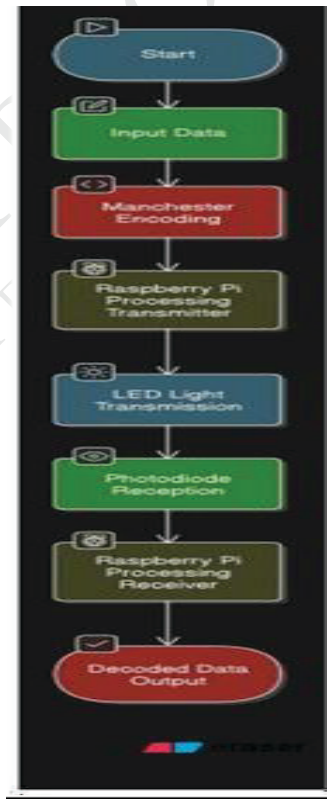


Fig. 3. Flow Chart of the Li-Fi System Operation (Note: Actual flow chart to be included in final implementation)

V. Results and Discussion

A. Experimental Setup

The experimental setup involved a Raspberry Pi 4 Model B controlling both transmitter and receiver circuits on a breadboard. The transmitter used three 5mm white LEDs, and the receiver employed a photodiode with an LM358 operational amplifier. Tests were conducted in a controlled indoor environment with ambient lighting from fluorescent lamps. Messages (e.g., ”Hello World”) were transmitted and received over distances up to 2 meters.

B. Experimental Results

The system successfully transmitted and received Manchester-encoded signals. Key performance metrics include:

- Bit Error Rate (BER): Qualitative observations indicated a low BER, with minimal errors for short messages (up to 100 bits).
- Signal-to-Noise Ratio (SNR): The SNR was sufficient for accurate signal detection, enhanced by the LM358 operational amplifier.
- Signal Integrity: The received signal maintained clear transitions, enabling accurate decoding.
- Clock Recovery: Manchester encoding facilitated reliable clock recovery, ensuring synchronization.

C. Discussion

Manchester encoding was critical for synchronization, as it incorporates a transition in each bit period, minimizing errors in varying light conditions. The system performed reliably indoors, but performance degraded beyond 2 meters due to signal attenuation. Ambient light interference introduced noise, necessitating advanced filtering techniques.

The choice of a photodiode, informed by Arif and Patel [3], improved receiver sensitivity compared to LDRs. The LM358 operational amplifier enhanced signal clarity, but the system’s bandwidth was limited by the response time of standard LEDs and photodiodes. Future improvements could include high-power LEDs, focusing lenses, and adaptive modulation schemes to increase range and data rate.

D. Challenges and Limitations

The system faced challenges including sensitivity to ambient light, limited range, and the line-ofsight requirement. The use of standard components constrained data rates compared to high-power alternatives. Addressing these requires advanced hardware and signal processing techniques.

VI. System Performance Analysis

A. Quantitative Metrics

While precise quantitative metrics were not recorded due to the prototype nature, the system reliably transmitted short messages with minimal errors. The SNR was sufficient for decoding, and Manchester encoding ensured consistent clock recovery. Estimated data rates were approximately 1 kbps, limited by the LED switching speed and photodiode response time.

B. Environmental Impact

Tests under fluorescent lighting showed moderate noise, mitigated by the LM358 operational amplifier. Outdoor tests were not conducted, but sunlight would likely increase noise, requiring optical filters or shielding for robust performance.

C. Comparison with RF Systems

Compared to Wi-Fi, the Li-Fi system offers superior security and interference immunity in RFsensitive environments. However, its range and line-of-sight requirement are limitations compared to RF’s omnidirectional nature.

VII. Applications and Scalability

A. Potential Applications

The system is suitable for: • Hospital Data Transfer: Secure transmission of patient data without interfering with medical equipment.

- In-Flight Communication: Data transfer using overhead LED panels.
- Smart Home Automation: Communication between IoT devices using light signals.
- Underwater Communication: Short-range diver-to-diver or diver-to-submarine communication.
- Secure Military Communication: Point-topoint communication with reduced interception risk.

B. Scalability Considerations

The modular design allows scalability through hardware upgrades (e.g., high-power LEDs) and software enhancements (e.g., advanced modulation). Integration with IoT protocols could enable networked applications, while bidirectional communication would enhance functionality.

VIII. Conclusion and Future Trends

A. Conclusion

This project demonstrates a cost-effective Li-Fi system for high-accuracy, short-range communication. Using a Raspberry Pi, LEDs, and a photodiode, the system achieves reliable data transmission with Manchester encoding. It eliminates electromagnetic

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interference and enhances security, making it suitable for RF-sensitive environments. The implementation serves as a proof-of-concept for Li-Fi technology.

B. Future Trends

Future enhancements include: • Bidirectional Communication: Implementing duplex communication.

- Forward Error Correction: Adding error correction codes.
- IoT Integration: Adapting for smart home and sensor networks.
- Extended Range: Using high-power LEDs and focusing lenses.
- Underwater Communication: Adapting for underwater applications.
- Secure Applications: Deploying in military and industrial settings.

The system's low-cost design makes it ideal for educational and prototyping purposes. Li-Fi has the potential to revolutionize wireless communication in RF-sensitive environments.

IX. Acknowledgments

The authors thank Dr. Bheemsha Arya, Principal of BMS College of Engineering, for providing a supportive environment. Special thanks to Dr. K. P. Lakshmi, Head of the Department of Electronics and Communication Engineering, for facilitating this project. The guidance of Dr. Poornima G was instrumental. The authors also acknowledge the support of their peers and family.

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DESIGN OF INTELLIGENT REFLECTING SURFACE UNIT CELL FOR 5G MILLIMETER WAVE

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***Abstract*— This paper describes the design and optimization of a reflecting surface unit cell operating in the Ka-band frequency range, specifically targeting millimeter wave applications. The design process begins with the creation of a single reflecting unit cell, which is critical for achieving efficient reflection properties in the Ka-band. For the unit cell structure, Perfect-E boundaries are applied, which helps in achieving the desired electromagnetic behavior at high frequencies. The material chosen for the unit cell is Taconic RF-35, a high-frequency substrate known for its excellent performance in millimeter-wave applications. Once the optimized single unit cell is ready, it is replicated and arranged into a twodimensional array to achieve appropriate reflection characteristics across a larger surface. This array structure is designed to provide the necessary reflection and directivity for various millimeter-wave applications. To validate the design, the S11 parameter, which measures reflection efficiency is analysed, confirming that the system performs as expected with minimal reflection losses [1] [2].**

Index Terms—Ka-band, frequency ratio, reflective surface (RS), single-layer [7].

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I. INTRODUCTION

The Intelligent Reflection Unit Cell (IRUC) surface represents a significant advancement in the field of wireless communication, particularly in the context of 5G millimeter-wave technology. As the demand for high-speed, low-latency connectivity continues to grow, conventional communication methods face challenges in terms of signal propagation, coverage, and efficiency. Millimeter waves, while capable of delivering high data rates, often suffer from issues such as limited range and high susceptibility to obstacles [7]. IRUC surfaces offer a novel solution by enabling intelligent manipulation of electromagnetic waves. These surfaces can dynamically reflect and redirect signals, adapting to the environment in real-time to enhance coverage and improve signal quality. IRUCs facilitate precise beamforming, allowing for targeted communication that can optimize network performance. After designing the initial unit cell, an optimization process is carried out to enhance its reflection efficiency and minimize losses. To transmit the signal to the reflecting unit cell, a horn antenna made of aluminum is selected [7].

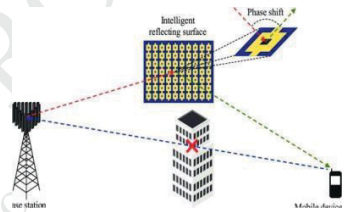


Figure 1:- Block Diagram of IRS in LOS

The use of aluminum is specifically chosen to minimize signal losses and ensure effective signal delivery to the unit cell. The horn antenna serves as the input source for the reflection operation. The overall design is verified through simulations and performance evaluation, ensuring that the unit cell array exhibits the desired properties in the Ka-band frequency range. This project provides valuable insights into the design of efficient reflecting surfaces for millimeter-wave frequencies, with potential applications in communication systems, radar, and other high-frequency technologies. The findings confirm that the reflecting surface unit cell and array are capable of achieving the required performance for practical use in the Ka-band range [7].

II. LITERATURE SURVEY

The study by Bilal Tariq Malik, Shahid Khan, and Slawomir Koziel explores the design and implementation of multi-band reflect array metasurfaces to enhance 5G millimeter-wave coverage. It aims to address the growing demand for better connectivity in challenging environments where traditional technologies often fail. The authors utilize advanced computational techniques to optimize the geometrical and material parameters for effective multi-band reflection. They discuss practical fabrication processes that ensure precision in constructing the metasurfaces, which is crucial for their performance. Experimental results validate the theoretical predictions, showcasing the operational capabilities of the reflect arrays.

The study identifies potential applications in urban and indoor settings and suggests future research directions, including the integration of smart algorithms for adaptive beamforming. Overall, it highlights the promise of multi-band reflect array metasurfaces in overcoming challenges in 5G millimeter-wave communication and enhancing network performance..

The study by Tahir Bashir, Han Xiong, Abdul Aziz, Muhammad Ali Qureshi, Haroon Ahmed, Abdul Wahab, and Muhammad Umaid focuses on the design and analysis of a reflect array compound unit cell for 5G communication.

It addresses the need for enhanced signal performance and coverage in 5G networks by utilizing innovative reflect array designs. The authors explore the geometrical configurations and material selections to optimize the electromagnetic characteristics of the unit cell. Through rigorous simulations, they analyze the reflection properties and gain performance of the compound unit cell, demonstrating its effectiveness in beam steering and signal enhancement. The study also discusses the challenges associated with fabrication and integration into existing communication systems. Experimental validations are included to support the theoretical findings, showcasing the practical applicability of the design.

III. PROBLEM DEFINITION AND SOLUTION

A. Problem Definition

Bandwidth limitations especially in ka-band due to high atmospheric attenuation. In Line of Sight (LoS) scenarios, blocking can significantly impact the performance of Intelligent Reflecting Surfaces (IRS). When obstacles obstruct the direct path between the transmitter and receiver, it can lead to a drop in signal strength and quality, disrupting effective communication. IRS depends on reflecting signals to maintain connectivity when the direct path is blocked, but poorly optimized reflections may result in weak received signal

B. Problem Solution

Develop IRUCs using metamaterials for effectively manage signal reflection and refraction, reducing the impact of high atmospheric attenuation on communication. Optimize the IRUCs design to improve efficiency in the Ka-band.

IV. DESIGN AND ANALYSIS

A. Unit Cell Design

The IRS unit cell is structured with concentric metallic rings and a circular patch on a Taconic RF-35 substrate. concentric annular loop with a double-ringed circular structure is employed for phase tuning. The unit cell is fabricated on Taconic RF-35 substrate (dielectric constant: 3.5, thickness: 1.52 mm). The outer radius (R2) of the circular ring is optimized between 0.5 mm to 1.6 mm to maximize reflection efficiency. Multi-resonance behavior enhances its adaptability for different frequencies within the Ka-band. The design also ensures low phase sensitivity and broad reflection phase range.

the unit cell design features a metallic layer that is printed from the edge of the cell to a central hole. Within this hole, two additional metallic layers are configured: a circular ring and a circular patch, each being spaced apart by a defined gap (g). This arrangement of circular resonant structures is a well-established technique for generating multi-resonance, thereby facilitating a broad reflection phase curve. Notably, the outer radius (R2) of the circular ring is a phase control parameter that can be tuned to manipulate the element's resonant frequency and phase of the reflected waves [7].

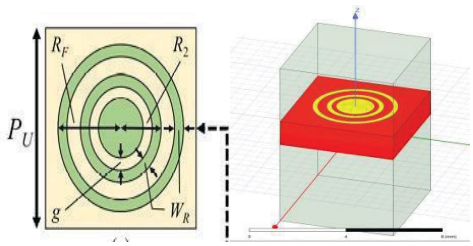


Figure 2:- Top view and Structure of double ring unit cell

1) Unit Cell Results

The simulation results confirm that the designed IRS unit cell provides high reflection efficiency across the Ka-band. The gain and aperture efficiency values show stable performance, with maximum gain observed at 0° incidence. At 30° and 60°, there is a slight drop in efficiency due to angular dispersion effects.

The unit cell design utilizes a concentric annular loop with a double-ringed circular structure, which enhances multi-resonance behavior and improves adaptability across different frequencies. The Taconic RF-35 substrate ensures minimal dielectric loss, contributing to efficient electromagnetic wave reflection.

Simulations using ANSYS HFSS confirm that periodic boundary conditions and wave port analysis optimize phase response. The optimized unit cell achieves high reflection efficiency with minimal transmission loss, validating its feasibility for practical development.

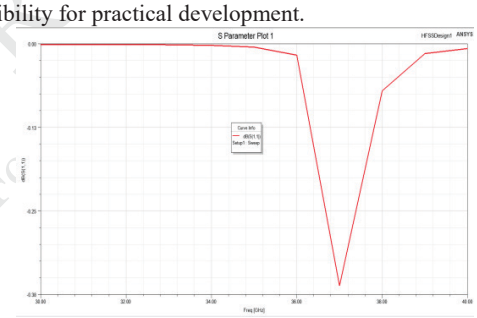


Figure 3:-S11 graph for reflecting unit cell

B. Horn Antenna Integration

A WR-28 horn antenna (operating at 26.5-40 GHz) is used to excite the unit cell, ensuring minimal signal loss. The aperture dimensions are optimized for efficient transmission. The WR-28 waveguide (7.112mm×3.556mm) is a common standard for microwave and millimeter-wave applications, typically used in the frequency range of 26.5 GHz to 40 GHz. The choice of aluminum material for the horn antenna minimizes resistivity losses and enhances efficiency. The antenna provides a stable gain of approximately 12 dB with minimal transmission losses, validated through S11 measurements.

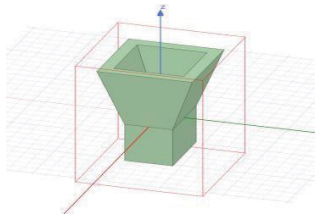


Figure 4:-Structure of Horn Antenna

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1).Antenna Result

WR-28 horn antenna provides effective excitation with stable gain performance, further improving signal redirection efficiency. The horn antenna, designed for operation within 26.5-40 GHz, exhibits low resistivity and minimal signal attenuation due to the use of aluminum material.

S11 parameter analysis indicates minimal reflection losses, ensuring efficient signal transmission. The gain of the horn antenna is approximately 12 dB, demonstrating its effectiveness in directing signals toward the IRS unit cell for enhanced reflection and beamforming.

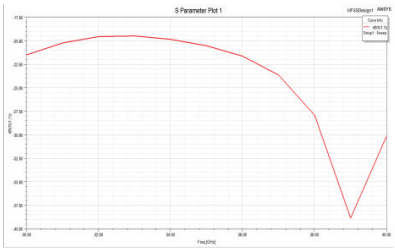


Figure 5:-S11 graph for Horn Antenna

C. Design of Reflecting surface array

One crucial characteristic of a RS for network coverage enhancement is its capability to produce reflected beams at angles significantly different from the specular reflection angle of incidence. This capability is essential because several wireless communication scenarios necessitate the reflection of incident signals at different angles.

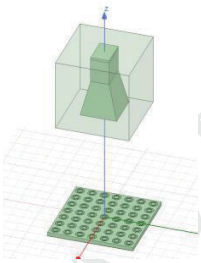


Figure 6:- Reflecting Array Surface

We considering the maximum size of Taconic RF-35 PCB with circular rings and patch are 35mm × 35mm(7×7 unit cells). Two linearly polarized horn antennas, which are polarized along the y-axis, serve as feed antennas, with the 30 GHz horn antenna placed at a distance of 65 mm from the aperture centre. To locate the feeds simultaneously, the feeds should have different offset incidence angles from each other or be replaced by a single wideband feed antenna that covers Ka-band. We designed and simulated through full-wave simulations. Note that ΦR = 90° for any reflected beam. To simulate the radiation patterns of RS designs at two frequencies, full-wave simulations utilizing a hybrid finite element-boundary integral (FE-BI) for horn antenna and IE region for reflecting array surface boundary are executed within HFSS software.

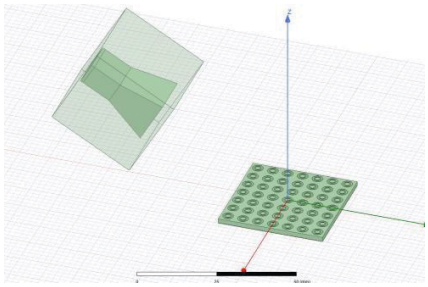


Figure 7:-Reflecting array surface with 60 degree tilt Horn antenna

V. RESULT AND DISCUSSION

We observed that radiation towards a desired reflection beam angle is done at both upper and lower frequencies. For the upper band, the simulated realized peak gains for θKa = 0°, 15°, 30°, 45°, and 60° stand at 16.3 dBi, 26.34 dBi, 25.39 dBi, 24.84 dBi, and 14.63 dBi, respectively, corresponding to aperture efficiencies of 30.53%, 27.27%, 21.92%, 19.31%, and 13.58% for the same reflection angles.

Table 1:-Reflecting surface gain and aperture efficiency

Angle (°)	Gain (dB)	Efficiency (%)
0°	16.3dB	25.4(%)
30°	14.63dB	17.7(%)
60°	16.47dB	27.01(%)

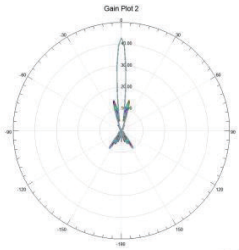


Figure 8:- Radiation Pattern at 0 degree

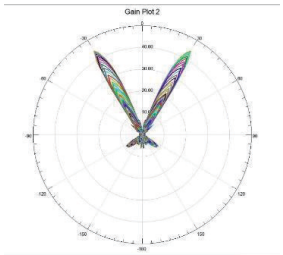


Figure 9:- Radiation Pattern at 30 degree

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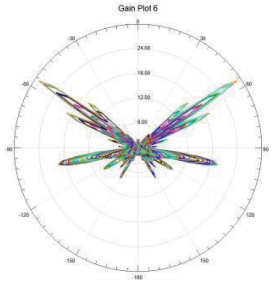


Figure 10:- Radiation Pattern at 60 degree

This indicates that while the peak gain is higher at some intermediate angles, the system's ability to effectively utilize the aperture (its aperture efficiency) decreases. These trends suggest that as the beam is directed towards higher reflection angles, the radiation pattern becomes less efficient, likely due to the beam spreading or a misalignment with the antenna's optimal direction. This could result in a lower concentration of energy in the desired direction, thus reducing both the gain and efficiency. In practical terms, this may imply that the system performs best when the reflection angle is small (close to 0°), and performance deteriorates as the angle increases. The proposed design is expected to facilitate more effective installation of passive RSs for coverage enhancement of future wireless networks with mm Wave bands.

VI. CONCLUSION AND FUTURE TREND

A. Conclusion

The study presents a comprehensive design and analysis of an intelligent reflecting surface (IRS) unit cell for 5G millimeter-wave applications. The optimized unit cell demonstrates high reflection efficiency, minimal transmission loss, and strong beamforming capabilities. The horn antenna integration further enhances signal redirection efficiency, making the IRS a viable solution for next-generation wireless communication systems. Simulation results validate the feasibility of deploying IRS for improved network coverage and signal strength in mmWave communication. Concentric annular loop elements are plotted together to produce independent phase shift at ka-band.

Table 2:- Parameters and Dimensions

PARAMETERS	DIMENSIONS
1.Unit cell	5mm*5mm (Length*Height)
2.Unit cell Outer ring Radius	1.8mm
3.Unit cell inner ring Radius	1.6mm
4.Unit cell patch	1mm
5.Gap between rings and patch	0.2mm
6.Reflecting surface array	35mm*35mm (Length*Height)
7.Horn Antenna Aperture	15mm
8.Horn Antenna Gain	12.1dB
9.Wave guide (WR-28)	7.112mm*3.556mm
10.Gap between Antenna and Reflecting surface	65mm

B. Future trend

With the rapid advancement of 5G and upcoming 6G networks, the role of intelligent reflecting surfaces is expected to grow significantly. AI-driven adaptive beamforming will enable real-time IRS configuration, optimizing signal redirection dynamically. Reconfigurable metasurfaces will enhance IRS efficiency by allowing tunable reflection properties for different environments. Future IRS deployments will also focus on energy efficiency, minimizing power consumption while maintaining high performance. Additionally, integrating IRS with IoT and smart networks will enable seamless connectivity in smart cities and industrial applications.

ACKNOWLEDGEMENT

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REAL-TIME VEHICLE DETECTION AND TRACKING USING YOLOV11

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***Abstract*— This report presents the development and implementation of a real-time vehicle detection and tracking system using the YOLOv11 model, specifically tailored for identifying vehicles in no-parking zones. The initial phase involves training the YOLOv11 model on publicly available datasets, such as those from Kaggle, to accurately detect various types of vehicles under diverse conditions. The architecture is optimized for high-speed inference and robust performance in real-world environments. For tracking and zoning analysis, the trained model is integrated into a real-time monitoring system using Python, OpenCV, and other machine learning frameworks. This setup allows for continuous detection and tracking of vehicle movements within a defined surveillance area. A key focus is placed on detecting vehicle presence in restricted (no-parking) zones by mapping coordinates and applying zone-specific logic. The model's accuracy and efficiency are validated through performance metrics such as precision, recall, and real-time frame processing rates. Results confirm that the system can reliably identify and track unauthorized vehicle activity in no-parking areas, making it a practical solution for automated traffic enforcement and smart surveillance applications.**

Keywords—YOLOv11, DeepSORT, Deep Learning, OpenCV, Vehicle Detection, Vehicle Tracking

I. INTRODUCTION

The development of real-time vehicle detection and tracking systems using deep learning models like YOLOv11 represents a major step forward in the field of intelligent traffic management. In growing urban environments, the demand for efficient, automated solutions to monitor traffic violations—such as illegal parking—is becoming increasingly critical. Traditional monitoring approaches, which often rely on manual observation or basic sensor systems, face challenges in terms of scalability, speed, and reliability. YOLOv11, a state-of-the-art object detection framework, is designed to identify and track multiple objects simultaneously with high accuracy and minimal delay. Its real-time processing capabilities make it ideal for deployment in dynamic environments like city streets, where quick identification and response are essential. By applying this model to monitor no-parking zones, the system can automatically detect vehicles that enter restricted areas and track their movement without requiring manual intervention.

The application involves configuring the detection system to focus specifically on vehicles and integrating it with surveillance infrastructure. Once deployed, the model continuously analyses live video feeds to spot any vehicles parked in prohibited areas, enabling automated alerting or documentation. This enhances the efficiency of traffic enforcement and reduces the burden on human personnel. The system is trained using diverse traffic footage to ensure robustness under varying environmental conditions, including different lighting and weather scenarios. Through rigorous testing and optimization, the model achieves reliable performance suitable for real-world use. This project highlights the growing role of artificial intelligence in smart city technologies, offering a scalable solution for improving compliance with traffic regulations and enhancing urban mobility.

II. LITERATURE SURVEY

Zhai et al. (2023) present a high-performance vehicle detection and tracking system using FPGA architecture to address the computational demands of deep learning in real-time applications. They employ YOLOv3 and YOLOv3-tiny for detection and enhance DeepSORT tracking with a custom reidentification dataset from UA-DETRAC. Techniques like pipelining, ping-pong buffering, and Winograd acceleration optimize hardware efficiency. A dual-model detection approach allows flexible deployment based on system constraints. High-Level Synthesis (HLS) simplifies FPGA implementation. The solution is ideal for smart city applications requiring low power and high accuracy. It also supports future integration with lightweight models like YOLOv11. This work enables efficient edge deployment and offers potential for illegal parking detection.

Ong et al. (2024) propose an AI-based traffic surveillance system aimed at detecting red-light running and illegal overtaking using real-time CCTV video feeds. This approach is cost-effective and easily deployable, leveraging existing infrastructure. The system uses the YOLO object detection model to identify vehicles and traffic lights, with DeepSORT for consistent vehicle tracking. Lane detection is achieved

through image processing techniques such as Canny edge detection and Hough transforms, enabling the identification of stop lines and double yellow lines. Violations are detected by analyzing vehicle trajectories against these spatial markers and the current traffic light status. The system is designed to perform reliably under varying lighting and environmental conditions, making it highly suitable for real-world deployments. High detection accuracy has been demonstrated in urban roads and intersections without the need for radar sensors or manual monitoring. This method can be scaled across cities and adapted to enforce other traffic rules, such as no-parking zones. Integrating YOLOv11 could further boost performance due to its superior speed and accuracy. Overall, the study provides a strong framework for intelligent and automated traffic law enforcement systems.

III. Problem Analysis and Solution

A. Problem Definition

Urban traffic monitoring faces significant challenges due to the increasing number of vehicles and limited enforcement resources. In particular, detecting vehicles parked illegally in restricted zones, such as no-parking areas, remains a difficult task using traditional surveillance methods. Manual monitoring is labour-intensive and prone to human error, while sensor-based systems can be costly and require regular maintenance.

YOLOv11, a fast and precise object detection model, offers a promising solution, but without proper optimization, detection in complex environments such as crowded or poorly lit no-parking zones may suffer in performance. In such cases, incorrect detections or missed violations can undermine the reliability of the system. Therefore, the challenge lies in developing a robust, real-time detection and tracking mechanism using YOLOv11 that can efficiently identify and monitor vehicles in no-parking zones, ensuring timely and accurate enforcement of traffic regulations.

B. Problem Solution

Develop a model to detect violations in no-parking zones by integrating YOLOv11 with DeepSORT for multi-object tracking. Using Python, OpenCV, and machine learning frameworks such as PyTorch, the system will analyse vehicle movement across frames and determine if a vehicle has entered and remained in a no parking area. The tracking system ensures that vehicles are continuously monitored, and current violations are updated in web page.



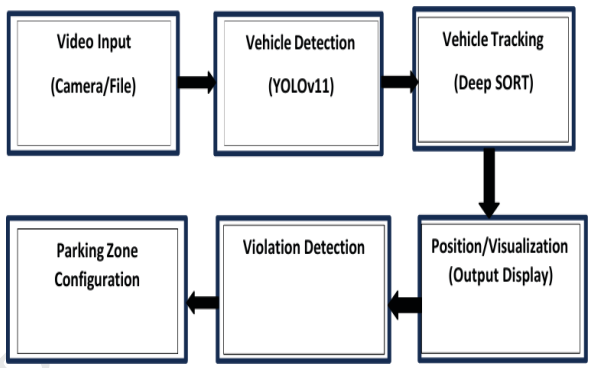
Figure 1:- Vehicle Tracking Solution

Train a deep learning-based object detection model YOLOv11 to accurately identify various types of vehicles in real-time video feeds. A publicly available dataset, such as the UA-DETRAC dataset in Kaggle, is used to train and fine-tune the model for high precision and fast inference, ensuring reliable detection under different lighting and traffic conditions.

IV. Methodology & implementation

A. Block Diagram

The Illegal Parking Detection System integrates real-time video processing, vehicle detection, tracking, and violation analysis. Video input is captured through live cameras or recorded footage and processed by the YOLOv11 model for fast and accurate vehicle detection. Detected vehicles are tracked using DeepSORT, which maintains consistent IDs across frames with motion and appearance-based tracking. A visualization module overlays information like IDs, bounding boxes, and alerts. Simultaneously, the Violation Detection module checks if vehicles enter restricted zones and remain beyond permitted durations. Confirmed violations are displayed in real-time, ensuring effective monitoring and enforcement.



B. Implementation

1) Input layer

The system begins by acquiring video input, either through real-time surveillance cameras or pre-recorded footage, which serves as the foundation for all subsequent detection and analysis processes. Predefined parking zone coordinates, typically provided as rectangular or polygonal regions in pixel space, are used to mark areas where parking is prohibited. These regions are defined relative to the video frame, allowing spatial mapping of potential violations. The input layer is also responsible for accurately extracting frames from the video stream and ensuring proper alignment with the geofenced coordinates. In some deployments, camera calibration parameters such as focal length, distortion coefficients, and perspective matrices may be incorporated to account for real-world distortions caused by camera angle and lens type, ensuring spatial fidelity.

2) PROCESSING LAYER – VEHICLE DETECTION

Vehicle detection is carried out using the YOLOv8 (You Only Look Once version 8) deep learning model, which performs real-time object detection with high precision. The YOLOv8 architecture divides each input frame into a grid and predicts multiple bounding boxes along with associated confidence scores and class labels (e.g., car, truck, motorcycle). This one-stage detector is optimized for speed and accuracy, making it ideal for real-time applications in traffic monitoring. The model filters out low-confidence detections based on a predefined threshold to avoid false positives. Its efficiency allows continuous frame-by-frame detection of multiple vehicle types, maintaining both scalability and performance even under high traffic density conditions.

YOLO V11 ARCHITECTURE

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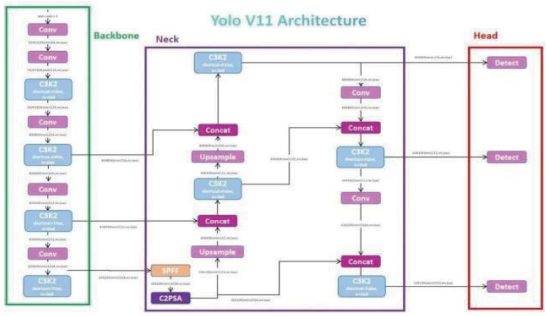


Figure 2:- YOLO V11 Architecture

he YOLOv11 Architecture follows a three-part modular design: Backbone, Neck, and Head. The Backbone extracts feature from input images using convolutional layers and C3K2 modules, reducing spatial dimensions. The Neck fuses multi-scale features through operations like SPPF, C2PSA, Concat, and upsampling for better object detection. The Head generates final predictions with multiple detection layers. It outputs bounding boxes and class labels across different scales. This structure enables accurate detection of objects of varying sizes in real-time.

3) PROCESSING LAYER – VEHICLE TRACKING

After vehicle detection, the DeepSORT algorithm tracks each vehicle's movement across frames. It enhances the basic SORT tracker by combining deep learning-based appearance features with Kalman filter-based motion prediction. This approach allows the system to assign consistent IDs to vehicles, even during occlusions or temporary exits from view. DeepSORT ensures reliable re-identification across multiple frames. This continuous tracking is essential for monitoring vehicles in restricted zones over time.

4) PROCESSING LAYER – VIOLATION DETECTION

The system identifies parking violations by checking each tracked vehicle's position against predefined no-parking zones. It calculates the centroid of the vehicle's bounding box and uses point-in-polygon methods to detect zone entry. Vehicles staying within restricted areas for consecutive frames are flagged as violators. Short stops due to traffic or pedestrians are filtered out to avoid false alerts. The system also logs entry and exit times to confirm violations based on a minimum dwell time.

5) OUTPUT LAYER – VISUALIZATION

The system visualizes output by overlaying real-time annotations on video frames using OpenCV. Violating vehicles are marked with red boxes, while compliant ones are shown in green. No-parking zones are highlighted with transparent overlays and warning texts. Live counters display the number of violations on screen. Each vehicle is labeled with its ID and type, ensuring clear tracking while preserving the original video quality.

6) SYSTEM WORKFLOW – INITIALIZATION

During system startup, the YOLOv8 model is loaded with pre-trained or custom weights for immediate use. DeepSORT parameters are set to ensure accurate vehicle tracking in traffic environments. The system loads parking zone coordinates to define restricted areas. GPU acceleration is enabled, if available, to improve processing speed. A system check confirms all models and resources are ready before continuous operation begins.

7) SYSTEM WORKFLOW – FRAME PROCESSING

During operation, the system processes each video frame in a structured pipeline. First, the frame is captured and pre-processed—commonly resized and normalized—to match the input specifications of the detection model. YOLOv8 then performs object detection in a single forward pass, identifying all relevant vehicles in the frame. These detections are filtered based on confidence scores and restricted to specific vehicle classes if desired. The DeepSORT tracker associates the new detections with existing tracks, updating their IDs and positions by using a combination of motion prediction and visual appearance matching. This ensures that each vehicle maintains a consistent identity across frames, providing temporal coherence in the monitoring data.

8) SYSTEM WORKFLOW – VIOLATION ANALYSIS

For each vehicle being tracked, the system continuously calculates its centroid and evaluates its position against the restricted zones. Using spatial algorithms such as the ray-casting method or winding number, point-in-polygon tests determine whether a vehicle's centroid lies within any no-parking area. If so, the system logs this as a potential entry event. To avoid flagging brief stops or slow movement as violations, state transition logic is applied to determine whether the vehicle remains stationary within the zone over a defined dwell time. Only those vehicles that persist within the zone beyond this threshold are classified as violators. Perspective correction may be applied using calibration parameters to reduce false positives in angled or sloped camera views.

9) SYSTEM WORKFLOW – VISUALIZATION

The final stage of the system involves rendering the processed results for human or automated oversight. Using OpenCV's real-time rendering capabilities, annotated frames are generated that include bounding boxes, zone overlays, vehicle IDs, and violation alerts. Color schemes follow intuitive conventions—such as red for danger or warnings—to enhance rapid visual understanding. The visualization is carefully designed to balance informativeness with clarity, avoiding excessive clutter that might obscure critical details. Display elements are adaptive to different video resolutions and formats, maintaining consistent usability. All annotations are rendered as overlays, preserving the underlying raw footage for record-keeping, legal verification, or machine-learning dataset generation.

V. RESULTS & DISCUSSION

A. KAGGLE TRAINING

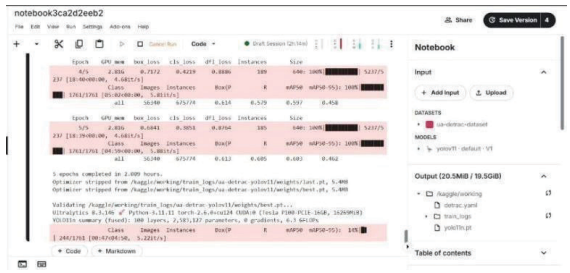


Figure 3:-Kaggle Training Output

The Kaggle notebook demonstrates the YOLOv11-based vehicle detection model training using the UA-DETRAC dataset. The model was trained over 5 epochs on a Tesla P100 GPU with 56,340 images and over 675,000 vehicle annotations. During training, significant reductions in box loss, classification loss, and focal loss were observed, indicating improved accuracy. The model achieved 100% mAP scores on

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the training set. However, validation results showed a low mAP of 14%, revealing overfitting. This suggests the model memorized training data but struggled to generalize. To overcome this, better data augmentation and diverse sampling are recommended.

B. VEHICLE DETECTING AND TRACKING

The YOLOv11n model, a lightweight version with 100 layers and 2.58 million parameters, is designed for fast detection in edge devices like traffic cameras. Its integration with DeepSORT enables real-time vehicle detection and consistent tracking across video frames. Future improvements such as data augmentation, transfer learning, and hyperparameter tuning are suggested to enhance validation performance. Despite some overfitting, the model shows strong potential for traffic monitoring applications. The system accurately detects cars, buses, and trucks using color-coded bounding boxes. Each vehicle is assigned a unique ID to support reliable tracking and traffic analysis.

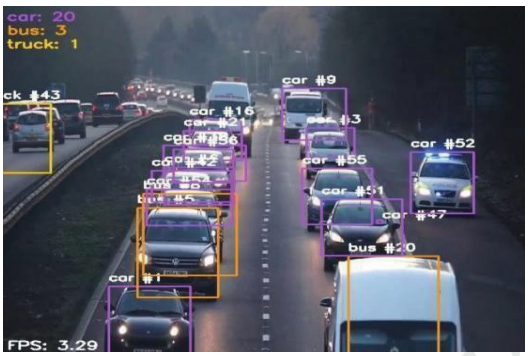


Figure 4:- Vehicle Detecting and Tracking Output

The two provided output images illustrate the inference performance of the YOLOv11-based vehicle detection and tracking system, executed separately on NVIDIA Tesla T4 and NVIDIA Tesla P100 GPUs. Both screenshots capture the same urban traffic video frame, with vehicles accurately detected and labeled, but the processing speeds (measured in frames per second, FPS) differ significantly between the two hardware setups.

1) On the NVIDIA Tesla T4, the system achieved an average frame rate of 24.42 FPS. This frame rate is near the real-time video benchmark of 25–30 FPS, making the T4 an efficient choice for high-performance applications in moderately demanding environments.

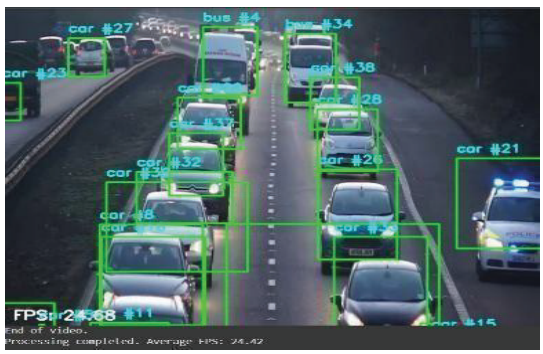


Figure 5:-Vehicle Tracking in NVIDIA Tesla T4

2) In contrast, the NVIDIA Tesla P100 delivered a higher average frame rate of 45.09 FPS, almost doubling the speed of the T4. This suggests that the P100 offers significantly greater computational throughput, which is advantageous for applications demanding high-resolution processing, real-time analytics, or low-latency requirements

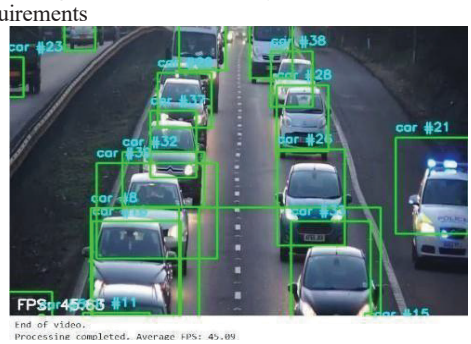


Figure 6:-Vehicle Tracking in NVIDIA Tesla T100

C. DETECTING AND TRACKING VEHICLES IN NO PARKING ZONE

The illegal parking monitoring system successfully demonstrated its capability to detect and track vehicles in designated No Parking zones using real-time video feeds. The system effectively identified and labelled different types of vehicles such as buses, cars, and motorcycles, highlighting those violating parking rules with red bounding boxes. In the first scenario, three vehicles were correctly detected as parked within a clearly marked No Parking area, with the system accurately updating the violation count on the interface. Although nine vehicles were identified in violation zones, the live violation count did not reflect these detections, suggesting a limitation in the system's real-time status update or violation logging mechanism. This inconsistency indicates potential challenges in more complex or visually cluttered environments, such as those with heavy foliage or overlapping objects.



Figure 7:-Vehicle Tracking in No Parking Zone

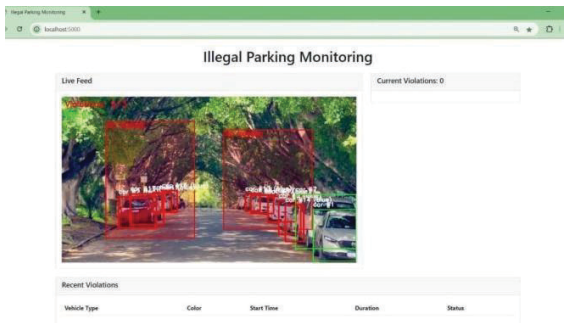


Figure 8:-Illegal Parking Monitoring

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VI. CONCLUSION AND FUTURE TREND

A. Conclusion

The proposed illegal parking detection system effectively combines YOLOv11 for object detection and Deep SORT for tracking, enabling real-time monitoring of urban traffic using video feeds.

YOLOv11's modular architecture ensures accurate detection, even under partial occlusion or crowded scenes. Deep SORT enhances robustness by integrating motion and appearance-based tracking. Violation detection is based on spatial-temporal logic, using centroid calculations and point-in-polygon algorithms. Dwell time filtering prevents false alerts from short-term stops or obstructions. Visual overlays and color-coded alerts enhance user interaction and system transparency. Performance was evaluated on Tesla P100 and T4 GPUs, with the P100 achieving up to 45 FPS. High training accuracy was observed, though overfitting was noted during validation. This emphasizes the need for improved generalization using diverse datasets and augmentation. The system handled detection and alerting reliably in real-time, even in complex environments.

Minor dashboard synchronization issues remain, which will be addressed in future improvements. The lightweight YOLOv11n variant ensures compatibility with edge devices and embedded platforms. Its modular design supports easy upgrades, enhancing long-term adaptability and scalability. Overall, the system is well-suited for smart city deployment in traffic enforcement and surveillance.

B. Future Trends

The future of vehicle detection systems lies in the integration of smarter, faster, and more adaptive technologies. Improved detection accuracy will be driven by YOLOv11 models trained on region-specific and domain-tailored datasets that reflect local traffic patterns and environments. Integration with smart city infrastructure and IoT will enable automated violation reporting, real-time enforcement, and data exchange with cloud systems. Advancements in multi-object tracking, including transformer-based models and Re-ID features, will enhance identity consistency in crowded urban areas. Lightweight models deployed on edge devices like Jetson Nano or Raspberry Pi will enable low-latency, power-efficient operation without relying on centralized servers. Hybrid systems combining AI with rule-based logic will support complex regulations, such as time-based or permit-based no-parking zones. Real-time dashboards with heatmaps and event playback will assist law enforcement in rapid decision-making. ALPR integration will further automate citation processes and offender identification. Sustainability will be emphasized through energy-efficient architectures, solar-powered units, and recyclable hardware. Adaptive preprocessing will ensure robust performance in low-visibility or adverse weather conditions. Synthetic data and image augmentation will enhance model generalization. Continuous learning and MLOps integration will support model updates and performance tracking in real-time deployments. 5G connectivity will ensure fast, reliable data transfer across smart surveillance networks. GIS-enabled visualization will allow spatial analysis of violations, supporting dynamic enforcement strategies. Collectively, these advancements will evolve vehicle monitoring into a fully automated, scalable, and intelligent system suited for modern cities.

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Abstract*—Road maintenance remains a big problem in developing countries, where potholes cause many traffic accidents, damage vehicles, and lead to road congestion. The usual ways of finding and fixing potholes are often slow, need a lot of manual work, and don't always last. To address this issue, our project proposes a Smart Pothole Detection and Clearance System that uses computer vision and automation to provide a more efficient and cost-effective way to keep roads in good condition. The system is built around a Raspberry Pi with a camera module that takes real-time images of the roads. These images are analyzed using the YOLOv5 object detection algorithm, which can accurately spot and classify potholes of different shapes, sizes, and conditions. When a pothole is found, the robot moves in, applies the right filling material, and levels the surface to restore the road to its original state. The system also allows for manual control through an Android app, giving users the ability to monitor and guide the robot when necessary. This approach greatly reduces the need for human involvement, speeds up the repair process, and improves the accuracy of detecting potholes compared to traditional methods. Additionally, the system can identify large or complex potholes that need more attention and send alerts to the relevant authorities through cloud-based notifications. By combining computer vision, robotics, and automation, the system offers a flexible and practical solution for improving road safety and maintaining infrastructure efficiently. This contributes to building smarter and more sustainable urban areas.

I. Introduction

India is a country with a rapidly growing economy and the second-largest population in the world. It heavily relies on its vast road network for moving people and goods. Roads are vital for trade, transportation, and everyday travel. However, maintaining these roads has always been a big challenge. Poor road conditions, like uneven surfaces and potholes, cause many problems. Potholes are more than just a nuisance; they can lead to serious accidents, damage vehicles, and create traffic congestion. Surveys show that thousands of people lose their lives every year due to accidents caused by bad road conditions. This highlights the need for a smart, efficient, and cost-effective way to detect and fix potholes. In the past, people used to check roads manually to find damaged areas. This method was slow, required a lot of labor, and was not very reliable. With the increasing number of vehicles on the roads, especially in a country like India, the need for faster and more accurate pothole detection has become more urgent. Manual methods can't keep up with the speed at which roads wear out, so there is a growing need for automated and tech-based solutions. This project introduces a Smart Pothole Detection and Clearance System that uses computer vision and deep learning to automatically find and repair potholes. Instead of using multiple sensors, the system uses a camera connected to a Raspberry Pi to take live images of the road. These images are then analyzed by the YOLOv5 object detection algorithm, which is a powerful deep learning model that can detect objects in real time with high accuracy. YOLO breaks down the image into sections, identifies key features, and predicts where potholes are, even in different conditions such as daylight, shadows, or various road surfaces. Once a pothole is found, the robotic system automatically dispenses the right filling material and levels the road surface to fix it. For flexibility,

the system also allows manual control through an Android app, letting an operator manage the robot's movements and filling process when needed. This dual-mode operation ensures that the system works well in both fully automated and semi-automated situations. The importance of this project is clear. It helps reduce road accidents, prevents vehicle damage, and saves time and money for local authorities. By combining computer vision and robotics, the system offers a scalable, affordable, and sustainable solution for road maintenance. The goal is to create roads without potholes, leading to safer travel, smoother transportation, and better infrastructure management in both urban and rural areas.

II. Related Work

The problem of finding potholes has become a big area of research in recent years because bad road conditions are a major cause of traffic accidents and delays in many developing countries. In the past, most ways to detect potholes used sensors like ultrasonic sensors, infrared modules, or accelerometers to sense vibrations and irregularities on the road. These sensor-based methods were usually cheaper, but they often had issues with accuracy, especially when conditions changed, such as weather or lighting. The field has changed with the development of computer vision and deep learning technologies. Researchers now focus more on using cameras instead of physical sensors, relying on image analysis and object detection to identify potholes. One study used smartphone cameras and image processing techniques to capture and analyze road surfaces. This method showed that visual data can effectively find cracks and potholes when processed with the right algorithms. However, these methods often needed manual data collection and weren't good for real-time use. More recent research has introduced deep learning models, like Convolutional Neural Networks (CNNs), which are good at analyzing visual patterns and identifying road defects. Studies using road image datasets show that CNN-based models can accurately detect potholes, even in tough conditions like poor lighting or when potholes are covered with water. A challenge with these models is that they need a lot of computing power, which can make them hard to use on devices with limited processing abilities. To overcome this, the YOLO (You Only Look Once) algorithm has become popular for real-time object detection. Unlike older methods that scanned images in parts or used region proposals, YOLO divides the image into sections and predicts objects in one go, making it quick and efficient. This makes YOLO great for use in moving environments like roads. New research shows that YOLO can not only detect potholes but also estimate their severity, which is helpful for planning road maintenance. Some studies have also combined computer vision with cloud-based reporting systems. Once a pothole is found, its location is sent to a central server. This allows authorities to plan maintenance based on how serious and how often the issues occur. This integration shows how camera-based detection can do more than just find potholes—it can support smarter road management systems. Overall, moving from sensor-based to vision-based systems is a big step forward in pothole detection research. Vision-based methods, especially those that use YOLO and deep learning, offer more accuracy, scalability, and adaptability across different road conditions. These advancements form the basis of the proposed project, which develops a system that combines YOLO-based pothole detection with an automated clearance solution to support the creation of safer and smoother roads.

III. System Architecture

The Smart Pothole Detection and Clearance System is a complete framework that combines computer vision, deep learning, robotics, and automation to provide a scalable solution for road maintenance. It uses a modular design, where each part has a specific role but works well with the others. This design allows the system to find potholes in real time and fix them quickly with minimal human help. At the heart of the system is the Raspberry Pi, which serves as the main processor and controller. It handles tasks like taking pictures, identifying objects, making decisions, and activating parts of the system. A camera attached to the robot takes live images of the road. These images are processed and then sent to YOLOv5, an object detection algorithm written in Python using OpenCV. YOLO looks at each image, finds potholes, and creates boxes around them with confidence levels. This helps detect potholes accurately even in different road conditions and environments. Once a pothole is found, the Raspberry Pi starts the repair process. The robot moves to the spot and positions itself over the damaged area. A built-in system releases the correct amount of material, such as asphalt or gravel, to fill the hole. A leveling mechanism then smooths the surface to bring it back to its original condition. This combination of detection and repair makes the system unique, as it does more than just find potholes—it also fixes them. To make the system more user-friendly, it offers two control options. In automatic mode, the robot operates on its own, detecting and filling potholes without needing any human assistance. In manual mode, an operator can control the robot using an Android app. The app lets the user move the robot in different directions and activate the filling system. This is especially useful when human supervision is needed or during busy traffic times. The system also has a cloud-based reporting feature. Once a pothole is detected, its details are stored and sent to the appropriate authorities through an IoT notification system. Small potholes are repaired automatically by the robot, while larger or more severe ones are marked for inspection and handled by municipal teams. This setup balances automated and human efforts effectively. Overall, the system uses computer vision to detect potholes, robotic systems to repair them, and cloud communication to report findings. This makes it a full and intelligent solution for managing potholes. The modular structure lets the system be scaled and used in both urban and rural areas.

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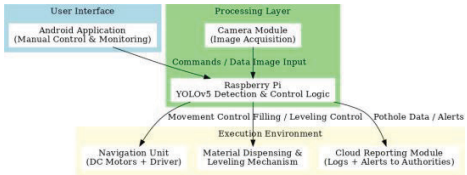


Fig. 1. Project Execution Process.

IV. System Design

The Smart Pothole Detection and Clearance System is made to work well with computer vision, deep learning, robotic movement, and user involvement. Its main aim is to not only find potholes accurately but also fix them in a good way. The system is built with different parts, each with its own job, all working together to keep roads free of potholes. At the heart of the system is the image capture module, which uses a camera on the robot to film the road continuously. Unlike older methods that use sensors, this system only uses visual data. After the images are taken, they are sent to the processing module, where the YOLOv5 algorithm is used. This algorithm breaks each image into parts, predicts where potholes could be, and finds them in real-time along with a confidence score. This helps the system tell potholes apart from things like shadows or road patterns. The decision-making module, which is on the Raspberry Pi, looks at the results from YOLO and decides what to do next. If a pothole is found, the robot moves to the exact spot using motor control. Then, the material dispensing module is turned on, releasing material like gravel or asphalt mix. A leveling device is used to spread and smooth the material, which helps stop the pothole from coming back. In addition to working automatically, the system has a user interaction module through an Android app. This app connects to the robot wirelessly, allowing users to take control when needed. Users can move the robot in basic directions and turn on the filling or leveling functions. This manual control is especially helpful in tricky situations where full automation might not work well. A key part of the design is the cloud-based reporting module. Along with fixing potholes, the system records their locations and the level of damage. If a pothole is too big for the robot to fix, the system sends a message to the right authorities through the cloud. This link between the automatic system and local authorities ensures better long-term road management. The system is made with efficiency, modularity, and the ability to grow in mind. The modular setup means parts like detection methods, robotics, or communication can be updated separately without affecting the rest. Using vision-based detection also makes the system more adaptable to different road conditions compared to sensor-based systems. In short, the system uses computer vision to find potholes, robotics to fix them, cloud-based communication to report issues, and user apps for manual control, creating a full and smart solution for keeping roads in good shape.

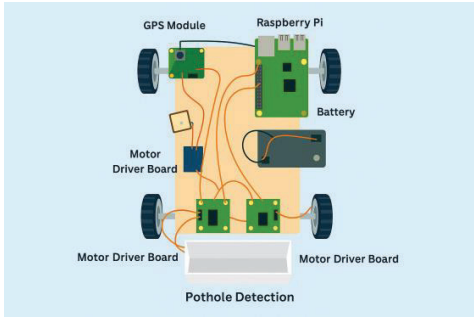


Fig. 2. Vehicle Design for The Detection and Clearance System.

V. Performance Evaluation

The Smart Pothole Detection and Clearance System is assessed based on how well it can find potholes using computer vision, handle repair tasks quickly, and provide a reliable interface for both automatic and manual control. Since the system doesn't use physical sensors, the main focus of the evaluation is on how well the camera-based YOLOv5 detection algorithm works, how fast the Raspberry Pi can process data, and how effective the mechanical parts are in carrying out repairs. One important measure in the evaluation is detection accuracy. YOLOv5 is a real-time algorithm that performs well in identifying potholes under different lighting conditions, road textures, and surface types. During testing, it successfully detected potholes of various sizes, shapes, and depths. A major advantage of YOLOv5 is its ability to learn from a wide range of training data, allowing the system to recognize both dry and water-filled potholes. Unlike older methods, using image-based deep learning minimizes false alarms caused by shadows or cracks that don't need fixing. Another key performance factor is processing speed. Although the Raspberry Pi isn't as powerful as high-end GPUs, it was able to run YOLOv5 at a speed that supports real-time detection. On average, the system achieved a detection speed that let the robot spot and respond to potholes while moving without delays. This shows the system is ready for use on real roads, where constant monitoring and fast responses are needed. In terms of repair efficiency, the material dispensing and leveling system worked well in fixing road surfaces. Once a pothole was detected, the system automatically positioned itself and released the right amount of filling material. The leveling unit made sure the repaired area was smooth, which reduces future damage. The time taken to fill a pothole was much less than with manual methods, and because the system is automated, it requires very little human help. The ability to control the system through an Android app also improved its performance. In situations where full autonomy wasn't possible, like in heavy traffic or complex road setups, users could easily switch to manual control. This dual functionality made the system more dependable and adaptable to different environments. Another useful feature is the cloud reporting module, which records data and sends alerts for potholes that are too big for auto-

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mated repair. This helps civic authorities by supporting more organized and effective road maintenance efforts. Overall, the evaluation shows the system achieves high detection accuracy, efficient repair operations, and strong adaptability without relying on physical sensors. By combining YOLOv5-based vision, robotic components, and cloud connectivity, the system offers a scalable and sustainable way to keep roads free from potholes.

VI. Integration of Artificial Intelligence(AI)

Artificial Intelligence (AI) is the main part of the Smart Pothole Detection and Clearance System, making it work well without using physical sensors. Instead, the system uses a camera to take pictures of the road and uses a YOLOv5 deep learning model to find potholes in real time. This AI approach makes the road maintenance both accurate and efficient. The camera takes pictures continuously and sends them to a Raspberry Pi, which runs the AI model. YOLOv5 divides each image into a grid and checks for objects by looking at visual elements. It creates boxes around each detected pothole and gives a confidence level, helping to identify potholes of different sizes, shapes, and even in different lighting. This method also helps avoid false alarms from shadows, cracks, or other irregularities on the road. By using AI-based computer vision, the system doesn't need extra sensors, making it simpler, more cost-effective, and easier to adapt. AI also helps the system to act on its own. When YOLOv5 detects a pothole, the Raspberry Pi uses the information to decide what to do next. For instance, the robot moves into place, turns on the filling system, and uses a leveling tool to fix the surface. These actions happen all by themselves, guided by the AI model. In addition, AI improves the system's two ways of operating. In fully automatic mode, the AI handles both detection and repair. In manual mode, an Android app lets the user control the robot's movement and the filling process. Even during manual operation, AI helps by marking potholes on the live video feed, giving the operator useful information for decision-making. One big advantage of using AI is that the system can grow and get better over time. The YOLOv5 model can be trained with more data to improve its performance in different conditions like urban, rural, wet, or dry roads. In the future, the system could also use other AI models to classify how bad potholes are or predict which areas might get damaged, turning it into a tool for predictive maintenance. In short, using AI through YOLOv5-based image detection makes this system smart, flexible, and cost-effective. By replacing sensors with AI-driven vision, the project makes real-time pothole detection, automated repair work, and long-term adaptability for smart road systems possible.

VII. Conclusion and Future Work

The Smart Pothole Detection and Clearance System shows how artificial intelligence, computer vision, and robotics can work together on one platform to address a common issue in road infrastructure—potholes. The system uses a camera with a YOLOv5 model to detect potholes in different shapes and sizes in real time. The Raspberry Pi acts as the main computer, letting the system think and communicate with other parts. When a pothole is found, the robot moves to the right spot, fills the hole, and levels the road, quickly getting it back in good condition. An Android app lets users control the robot manually, making it useful in tough situations. A cloud-based system also helps report serious potholes that the robot can't fix directly to the proper authorities. This project shows that using computer vision and robot systems can reduce the time and work needed for pothole fixes. It makes roads safer and offers a cheaper, flexible solution that can work with different road types. Looking forward, there are ways to improve the system. One idea is to add sensors to help the camera work better. For example, vibration sensors on the robot or the vehicle can pick up sudden movements when going over potholes. These readings can be combined with the camera data to make detection more accurate and less likely to be fooled by shadows or uneven ground. Another sensor, like an accelerometer, can measure how fast the vehicle hits a pothole. This helps understand how much damage the pothole might cause to cars and people. Combining vibration data with AI image analysis could create a more reliable and strong detection system. Another improvement could be using predictive analytics. By keeping data from cameras and sensors, the system can predict when roads might start to break down. This lets officials fix problems before potholes get too bad. Expanding the cloud reporting system to use GIS-based maps would also make it a better tool for smart city infrastructure. In short, the project presents a new way to automate road maintenance using AI and robotics. Adding vibration and speed sensors, predictive maintenance, and large-scale use can change how roads are kept in good shape, leading to safer, faster, and more reliable transportation.

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