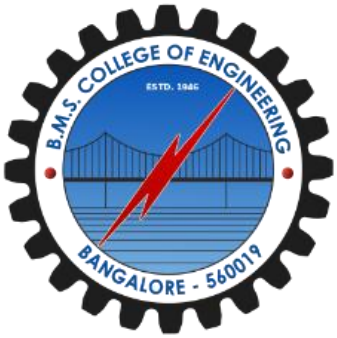
BMS COLLEGE OF ENGINEERING, BENGALURU-19
Autonomous Institute, Affiliated to VTU
Department of Electronics and Communication Engineering



Scheme and Syllabus
M. Tech (VLSI Design & Embedded system)
Batch 2016 onwards

Web: www.bmsce.ac.in

Vision of BMS College of Engineering

Promoting Prosperity of mankind by augmenting human resource capital through Quality Technical Education & Training

Mission of BMS College of Engineering

Accomplish excellence in the field of Technical Education through Education, Research and Service needs of society

Vision of Electronics and Communication Department

To emerge as a Centre of Academic Excellence in Electronics, Communication and related domains through Knowledge acquisition and Knowledge dissemination meeting the global needs and standards.

Mission of Electronics and Communication Department

***Imparting quality education through state of the art curriculum, conducive learning environment and Research with scope for continuous* improvement *leading to overall Professional Success*.**

PROGRAM EDUCATIONAL OBJECTIVES

PEO1:

Graduates shall be capable of building their career in related industries, R&D establishments as well as in Teaching with their scholarly knowledge with respect to advanced topics in VLSI Design & Embedded system

PEO-2:

Graduates shall be capable of conceptualizing and analysing engineering problems of societal importance related to Design, implement, verification of Integrated circuit and embedded system, conduct independent research leading to technology solutions and communicate the outcomes through verbal and written mechanisms.

PEO-3:

Graduates shall be able to collaborate, manage and execute projects in teams using appropriate tools/technologies with utmost professionalism and acceptable good practices.

PROGRAM OUTCOMES

Program Outcomes (POs), are attributes acquired by the student at the time of graduation. The POs are aligned to the Graduate Attributes (GAs) specified by National Board of Accreditation (NBA). These attributes are measured at the time of Graduation, and hence computed every year for the outgoing Batch. The POs are addressed and attained through the Course Outcomes (COs) of various courses of the curriculum.

PO1: Acquire scholarly knowledge beginning with fundamentals up to the global perspective.

PO2: Think critically, and shall be able to plan and conduct research oriented experiments along with collection and analysis of results.

PO3: Conceptualize and solve contemporary engineering problems and propose optimal solutions in core and related areas.

PO4: Acquire necessary research skills and contribute individually/in group(s) to the development of technology in his/her core area of expertise.

PO5: To select, learn and apply appropriate techniques, resources, and modern engineering and IT tools in his/her core area and allied areas.

PO6: Collaborate and develop a capacity for self-management and team work.

PO7: Manage and execute projects efficiently at engineering, financial and personnel levels.

PO8: Demonstrate effective verbal and written communication skills, in the form of technical documentation, presentations, standards compliance etc.

PO9: Recognize the need for, and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

PO10: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO11. Observe and examine critically the outcomes of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback.

Total

Category	No of Credits
Program Core Course	**30**
Program Elective Course	**14**
All programme core Course	**02**
Institution Elective Course	**04**
Internship	**21**
Technical seminar	**02**
Project Work	**27**

Number of Credits (I Sem – IV Sem) = 100 Credits

Distribution of credits

Distribution of self-study components:

Category	No of Credits
Department Core Course	3

Note: Self-Study components is provided for the Program Core Course

M.Tech. (VLSI Design and Embedded system)

I Semester **CREDIT BASED**

Subject Code	Course Title	Credits				CREDITS
		L	T	P	S	
16ECVEPCAM	Advanced Mathematics	3	0	0	0	3
16ECVEGCDV / 16ECELGEDV	Digital VLSI design	3	1	0	0	4
16ECVEGCES / 16ECELGCES	Advanced Embedded system	3	0	1	1	5
16ECVEPCAI	Analog IC design	3	0	1	1	5
16ECVEPEZZ	Elective -1	3	0	0	0	3
16ECVEPEZZ	Elective -2	3	0	0	0	3
16APRDICRM	Research Methodology	2	0	0	0	2
Total		20	1	2	2	25

Note : Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

Course Elective			
16ECVEPELD	Advanced Digital Logic Design	16ECVEPELP	Low Power VLSI
16ECVEPEEC	Embedded C	16ECVEPEEC	Embedded Computing and Networking
16ECVEPEST	Static Timing Analysis	16ECVEPEAV	Advances in VLSI Structure
16ECVEPEMP	Device Modeling and Processing Technology	16ECVEPESP	VLSI Signal processing

Note: (i) The Course Code Expansion: Exa: 16ECVEPCAM: 16 = Year, EC = Dept., VE = Program, PC = Program Core, AM = Advanced Mathematics.

ZZ(course abbreviation),GC/GE: Group Core / Group Elective

(ii) Exception for 16APRDICRM: AP = All Program, RD = Research & Development, I = Institution C = Core, RM = Research Methodology.

M.Tech. (VLSI Design and Embedded system)

II Semester **CREDIT BASED**

Subject Code	Course Title	Credits				CREDITS
		L	T	P	S	
16ECVEPCMS	Mixed Signal Circuit Design	3	0	1	0	4
16ECVEPCDT	Design for Testability	3	1	0	0	4
16ECVEGCRO /16ECELGCRO	Real Time operating system	3	0	1	1	5
16ECVEPEZZ	Elective -3	3	1	0	0	4
16ECVEPEZZ	Elective -4	3	1	0	0	4
16ECVEICZZ	Institution Elective	4	0	0	0	4
	Total	19	3	2	1	25

Note: Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

Course Elective			
16ECVEPESV	System Verilog and verification	16ECVEPEHS	Hardware/Software Co-design
16ECVEPEPD	Physical Design	16ECVEPEAM	Embedded Design using ARM Architecture
16ECVEPESC	System On Chip Architecture	16ECVEPECA	Advanced Computer Architecture
16ECVEPEMD	Memory Design and Testing		

Institution Elective		**L T P S**
16ECVEIEMN	Advanced Micro and Nano devices	4 0 0 0
16ECVEIERB	Robotics	3 0 1 0

M.Tech. (VLSI Design and Embedded system)

III Semester **CREDIT BASED**

Subject Code	Course Title	Credits				CREDITS
		L	T	P	S	
16ECVEPCIN	Internship					21
16ECVEPCIP	Project work (I-phase)					4
	Total					**25**

M.Tech. (VLSI Design and Embedded system)

IV Semester **CREDIT BASED**

Subject Code	Course Title	Credits				CREDITS
		L	T	P	S	
16 ECVEPCPR	Project work (final phases)					23
16 ECVEPCTS	Technical Seminar					02
	Total					**25**

Advanced Mathematics

COURSE CODE	16ECVEPCAM	COURSE TITLE	Advanced Mathematics
CREIDTS	3	L-T-P-S	3-0-0-0

CO	Course Outcomes	PO
CO-1	**Demonstrate** an understanding to multiple random variables, vector spaces, linear transformations and inner product spaces and **Apply** probability techniques to determine the mutual information in a communication channel and Apply various algorithms in graph theory to solve networking and communication problems.	**PO1,PO3**
CO-2	**Analyse** the random process for SSS, WSS, and ergodic in the mean or ergodic in the autocorrelation.	**PO2,**
CO-3	**Construct** the Singular value decomposition of a matrix A.	**PO3**
CO-4	**Conduct** numerical experiments with matlab in Gram-Schmidt orthogonalisation process, advanced matrix theory and graph theory and Make an **effective oral presentation** of the applications of random variables, random processes, vector spaces and network flow algorithms	**PO5,6,8**

Pre-requisites: Basic concepts of Probability, Bayes' theorem. Vector algebra, matrix operations.

Random Variables: Discrete and continuous type Random Variables, Sequence of random variables, limit theorem, random correlation function, spectral densities, linear systems with random inputs, Distribution and Density Functions: PMF, CDF, PDF, Gaussian random variable, and other standard random variables, Expectation operator, Multiple random variables: Joint PMF, CDF, PDF, Expectation involving multiple Random variables.

Random Processes: Definition and characterization, Stationary and Ergodic Random processes, Autocorrelation function and its properties, Example Processes: introduction to Markov process, Gaussian Process, Poisson Process.

Vector Spaces and subspaces: Vector spaces, basis and dimension, linear transformations, inner product spaces orthonormal bases and Gram-Schmidt orthogonalisation process.

Advanced Matrix Theory: Introduction to eigenvalues and eigenvectors, Positive definite matrices, Singular value decomposition, Principal component analysis by SVD, geometry of SVD - Least square approximations.

Computational Graph Theory: Graph enumerations and optimization: DFS-BFS algorithm, shortest path algorithm, min-spanning tree and max-spanning tree algorithm, basics of minimum cost spanning trees, optimal routing trees, optimal communication trees. planarity algorithm, Fundamental algorithmic techniques for solving graph problems- Traversal and search techniques, Greedy approach, Backtracking, Branch and bound techniques and their applications to various graph problems, Network flow algorithms, Classification of graph problems P, NP-hard and NP-complete.

Text Books:

1. S L Miller and D C Childers**, "Probability and random processes: application to signal processing and communication**", Academic Press / Elsevier 2004.

2. David C. Lay, "**Linear Algebra and its Applications**", 3rd Edition, Pearson Education, 2003.

3. Geir Agnarsson and Raymond Greenlaw" **Graph Theory- Modeling, Applications and Algortihms",** Pearson Education, 2007.

Reference books:

1 A. Papoulis and S U Pillai, **"Probability, Random variables and stochastic processes",** McGraw Hill 2002

2 Roy D. Yates and David J. Goodman, **Probability and Stochastic Processes: A friendly introduction for Electrical & Computer Engineers**/

3. MIT Open courseware**, Introduction to Linear Algebra, Course 18.06**

4Nausing Deo, "**Graph Theory with applications to Engineering and Computer Science**", Prentice Hall of India, 1999.

Digital VLSI Design

COURSE CODE	16ECVEPCDV/ 16ECELGEDV	COURSE TITLE	Digital VLSI Design
CREIDTS	4	L-T-P-S	3-1-0-0

CO1	**Apply** the concepts of MOS system in digital VLSI design	**PO2**
CO2	**Analyse** the electrical and physical properties, Switching characteristics and interconnect effect of a MOS system in digital VLSI design	**PO2**
CO3	**Design** dynamic logic circuits, Semiconductors Memory circuits, and different CMOS logic circuits.	**PO3**
CO4	Use **modern tools** to simulate Schematic and Layout of Digital circuits individually/ in group (s) and Make an **effective oral presentation** and documentation on advanced topics related to the course by referring IEEE Journals.	**PO5 PO6, PO8**

MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **Layout and stick diagrams**

MOS Inverters: Static Characteristics: Resistive load inverters, CMOS Inverter.

Switching Characteristics and Interconnect Effects: Delay-Time Definition, Calculation, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitic, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM).

Reference Books

1. Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.

2. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.

Advanced Embedded Systems

COURSE CODE	**16ECVEGCES / 16ECELGCES**	**COURSE TITLE**	**Advanced Embedded Systems**	
CREIDTS	**5**	**L-T-P-S**	**3-0-1-1**	
CO-No	**Course Outcomes**			**PO**
CO-1	Understand and explain the concepts of Embedded Systems and **Apply** the knowledge of Computer Architecture in **building** Embedded Systems.			**PO1,2**
CO-2	**Analyze** the real-time deterministic response of embedded systems and various peripherals involved in **Embedded** system.			**PO2**
CO-3	**Design** low power, real time deterministic Embedded Systems and **Develop C programs, execute & demonstrate** on embedded target boards like Beagle Bone Black, Raspberry Pi, Arduino, etc.			**PO5,2,3**
CO-4	**Perform in a team** to design and develop useful embedded systems and Make an **effective oral presentation** on topics allocated by instructor pertaining to Computer Architecture, Embedded Systems, Analog and Digital peripherals.			**PO6,7,8,9**

Introduction to Embedded Systems, Real time nature of ES, Architectures of ES including multi core architecture, Graphic Processing Units (GPU), Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components. **Case Study Raspberry Pi 3**.

Characteristics and Quality Attributes of Embedded Systems: Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software Trade-offs. Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages(C, C++, Python, VHDL/Verilog).

Introduction to SoC, Case Study Xilinx Zynq, Anatomy, Design Reuse, Abstraction, SoC Design Flow, Zynq APU, ARM Model, Logic Fabric, Block RAM, GPIO, Communication Interfaces, Zynq Soc Design Overview.

Device Comparison, Device Selection Criteria, Zynq vs FPGA, Zynq vs Standard Processor, Zynq vs Dicrete FPGA Processor, Zynq Architecture and Design Flow, Embedded Systems and FPGA, Processors and Buses.

USB Basics, Uses and limits, Benefits, Evolution, Bus components, Division of labor, Transfer basics, Elements of a transfer, USB 2.0 transactions, Ensuring successful transfers, Control transfers, Bulk transfers, Interrupt transfers, Isochronous transfers, Enumeration: Process and Descriptors.

Hosts for Embedded Systems, Targeted Host, Targeted Peripheral List, Targeted Host types, Bus current, Turning off bus power, Embedded Hosts, Differences from conventional host ports, Functioning as a USB device, OTG devices, A-Device and B-Device, OTG descriptor, Host Negotiation Protocol, Role Swap Protocol.

Lab Experiments:

1. Raspberry Pi 3: Booting the Board with multiple OS, Programming of GPIO, Programming of Serial Peripherals, Control of ADC.
2. Zynq Board: Implement Timers and GPIO modules in FPGA and control it with ARM SOC.
3. Implement a USB generic serial emulator device on FPGA, interface it with Raspberry Pi 3.

Reference Books:

1. Hennessy and Patterson, Computer Architecture: A Quantitative Approach", Latest Edition

2. Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2009

3. The Zynq Book, by Crockett, Elliot, Enderwitz & Stewart, University of Strathclyde Glasgow, 2014

4. USB Complete: The Developer's Guide, Jan Axelson

Analog IC design

COURSE CODE	16ECVEPCAI	COURSE TITLE	Analog IC design
CREIDTS	5	L-T-P-S	3-0-1-1

CO	**Course Outcomes** of Analog IC design	PO
CO-1	**Understand and explain** Basic physics and operation of MOS devices and **apply** the knowledge of Network theory, Electronic circuit design, VLSI design to **obtain Analog design actagon.**	PO1,3
CO-2	**Analyse** the Analog circuits by developing efficient analytical tools for quantifying the circuits by inspection.	PO2
CO-3	**Design** stable Analog Integrated Circuits to meet given specification	PO2,3
CO-4	**Conduct Research based experiments to demonstrate** optimized Analog Integrated Circuit design by suitable literature survey and suitable EDA Tool (Cadence, Synopsis, Mentor graphics)	PO2,4
CO-5	Involve in independent/team learning, Communicate effectively and engage in life-long learning	PO6,8,9

Basics of MOSFET, MOS I/V Characteristics, second order effects, MOS device models.

Single stage Amplifier: CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source Degeneration, source follower, common-gate stage, cascade stage, choice of device models.

Differential Amplifiers & Current Mirrors: Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell.

Basic current mirrors, Cascade mirrors, active current mirrors.

Operational Amplifiers: One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, Power Supply Rejection, Noise in Op Amps.

Band Gap Reference Design: General considerations, Supply independent biasing, temperature independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, constant gm biasing

Lab Experiments:

1. Design the analog circuits using MOS transistors,

a. Draw the schematic and verify the following
(i) DC Analysis
(ii) AC Analysis
(iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS.

2. Design, an op-amp with given specification using given differential amplifier in library and complete the design flow mentioned below:

a. Draw the schematic and verify the following
(i) DC Analysis
(ii) AC Analysis
(iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC

Reference Book:

1. "**Design of Analog CMOS Integrated Circuits**", Behzad Razavi, TMH, 2007.

2. Paul. R.Gray, Robert G. Meyer**, "Analysis and Design of Analog Integrated Circuits", Wiley, (4/e), 2001**

I Semester electives

Advanced Digital logic Design

COURSE CODE	16ECVEPELD	COURSE TITLE	Advanced Digital Logic Design
CREIDTS	3	L-T-P-S	3-0-0-0

CO	Course Outcomes	PO
CO-1	**Apply** the concepts of Digital design to create digital building blocks using Verilog.	PO3
CO-2	**Analyse** the RTL timing to report violations and synthesize to generate gate level net list.	PO2
CO-3	**Able to write** RTL using knowledge of finite state machines along with design optimization.	PO1
CO-4	**Simulate and debug** the design using test benches and analyse the synthesis timing and power reports using modern tools.	PO2,3,5

Logic Design Using Verilog: Moore's law, Technology Scaling, Die size growth, Frequency, Power dissipation, Power density, Challenges in digital design, Design metrics, and Cost of Integrated circuits, Digital Combinational & Sequential circuits, Lexical Conventions, Data Types, Levels of Abstraction, Modules, Nets, Values, Comments, arrays in Verilog, Expressions, Operators, Operands, Arrays, memories, Strings, Delays, parameterized designs, Procedural blocks, Blocking and Non-Blocking Assignment, looping, flow Control, Task, Function, basic test bench generation and Simulation, Verilog modeling of combinational and sequential logic.

Principles of RTL Design, Timing concepts: Verilog Coding Concepts, Verilog coding guide lines: Combinational, Sequential, FSM. General Guidelines, Synthesizable Verilog Constructs, Sensitivity List, Verilog Events, RTL Design Challenges, Introduction to timing concepts. Setup and hold times. Setup and hold time equalities and inequalities, timing paths. Static timing delay calculation for basic flip flop & sequential circuits, Clock Domain Crossing.

Synthesis, Libraries and Technology Mapping: Introduction to synthesis, logical synthesis of basic combinational and sequential circuits, Synthesis Methodologies, Pre and post synthesis mismatch, Translation, mapping and optimization. Overview of Libraries, design constraints, importance of wire load models.

Design and simulation of Architectural building blocks: Basic Building blocks design using Verilog HDL: Arithmetic Components – Adder, Subtractor, and Multiplier design, Data Integrity – Parity Generation circuits, Control logic – Arbitration schemes, FSM Design – overlapping and non-overlapping Mealy and Moore state machine design.

Verification Concepts: Concepts of verification, importance of verification, Types of verification (black ,white and gray box verification), Stimulus vs Verification, functional

verification, functional verification approaches, typical verification flow, directed and random verification, **Coverage**: Code and Functional coverage, Coverage driven verification.

Reference Books:

1. Digital Design by Morris Mano M, 4th Edition
2. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition
3. *Verilog* HDL Synthesis A Practical Primer by J. Bhasker
4. Fundamentals of Digital Circuits by A. Anand Kumar, 2nd Edition
5. Principles of VLSI RTL Design: A Practical Guide by Sanjay Churiwala , Sapan Garg, 2011

Embedded C

COURSE CODE	16ECVEPEEC	COURSE TITLE	Embedded C
CREIDTS	3	L-T-P-S	3-0-0-0

CO1	**Understand** the syntax and semantic of the C language for embedded programming and various Inter Process Communication mechanism.	**PO1**
CO2	**Apply** C Features to develop Embedded C.	**PO2**
CO3	**Analyse** various usage of pointer, user defined types in C programming.	**PO2**
CO4	**Develop** multitasking and multithreading programming.	**PO3**

Quick Overview of C: C Features, Application of C, Build Process, Scope of a variable, Storage Class, operators, Condition statement, Memory layout of C program

User Define Data type: Arrays, Structures, Union, enum.

Purpose of Pointers: Need for pointers, Pointer to built in type, Pointer to user defined type, Command line arguments, Dynamic memory allocation, Function pointer, call back functions, pointer to pointer, Memory mapping.

Functions and C Pre-processor Directives: using built in function/library, user defined functions, Developing Static Library and Dynamic Library.

File I/O: Formatted I/O, system I/O, treatment of devices as files in Posix, File I/O in Windows, fopen, fwrite, fread, fclose, fprintf, fscanf, open, read, write, close,& ioctl calls

Multitasking using Process and Thread: Process creation, Process termination, Thread creation and termination,

Inter Process Communication: Signals, Pipe, FIFO, Message Queue, Shared Memory, Semaphores

References:

1. The C Programming: Brian W Kernighan, Dennis M Ritchie
2. Understand Pointer in C: Yeshavanth Kanetkar
3. Linux System Programming: Robert Love

Device Modeling and Processing Technology

COURSE CODE	**16ECVEPEMP**	**COURSE TITLE**	**Device Modeling and Processing Technology**
CREIDTS	**3**	**L-T-P-S**	**3-0-0-0**
CO	Course Outcomes		
CO-1	**Understand** fundamentals of semiconductors, theoretical and practical aspects of electronics technology – Very Large Scale Integration. All the unit process steps involved in planar process starting from silicon crystal growth to CMOS Process.		
CO-2	**Analyse** SPICE Models of Diodes, BJT, MOSFETs, MESFETs & HBTs.		
CO-3	Ability to submit a report on the SPICE models fabrication process		

Fundamentals: Semiconductor Physics, Principle of circuit simulation and its objectives.

Introduction to SPICE: AC, DC, Transient, Noise, Temperature extra analysis.

Junction Diodes: DC, Small signal, large signal, High frequency and noise models of diodes, Measurement of diode model-parameters.

Modelling of BJT: DC, small signal, high frequency and noise models of bipolar junction transistors. Extraction of BJT model parameters.

MOSFETs: DC, small signal, high frequency and noise models of MOSFETs, MOS Capacitors. MOS

Models: Level-1 and level-2 large signal MOSFET models. Introduction to BSIM models. Extraction of MOSFET model parameters.

JFET, MESFETs & HBTs: Modelling of JFET & MESFET and extraction of parameters. Principles of hetro-junction devices, HBTs, HEMT.

CMOS Processing Technology: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

Text Books

1. S.M.Kang & Y.Leblibici, CMOS Digital Integrated Circuits-Analysis & Design, TMH, 3rd Ed.

2. S.M. Sze, Physics of Semiconductor Devices, Wiley Pub.

3. Neil H E Weste, David Harris, Ayan Banerjee, CMOS VLSI Design 3rd edition, Pearson Education.

References

1. Sedra and Smith, SPICE.

2. H.M. Rashid, Introduction to PSPICE, PHI.

3. B.G. Streetman & S. Baneerjee, Solid State Electronic Devices, PHI.

4. R. Raghuram, Computer Simulation of Electronic Circuits, Wiley Eastern Ltd.

Static Timing Analysis

COURSE CODE	**16ECVEPEST**	**COURSE TITLE**	**Static Timing Analysis**
CREIDTS	**3**	**L-T-P-S**	**3-0-0-0**

CO	Description	**PO**
CO1	Apply the learnt basic concepts of STA to evaluate the delay of the circuits.	**PO3**
CO2	Analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing.	**PO2**
CO3	Able to generate their own constraint file and create the environment required for the given design and its specification to undergo for analysis in the tool.	**PO2,PO3**
CO4	Understand the journal research papers related to Timing analysis techniques and able to present the knowledge of new techniques for the given design.	**PO5, PO8**

Static Timing Analysis Concepts: Propagation delay, slew, timing arcs, min and max timing paths, clock domains.
Standard Cell Library: Pin capacitance, timing models: linear v/s. non-linear delay model, combinational v/s. sequential cells, state-dependent models, models for crosstalk and noise, characterization.
Interconnect Parasitic: RLC modelling, wire load models, representation of coupling capacitances, reducing parasitic for critical nets.
Delay Calculation: Basics, delay calculation with interconnect, calculation at pre- and post-layout stages, calculation using effective capacitance, interconnect delay, slew merging, path delay calculation, slack calculation
Crosstalk and Noise: Crosstalk glitch analysis, crosstalk delay analysis, setup and hold analysis.

The STA Environment: timing path groups, modelling of external attributes, virtual clocks, refining the timing analysis, point-to-point specification.
Timing Verification: Setup and Hold timing checks, recovery and removal checks, multi-cycle paths, false paths, timing across clock domains.
Robust Verification: on-chip variations, time borrowing, clock gating checks, sign-off methodology, Best case (BCS) Typical(Typ) and Worstcase(WCS) corners. statistical static timing analysis

References:

1. "Static Timing Analysis for Nanometer Designs: A Practical Approach", J. Bhasker, R. Chadha, Springer, 2009.
2. "Handbook of Algorithms for Physical Design Automation", CRC Press, 2009. Chapters 42 and 43. (provides a case study)
3. Research papers

Low Power VLSI

COURSE CODE	**16ECVEPELP/ 16ECELPELP**	**COURSE TITLE**	**Low Power VLSI**
CREIDTS	**3**	**L-T-P-S**	**3-0-0-0**

CO	**Course Outcomes**	**PO**
CO-1	Extend the knowledge on basics of MOSFETs and Power Dissipation in MOS circuits to obtain the concepts of different techniques for power optimization.	**PO1**
CO-2	Ability to apply the low power concepts to find the static and dynamic power consumption in a design	**PO2**
CO-3	Ability to design the power optimised circuit for the given specification.	**PO2,PO3**
CO-4	Usage of EDA tool to implement the designed circuit with techniques of power optimisation in the design and justify obtained report by class room presentation.	**PO5,PO8**
CO-5	Understand the journal research papers related to low power and update the knowledge for new techniques to incorporate in projects of the specified stream.	**PO9**

Basics of MOS circuits, Sources of Power dissipation, Dynamic Power Dissipation -Short Circuit Power, Switching Power, Glitching Power, Static Power Dissipation, Degrees of Freedom.

Supply Voltage Scaling Approaches: Device feature size scaling Multi-Vdd Circuits Architectural level approaches: Parallelism, Pipelining Voltage scaling using high-level transformations Dynamic voltage scaling Power Management

Switched Capacitance Minimization Approaches: Hardware Software Tradeoff Bus Encoding Two's complements Vs Sign Magnitude Architectural optimization Clock Gating Logic styles

Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-V_t assignment approach (DTCMOS)

Special Topics: Adiabatic Switching Circuits Battery-aware Synthesis Variation tolerant design CAD tools for low power synthesis

Text

1. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata Mcgrag Hill.

2. Neil H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Addison Wesley (Indian reprint).

3. A. Bellamour, and M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic Press, 1995.

4. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.

Reference

1. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Inter science, 2000.
2. NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering ,IIT Kharagpur

Embedded Computing and networking

COURSE CODE	16ECVEPEEC	COURSE TITLE	Embedded Computing and networking
CREIDTS	3	L-T-P-S	3-0-0-0

CO1	**Understand** different types of Embedded Applications.
CO2	**Analyse** various development tools, WAN, LAN and PAN protocols
CO3	**Customize** Linux for different environment
CO4	Port OS to embedded board and to build Arm tool Chain

Types of embedded application: Super loop, Interrupt driven, priority, round robin, OS based.

Embedded Android: Android Mobile and Tablet**,** Android TV, Android Wearable, Android Auto, Glass.

WAN : MPLS, HHTP, MQTT, Coap etc

LAN: TCP / IP, UDP, Socket Programming

PAN: Bluetooth, BLE, zigbee

Introduction to Software Development Tools: GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

Interfacing Modules: Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

Building an Embedded System: Creating the Root File system, Building the Linux Kernel, Building the Root File system, Running UML, Networking.

Embedded ARM Devices: Building ARM tool chain, Installing an Operating System on ARM board, Using ARM board Serial Port, Remote Serial Port.

Text books:

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Embedded Operating System - Alan Holt, Chi-Yu Huang, Springer
5. Intel® 64 and IA-32 Architectures Software Developer Manuals

Reference books:

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

Advances in VLSI Structure

COURSE CODE	**16ECVEPEAV**	**COURSE TITLE**	**Advances in VLSI Structure**
CREIDTS	**3**	**L-T-P-S**	**3-0-0-0**

CO	Description
CO1	Ability to understand multiple-gate MOSFET's. Strained-Si technology, thin body MOSFET's and Emerging nano materials
CO2	Apply the short channel effect to define new structures and requirement of new materials
CO3	Analyse thin body MOSFET structure and its impact, Impacts of substrate; nano materials
CO4	Use modern tool to simulate different structure and observe the performance comparison

Transistor and multiple-gate MOSFET's development, history, review of MOSFET principles and performance metrics

Issues in short-channel MOSFET electrostatics; scale length fundamentals for thin-body MOSFETs (FinFET, planar Fully-Depleted SOI MOSFET and Gate-All-Around MOSFET)

Advantages of thin body MOSFET's electrostatics quantum mechanical effects; effective carrier mobility; high-field velocities. Parasite resistance; thin-body MOSFET's carrier transport MOSFET compact modelling and Technology CAD (TCAD)

Impacts of substrate; Fin shape tuning; Gate stack process, FinFET's source/drain process, Multiple-gate MOSFET's threshold voltage engineering. Multiple-gate MOSFET performance dependence on channel orientation and strain

Strained-Si technology and its effectiveness on Multiple-gate MOSFETs high-mobility channel transistors (Group III-V)

Emerging nano materials: Nanotubes, nanorods and other nano structures, MOSFET like structure of carbon nano tubes.

Reference:

1. Research papers

2. **MOOC**: http://www.flexilearn.ie/course/Nanoelectronics/43

VLSI Signal Processing

COURSE CODE	**16ECVEPESP**	**COURSE TITLE**	**VLSI Signal Processing**
CREIDTS	**3**	**L-T-P-S**	**3-0-0-0**

CO	Description
CO1	Understand Pipelining architecture and parallel processing of FIR filters , Fast convolution algorithms for IIR filters
CO2	Analyse Retiming folding and unfolding algorithms and implement into the different FIR filters, Fast convolution algorithms for IIR filters.
CO3	Implementing algorithms into different architectures and synchronous, asynchronous systems

Introduction to DSP systems, pipelining and parallel processing of FIR filters: Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

Retiming, algorithmic strength reduction: Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

Fast convolution, pipelining and parallel processing of IIR filters: Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

Bit-level arithmetic architectures: Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

Numerical strength reduction, synchronous, wave and asynchronous pipelining: Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered

single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

References:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.

2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

RESEARCH METHODOLOGY

COMPULSORY TO ALL BRANCHES

COURSE CODE	16APRDICRM	COURSE TITLE	RESEARCH METHODOLOGY
CREIDTS	2	L-T-P-S	2-0-0-0

Module 1:
Meaning, Objectives and Characteristics of research, Research methods vs Methodology. Types of research, Descriptive vs Analytical, Applied V/s. Fundamental, Quantitative vs. Qualitative, Conceptual vs. Empirical, Research process, Criteria of good research, Developing a research plan.

Module 2:
Defining the research problem, selecting the problem, Necessity of defining the problem, Techniques involved in defining the problem. Importance of literature review in defining a problem, Survey of literature, Primary and secondary sources, Reviews, Treatise, mono graphs, patents. Web as a source, searching the web, Identifying gap areas from literature review. Development of working hypothesis.

Module 3:
IPRs, Invention and Creativity, Intellectual Property, Importance and Protection of Intellectual Property Rights (IPRs), A brief summary of: Patents, Copyrights, Trademarks, Industrial Designs, Integrated Circuits, Geographical Indications, Establishment of WIPO-Application and Procedures.

Module 4:
Aim is to strengthen student's minds towards high quality research through publications, patents and also to learn research ethics. Publications (8-9 hours).

Research concepts (2 hour), Research importance on economy, Research in India and abroad, Importance of publications, Why, where, when to publish?

Publication ethics (2 hour), Plagiarism (how to use turn it in effectively), International ethics on research, what not to publish, Ethical guidelines, Case studies.

Quality vs quantity (2 hour), Searching literature with high quality, Impact factor, Citations (google scholar vs web of science), H-index, Case studies.

How to write paper (2 hour), In High quality journals, Conference Articles, Poster preparation, PhD thesis, Inclusion of References.

Journal reviewing process(1 hour), Selection of the good journal, Knowledge bout journal template, Refereeing process, Research topic selection, Research today and tomorrow, Lab scale to Industry, Traditional research to Technology based research.

Module 5: Self study

Interpretation and report writing, Techniques of interpretation, Structure and components of Scientific reports, Different steps in the preparation, Layout, structure and language of the Report, Illustrations and tables, Types of report, Technical reports and thesis,

References:

1. Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002. An introduction to Research Methodology, RBSA Publishers.
2. Kothari, C.R., 1990. Research Methodology: Methods and Techniques. New Age International. 418p.
3. Anderson, T. W., An Introduction to Multivariate Statistical Analysis, Wiley Eastern Pvt., Ltd., New Delhi
4. Sinha, S.C. and Dhiman, A.K., 2002. Research Methodology, Ess Ess Publications. 2 volumes.
5. Trochim, W.M.K., 2005. Research Methods: the concise knowledge base, Atomic Dog Publishing. 270p.
6. Day, R.A., 1992.How to Write and Publish a Scientific Paper, Cambridge University Press.
7. Fink, A., 2009. Conducting Research Literature Reviews: From the Internet to Paper. Sage Publications.
8. Coley, S.M. and Scheinberg, C. A., 1990, "Proposal Writing", Sage Publications.
9. Intellectual Property Rights in the Global Economy: Keith Eugene Maskus, Institute for International Economics, Washington, DC, 2000
10. Subbarau NR-Handbook on Intellectual Property Law and Practice-S Viswanathan Printers and Publishing Private Limited.1998

II SEMESTER

Program Core Course Syllabus

II SEMESTER

Program Core Course Syllabus

Mixed Signal Circuit Design

COURSE CODE	**16ECVEPCMS**	**COURSE TITLE**	**Mixed Signal Circuit Design**	
CREIDTS	**4**	**L-T-P-S**	**3-0-1-0**	
CO	**Course Outcomes**			**PO**
CO-1	**Apply** the knowledge of Network theory, Electronic circuit design, VLSI design to obtain **optimised Mixed signal circuits**			**PO3**
CO-2	Analyze, Mixed Signal building blocks.			**PO2**
CO-3	Design, Data converters for the given specification.			**PO2,3**
CO-4	Ability to **conduct experiments to demonstrate** Mixed Signal building blocks (AMS flow using Cadence), perform research to identify best possible circuit suitable for **Mixed signal operation**			**PO2,3,4,5**
CO-5	Ability to make an **effective oral presentation and perform in a team** to build Mixed signal circuits using modern tools.			**PO6,8,9**

Switched capacitor circuits, Design of sample and hold circuits and comparators.

Oscillators and Phase Locked Loops: VCO, Mathematical Model of VCO, **PLL**, Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

Data converter fundamentals

DAC & ADC Specifications, Resistor String DAC, R-2R Ladder Network, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

Reference Book:

1. "Design of Analog CMOS Integrated Circuits", Behzad Razavi, TMH, 2007.

2. CMOS: Circuit Design, Layout, and Simulation, 3rd Edition –R. Jacob baker.
3. Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley.
4. David A Johns, Ken Martin: Analog IC design, Wiley 2008.

Lab Experiments:

1. Design a PLL and measure all the parameters.
2. Design a simple ADC/DAC and measure the data conversion time.
3. To measure INL and DNL of ADC/DAC

Design for Testability

COURSE CODE	**16ECVEPCDT**	**COURSE TITLE**	**Design for Testability**
CREIDTS	**4**	**L-T-P-S**	**3-1-0-0**

CO	Description	**PO**
CO1	Apply the concept of faults and failure models to generate the number of fault models & Automatic Test Pattern Generator (ATPG) for the given design under test (DUT)	**PO3**
CO2	Analyze and identify the given fault in given CUT(can be logic circuit or memory) and conclude the solution to test these faults	**PO2,PO3**
CO3	Ability to generate the Automatic Test Pattern Generator (ATPG) with different techniques using CAD tool.	**PO5**
CO4	Ability to search the research papers and attempt to suggest new solution as a team	**PO4,PO8, PO9**

Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG. Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.

Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Power issues in IC Testing

Text books:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L.Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

Reference books:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, JaicoPublishing House.

2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

Real Time Operating Systems

COURSE CODE	**16ECVEGCRO/ 16ECELGCES**	**COURSE TITLE**	**Real Time Operating Systems**
CREIDTS	**5**	**L-T-P-S**	**3-0-1-1**

CO1	Define, understand and explain concepts of Real Time Operating Systems.	**PO1**
CO2	**Apply** the knowledge of RTOS in Process & File Management, Inter-process Communication, etc and obtain performance difference when compared to normal OS.	**PO3**
CO3	**Analyze** the real-time deterministic response from interrupt service routines, signals and real time timers.	**PO2**
CO4	Design high performance software applications with real time deterministic response.	**PO2,3**
CO5	Develop C programs, execute & demonstrate concepts.	**PO2,3,5**
CO6	Ability to make an effective oral presentation on topics allocated by instructor pertaining to RTOS and related high performance computing concepts and Ability to perform in a team to code, compile and execute modular software applications.	**PO6,7,8,9**

Real Time Operating Systems

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

Objects, Services and I/O

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O

Concepts, I/O Subsystem

Exceptions, Interrupts and Timers

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

Case Studies of RTOS

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Text books:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

Reference books:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Lab Experiments:

1. Write a C program to copy contents from file1 to file2 by using.
    a. Linux System Calls.
    b. C Library Functions

Note: the outuput must be in the following format $mycp sourcefile destinationfile

2. Write a C program to program to print the following file attributes of given file.
    a. Number of Hard Links
    b. Inode Number
    c. Size of a file
    d. Group id and User id
    e. Time Stamp Information such as last access, last modified, last change
    f. I/O Block size
    g. File Type
3. Write a C Program
    a. To print the System Resource limit(at least 5) of a process by using getrlimit System call
    b. To modify any two System Resource limit by using setrlimit system call.

4. Write a C Program to catch the following signals
    a. SIGINT
    b. SIGSEGV
    c. SIGFPE
    d. SIGALRM (using alarm system call)
    e. SIGALRM (using setitimer system call)
5. Write a C program to ignore a SIGQUIT signal then reset the default action of the SIGINT signal by using
    a. signal system call
    b. sigaction system call
6. Write a C program to achieve inter process communication mechanism by using
    a. Pipe system call
    b. fifo/named pipe (write two programs, one for sender and another for receiver)
7. Write a C program to
    a. Create a message queue, by taking key value from the command prompt
    b. To send a message to message queue by taking message and key value from the command prompt
    c. To receive a message from a queue, by taking key value and message id from the command prompt
8. Write a C program to protect the critical section of a code by creating a binary semaphore
9. Write
    a. A C Program to store message in a shared memory segment by taking key and message from the command prompt
    b. A C program to demonstrate that more than one process can access the message stored in the shared memory
10. Configure the Linux kernel source code, build and boot the system with the newly built kernel.

II Semester electives

System Verilog and Verification

COURSE CODE	**16ECVEPESV**	**COURSE TITLE**	**System Verilog and Verification**	
CREIDTS	**4**	**L-T-P-S**	**3-1-0-0**	

CO-No	Course Outcomes	PO
CO-1	**Define, Understand and Explain** OOPs concepts and system Verilog data types	**PO1**
CO-2	**Apply** system Verilog constructs to create verification environment	**PO3**
CO-3	**Analyze** coverage driven verification for given design under test(DUT)	**PO2,5**
CO-4	**Able to conceptualize and obtain** 100% code coverage and functional coverage by determining the set of input constraints and assertions in test benches.	**PO3,5**

Verification Concepts: Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.

System Verilog: System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.

System Verilog: SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism.

Randomization:Directed Vs Random Testing. Randomization:Constraint Driven Randomization.

System Verilog: Assertions, Introduction to Assertion based verification, Immediate and concurrent assertions.

Coverage driven verification: Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

Building Test bench: Layered testbench architecture.

Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

References:

1. Janick Bergeron, Writing Testbenches Using SystemVerilog
2. Chris Spear, SystemVerilog for Verification
3. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, Verification Methodology Manual for SystemVerilog

Physical Design

COURSE CODE	**16ECVEPEPD**	**COURSE TITLE**	**Physical design**
CREIDTS	**4**	**L-T-P-S**	**3-1-0-0**

CO	**Course Outcomes**	**PO**
CO-1	Apply the Knowledge gained on the advanced concepts of modern VLSI system design including standard cells, cell libraries, IPs etc to partition, place the given netlist using algorithms.	**PO2**
CO-2	Analyse and Estimate the parameters for physical design of Proper ASIC	**PO2, PO3**
CO-3	Ability to run the netlist in EDA tools to perform Physical design.	**PO4, PO5 PO6**
CO-3	Ability to work as a team to understand the research papers on Physical design and educate other scholars by seminar presentation	**PO6**

Libraries

Standard cells, Transistor sizing, input-output pads, ESD and its sources, Library characterization, Timing models: Delay model, NLDM, Polynomial Delay model, Current source model.

Partitioning and Floor planning

Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition,

Fiduccia & Mattheyses, Technology File, Circuit Description Design Constraints, Design planning, Pad placement, power planning, Macro placement, Clock planning.

Placement

Global Placement, detail placement, clock tree synthesis, power analysis.

Routing (clock, power/ground, signal nets):

Special routing, Global routing, Detailed routing, Extraction

Verification

Functional Verification,

Timing verification (STA),

Physical Verification, SI analysis, Power Analysis

Text Book:

Khosrow Golshan,"Physical Design Essentials-An ASIC Design Implementation Perspective", 2007 Springer Science+Business, Media.

Reference books:

- F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs).Prentice Hall PTR, 1999.
- Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill International Edition 1995.
- Preas M. Lorenzatti, " Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.

Hardware/Software Co-design

COURSE CODE	**16ECVEPEHS**	**COURSE TITLE**	Hardware/Software Co-design
CREIDTS	**4**	**L-T-P-S**	**3-1-0-0**

CO	**Course Outcomes**
CO-1	Understand fundamental issues in co-design
CO-2	Learn about prototyping and emulation
CO-3	Understand compilation techniques, and learn related tools

CO-4	Acquire ability to differentiate various target architectures
CO-5	Acquire ability to generate specifications and develop verification plans

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

Text books:

1.Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.

2.Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

Reference books: 1. A Practical Introduction to Hardware/Software Co-design - Patrick R. Schaumont - 2010 – Springer

System On Chip Architecture

COURSE CODE	**16ECVEPESC**	**COURSE TITLE**	**System On Chip Architecture**
CREIDTS	**4**	**L-T-P-S**	**3-1-0-0**

CO	Course Outcomes
CO-1	**Apply** concepts of Moore's law, CMOS scaling to understand the System on Chip with its need, evolution, challenges, goals, superiority over system on board & stacked ICs in package.
CO-2	**Analyze** Typical goals in SoC design and also inter connect architecture
CO-3	**Design** solutions for issues at system level, and issues of Hardware-Software co design

Review of Moore's law and CMOS scaling, benefits of System On Chip integration in terms of cost, power, and performance. Comparison on System on Board, System on Chip, and System-in-Package. Typical goals in SoC design cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

System On Chip Design Process: A canonical SoC Design, SoC Designflow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software co design, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc.

Embedded Memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in an NoC. Packet switching and wormhole routing.

MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design

Case Study: A Low Power Open Multimedia Application Platform for 3G Wireless.

Reference Books:

1. Sudeep Pasricha and Nikil Dutt,**"On-Chip Communication Architectures: System on Chip Interconnect"**, Morgan Kaufmann
Publishers © 2008.
2. Rao R. Tummala, Madhavan Swaminathan, **"Introduction to system on package sop-Miniaturization of the Entire Syste"**,
McGraw-Hill, 2008.
3. James K. Peckol, **"Embedded Systems: A Contemporary Design Tool"**, Wiley Student Edition.
4. Michael Keating, Pierre Bricaud, **"Reuse Methodology Manual for System on Chip designs"**, Kluwer Accademic Publishers, 2nd
edition, 2008.
5. Sung-Mo Kang, Yusuf Leblebici, **"CMOS Digital Integrated Circuits"**, Tata Mcgraw-Hill, 3rd Edition.

Embedded design using ARM architecture

COURSE CODE	**16ECVEPEAM**	**COURSE TITLE**	**Embedded design using ARM architecture**
CREIDTS	**4**	**L-T-P-S**	**3-1-0-0**

CO1	**Acquire the knowledge** on ARM organization and the feature rich ARM Cortex architecture and to understand serial communication techniques with microcontroller. **apply** skills to model complete Embedded System.
CO2	**Analyze** digital and analog peripherals, memory of ARM Cortex-Mx microcontrollers
CO3	**Conduct experiments** with ARM Cortex board to develop various application
CO4	Ability to **Demonstrate** the development of embedded applications using ARM Cortex platforms, in a team or individual

Introduction to Embedded Systems, Microprocessors and Microcontrollers, RISC & ARM Architecture, Introduction to ARM Cortex – M Processor Family, Introduction to Software development process and platform.

Lab: Introduction to mbed/similar development board, Keil/similar IDE environment, Blinky Code, Key Input Single/linear/matrix, Interfacing character & graphic LCD.

ARM Cortex – M Architecture Programming Model, Instruction Set, Interrupts & Exception Handling, Timers & PWM

Lab: Experiments with Timers, Generation of 3 phase PWM, Sine wave generation, speed control of DC motor using PWM

Memory model, DMA, Floating Point Operations, Serial Communication peripherals: UART+SPI+I2C, Cortex Microcontroller Software Interface Standard

Lab: Interfacing two devices using UART, Read/Write Memory chip using SPI, Interface RTC chip using I2C

Analog peripherals ADC, DAC, interfacing analog sensors like, temperature, pressure sensors. Low power configurations of ARM microcontrollers

Lab: Generating waveforms using DAC, Acquiring analog signals using ADC and characterizing using FFT

DSP on ARM Cortex-M4, Developing Closed Loop & PID Control Systems

Lab: Interfacing with PC using Serial peripherals are using wireless devices

Reference Books:

1. Fast and Effective Embedded Systems Design: Applying the ARM mbed, by Rob Toulson & Tim Wilmshurst, Newnes, 2012

2. The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors, by Joseph Yiu, Newnes, 2013

3. The Designer's Guide to the Cortex-M Processor Family: A Tutorial Approach, by Trevor Martin, Newnes, 2013

Memory Design and Testing

COURSE CODE	**16ECVEPEMD**	**COURSE TITLE**	**Memory Design and Testing**
CREIDTS	**4**	**L-T-P-S**	**3-1-0-0**

CO1	Acquire the knowledge on Semiconductor memories
CO2	Ability to Apply the knowledge of CMOS technology and electronic circuits theory to design semiconductor memories
CO3	Ability to Analyze different types of memories.
CO4	**Model and Design** for Reliability and analyse radiation effect
CO5	Ability to submit a report on the impact/growth of Advanced Memory Technologies for societal and sustained development.

Random Access Memory Technologies: SRAM Cell Structures-MOS SRAM Architecture, MOS SRAM Cell and Peripheral, Circuit Operation, Bipolar SRAM Technologies, Silicon On Insulator (SOl) Technology, Advanced SRAM Architectures and Technologies, Application Specific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs, Soft Error Failures in DRAMs, Advanced DRAM Designs and Architecture, Application Specific DRAMs.

Non-volatile Memories: Masked Read-Only Memories (ROMs), High Density ROMs, Programmable Read Only Memories (PROMs), Bipolar PROMs, CMOS PROMs, Erasable (UV), Programmable Road-Only Memories (EPROMs), Floating-Gate EPROM Cell, One-Time Programmable (OTP) EPROMS, Electrically Erasable PROMs (EEPROMs), EEPROM Technology and Architecture, Non-volatile SRAM, Flash Memories (EPROMs or EEPROM), Advanced Flash Memory Architecture.

Memory Fault Modelling, Testing and Memory Design For Testability and Fault Tolerance. RAM Fault Modelling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Non-volatile Memory Modelling and Testing, IDDQ Fault Modelling and Testing, Application Specific Memory Testing.

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory Reliability, Reliability Modelling and Failure Rate Prediction. Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification. Radiation Effects, Single Event Phenomenon (SEP), Radiation Hardening Techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test Structures.

Advanced Memory Technologies and High-Density Memory Packaging Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs. Analog Memories, Magneto resistive Random Access Memories (MRAMs). Experimental Memory Devices. Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM Testing and Reliability Issues, Memory Cards, High Density Memory Packaging Future Directions.

Text Books

1. A.K Sharma, "Semiconductor Memories Technology, Testing and Reliability", IEEE Press.
2. Luecke Mize Care, "Semiconductor Memory design & application", Mc-Graw Hill.
3. Belty Prince, " Semiconductor Memory Design Handbook"
4. Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor.

Advanced Computer Architecture

COURSE CODE	**16ECVEGEAC 16ECELGEAC**	**COURSE TITLE**	**Advanced Computer Architecture**
CREIDTS	**4**	**L-T-P-S**	**3-1-0-0**
CO1	Acquire knowledge on the basic concepts of computer design, identifying the performance parameters and quantitative principles.		

CO2	Recognize the instruction level parallelism and different methods used for scheduling and structuring the code.
CO3	Analyse the performance and Identify the limitations of ILP for the efficiency of multi pipeline architecture
CO4	Understand the memory hierarchy, the I/O system and their impacts on system development.
CO5	Recognize the performance improvements by implementing shared memory and cache coherence and Identify associated issues in Inter-processor communication.

Introduction and Review of Fundamentals of Computer Design: Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design.

Some topics in Pipelining, Instruction –Level Parallelism, Exploitation and Limits on ILP: Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining; Basic concepts and challenges of ILP.

Memory Hierarchy Design, Storage Systems: Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy; Fallacies and pitfalls in the design of memory hierarchies.

Advanced topics in disk storage: Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls Definition and examples of real faults and failures; I/O performance, reliability measures, and benchmarks**,** Queuing theory; crosscutting issues.

Hardware and Software for VLIW and EPIC Introduction: Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism.

Large-Scale Multiprocessors and Scientific Applications Introduction, Inter processor Communication: The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications.

References:

1. John L. Hennessey and David A. Patterson, "**Computer Architecture – A quantitative approach",** Morgan Kaufmann / Elsevier, Fifth edition, 2012.
2. Richard Y. Kain, "**Advanced Computer Architecture a Systems Design Approach**", PHI, 2011

Institutional elective

Institutional elective

ADVANCED MICRO & NANO DEVICES

COURSE CODE	16ECVEIEMN	COURSE TITLE	ADVANCED MICRO & NANO DEVICES
CREIDTS	4	L-T-P-S	4-0-0-0

CO1	Acquire knowledge on the fundamental concepts of nano science engineering.	**PO1**
CO2	Analyse properties of different types of nano structure	**PO2**
CO4	Ability to submit a report on the impact/growth of micro/nano devices on societal and sustained development and also to submit report on fabrication of nano structures	**PO8**
CO5	Involve in independent/team learning, Communicate effectively and engage in life-long learning	**PO6,9**

Introduction: Overview of nano science and engineering. Development milestones in micro fabrication and electronic industry. Moores law and continued miniaturization.

Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nano meter length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nano materials, ordering of nano systems.

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.

Hetero Structures and Quantum Well devices: Quantization and low-dimensional electron gas, band alignment in Si/SiGe hetero-structures, HEMTs, Carbon Nano-tube, Graphene device.

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nano crystals, colloidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural.

Methods of measuring properties structure: atomic, crystallography, microscopy, spectroscopy. Properties of nanoparticles: metal nano clusters, semiconducting nanoparticles, rare gas and molecular clusters, methods of synthesis(RF, chemical, thermolysis, pulsed laser methods) Carbon nanostructures and its applications(field emission and shielding, computers, fuel cells, sensors, catalysis).Self assembling nano structured molecular materials and devices: building blocks, principles of self assembly, methods to prepare and pattern nanoparticles, template nanostructures, liquid crystal mesophases. Nano magnetic materials and devices: magnetism, materials, magneto resistance, nano magnetismin technology, challenges facing nano magnetism.

Text Book:

1. The MOS Transistor (second edition) Yannis T sividis, Oxford publishing press 2007

Reference Book:

2. Ed Robert Kelsall,IanHamley,MarkGeoghegan, " Nanoscale science and technology" ,John wiley and sons,2007.

3. Charles P Poole,Jr,Frank J owens, "Introduction to Nanotechnology" ,John wiley,copyright 2006,Reprint 2011.

4. Ed William A Goddard III,Donald W Brenner,SergeyEdwardLyshevski,Gerald J Lafrate, " Hand Book of Nanoscience Engineeringand Technology" ,CRC press,2003

ROBOTICS

COURSE CODE	**16ECVEIERB**	**COURSE TITLE**	**ROBOTICS**
CREIDTS	**4**	**L-T-P-S**	**3-0-1-0**

CO1	Acquire knowledge on the fundamentals in Robotics namely Kinematics, Controls, sensors and actuators	**PO**
CO2	Apply the knowledge of signal processing in Vision and Processing and to move towards Higher-Level Vision.	**PO3**
CO3	Analyse the integration of Kinematics, Sensors and Control system	**PO2**
CO4	Build prototype robot on his/her own and demonstrate the basic physics and mathematics behind it	**PO2,3,4,5**
CO5	Involve in independent/team learning, Communicate effectively and engage in life-long learning	**PO6,8**

Introduction: Objectives, Classification of robots, Major components of robot, definitions: Kinematics, Controls, and actuators. Robot history, types and applications current and future with examples. Fixed and flexible automation

Robot Arm Kinematics: Introduction, The direct kinematics problem, Rotation Matrices, Composite rotation Matrix, Rotation matrix about arbitrary axis, Rotation matrix with Euler angle representation, Geometric interpretation of rotation matrix, Homogenous coordinates and transformation matrix, Geometric interpretation of Homogenous transformation matrices, Composite homogenous transformation matrices, Links, Joints, and their parameters, The Denavit - Hartenberg representation, Kinematic equation for manipulator, Other specifications of the locations of the end effectors, Inverse kinematics problem.

Control of Actuators: Objective, Motivation, Closed loop control in position servo, Effect of friction and gravity, Adaptive control, Optimal control, Computed torque technique, Transfer function of single joint, Position control for single joint, Brief discussion on performance and stability criteria.

Sensors Robotic system, Sensor definition and classification, Sensor characteristics, Sensor calibration, Range sensing techniques: Triangulation, Structured light approach, Time of flight, Binary sensors, Analog sensors, Position sensors or Displacement sensor - Potentiometers, Encoders, LVDT, Resolvers, Hall Effect sensors. Velocity sensor- Tachometers (Magnetic and optical encoders). Force and Pressure sensors or Force and Torque sensing - Piezoelectric, Strain guage, Proximity sensors - Magnetic, Optical, Ultrasonic, Inductive, Capacitive, Eddy-current sensors, Touch and tactile sensor, Torque sensors, Elements of a Wrist sensor. SAMs

Vision and Processing: Image acquisition, illumination Techniques, imaging geometry, some basic transformations, perspective transformations. Camera model, camera calibration, stereo imaging,

Higher-Level Vision: Segmentation, Edge Linking and Boundary detection, Thresholding. Region-oriented segmentation, Use of motion, Description, Boundary descriptors, Regional descriptors

TEXT BOOKS:

1. Robotics – control, sensing, Vision and Intelligence", K.S.Fu, R.C.Gonzalez, C.S.G. Lee, McGraw Hill, 1987.

2. "Robotic Engineering" - Richard D Klafter, PHI

REFERENCE BOOKS:

1."Introduction to Robotics Mechanics and control", John J. Craig, 2nd Edition, Pearson education, 2003

2."Mechatronics" - W. Bolton

Master of Technology

In

VLSI Design and Embedded system

III SEMESTER

CO1	Ability to develop a sound theoretical and practical knowledge of new technologies.	PO1,PO2,PO5
CO2	Ability to Develop domain specific problem solving and critical thinking skills	PO2,PO3,PO4

COURSE CODE	**16ECVEPCIN**	**COURSE TITLE**	**INTERNSHIP**
CREDITS	**21**	**L-T-P-S**	**0 – 0 – 21 - 0**

Course Title: INTERNSHIP

COURSE OUTCOMES

CO3	Ability to develop individual responsibility towards their internship goal as well as participate as an effective team member	PO6,PO7
CO4	To gain exposure to professional work culture & practices	PO9,PO10
CO5	Develop effective presentation & communication skills, and create proper documentation of the work	PO8,PO11

CO1	Identify a suitable project making use of the technical and engineering knowledge gained from previous courses with the awareness of impact of technology on the	PO1,PO2,PO3PO4, PO5,PO9,PO10

COURSE CODE	**16ECVEPCIP**	**COURSE TITLE**	**PROJECT WORK(I-Phase)**
CREDITS	**04**	**L-T-P-S**	**0 – 0 – 4 - 0**

Course Title: Project work (I-phase)

COURSE OUTCOMES OF I-phase

CO2	Collect and disseminate information related to the selected project within given time frame.	PO6,PO7
CO3	Communicate technical and general information by means of oral as well as written Presentation skills with professionalism.	PO8,PO11

Master of Technology

In

VLSI Design and Embedded system

IV SEMESTER

Course Title: PROJECT WORK (FINAL PHASE)

COURSE CODE	16ECVEPCPR	COURSE TITLE	PROJECT WORK (Final-Phase)
CREDITS	23	L-T-P-S	0 - 0 – 23 - 0

COURSE OUTCOMES –phase-II

CO1	Identify the modern tools required for the implementation of the project.	PO5
CO2	Design, examine critically and implement or develop a prototype for the identified problem during Phase I	PO1,PO2,PO3, PO4
CO3	Communicate technical information by means of oral as well as written presentation skills with professionalism and engage in	PO8,PO9,PO10, PO11

Course Title: Technical Seminar

COURSE CODE	16ECVEPCTS	COURSE TITLE	TECHNICAL SEMINAR
CREDITS	02	L-T-P-S	0 – 0 – 2 – 0

COURSE OUTCOMES

CO1	Identify the problem through literature survey by applying depth knowledge of the chosen domain	PO1,PO4
CO2	Analyse, synthesize and conceptualize the identified problem	PO2,PO3
CO3	Communicate clearly, write effective reports and make effective presentations following the professional code of conduct and ethics	PO8,PO10
CO4	Comprehensively study the domains and reflect the same towards the future enhancements of the work	PO11