BMS COLLEGE OF ENGINEERING, BENGALURU-19

Autonomous Institute, Affiliated to VTU

Department of Electronics and Communication Engineering

Scheme and Syllabus: M.Tech. in Electronics and Communication Engineering

(Specialization in Electronics)

Batch 2024 onwards

INSTITUTE VISION

Promoting Prosperity of mankind by augmenting human resource capital through QualityTechnical Education & Training

INSTITUTE MISSION

Accomplish excellence in the field of Technical Education through Education, Research andService needs of society

DEPARTMENT VISION

To emerge as a Centre of Academic Excellence in Electronics, Communication and related domains through Knowledge acquisition, knowledge dissemination and Knowledge generation meeting global needs and standards

DEPARTMENT MISSION

Imparting quality education through state-of-the-art curriculum, conducive learning environment and Research with scope for continuous improvement leading to overall Professional Success

PROGRAM EDUCATIONAL OBJECTIVES

The department has defined the following PEOs for the PG program in Electronics.

PEO1: Graduates shall be capable of building their career in related industries, R&D Establishments as well as in teaching with their scholarly knowledge with respect to advanced topics in Applied Electronics and VLSI Engineering.

PEO2: Graduates shall be capable of conceptualizing and analyzing engineering problems of societal importance related to Embedded Systems, VLSI and signal Processing, conduct independent Research leading to technology solutions and communicate the outcomes through verbal and written mechanisms.

PEO3: Graduates shall be able to collaborate, manage and execute projects in teams using appropriate tools/technologies with utmost professionalism and acceptable good practices.

PROGRAM OUTCOMES

Program Outcomes (POs) are attributes acquired by the student at the time of graduation. These attributes are measured at the time of graduation and hence computed every year for the outgoing batch. The POs are addressed and attained through the Course Outcomes (COs) of various courses of the curriculum.

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An Ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirementsin the appropriate bachelor program.

Distribution of Credits

Category	No of Credits
Program Core Courses (PC)	**23**
Program Elective Courses (PE)	**21**
Lab Component	**04**
Internship	**11**
Project Work	**20**
Ability Enhancement Course	**1**
Non-credit Mandatory Course	**No credits**

Total Number of Credits (1st Sem. ~ 4th Sem.) = 80Credits

Note:

1 Credit = 15Hrs of Teaching

2 Credit= 25Hrs of Teaching

3 Credit = 40Hrs. of Teaching

4 Credit= 50Hrs of Teaching

M.Tech. in Electronics and Communication Engineering

Specialization in Electronics

I Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits			Credits
				L	T	P	
1	PCC	MEC101	Advanced Machine Learning and Deep Learning	3	0	0	3
2	IPCC	MEC102	Advanced Embedded Systems	3	0	1	4
3	PCC	MEC103	Digital Circuits & Logic Design	3	0	0	3
4	PEC	MEC114	Elective- 1	3	0	0	3
5	PEC	MEC115	Elective- 2	3	0	0	3
6	PECL	MECL116 X	Lab Elective	0	0	2	2
7	NCMC	MRMI107	Research Methodology & IPR	0	0	0	0
		Total		15	0	3	18

Professional Elective I		Professional Elective II	
MEC114A	ASIC Design	MEC115A	System Verilog
MEC114B	Advanced Computer Networking	MEC115B	Advanced Wireless Communication
MEC114C	Advanced Signal Processing	MEC115C	Multimedia & Applications
MEC114D	Power Converters	MEC115D	Process Control
MEC114E	Digital IC design	MEC115E	Static Timing Analysis
MEC114F	Data Networks	MEC115F	Advanced Digital Communications

Lab Elective			
MECL116A	Advanced Machine Learning and Deep Learning Lab	MECL116B	Electronics and Communication Lab
MECL116C	Digital System Design Lab		

M.Tech. (Electronics)

II Semester **CREDIT BASED**

Sl. No	**Course Type**	**Course Code**	**Course Title**	**Credits**			**Credits**
				L	**T**	**P**	
1	PCC	MLEL201	Antenna Theory and Design	3	0	0	3
2	IPCC	MLEL204	Real Time operating systems	3	0	1	4
3	PCC	MLEL205	Low power VLSI Design	3	0	0	3
4	PCC	MLEL206	VLSI Testing and Verification	3	0	0	3
5	PEC	MLEL215x	Elective-3	3	0	0	3
6	PEC	MLEL216x	Elective-4	3	0	0	3
7	PECL	MLELL209	VLSI Testing and Verification Lab	0	0	2	2
8	AEC/SEC	MLEL258x	Ability/ Skill Enhancement Course (Offline/Online)	1	0	0	1
		Total		19	0	3	22

Professional Elective 3		Professional Elective 4	
MLEL215A	CMOS RF Circuit Design	MLEL216A	Mechatronics
MLEL215B	Statistical Signal Processing	MLEL216B	Internet of Things and Applications
MLEL215C	Probability and Random Process	MLEL216C	Cyber Security
MLEL215D	Simulation, Modelling and Analysis	MLEL216D	Automotive Electronics
MLEL215E	Scripting Languages	MLEL216E	Cryptography and Network Security

III(A)

III Semester **CREDITBASED**

Sl. No	Course Type	Course Code	Course Title	Credits			Credits
1	PEC /MDC	MISS311x	(Online Courses) 12weeks duration				3
2	PEC /MDC	MISS312x	(Online Courses) 12weeks duration				3
3	PEC /MDC	MISS313x	(Online Courses) 12weeks duration				3
4	INT	MINT384	Research Internship /Industry Internship leading to project work/ Startup				3
		Total					12

IV(A)

IV Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits			Credits
1	INT	MINT481	Research Internship /Industry-Internship leading to project work/ Startup				12
2	PROJ	MPRJ482	Project				16
		Total					28

III(B)

III Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits			Credits
1	PEC /MDC	MISS311x	(Online Courses) 12weeks duration				3
2	PEC /MDC	MISS312x	(Online Courses) 12weeks duration				3
3	PEC /MDC	MISS313x	(Online Courses) 12weeksduration				3
4	INT	MINT384	Industry-Internship				11
		Total					20

IV(B)

IV Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits			Credits
1	Project	MPRJ481	Project work				20
		Total					20

III(C)

III Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits			Credits
1	PEC/IPCC/ MDC/PEC	MISS311x	(Online Courses) 12weeks duration				3
2	PEC/IPCC/ MDC/PEC	MISS312x	(Online Courses) 12weeks duration				3
3	PEC/IPCC/ MDC/PEC	MISS313x	(Online Courses) 12weeks duration				3
4	PEC/IPCC/ MDC/PEC	MISS314x	(Online Courses) 12weeks duration				3
4	PROJ	MPRJ385	Project Phase-1				6
		Total					18

IV(C)

IV Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits			Credits
1	Project	MPRJ481	Project Work				22
		Total					22

First Semester Syllabus

Course Title	Advanced Machine Learning and Deep Learning				
Course Code	**MEC101**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites:
- Understanding of Linear Algebra, Statistics & probability, Discrete Mathematics and Differential Calculus
- Basic Programming Skills in Python

Course Outcomes:

CO1	Comprehend concepts in the field of Artificial Intelligence	PO3
CO2	Apply the knowledge of mathematics and programming to structure datasets and algorithms to build machine learning models.	PO3
CO3	Analyze the neural networks CNN & RNN architectures in application to different use cases and performance measures to evaluate the models.	PO3
CO4	Design and develop machine learning and deep learning models for computer vision and natural language processing.	PO3
CO5	Engage on survey of various available datasets and possible sustainable solutions that could be developed for the societal need.	PO2

Unit I

Introduction to Machine Learning & Data Analysis: Basic concepts of Artificial Intelligence, Necessity of learning AI, Applications of AI, Cognitive modelling, Introduction to Machine learning and Deep learning, Essentials of Linear Algebra and Applied Statistics, Introduction to Python Libraries, Exploratory data analysis, Supervised learning: Unsupervised learning, Reinforcement learning**.**

Unit II

Neural Networks: Introduction, Neurons, Perceptrons, Multilayer Neural Networks, Various activation functions, loss functions, Optimizers, Hyperparameters, Evolving Neural Networks.

Unit III

Convolutional Neural Networks: The operation, Pooling, Convolution and Pooling as an infinitely strong prior, CNN architectures, efficient algorithms, Random or Unsupervised Features, Neuroscientific Basis for Convolutional Networks.

Unit IV

Recurrent Neural Networks: RNN, Bidirectional RNN, Encoder-Decoder Sequence to sequence architecture, Deep Recurrent Networks, Recursive Neural Networks, The Long Short Term Memory and other Gated RNNs, Optimization for Long Term Dependencies.

Unit V

Applications: Large-Scale Deep Learning, Computer Vision, Speech Recognition, Natural Language Processing, Other Applications.

Text books:

1. Introduction to Machine Learning with Python: A Guide for Data Scientists", Andreas C. Muller and Sarah Guido, O'Reilly Publication, 2019.
2. Deep Learning- A Practitioner's Approach, Josh Patterson & Adam Gibson, O'Reilly Publication, 2019
3. Deep Learning with Python: Francois Chollet , Manning Publications, 1st edition.
4. Handbook of Reinforcement Learning and control, Kyriakos G. Vamvoudakis, Yan Wan, Frank L. Lewis, DeryaCanseve, Springer- 2021

REFERENCE BOOKS:

1. Python Data Science Hand Book – Jake VanderPlas, O'Reilly Publication, 2016-17

E Books:

1. https://www.pdfdrive.com/machine-learning-with-python-cookbook-practical-solutions-from-preprocessing-to-deep-learning-d176361144.html
2. Machine Learning in Action, Peter Harrington, Dreamtech Press Indian Edition, 2017

MOOCs:

https://www.simplilearn.com/artificial-intelligence-masters-program-training-course

Course Title	Advanced Embedded Systems				
Course Code	MEC102	Credits	4	L-T-P	3:0:1
CIE	50 Marks	SEE		50 Marks	

Prerequisites:
Introductory course on Embedded Systems, Microcontrollers (any), Basic C Programming Skills

Course outcomes:

CO1	Analyze the advanced features of ARM processors to develop efficient Embedded Systems	PO3
CO2	Develop and analyze the performance of C programs for execution on microcontroller/SOC development board based on ARM architecture. Develop Python programs to interface with Embedded Systems.	PO3
CO3	Develop embedded systems using different approaches	PO3
CO4	Engage on market survey of various available embedded hardware and software architecture for performance, power and cost optimization. Present a report on the same.	PO1,2

Unit I
ARM architecture: ARM product profiles and features, Cortex M features and applications, performance, operation modes and privilege levels, switching of operation modes, register classification and importance, memory map, advantages of bit band region, aligned and unaligned access, endianess and performance, SYSTICK timer and interrupt, exception types, NVIC, interrupt and execution sequences, vector fetches, tail chaining, faults caused by exceptions, ARM busses and their role to enhance performance.

Unit II
Embedded C Programming: C and embedded C data types, bit manipulation, advanced pointer use, function pointers arrays and dynamic memory allocation, introduction to data structures, enumerations, unions, structures and encapsulation, bit fields, LIFO buffer, circular buffer, linked list. Modular C programming, writing header files and exception handlers.

ARM memory access using variables and pointers, design of CPU Core and Peripheral register structures using bit fields, IO port configuration example, creating software interfaces for hardware, Pre-processor directives in C. Storage Classes of C. Storage type qualifiers, inline assembly, performance optimization through appropriate data type selection and data alignment.

Unit III

Python Programming: Introduction Python Programming, data types, lists, tuples, dictionaries, conditional statements, iterative statements, functions. File and I/O handling, serial device interfaced to external devices. Strings and data formatting, integer, bytes, hexadecimal representation, embedded programming using python case studies, UI design (arduino/RPi).

Unit IV

Firmware Architecture for Embedded Systems: Super Loop, Interrupt driven, RTOS, CMSIS RTOS, Low Power Operations. Speed Power Product, Optimization for time and space.

Unit V

Develop an embedded system using different approaches: using GPP, using FPGA and as a SPP. Debugging Techniques for Embedded Systems: Introduction to GNU Debugger gdb. uVision IDE based debugging techniques. Single Stepping, Break Points, Watch Points, and Memory Probing. Simulation using uVision.

Text Books:

1. Joseph Yiu, “Definitive guide to the ARM Cortex-M3”, Latest available edition
2. Hennessy and Patterson, “Computer Architecture: A Quantitative Approach”, Latest available edition
3. Michael J Pont, “Embedded C”, latest available edition
4. Leonard Edison, “Python Programming”, latest available edition

Reference Books:

1. Technical reference manual and datasheets of Cortex-M3 microcontroller and other components.
2. Shibu K V, “Introduction to Embedded Systems”, Latest available edition
3. And many other online tutorials and references.

E Books:

1. Joseph Yiu, "Definitive guide to the ARM Cortex-M3", Latest available edition
2. Practical C Programming, 3rd Edition by by Steve Oualline, Publisher(s): O'Reilly Media, Inc. ISBN: 9781565923065
3. Introducing Python, 2nd Edition by Bill Lubanovic Released November 2019
Publisher(s): O'Reilly Media, Inc. ISBN: 9781492051367

MOOC/Online courses:

- Embedded Software and Hardware Architecture by University of Colorado Boulder – Coursera
- Embedded system Design IIT by AnupamBasu, IIT Kharagpur https://nptel.ac.in/courses/106/105/106105159/

LABORATORY EXPERIMENT LIST

Sl.No	Title of the Experiments
	PART 1
1.	Install Keil MDK for ARM along with development board drivers. Interface development board to development PC. Download and test blinky code example.
2.	Develop a super loop to transmit ADC data on UART every 'x' Unit-s of time.
3.	Receive data from an analog sensor, digitize it and send it to display Unit-.
4.	Develop an interrupt routine to accept 100 bytes of data from sensors and send out on SPI or I2C bus. Consider buffering and non-buffering approaches.
5.	Develop an interrupt routine to control any actuator aa per given specifications.
6.	Configure port pin to function as external interrupt and develop interrupt handler as per specifications (discussed in class).
	PART 2
1.	Develop services and instantiate them in different ways.
2.	Create structures to realize special registers of ARM microcontroller.
3.	Develop APIs to access individual bits/nibble/whole register contents and to configure MC for specific modes.
4.	Create APIs to realise exception facilities as in ARM controllers (use unions).

	PART 3
1.	Create databases using python scripts. Store sensor data as a database.
2.	Develop Python code to interface external peripherals.
3.	Create webpages using python scripts.
4.	Read data from webpage using python program and transfer the same to microcontroller over UART.
5.	Post data on to any webpage using Python.
6.	Send emails using Python program.
7.	Receive data from microcontroller on to PC using Python and either email that data or post it on to any webpage.

NOTE: Any ARM Cortex M development board can be used. Audrino /RPi can be used to port python codes.
Platform used: Kiel uVision MDK IDE, C compiler on Windows. Lab and Theory sessions are integrated.

Course Title	Digital Circuits & Logic Design				
Course Code	MEC103	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Prerequisites:
Digital Electronics, HDL (Verilog/ VHDL)

Course outcomes:

CO1	Ability to demonstrate In-depth knowledge of Verilog for advanced digital circuits and logic design.	PO3
CO2	Analyze and design different combinational and sequential digital circuits using Verilog.	PO3
CO3	Engage in independent mini project and to prepare a Technical document and oral presentation for a design of digital system using Verilog.	PO2,PO1

Unit I
Introduction to Digital design Methodology: Design methodology and technology overview: Digital Systems and Embedded Systems, Real-World Circuits: Static load levels, Capacitive load & propagation delay, Sequential timing, Area and Power. Models, Design methodology**,** Modeling of Verilog Combinational and Sequential circuits.

Unit II
Design of Combinational and Sequential logic:
Binary coding, Adders, Multipliers, Counters, Memories, Multiport Memories, Design of Error Detection and Correction circuits**,** Design of memories, Sequential Data paths and Control Path, Finite state Machines, Clocked Synchronous Timing Methodology, Asynchronous inputs, Design of sequential circuits, asynchronous timing methodology.

Unit III
Synthesis of Combinational and Sequential logic:
Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit State Machines. Threshold Logic: Introductory

Concepts, Synthesis of Threshold Networks Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities

Unit IV

System Implementation Fabric: Introduction of Programmable Logic Array (PLA), Programmable Array Logic (PAL), Programmability of PLDs. Complex PLDs (CPLDs), Field-Programmable Gate Arrays. FPGA Technologies. Verilog-Based Design Flows for FPGAs.

Unit V

Processor Design and System development: Hierarchical Decomposition STG-Based
Controller Design, Efficient STG-Based Sequential Binary Multiplier.
Algorithms and Architectures for Digital Processors: Algorithms, Nested-Loop Programs, and Data Flow Graphs.

Text books:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.
2. Advanced Digital Design with the Verilog HDL, Michael D. Ciletti, 2nd Edition, PHI, ISBN: 978–0–07–338054–4 2015.
3. Fundamentals of Digital Logic with Verilog Design, Stephen Brown and ZvonkoVranesic, 6th Edition, 2014, McGraw Hill publication, ISBN: 978–0–07–338054–4

REFERENCE BOOKS

1. Digital Design: An Embedded Systems Approach Using VERILOG, Peter J. 1st Edition, 2010,
Ashenden, Elsevier, ISBN: 978-0-12-369527-7
2. Digital Systems Design Using Verilog, 1st Edition, 2015, Charles Roth, Lizy K. John, ByeongKil Lee,Cengage Learning, ISBN-10: 1285051076
3. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design & Synthesis", SunSoft Press,
1stEdition, 1996, ISBN: 978-81-775-8918-4.
4. Digital Design using Verilog, Elsevier, 2007 W. Wolf

5. Stuart S, Simon David & Peter Flake "System Verilog for Design" A guide to using system Verilog for Hardware design and modelling Springer publication 2nd Edition, 2006.

E Books:

1. https://freevideolectures.com/course/2319/digital-systems-design
2. http://www.asicguru.com/system-verilog/tutorial/introduction/1/
3. https://www.chipverify.com/systemverilog/systemverilog-tutorial
4. http://www.testbench.in

MOOCs:

1. https://nptel.ac.in/courses/106/108/106108099/
2. https://nptel.ac.in/courses/117/106/117106092/
3. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-111-introductory-digital-systems-laboratory-spring-2006/index.htm

Course Title	ASIC Design					
Course Code	**MEC114A**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: VLSI Design

Course outcomes:

CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort	PO3
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow	PO3
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay	PO3
CO4	Create floor plan including partition and routing with the use of CAD algorithms	PO3
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design	PO3

Unit I

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carryselect, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.

Unit II

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi-stage cells, Optimum delay and number of stages, library cell design. Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.

Unit III

Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms. RBT L.

Unit IV

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.

Unit V

Routing: Global Routing - Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing - Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.

Text books:

1. Michael John Sebastian Smith, “Application - Specific Integrated Circuits”, Addison- Wesley Professional, 2005
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, “CMOS VLSI Design: A Circuits and Systems Perspective” , Addison Wesley/ Pearson education 3rdedition, 2011.
3. Vikram Arkalgud Chandrasetty, “VLSI Design: A Practical Guide for FPGA and ASIC Implementations” Springer, ISBN: 978-1-4614-1119-2. 2011.
4. Rakesh Chadha, Bhasker J, “An ASIC Low Power Primer”, Springer, ISBN: 978-14614-4270-7.
5. Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog,1st Edition, Kindle Edition.

Course Title	Advanced Computer Networking				
Course Code	MEC114B	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Prerequisites: Basics of Computer networking

Course outcomes:

CO1	Understand advanced concepts and next generation networks.	PO 3
CO2	Analyze network Algorithms, Protocols and their functionalities.	PO 3
CO3	Comprehend features of SDN and its application to next generation systems.	PO 3
CO4	Analyze the performance of various server implementations.	PO 3

Unit I

Medium Access Control Sub Layer: Wireless LANs, Broadband Wireless, Bluetooth, RFID. The Network Layer: Network Layer Design Issues, Congestion Control Algorithms, Quality of Service, The Network Layer in the Internet.

Unit II

The Application Layer: The Domain Name System, Electronic Mail, The World Wide Web

Unit III

Software Defined Network (SDN): Evolution of Switches and Control Planes, Cost, SDN Implications for Research and Innovation

Genesis of SDN: The Evolution of Networking Technology, Forerunners of SDN, Software Defined Networking is Born, Sustaining SDN Interoperability, Open Source Contributions, Network Virtualization

How SDN Works: Fundamental Characteristics of SDN, SDN Operation, SDN Devices, SDN Controller, SDN Applications, Alternate SDN Methods

Unit IV

The Openflow Specification: OpenFlow Overview, OpenFlow 1.0 and OpenFlow Basics, OpenFlow Additions - 1.1, 1.2, 1.3, 1.4, 1.5, Improving

OpenFlow Interoperability, Optical Transport Protocol Extensions, OpenFlow Limitations

Unit V

Network Functions Virtualization: Definition of NFV, Virtualize, Standards, OPNFV, Leading NFV Vendors, SDN Vs NFV, In-Line Network Functions

SDN Open Source: SDN Open Source Landscape, The OpenFlow Open Source Environment, Profiles of SDN Open Source Users, OpenFlow Source Code, Switch Implementations, Controller Implementations, SDN Applications, Orchestration and Network Virtualization, Simulation, Testing and Tools, Open Source Cloud Software, Example: Applying SDN Open Source.

Text Books:

1. Andrew S. Tanenbaum, David J. Wetherall, Computer Network, 5th Edition. Pearson Education.

2. Paul Goransson, Chuck Black and Timothy Culver, Software Defined Networks – A Comprehensive Approach, 2nd Edition, 2017, Morgan Kaufmann.

REFERENCE BOOKS

1. Behrouz A. Forouzan, Data Communications and Networking, Fourth Edition, Tata McGraw Hill, 2007.

2. James F Kurose, Keith W Ross, Computer Networking- A Top-down Approach Featuring the Internet, 7th Edition, 2017, Pearson Education.

3. Alberto Leon Garcia, Indra Widjaja, Communication Networks- Fundamental Concepts and Key Architectures, Fifth reprint 2002 , Tata McGraw Hill.

Course Title	Advanced Signal Processing				
Course Code	MEC114C	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Prerequisites: Basics of Signals and System,DSP

Course outcomes:

CO1	Understand advanced concepts and next generation networks. Analyze the effect of sampling and quantisation of signals and appraise its relevance with reference to applications	PO 3
CO2	Formulate various transform domain representations of 1D and 2D signals and demonstrate their applications with reference to practical signals	PO 3
CO3	Examine finite word length effects and design practical filters for real life	PO 3
CO4	Demonstrate the effect of sampling rate converters and design distortion free digital filter banks illustrating their applications to process real life signals.	PO 3
CO5	Analyze and choose architectures to efficiently implement the DSP systems for various applications taking into consideration the practical aspects.	PO 3

Unit I

Analysis of Discrete Time Signals: Basic elements of a DSP System – Review of Sampling and Quantisation – Sampling theorem for low pass and band pass signals, uniform and non-uniform quantization, Application of quantisation in lossy compression of signals – Lloyd Max quantizer; Fourier analysis of Continuous and Discrete time signals –Review of Fourier series and Fourier transform, Discrete Time Fourier Transform (DTFT), Discrete Fourier Transform (DFT), Interpretation of DFT Spectrum, Review of DFT properties – Convolution and correlation, Convolution of long sequences, Leakage effect, Windowing – Introduction to other transforms : Discrete Cosine Transform (DCT), Walsh Hadamard Transform (WHT), Karhunen Loeve Transform (KLT) – Applications.

Unit II

Digital Filters and Implementation: Review of FIR and IIR filter design – Notch filter– Comb filter– All pass filters – Applications – Structures for digital filter realization: Signal flow graph and block diagram representations, FIR and IIR Filter structures, Lattice structures – Finite word length effects – Fixed-point and floating-point DSP arithmetic, Effects of quantization, Scaling, Limit cycles in fixed point realizations of IIR digital filters, Limit cycles due to overflow. Quantization effect in DFT and FFT computation

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Unit III

Multirate Signals and Systems: Introduction to multirate signal processing with applications, Multirate System Fundamentals – Decimation and Interpolation, Transform domain analysis of Decimators and Interpolators, Decimation and Interpolation filters, Fractional sampling rate alteration, Practical sampling rate converter design.

Unit IV

Introduction to 2-D Signals and Systems: Polyphase decomposition and efficient structures – Introduction to digital filter banks – The DFT filter bank, Two Channel Quadrature Mirror Filter bank (QMF), Perfect Reconstruction.

Unit V

Introduction to 2-D Signals and Systems: Elementary 2D signals – Linear shift Invariant systems – Separability – 2D convolution – Introduction to 2D transforms: 2D DFT, 2D DCT, Applications.

Text Books:

1. John G. Proakis, Dimitris G. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, 4th Edition, Pearson India, 2007.
2. P.P. Vaidyanathan, Multirate systems and filter banks, 2nd Edition, Pearson Education India, 1992.
3. Lim J. S., Two-dimensional signal and image processing, Prentice Hall, 1990.

4. K Deergha Rao, M N S Swamy, Digital Signal Processing: Theory and Practice, Springer, 2018.

5. Steven W. Smith, The Scientist and Engineer's Guide to Digital Signal Processing, California, 1999.

6. Mitra S. K., Digital Signal Processing: A Computer Based Approach, McGraw-Hill Publishing Company, 2013.

Course Title	Power Converters				
Course Code	MEC114D	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Course Outcomes:

CO1	Analyse switched circuits.	PO3
CO2	Analyse single phase and three phase AC to DC converters.	PO3
CO3	Analyse and design DC to DC converters.	PO3
CO4	Analyse DC to AC converters	PO3
CO5	Analyse AC to AC converters.	PO3

Unit I

Analysis of switched circuits: thyristor controlled half wave rectifier – R, L, RL, RC load circuits, classification and analysis of commutation.

Unit II

Single-Phase and Three-Phase AC to DC converters: half controlled configurations- operating domains of three phase full converters and semi-converters – Reactive power considerations.

Unit III

Analysis and design of DC-to-DC converters: Control of DC-DC converters, Buck converters, Boost converters, Buck-Boost converters, Cuk converters.

Unit IV

Single phase and Three phase inverters: Voltage source and Current source inverters, Voltage control and harmonic minimization in inverters.

Unit V

AC to AC power conversion using voltage regulators: choppers and cyclo-converters, consideration of harmonics.

Text books:

1. Ned Mohan, Undeland and Robbin, 'Power Electronics: converters, Application and design', John Wiley and sons.Inc, Newyork, 1995.
2. Rashid M.H., 'Power Electronics Circuits, Devices and Applications ', Prentice Hall India, New Delhi, 1995.
3. P.C Sen.,' Modern Power Electronics ', Wheeler publishing Co, First Edition, New Delhi, 1998.

Course Title	Digital IC Design				
Course Code	**MEC114E**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisite:

The Metal Oxide Semiconductor (MOS) Structure, Network theory.

Course outcomes:

CO1	Analyze the existing problem of Digital ICs to arrive at suitable specifications at various levels of design	PO3
CO2	Design high performance Digital IC blocks by using various optimization techniques to meet the specification	PO3
CO3	To design and analyze complex Digital circuits, using appropriate analytical methods as well as front-end or backend tools including prediction and modelling with an understanding of the limitations.	PO3

Unit I

MOS Transistor Principles and CMOS Inverter: MOSFET characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.

Unit II

Dynamic Logic Circuits: Basic Principles of Pass Transistor Circuits, Transmission gates. Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. Charge leakage and sharing in Dynamic Logic,

Unit III

Sequential MOS Logic Circuits

Behavior of Bistable Elements, the SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, CMOS D-Latch and Edge-Triggered Flip-Flop**,** Timing Issues, Pipelines.

Unit IV

Modelling Of MOS Transistors Using SPICE: Basic Concepts. The LEVEL 1 Model Equations, The LEVEL 2 Model Equations, The LEVEL 3

Model Equations, BSIM Models, Capacitance Models, Comparison of the SPICE MOSFET Models, Typical SPICE Model Parameters. Device Characterization.

Unit V

Memory Architecture: Memory Architectures and Memory control circuits: Read Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.

Text Books

1. Sung Mo Kang & YosufL eblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.
2. Pal, Ajit, Low-Power VLSI Circuits and Systems, Springer publisher, 2015

Reference Books

1. Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design,: A Circuits and Systems Perspective, 3rd edition.

MOOCs:

1. https://archive.nptel.ac.in/courses/106/105/106105034/
2. https://www.youtube.com/watch?v=IXjNLK7GC70&list=PL3pGy4HtqwD15wr99U4CBhYqiZIwWbl12

Course Title	Data Networks					
Course Code	MEC114F	Credits	3	L-T-P	3:0:0	
CIE	50 Marks	SEE		50 Marks		

Prerequisites: Basic Networking Concepts, Wireless Communication

Course outcomes:

CO1	To develop a comprehensive understanding of wireless systems in the context of modern networks.	PO3
CO2	To learn the core concepts of sensor networks, including their architecture and protocol design.	PO3
CO3	To understand the building blocks of IoT, their characteristics, and explore various application domains of IoT.	PO3
CO3	To critically analyze current research trends in wireless networks and effectively prepare and present a technical document on the findings.	PO2

Unit I

Introduction: Importance of networking in modern communication, Overview of PAN, LAN, Basic networking concepts -topology, protocols, data transmission, Technologies and Standards- Bluetooth (IEEE 802.15.1), Zigbee (IEEE 802.15.4)

Unit II

Introduction to sensor networks: Single-node architecture - Hardware components, Energy consumption, Issues and Challenges in providing QoS, network layer solutions, QoS frameworks, need for energy management, classification, battery, transmission power, and system power management schemes, Optimization goals and figure of merit, Design principles for WSNs, Service interfaces, Gateway concepts

Unit III

MAC AND ROUTING PROTOCOLS: MAC protocols – fundamentals, low duty cycle protocols and wakeup concepts, contention and Schedule-based protocols - SMAC, BMAC, TRAMA, Routing protocols – Issues in designing a routing protocol, Classification - SPIN, Directed Diffusion, COUGAR, ACQUIRE, LEACH, PEGASIS

Unit IV

Internet of Things- Physical and Logical Design, Enabling Technologies, Reference Model and architecture, Levels and Deployment, Internet Connectivity Principles, Data Acquiring, Organising, Processing and Analytics, Privacy, Security and Vulnerabilities Solutions

Unit V

Case Study & Advanced IoT Applications: IoT applications in home automation, cities, environment, agriculture, industry, Use of Big Data and Visualization in IoT, Industry 4.0 concepts.

Text Books:

1. S. S. Manvi, M. S. Kakkasageri, “Wireles and Mobile Networks: Concepts and Protocols”, 2010, John Wiley & Sons, 2010, ISBN 8126520698, 9788126520695.
2. C. Siva Ram Murthy, and B. S. Manoj, "AdHoc Wireless networks ", Pearson Education - 2008.
3. Protocols and Architectures for Wireless Sensor Networks. Holger Karl and Andreas Willig, 2005, John Wiley & Sons, Ltd. ISBN: 0-470-09510-5]
4. INTERNET OF THINGS Architecture and Design Principles Raj Kamal Professor, Computer Science and Engineering Medi-Caps University Rau, Indore, Madhya Pradesh, India, McGraw Hill Education (India) Private

E Books:

1. “Introduction to Wireless Sensor Networks”, Anna Forster
2. “Fundamentals of Wireless Sensor Networks: Theory and Practice”,Waltenegus Dargie, Christian Poellabauer
3. “Building the Internet of Things: Implement New Business Models, Disrupt Competitors, Transform Your Industry”, Maciej Kranz

MOOC Courses:

1.Introduction to the Internet of Things, Offered by Stanford Online

2. Wireless Ad Hoc and Sensor Networks, NPTEL

Course Title	System Verilog				
Course Code	MEC115A	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Prerequisites: Basics of Digital Circuit design and Verilog

Course Outcomes:

CO1	Apply the System Verilog concepts to verify the design	PO 3
CO2	Apply constrained random tests benches using System Verilog.	PO 3
CO3	Appreciate Functional Coverage.	PO 3

Unit I

Verification Guidelines: The Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Randomization, Functional Coverage, Tet Bench Components, Layered Test Bench.

Data Types: Built-In Data Types, Fixed and Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing A Storage Type, Creating New Types With typedef, Creating User Defined Structures, Type Conversion, Enumerated Types, Constants and Strings, Expression Width.

Unit II

Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.

Connectingthe Test Bench and Design: Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions.

Unit III

Randomization: Introduction, Randomization in System Verilog, Constraint Details, Solution Probabilities, Valid Constraints, InLine Constraints, Random Number Functions, Common Randomization Problems, Random Control, Random Number Generators.

Unit IV

Threads and Inter process Communication: Working with Threads, Disabling Threads, Inter Process Communication, Events, Semaphores, Mailboxes, BuildingA Test Bench with Threads and InterProcess Communication.

Unit V

Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of Cover Group, Triggeringa CoverGroup, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, Measuring Coverage Statistics During Simulation.

Reference Books:

1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.

2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.

Course Title	Advanced Wireless Communication				
Course Code	**MEC115B**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: Basics of Communication Systems

Course outcomes:

CO1	Implement physical models of wireless channels. Gain knowledge on communication links and physical model	PO 3
CO2	Gain knowledge of key concepts of wireless communication	PO 3
CO3	Measure capacity of AWGN channel, LTI Gaussian channels and various fading channels.	PO 3
CO3	Study uplink and downlink model of AWGN channel, fading channels and multiuser diversity	PO 3

Unit I

Physical modeling for wireless channels, Input/output model of the wireless channel: Free space, fixed transmit and receive antennas, Free space, moving antenna, reflecting wall, fixed antenna, reflecting wall, moving antenna, Reflection from a ground plane, Power decay with distance and shadowing, Moving antenna, multiple reflectors, The wireless channel as a linear time-varying system, Baseband equivalent model, discrete-time baseband model, Additive white noise.

Unit II

Time and frequency coherence, AWGN channel capacity: Time and frequency coherence: Doppler spread and coherence time, delay spread and coherence bandwidth, Repetition coding, Packing spheres, Capacity-achieving AWGN channel codes, Reliable rate of communication and capacity, Resources of the AWGN channel-Continuoustime AWGN channel, Power and bandwidth, Bandwidth reuse in cellular systems.

Unit III

Linear time-invariant Gaussian channels, Capacity of fading channels: Single input multiple output (SIMO) channel, Multiple input single output (MISO) channel, Frequency-selective channel, Slow fading channel, receive diversity, Transmit diversity, Transmit and receive diversity,Time and frequency diversity, Outage for parallel channels, Fast fading channel, Transmitter side information, Frequency-selective fading channels.

Unit IV

Uplink and Downlink AWGN channel, Uplink and Downlink fading channel: Capacity via successive interference cancellation, Comparison with conventional CDMA, Comparison with orthogonal multiple access, General K-use ruplink capacity, Symmetric case: two capacity achieving schemes, General case: superposition coding achieves capacity, Slow fading channel, Fast fading channel, Full channel side information, Channel side information at receiver only, Full channel side information, Frequency selective fading channels

Unit V

Multiuser diversity, Physical Modeling of MIMO channels: Multiuser diversity gain, Multiuser versus classical diversity, Fair scheduling and multiuser diversity, Channel prediction and feedback, Opportunistic beam forming using dumb antennas, Multiuser diversity in multicell systems, Line-of- sight SIMO channel, Line-of-sight MISO channel, Antenna arrays with only a line-of-sight path, Geographically separated antennas, Line-of-sight plus one reflected path, MIMO multipath channel, Angular domain representation of signals, Angular domain representation of MIMO channels, Statistical modeling in the angular domain, Degrees of freedom and diversity, Dependency on antenna spacing.

Text Books:

1. Andrea Goldsmith, Wireless Communications, Cambridge University Press, 2005.
2. David T, Pramod Viswanath, Fundamentals of Wireless Communications, Cambridge.

Course Title	Multimedia and Applications				
Course Code	MEC115C	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Prerequisites: Basic Networking Concepts, Wireless Communication

Course outcomes:

CO1	Deploy the right multimedia communication models.	PO3
CO2	Apply QoS to multimedia network applications with efficient routing techniques.	PO3
CO3	Discuss the various standards and quality aspects of digital video formats used for multimedia application.	PO3
CO4	Solve the security threats in the multimedia networks	PO3
CO5	Develop the real-time multimedia network applications.	PO3

Unit I

Introduction: Multimedia information representation, Multimedia networks, Multimedia applications, Application and networking terminology, Network QoS and application QoS, Digitization principles, Text, images, audio and video.

Unit II

Text and image compression: Compression principles, Text compression- Run length, Huffman, LZW, Document Image compression using T2 and T3 coding, image compression- GIF, TIFF and JPEG.

Unit III

Audio and Video Compression: Audio compression – principles, DPCM, ADPCM, Adaptive and Linear Predictive coding, Code-Excited LPC, Perceptual coding, MPEG and Dolby coders video compression, Video compression principles.

Unit IV

Video Compression Standards: H.261, H.263, MPEG, MPEG 1, MPEG 2, MPEG-4 and Reversible VLCs, MPEG-7 standardization process of multimedia content description, MPEG 21 multimedia framework.

Unit V

Multimedia Networks: Basics of Multimedia Networks, Communications and Applications: Quality of Multimedia Data Transmission, Multimedia over IP, Multimedia over ATM Networks, Transport of MPEG-4, Media on Demand (MoD).

Text Books:

1. Fred Halsall, "Multimedia Communications: Applications, Networks, Protocols and Standards" Pearson Education Publishers, 2001, ISBN: 97802013981871.
2. Raif Steinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002.

Reference Books:

1. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004.
2. Hans. W. Barz, Gregory A. Bassett, "Multimedia Networks: Protocols, Design and Applications", John Wiley & Sons publications, 2016. ISBN: 9781119090137.
3. John Billamil, Louis Molina, "Multimedia: An Introduction", PHI, 2002.

Course Title	Process Control				
Course Code	**MEC115D**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Course Outcomes:

CO1	Understand the need of process control, basic principles of various manufacturing processes and apply engineering knowledge to do problem analysis in process control.	PO3
CO2	Define common dynamics of processes found in many industries and model them mathematically.	PO3
CO3	Select the proper controller and apply the tuning rules to achieve optimum performance.	PO3
CO4	Understand, interpret and implement tuning of the controllers using various methods and study about digital controllers.	PO3
CO5	Select advanced control strategy to enhance the performance.	PO2

Unit I

Introduction: Introduction to Process Control. Control objectives, servo regulatory control, and classification of process variables.

Modeling of some Chemical Process Systems: Modeling basics, Degree of Freedom, Mass Balance, Energy Balance equations, linearization of nonlinear systems, Modeling of Level Tank System, Continuous Stirred Tank Heater, Continuous Stirred Tank Reactor, Transfer function.

Unit II

Elements of Process Control: Dead time, Interacting and non-interacting systems, self-regulation, inverse response, capacity of process, integrating systems, multi-capacity process.

Process Identification: Dynamic behavior of first and second order processes, Obtaining First Order Plus Time Delay (FOPTD) model with Process Reaction curve. Obtaining second order model of processes. RB.

Unit III

Common Controller Modes: Controller Modes, ON OFF, Multi position, time proportional controller, Theory Proportional, Integral and Derivative modes, PI, PD, PID Controller, Electronics Controller implementation, Dynamic Behavior of closed loop systems with P, I, D, PI , PID modes.

Unit IV

Discretisation and Implementation Issues: Discrete time control mode realization. Velocity and Position algorithm of PID control. Integral windup, anti-windup systems, controller bias, bumps less transfer.

Tuning of Controllers: Application and tuning, ZN Tuning (Open loop and Closed loop), Performance criteria, Integral criteria.

Unit V

Some Advance Control Techniques: Cascade Control, Feed forward Control, ratio Control, Air Fuel Ratio Control for Drum Boilers. Level Control in Drum Boiler, Shrinking and Swelling, Inverse response of Drum Boiler.

Text books:

1. G. Stephanopolous, “Chemical Process Control An Introduction to Theory and Practice”, Prentice Hall India, August 2000.
2. Surekha Bhanot, “Process Control Principles and Applications”, Oxford, 2008
3. C.D. Johnson, “Process Control Instrumentation Technology”, Prentice Hall India.
4. Thomas Marlin, “Process Control Designing Processes and Control for Dynamic Performance”, Tata MC Graw Hill, 2012.
5. F.G. Shinskey, “Process Control Systems Application Design and Adjustment” 3rd editionn, McGraw Hill International
6. D. E. Seborg, T.F. Edgar, D. A. Mellichamp, “Process Dynamics and Control”, Wiley, 2004.

Course Title	Static Timing Analysis				
Course Code	MEC115E	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Prerequisites:
Courses on Digital circuit design, knowledge about combinational circuits, synchronous and asynchronous circuits. Courses on Semiconductor devices characteristics

Course outcomes:

CO1	**Apply** the learnt basic concepts of STA to evaluate the delay of the circuits and **analyse** the generated report to identify critical issues and bottleneck for the violation and **suggest** the techniques to make the design to meet timing	PO3
CO2	**Write** their own constraint file and create the environment required for the given design and its specification to undergo for **analysis using the EDA tool.**	PO2,3
CO3	Understand the **journal research papers related to Timing analysis techniques** and able to present suitable techniques for the given design.	PO1,3

Unit I
Introduction: Basics of timing concepts
Delay Concepts for Digital Designing: Types of Delays in Digital Circuits, Different Cause for Delay
Timing parameters of digital circuits: Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design, Clock Concepts

Unit II
Resources for Static Timing Analysis Flow: Libraries, Netlist, Parasitics for Delay Calculation: Device Parasitics, Interconnects, Parasitics Extraction Formats, linear v/s. non-linear delay model. Wire load models, wire load modes, Delay calculations of different wire load models

Unit III

Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries, Crosstalk Effect on Timing Analysis, Strategy of Crosstalk on Nanometre Design: Cause for Crosstalk on Integrated Circuits, Crosstalk Prevention Methods.

Unit IV

Constraints for STA: Clock Constraints, Other Timing Constraints, 5.2.2 External Delays of DUA, Timing Exceptions: Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate

Unit V

Timing Violations and Verification: Slack, Critical Path of Timing Report, Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Recovery and Removal Violation Check, Input / Output Timing Path Checks ,DRC Violation Check ,Multi Speed Clock Domain, Crosstalk Checks, Techniques to Fix Timing Violation: Techniques to Fix Setup Violations, Techniques to Fix Hold Violations

Text Books:

1. "Static Timing Analysis for VLSI circuits", R. Jayagowri, Pushpendra S. Yadav, MEDTECH, A Division of Scientific International, 2020.

Reference Book:

1. "Static Timing Analysis for Nanometer Designs: A Practical Approach", J. Bhasker, R. Chadha, Springer, 2009.

MOOC/ NPTEL courses:

1. https://nptel.ac.in/courses/106/102/106102181/ NOC: synthesis of digital systems.

Course Title	Advanced Digital Communications				
Course Code	**MEC115F**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: Course in Digital communications and signal processing in undergraduate level

Course outcomes:

CO1	Use the scholarly knowledge to analyse digital modulation and demodulation techniques, channel coding, decoding techniques.	PO 3
CO2	Comprehend the performance of bandlimited channels, fading in multipath channels and use of equalisers, diversity and spread spectrum to combat the channel effects	PO 3
CO3	Perform a study on one advanced topic related to trends in digital communications through journal papers and Prepare a technical document for presentation of the study.	PO 1,2

Unit I

Representation of digitally modulated signals in constellation, Bandwidth efficient and power efficient Modulation Schemes - PAM, QPSK, MQAM, and their PSD, Vector and AWGN Channels, Signal space concepts, Optimum coherent receivers for Gaussian channels and their performance evaluation through BER.

Unit II

Linear block codes encoding and syndrome decoding. Convolutional codes - encoding and Viterbi Decoding of convolutional codes.Introduction to turbo codes and LDPC codes.

Unit III

Fading –Statistical characterization of multipath channels –Large scale, small scale; Delay and Doppler spread, classification of multipath channels and channel models, Binary signalling over frequency non-selective Rayleigh fading channel.

Unit IV

Analysis of signalling through band limited linear filter channels, Linear Equalizers- Zero forcing Equalizer, MSE and MMSE, Decision feedback equalisers.

Analysis of Fading channels-Introduction to Diversity, Multi-antenna system, Maximal Ratio Combiner.

Unit V

Spread spectrum: DSSS with BPSK, processing gain and Jamming margin. Introduction to Multicarrier Modulation and Cyclic Prefix, OFDM – modulation and demodulation, PAPR, Frequency and Timing Offset Issues.

Text books

J.G.Proakis, Digital Communication (4/e), McGraw- Hill, 2001

S.Haykin, Communication Systems (4/e), Wiley,2001.

B. Sklar, Digital Communications: Fundamentals and Applications, 2/e, Prentice Hall,2001.

e-learning: MOOCS/NPTEL lectures on Advanced digital communication course

Course Title	**Advanced Machine Learning and Deep Learning Lab**				
Course Code	**MECL116A**	**Credits**	**2**	**L-T-P**	**0:0:2**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: Basic of AI and ML

Course outcomes:

CO1	To apply theoretical knowledge to practical scenarios.	PO 3
CO2	To gain proficiency in implementing machine learning algorithms.	PO 3
CO3	To analyse real-world problems and develop appropriate solutions.	PO 3

Sl.No.	Experiments
1	Implement multivariate linear regression.
2	Implementing Decision tree Classification.
3	Implement K-means clustering algorithm
4	Write a program for Gradient Descent Learning.
5	Implement Bidirectional Recurrent neural network
6	Implementation of Natural Language Processing.
7	Implementation of Speech Recognition
8	Case study- Convolutional Neural Networks.
	Demonstration Experiments
9	Visualizing linear regression: Use a physical model or software to demonstrate how a line fits to data points.
10	Overfitting and underfitting: Demonstrate the effects of overfitting and underfitting using simple datasets.
11	Convolution operation: Visualize the convolution process using image patches.
12	Language modelling: Generate text using a simple RNN model.

Course Title	Electronics and Communication Lab				
Course Code	**MECL116B**	**Credits**	**2**	**L-T-P**	**0:0:2**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: Basic of Analog circuits and Communication Systems

Course outcomes:

CO1	To apply theoretical knowledge to practical scenarios	PO 3
CO2	To design and analyseanalog and mixed-signal circuits.	PO 3
CO3	To implement and evaluate timing and oscillation circuits.	PO 3
CO4	To analyse and implement communication systems.	PO 3

Sl.No.	Experiments
	Part - A
1	Design a Two-Stage direct coupled Differential Amplifier with series voltage Negative Feedback of β=50.
2	Design a Voltage regulator using operational amplifier to produce output of 12V with maximum load current of 50mA.
3	Design a Two-stage CS Amplifier with overall gain of 100. Plot the frequency response and estimate the Bandwidth and Q factor.
4	Design a Darlington Emitter follower using MOSFET/BJT with and without bootstrap; plot the frequency response. Also calculate gain and bandwidth.
5	Design and realize:i) Four-bit weighted R – 2R ladder DAC. ii) Two-bit Flash ADC using Op-amp.
6	Design and verify an IC 555 timer-based pulse generator for the specified pulse of 2ms.
7	Using IC NE 566 Voltage Controlled Oscillator, design a circuit to generate square and triangular waveform with a time period of 0.2ms.
	Part - B
	Demonstration Experiments
8	Design a radio receiver for a given frequency (88 to 108 MHz) and measure the sensitivity, selectivity, and fidelity of the same.
9	Generate PAM and PDM signals for a pulse duration of 10 msec using IC 555 Timer.

10	Implement an AM and FM systems and measure its noise figure.
11	Consider the bit sequence of length 10,000. Modulate it with BPSK, BASK, BFSK. Transmit the signal through AWGN channel. Vary the SNR. Compare the theoretical and simulated probability of error.
12	Design and implement the Adaptive delta modulation and demodulation.

Course Title	Digital System Design Lab				
Course Code	**MECL116C**	**Credits**	**2**	**L-T-P**	**0:0:2**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: Basic of Digital Circuit System

Course outcomes:

CO1	Able to design and simulate VLSI circuits by selecting suitable tools fromthe industry standard EDA tools and suitable technology nodes, by writing programs as well as transistor level schematics.	PO3
CO2	Able to use different techniques to improve the performance of the given circuit and verify them	PO3
CO3	Able to submit a report of the experiments conducted on EDA tool	PO2

Sl. No	Experiments
	Part - A
1	Write Verilog code for the design of 8-bit Ripple Carry Adder.
2	Write Verilog code for the design of 8-bit Carry Look Ahead adder.
3	Write a Verilog code for the design of 8-bit Booth’s multiplier.
4	Write a Verilog code to design a 8-bit Magnitude comparator
5	Write a Verilog code to design a 4-bit universal shift register
6	Write a Verilog code to design 8-bit parity generator
7	Design and develop a Verilog code for a dual port, 4k x 32-bit flow through SSRAM (Synchronous Static Random-Access Memory), and one port allows data to be written & read, while the other port allows only data to be read.

8	Design and develop a Verilog model for an accumulator that calculates the sum of sequence of fixed-point numbers. Each input number is signed with 6 pre-binary-point and 12 post binary-point bits. The accumulated sum has 8 pre-binary-point and 12 post-binary-point bits. A new number arrives at the input during a clock cycle when data_en control input is '1'. The accumulated sum is cleared to '0' when the rest counter input is '1', Both control inputs are synchronous.
	PART-B
9	1. For the following NMOS transistor, 45nm process devices, (1) nmos1v – 1.2 volt nominal VT, (2)nmos1v_hvt – 1.2 volt high VT, (3) nmos1v_lvt – 1.2 volt low VT, a. Input Characteristics Analysis a) Plot and analyze ID v/s. VGS at different drain voltages. Determine Vt. b. Plot log ID vs. VGS at particular gate voltage (high), determine IOFF and sub-threshold slope. c. Output Characteristics Analysis a) Plot ID vs. VDS at different gate voltages, determine Channel Length modulation factor. b) Plot ID vs. VDS at different drain voltages. plot DC load line and calculate gm, gds ,gm/gds .
10	For the following devices, NMOS transistor and PMOS transistor, 45nm process, (1) nmos1v – 1.2 volt nominal VT , pmos1v – 1.2 volt nominal VT (2) nmos1v_hvt – 1.2 volt high VT, pmos1v_hvt – 1.2 volt high VT (3) nmos1v_lvt – 1.2 volt low VT, pmos1v_lvt – 1.2 volt low VT. a. Perform the following experiment ,Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine Transition voltage. Calculate VIL , VIH, NMH, NML for the inverter. Plot VTC for CMOS inverter with varying VDD.Plot VTC for CMOS inverter with varying device ratio. b. Perform transient analysis of CMOS inverter with no load and with load and determine tpHL , tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF) c. Perform AC analysis of CMOS inverter with fan-out 0 and fan-out 1. (Use Cin= 0.012pF, Cload = 4 PF, Rload = k) d. Calculate switching and leakage power dissipation with nominal VT, high VT, low VT and compare them.

11	3. Perform Power analysis for the following Low voltage low power logic circuits. (1) XOR/ XNOR gate using Full static CMOS. (2) XOR/ XNOR implementation of the CPL (Complementary Pass transistor Logic). (3) XOR/ XNOR implementation of the CPL with PMOS feedback. (4) XOR/ XNOR implementation of Double Pass transistor Logic (DPL). (5) XOR/ XNOR implementation of Domino logic style.

Second Semester Syllabus

Course Title	Antenna Theory and Design				
Course Code	**MLEL201**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: Fundamentals of time-varying fields, Microwave Engineering

Course Outcomes:

CO1	Acquire knowledge in antenna parameters and radiating systems	PO 1
CO2	Ability to identify, analyse and implement different types of antennas	PO 1
CO3	Ability to design and characterize antennas using commercial full-wave solver	PO 3
CO4	Design, simulate, fabricate and experimentally characterize antenna for given technical specifications	PO 1,2

Unit 1

Antenna Fundamentals and Definitions: Radiation Mechanisms, Overview, EM Fundamentals, Solution of Maxwell's Equations for Radiation Problems, Ideal Dipole, Radiation patterns, Directivity and Gain, Antenna impedance, Radiation efficiency, Antenna polarization

Unit 2

Arrays: Array factor for linear arrays, Uniformly excited equally spaced linear arrays, Pattern multiplication, Directivity of linear arrays, Non uniformly excited equally spaced linear arrays, Mutual coupling.

Antenna Synthesis: Formulation of the synthesis problem, Synthesis principles, Line sources shaped beam synthesis, Linear array shaped beam synthesis, Fourier series, Woodward - Lawson sampling method, Comparison of shaped beam synthesis methods, low side lobe narrow main beam synthesis methods, Dolph Chebyshev linear array, Taylor line source method.

Unit 3

Resonant Antennas: Wires and Patches, Dipole antenna, Yagi-Uda antennas, Micro-strip antenna.

Broadband antennas: Traveling wave antennas Helical antennas, Biconical antennas, Sleeve antennas, and Principles of frequency independent antennas, Spiral antennas, and Log - periodic antennas

Unit 4

Aperture antennas: Techniques for evaluating gain, Reflector antennas, Parabolic reflector antenna principles, Axi-symmetric parabolic reflector antenna, offset parabolic reflectors, Dual reflector antennas, Gain calculations for reflector antennas, Feed antennas for reflectors, Field representations, Matching the feed to the reflector, General feed model, Feed antennas used in practice.

Unit 5

Antenna in systems & Measurements: Receiving properties of antennas, Antenna temperature &

radiometry. CEM for antennas: The method of moments: Introduction of the methods moments, Pocklington's integral equation, Integral equation and Kirchhoff's networking equations, Source modeling weighted residual formulations and computational consideration, Calculation of antenna and scatter characteristics

Text Books:

1. 'Antenna Theory and Design', Stutzman and Thiele, John Wiley, 2nd Edition, 2010

Reference Books:

1. 'Antenna Theory Analysis and Design', C. A. Balanis, John Wiley, 2nd Edition, 2007
2. 'Antennas and Wave Propagation', J. D. Krauss, McGraw Hill TMH, 4th Edition, 2010

'Antennas and propagation', A.R.Harish, M.Sachidanada, Pearson Education, 2015

Course Title	Real Time Operating Systems				
Course Code	MLEL204	Credits	4	L-T-P	3:0:1
CIE	50 Marks	SEE		50 Marks	

Course outcomes:

CO1	Design high performance software applications with real time deterministic response.	PO3
CO2	Configure and Optimize Embedded RTOS to achieve desired High Performance Computing response.	PO3
CO3	Make an effective oral presentation pertaining to RTOS and related high performance computing concepts.	PO2
CO4	Engage on Literature survey about High Performance & Deterministic systems, both from hardware and software perspective and submit a report	PO1

Unit I

Basic concepts of RTOS: Defining RTOS, characteristics of RTOS, objects and services, real time scheduling approaches, Library-Based RTOS (Kernel-less approach), monolithic kernels, microkernels, virtual machines.

Unit II

RTOS objects: Tasks and task states, Semaphores: need, types, typical operations, mutual exclusion, priority inversion avoidance.

Queues: States, typical operations, non-interlocked one-way data communication, no-interlocked and interlocked two-way data communication, broadcast data communication, Queues within an Interrupt Service Routine.

Unit III

RTOS objects:

Critical Sections and Resource Management, **Pipes:** Pipe states, pipe control blocks, typical operations, uses of pipes

Unit IV

RTOS services: TCP/IP communication, client server model, sockets and ports, exception handling, interrupt mechanism

Unit V

Comparison of available RTOS, Selection criteria of an RTOS for an IoT application

Application implementation: Process of designing firmware, boot loader, device drivers, developing interface code for module developed for any hardware: C program-based application layer code and kernel level code to configure and access data in/out of any chosen hardware.

Text Books:

Reference Books:

- Embedded and real time operating systems by Wang, K.C., Springer 2017, ISBN-10 : 3319515160 and ISBN-13 : 9783319515168
- Real-Time Concepts for Embedded Systems by Qing Li and CarolynYaoISBN:1578201241
  CMP Books
  NPTEL lectures on 'Real Time Systems'
- Mastering embedded Linux programming by Chris Simmonds Publisher: Packt Publishing, 2017 ISBN: 9781787283282**OR**
- Using the free RTOS Real Time Kernel by Richard Barry, http://www.FreeRTOS.org

Lab exercises: (Can be implemented using any RTOS and any hardware)

1. Create a task control block using suitable datatypes. Have this as a header file for all scheduling programs.
2. Write C/C++ programs for realizing FCFS or Round Robin scheme.
3. Write C/C++ programs for realizing any priority driven approach.
4. Download Free RTOS and Visual Studio, run a sample program to verify the working.
5. WAP with arguments for main() and verify the working.
6. Create header files for exception handling, include in user program and execute.
7. Write an algorithm for rate monotonic scheduling and verify the working. Create 4 tasks as follows: In version 1 do not include deadline. Compare

the complexity after including deadline in version 2 and compile the analysis.

Task #	Arrival time (ms)	Execution time (ms)	Deadline (ms)
1	0	4	6
2	2	2	5
3	4	1	6
4	5	5	10

8. Write an algorithm for Earliest Dead time First (EDF) and verify the working for the above task table.

To be executed on ARM cortex boards (Supplied by Bosch) and code warrior studio / RPi with QNX / LPC Arm boards with threadX / FreeRTOS

Use the features of RTOS available and program: LED, relay, sensor-ADC, LCD to realize a RT application. Use interrupt handling concepts in your application. Demonstrate how priorities can be varied?

Course Title	Low Power VLSI Design				
Course Code	**MLEL205**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: CMOS VLSI Design

Course outcomes:

CO1	Extend the knowledge on basics of MOSFETs and Power Dissipation inMOS circuits to obtain the concepts of different techniques for power optimization.	PO3
CO2	Ability to analyze various techniques to minimize power dissipation during the design at different levels of abstraction.	PO3
CO3	Ability to design the power optimised circuit for the given specification	PO3
CO4	Design low power circuits using EDA tools and demonstrate the design with report	PO1,2

Unit-I

Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. Simulation power analysis: SPICE circuit simulation, Monte Carlo simulation.

Unit-II

Supply Voltage Scaling Approaches: Device feature size scaling Multi-Vdd Circuits Architectural level approaches: Parallelism, Pipelining Voltage scaling using high-level transformations Dynamic voltage scaling Power Management Clock Gating Logic styles

Unit-III

Circuit and Logic: Transistor and Gate Sizing, Equivalent Pin Ordering, Signal Encoding, Logic Encoding, State Machine Encoding, pre-computation logic, Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus

Unit-IV

Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-V_t assignment approach

(DTCMOS)

Unit-V

Advanced Techniques: Adiabatic Computation, Asynchronous circuits. Battery-Driven System Design, Energy Aware Routing, Variation tolerant design, CAD tools for low power synthesis

Text books:

1. "CMOS VLSI Design: A Circuits and Systems Perspective", Neil H. E Weste and David Harris, Pearson Education, 4th edition, 2011,ISBN: 0-321-54774-8.
2. "Practical Low Power Digital VLSI Design", Gary Yeap, Kluwer Academic Publishers, 1998.
3. "Low Power VLSI Circuits and Systems", Ajit Pal, Springer, 2015. ISBN 978-81-322-1936-1.
4. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata Mcgrag Hill.
5. A. Bellamour, and M. I. Elmasri, Low Power VLSI CMOS Circuit Design, KluwerAcademic Press, 1995.

Reference Books:

1. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.
2. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Inter science, 2000.
3. Kiat-Seng Yeo and Kaushik Roy, Mc-Graw-Hill Low-Voltage Low-Power CMOS VLSI Subsystems, 2005

E-Book:

1. http://leda.elfak.ni.ac.rs/education/projectovanjeVLSI/predavanja/10%20Low%20Power%20Design%20in%20VLSI.pdf

MOOC/Online course:

1. NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering ,IIT Kharagpur

Course Title	VLSI Testing and Verification				
Course Code	**MLEL206**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Course outcomes:

CO1	To study Faults in digital circuits & to learn various algorithms for test generation of Combinational Logic Circuits	PO3
CO2	To study the approach to deal with the testing problems at the chip level (BIST).	PO3
CO3	Engage on Literature survey and make an effort to suggest new solution as a team in VLSI Testing.	PO1,2
CO4	To know about Design Verification Concepts	PO3

Unit I

Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits (One-Dimensional Path Sensitization, Boolean Difference, D-Algorithm).

Unit II

Test generation for Combinational Logic circuits: Test generation techniques for combinational circuits (PODEM, FAN, Delay Fault Detection), Detection of multiple faults in Combinational logic circuits.

Unit III

Design of testable sequential circuits: Controllability and Observability, High Level Testability Measures (SCOAP measures), scan-path technique for testable sequential circuit design, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits.

Unit IV

Built-In Self-Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures, Memory BIST

Advances in DFT: Test Compression Introduction, Stimulus compression, Response compression

Unit V

Design Verification: What is design verification? The basic verification principle, Verification methodology, Simulation-based verification versus formal verification

Coding for Verification: Assertions, Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification: Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

Text Books:

1) Lala Parag K,“Digital Circuit Testing and Testability”,NewYork,AcademicPress1997.

2) Abramovici M, Breuer MA, “Digital Systems Testing and Testable Design and Friedman AD”, Wiley1994.

3)William K. Lam,“Hardware Design Verification: Simulation and Formal Method Based Approaches”, Prentice Hall PTR,2005.

4)Vishwani D Agarwal,“Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits”, Springer, 2002

E-Resources:

- https://www.youtube.com/watch?v=O5lyBoWR-PA&list=PLx98Qgh5zPjh6oWI73QfQHZAmAiyt8Wkf
- https://www.youtube.com/watch?v=Abld-fSxjNM&list=PLbMVogVj5nJTClnafWQ9FK2nt3cGG8kCF
- https://www.youtube.com/watch?v=MEaMm423t0w&list=PLZjlBaHNchvOFBWBAtAP9exwQgYpKqsO4& index=1

Course Title	CMOS RF Circuit Design				
Course Code	MLEL215A	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Course outcomes:

CO1	Analyse the effect of nonlinearity and noise in RF and microwave design.	PO3
CO2	Exemplify the approaches taken in actual RF products.	PO3
CO3	Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.	PO3
CO4	Explain various receivers and transmitter topologies with their merits and drawbacks.	PO3
CO5	Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance	PO3

Unit I

Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion.

Unit II

Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.

Unit III

Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

Unit IV

Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.

Unit V

VCO and PLLs- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design.

REFERENCE BOOKS

1. B. Razavi, "RF Microelectronics" second edition, PHI
2. R. Jacob Baker, H.W. Li, D.E. Boyce, "CMOS Circuit Design, layout and Simulation" PHI 1998
3. Thomas H. Lee, "Design of CMOS RF Integrated Circuits" Cambridge University press 1998 Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology" , TMH 19962.

E-Resources:

1. https://nptel.ac.in/courses/108106105.
2. https://www.youtube.com/watch?v=T0Kbt7CcqUA&list=PLQorUaRee4 AEeyuqnpysZcGT4FFgR d kuM

Course Title	Statistical Signal Processing				
Course Code	**MLEL215B**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Course outcomes:

CO1	Design statistical DSP algorithms to meet desired needs	PO3
CO2	Apply vector space methods to statistical signal processing problems	PO3
CO3	Identify the engineering problems that can be put in to the frame of statistical signal processing	PO3
CO4	Understand Wiener filter theory and design discrete and continuous Wiener filters	PO3
CO5	Understand Kalman Filter theory and design discrete Kalman filters	PO3

Unit I

Random Processes: Random variables, random processes, white noise, filtering random processes, spectral factorization, ARMA, AR and MA processes.

Unit II

Signal Modeling: Least squares method, Pade approximation, Prony's method, finite data records, stochastic models, Levinson- Durbin recursion; Schur recursion; Levinson recursion.

Unit III

Spectrum Estimation: Nonparametric methods, minimum-variance spectrum estimation, maximum entropy method, parametric methods, frequency estimation, principal components spectrum estimation

Unit IV

Optimal and Adaptive Filtering: FIR and IIR Wiener filters, Discrete Kalman filter,

FIR Adaptive filters: Steepest descent, LMS, LMS-based algorithms, adaptive recursive filters, RLS algorithms

Unit V

Array Processing: Array fundamentals, beam-forming, optimum array processing, performance considerations, adaptive beam-forming, linearly constrained minimum-variance beam-formers, side-lobe cancellers.

Text books:

1. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley & Sons(Asia)Pvt. Ltd.,2002.
2. Dimitris G. Manolakis, Vinay K. Ingle, and Stephen M. Kogon,"Statistical and Adaptive Signal Processing: SpectralEstimation, Signal Modeling, Adaptive Filtering and Array Processing”, McGraw-Hill International Edition,2000.

E-Resources:

1. https://www.youtube.com/playlist?list=PLwdnzlV3ogoVj-FLNpzXInhZxcnibqb56
2. https://onlinecourses.nptel.ac.in/noc20_ee53/preview
3. https://archive.nptel.ac.in/course

Course Title	Probability and Random Process				
Course Code	MLEL215C	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Course outcomes:

CO1	Understand Discrete and Continuous Random variables, Random Processes and their applications in Electronic Transmissions	PO3
CO2	To apply concepts of Probability to solve problems in Communication Engineering.	PO3
CO3	To find functional relationship between random inputs and outputs with the use of Random Process Techniques	PO3
CO4	Analyse about the correlation Functions	PO3

Unit I

Probability and Random Variable Probability: Set theory, Experiments and Sample Spaces, Discrete and Continuous Sample Spaces, Events, Probability Definitions and Axioms, Mathematical Model of Experiments, Joint Probability, Conditional Probability, Total Probability,
Bayes 'Theorem, and Independent Events, Bernoulli 's trials. The Random Variable: Definition of a Random Variable, Conditions for a Function to be a Random Variable, Discrete and Continuous, Mixed Random Variable.

Unit II

Distribution and density functions and Operations on One Random Variable Distribution and density functions: Distribution and Density functions, Properties, Binomial, Poisson, Uniform, Exponential Gaussian, Rayleigh and Conditional Distribution, Methods of defining Conditioning Event, Conditional Density function and its properties, problems. **Operation on One Random Variable:** Expected value of a random variable, function of a random variable, moments about the origin, central moments, variance and skew, characteristic function, moment generating function, transformations of a random variable, monotonic transformations for a continuous random variable, non-monotonic. Transformations of continuous random variable, Transformations of Discrete random variable.

Unit III

Multiple Random Variables and Operations on Multiple Random Variables Multiple Random Variables: Vector Random Variables, Joint Distribution Function and Properties, Joint density Function and Properties, Marginal Distribution and density Functions, conditional Distribution and density Functions, Statistical Independence, Distribution and density functions of Sum of Two Random Variables and Sum of Several Random Variables, Central Limit Theorem- Unequal Distribution,

Equal Distributions Operations on Multiple Random Variables: Expected Value of a Function of Random Variables, Joint Moments about the Origin, Joint Central Moments, Joint Characteristic Functions, and

Jointly Gaussian Random Variables: Two Random Variables case and N Random Variable case, Properties, Transformations of Multiple Random Variables.

Unit IV

Stochastic Processes Temporal Characteristics: The Stochastic process Concept, Classification of Processes, Deterministic and Nondeterministic Processes, Distribution and Density Functions, **Statistical Independence and concept of Stationarity:** First-Order Stationary Processes, Second Order and Wide- Sense Stationarity, Nth-Order and Strict Sense Stationarity, Time Averages and 1Ergodicity,Mean-Ergodic Processes, Correlation-Ergodic Processes Autocorrelation Function and Its Properties, Cross-Correlation Function and Its Properties, Covariance Functions and its properties, Gaussian Random Processes.

Linear system Response: Mean and Mean-squared value, Autocorrelation, Cross-Correlation Functions.

Unit V

Stochastic Processes-Spectral Characteristics: The Power Spectrum and its

Properties, Relationship between Power Spectrum and Autocorrelation Function, the Cross-Power Density Spectrum and Properties, Relationship between Cross-Power Spectrum and Cross-Correlation Function.

Spectral characteristics of system response: power density spectrum of response, cross power spectral density of input and output of a linear system.

Text Books:

1. Probability, Random Variables & Random Signal Principles -Peyton Z.Peebles, TMH, 4thEdition, 2001.
2. Probability and Random Processes-Scott Miller, DonaldChilders,2nd Edn, Elsevier,2012

E-Resources:

1. https://archive.nptel.ac.in/courses/117/105/117105085/
2. https://www.youtube.com/watch?v=p6lze5nPkzk
3. https://www.youtube.com/watch?v=C3srT7bVJrs

Course Title	Simulation, Modelling and Analysis				
Course Code	**MLEL215D**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Course outcomes:

CO1	Describe the role of important elements of discrete event simulation and modeling paradigm	PO3
CO2	Conceptualize real world situations related to systems development decisions, originating from source requirements and goals.	PO3
CO3	Develop skills to apply simulation software to construct and execute goal driven system models..	PO3
CO4	Interpret the model and apply the results to resolve critical issues in a real world environment.	PO3

Unit I

Basic Simulation Modeling: Nature of simulation, Systems, Models and Simulation, Discrete-Event Simulation, Simulation of Single Server Queuing System, Simulation of inventory system, Parallel and distributed simulation and the high level architecture, Steps in sound simulation study, and Other types of simulation, Advantages and disadvantages.

Unit II

Review of Basic Probability and Statistics: Random Variables and their properties, Simulation Output Data and Stochastic Processes, Estimation of Means, Variances and Correlations, Confidence Intervals and Hypothesis tests for the Mean.

Building valid, credible and appropriately detailed simulation models: Introduction and definitions, Guidelines for determining the level of models detail, Management's Role in the Simulation Process, Techniques for increasing model validity and credibility, Statistical procedure for comparing the real world observations and simulation output data.

Unit III

Selecting Input Probability Distributions: Useful probability distributions, activity I, II and III. Shifted and truncated distributions; Specifying multivariate distribution, correlations, and stochastic processes; Selecting the distribution in the absence of data, Models of arrival process.

Unit IV

Random Number Generators: Linear congruential Generators, Other kinds, Testing number generators, **Generating the Random Variates:** General approaches, generating continuous random variates, generating discrete random variates, generating random vectors, and correlated random variates; Generating arrival processes

Unit V

Output data analysis for a single system: Transient and steady state behavior of a stochastic process; Types of simulations with regard to analysis; Statistical analysis for terminating simulation; Statistical analysis for steady state parameters; Statistical analysis for steady state cycle parameters; Multiple measures of performance, Time plots of important variables.

Text Books:

1. AverillLaw,"Simulationmodelingandanalysis",McGrawHill4thedition,2007.

Reference Books:

1. TayfurAltiok and Benjamin Melamed, “Simulation modeling and analysis with ARENA”,Elsevier, Academicpress, 2007.
2. Jerry Banks," Discrete event system Simulation", Pearson,2009
3. SeilaCericandTadikamalla,"Appliedsimulationmodeling",Cengage,2009.
4. George.S.Fishman,"Discreteevent simulation",Springer,2001.
5. FrankL. Severance," System modeling and simulation", Wiley, 2009.

E-Resources:

1. https://www.youtube.com/watch?v=X4q-a2dqnBM
2. https://ocw.mit.edu/courses/3-021j-introduction-to-modeling-and-simulation-spring-2012/
3. https://archive.nptel.ac.in/courses/112/107/112107220/
4. https://archive.nptel.ac.in/courses/112/

Course Title	Scripting Languages				
Course Code	MLEL215E	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Prerequisites:
Fundamentals of command line interface in windows/Linux/Unix Environments, Basic Programming skills.

Course Outcomes:

CO1	Understand, Analyse and execute scripts for automation of tool commands in CAD tools	PO3
CO2	Create and execute scripts using Bash/Perl/TCL/Python and automate CAD design flow and design verification flow on open-source tools	PO3

Unit I
Linux Fundamentals & Bash Scripting
Overview of Linux: File system structure, shell environment, permissions, and process management. Essential Linux commands for VLSI workflows. Shell scripting basics and automation using cron jobs.

Unit II
Make file and Build Automation
Make file basics: Structure, targets, dependencies, and automation. Automating RTL compilation, simulation, and verification.

Unit III
Tcl Scripting for EDA Tools
Tcl scripting fundamentals: Syntax, commands, variables, loops, procedures, and lists. Tcl for EDA Tools: Scripting for **Synthesis** (Synopsys DC, Cadence Genus, Xilinx Vivado). Automating **Static Timing Analysis (STA)** using **PrimeTime.** Simulation automation with **ModelSim, VCS.**

Unit IV
Perl & Python for Automation
Perl scripting: Data handling, pattern matching, and automation. Parsing ASIC/FPGA simulation logs and design reports. Python scripting: Basics of

Python programming for VLSI automation, data handling using **NumPy, Pandas**, and interfacing with hardware using **pySerial**.

Unit V
EDA Tool Integration & Version Control
Automation of ASIC/FPGA flows: Synthesis, simulation, and verification. EDA Tool Integration using scripting for enhanced design productivity.
Case Studies:
Automating Verilog simulation using **Icarus Verilog and Verilator**.
Python for **post-processing ASIC simulation and timing reports**.
Version Control Systems:
Perforce (P4) / CVS – Repository management, branching, and version control in ASIC/FPGA development.**Git** – Workflow, branching strategies, and industry best practices.

Text Books:

1. **Bash Guide for Beginners** – Machtelt Garrels
   Link: https://tldp.org/LDP/Bash-Beginners-Guide/html/index.html
2. **Practical Programming in Tcl and Tk** – Brent B. Welch
   Link: https://www.beedub.com/book/
3. **Beginning Perl** – Simon Cozens
   Link: https://www.perl.org/books/beginning-perl/
4. **Automating System Administration with Perl** – David N. Blank-Edelman**Link:** https://www.oreilly.com/openbook/automating/
5. **Dive Into Python 3** – Mark Pilgrim
   Link: https://diveintopython3.problemsolving.io/

Reference Books:

1. **Bash Reference Manual**
   Link: https://www.gnu.org/software/bash/manual/bash.html
2. **Perl Documentation**
   Link: https://perldoc.perl.org/
3. **GNU Make Manual**
   Link: https://www.gnu.org/software/make/manual/make.html
4. **Tcl/Tk Documentation**
   Link: https://www.tcl.tk/doc/
5. **Pro Git** – Scott Chacon and Ben Straub
   Link: https://git-scm.com/book/en/v2

Course Title	Mechatronics				
Course Code	MLEL216A	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Course Outcomes:

CO1	Explain the basics of Mechatronics and its design approach.	PO3
CO2	Explain the operation and applications of various sensors	PO3
CO3	Explain and discuss the operation of various actuators and their applications in systems.	PO3
CO4	Explain and discuss the concepts of logic design, computer communication networks and Fault diagnosis and Analysis in Mechatronic Systems.	PO3
CO5	Explain and discuss the concepts of data acquisition, software design and development.	PO3

Unit I

Overview of mechatronics: What is Mechatronics? Integrated Mechatronic Design Approach, System Interfacing, Embedded Systems, Instrumentation and Control Systems, Open and closed loop systems, importance of feedback systems, transfer function, Microprocessor Based Controllers and Microelectronics. An Introduction to Micro-technology and Nanotechnology, Mechatronics: Miniaturized, Examples and applications.

Unit II

Sensors and application: Introduction to Sensors, Classification of sensors, Sensor – Static and Dynamic Characteristics, Sensors, Linear and Rotational Sensors, Acceleration Sensors, Force Measurement, Torque and Power Measurement, Flow Measurement, Temperature Measurements, Distance Measuring and Proximity Sensors, Light Detection, Use of RF, Infra-Red sensors in automobiles, Micro-sensors.

Unit III

Actuators: Introduction to Actuators – Mechanical, Electrical and combinational actuators, Electromechanical Actuators, Electrical Machines, Piezoelectric Actuators, Hydraulic and Pneumatic Actuation Systems, Applications of few types of actuators in automobiles.

Electrical Actuation Systems: Importance of actuators, classification of Actuators, Mechanical Switches, Bouncing and De-bouncing in Mechanical Switches, Solid State Switches: transistors, Darlington pair, Thyristors, Triacs.

Unit IV

Computers and Logic Systems: Logic System Design, Synchronous and Asynchronous Systems, Sequential Systems, Control System Architecture, Control with Embedded Computers and Programmable Logic Control, Digital Signal Processing for Mechatronic Applications, Neural Networks and Fuzzy Systems, Artificial Intelligence and Expert System Approach to control System design, Design Optimization of Mechatronic Systems.

Unit V

Data Acquisition and Software Development: Introduction to Data Acquisition, Measurement, Techniques, Data Acquisition systems, Importance of data acquisition in automobiles. Computer-Based Instrumentation Systems, Software Design and Development, Data Recording and Data Logging, DAQ for automotive engine system and other Measurements, Electronic Control Unit (ECU), Features of design and system logic in multiple signal measurements.

Text books:

1. Mechatronics – W.Bolton, Longman, 2Ed, Pearson Publications, 2007
2. Microprocessor Architecture, Programming & Applications With 8085/8085A – R.S. Ganokar, Wiley Eastern, 2008

Reference Books

1. Mechatronics – Principles, Concepts and Applications – Nitiagour and Premch and Mohalik – Tata McGraw Hill – 2003.
2. Measurement, Instrumentation, and Sensors Handbook - John G. Webster. Editor-inchief, CRC Press. 1999. 0-8493-2145-X. PDF files online available at www.engnetbase.com
3. Mechatronics Principles & Applications by Godfrey C. Onwubolu, Elsevier.
4. Introduction Mechatronics & Measurement Systems, David.G. Aliciatore

Course Title	Internet of Things and Applications				
Course Code	MLEL216B	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Course outcomes:

CO1	Explain IoT concepts and network architecture for practical application.	PO3
CO2	Analyse roles in IoT, apply simplified architecture and computing hierarchy.	PO3
CO3	Analyse smart objects, sensor networks, and IoT access technologies.	PO3
CO4	Analyze and apply IoT application protocols, data analytics, and big data technologies.	PO3
CO5	Explain IoT security strategies and apply best practices effectively.	PO3

Unit I

What is IoT: Introduction to IoT, Genesis of IoT, IoT and Digitization, IoT Impact, Convergence of IT and OT, Iot Challenges

IoT Network Architecture and Design: Drivers Behind New Network Architectures, Comparing IoT Architectures

Unit II

Simplified IoT Architecture: The Core IoT Functional Stack, Layer1, Layer 2, Layer3.

IoT Data Management and Compute Stack: Fog Computing, Edge Computing, The Hierarchy of Edge, Fog and Cloud.

Unit III

Smart Objects: The "Things" in IoT: Sensors, Actuators and Smart Objects, Micro-Electro-Mechanical Systems (MEMS), Smart Objects, Sensor Networks.

Connecting Smart Objects: Communications Criteria, Range, Frequency Bands, Power Consumption, Topology, Constrained Devices, Constrained-Node Networks, Data Rate and Throughput, Latency and Determinism, Overhead and Payload.

IoT Access Technologies: IEEE 802.15.4, Standardization and Alliances, Physical Layer, MAC Layer, Topology, Security, Competitive Technologies, IEEE 802.15.4g and 802.15.4e, Standardization and Alliances, Physical Layer, MAC Layer, Topology, Security, Competitive Technologies.

Unit IV

Application Protocols for IoT: The Transport Layer, IoT Application Transport Methods, Application Layer Protocol Not Present, SCADA, A Little Background on SCADA, Adapting SCADA for IP, Tunneling Legacy SCADA over IP Networks, SCADA Protocol Translation, SCADA Transport over LLNs with MAP-T, Generic Web-Based Protocols.

Data and Analytics for IoT: An introduction to Data Analytics for IoT, Big Data Analytics Tools and Technology, Edge Streaming Analytics

Unit V

Securing IoT: A Brief History of OT Security, Common Challenges in OT Security, How IT and OT Security Practices and Systems Vary, Formal Risk Analysis Structures, The Phased Application of Security in an Operational Environment.

Text Books

2. David Hanes , Gonzalo Salgueiro, Patrick Grossetete , Robert Barton , Jerome Henry "IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things".

Reference books:

1. Arshdeep Bhaga, Vijay Madishetti, "Internet of things: A hands on Approach", Universities Press, ISBN:978172719547, 2015.

Course Title	**Cyber Security**				
Course Code	**MLEL216C**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Course Outcomes:

CO1	Understand the basics of cyber security.	PO3
CO2	Understand the basics architecture of cyber security	PO3
CO3	Understand the basics of ethical Hacking	PO3
CO4	Understand the concepts of web Hacking	PO3
CO5	Understand the concepts of Computer Forensics and encryption Forensics	PO3

Unit I

Introduction Cyber network security concepts: **Security Architecture, antipattern:** signature-based malware detection versus polymorphic threads, document driven certification and accreditation, policy driven security certifications.

Refactored solution: reputational, behavioral and entropy based malware detection.

The problems: cyber anti patterns concept, forces in cyber anti patterns, cyber anti pattern templates, cyber security anti pattern catalog

Unit II

Cyber network security concepts contd.: Enterprise security using Zachman framework Zachman framework for enterprise architecture, primitive models versus composite models, architectural problem solving patterns, enterprise workshop, matrix mining, mini patterns for problem solving meetings.

Unit III

Introduction To Hacking: Introduction to Hacking – Important Terminologies – Penetration Test – Vulnerability Assessments versus Penetration Test – Pre-Engagement – Rules of Engagement -Penetration Testing Methodologies – OSSTMM – NIST – OWASP – Categories of

Penetration Test – Types of Penetration Tests – Vulnerability Assessment Summary –Reports.

Unit IV

Web Hacking – Attacking the Authentication – Brute Force and Dictionary Attacks – Types of Authentication – Log-In Protection Mechanisms – Captcha Validation Flaw – Captcha RESET Flaw – Manipulating User-Agents to Bypass Captcha and Other Protection

Unit V

Introduction to Computer Forensics-what is Forensics? The Growing Problem of Computer Crime What Exactly Is Computer Forensics? Encryption & Forensics Cryptographic Integrity Services, Cryptographic Privacy Services, Time Stamping.

Reference Books

1. Thomas J. Mowbray, ―Cyber Security – Managing Systems, Conducting Testing, and Investigating Intrusions‖, Wiley.
2. Rafay Baloch, "Ethical Hacking and Penetration Testing Guide", CRC Press, 2014.
3. Warren G. Kruse II and Jay G. Heiser, "Computer Forensics: Incident Response Essentials", Addison Wesley, 2002.

E-Resources:

1. https://onlinecourses.nptel.ac.in/noc22_cs13.
2. https://onlinecourses.swayam2.ac.in/cec20_cs15
3. https://www.youtube.com/watch?v=aRwJHB0jYKM
4. https://onlinecourses.nptel.ac.in/noc23_cs127/preview

Course Title	Automotive Electronics				
Course Code	**MLEL216D**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Prerequisites: Basic understanding of systems

Course Outcomes:

CO1	Ability to carry out quantitative and qualitative assessment of performance of automotives in terms of the underlying system dynamics with emphasis on emission and fuel consumption	PO3
CO2	Ability to design and implement in-vehicle communication systems of varied capabilities and capacities as electronic embedded systems	PO3
CO3	Ability to architect (for new development) or migrate (in case of existing design) automotive ECUs and infrastructure requirements in compliance to state-of-the-art standards	PO3

Unit I

Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System, Battery, Starting System

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition Control, Idle speed control, EGR Control **Air/Fuel Systems** – Fuel Handling, Air Intake System, Air/ Fuel Management

Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Anti-Lock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, electronically controlled suspension

Automotive Diagnostics – Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics

Modern Vehicle Architectures: Electric Vehicles, Hybrid Electric Vehicle, Plug-in Hybrid Electric Vehicle, Powertrain Component Sizing, Mass Analysis & Packaging, Vehicle Simulation

Unit II

Sensors and actuators – Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

Unit III

Automotive in-Vehicle communication systems: Characteristics and constraints, In-car embedded networks: CAN, Flexray, LIN, MOST and IDB1394 protocols, Car-to-Car (C2C) and Car-to-infrastructure (C2I) communications –Programmers model of communication controllers – communication hardware and bus – case studies

Unit IV

Automotive Open System Architecture: AUTOSAR–Introduction, AUTOSAR Classical Platform (CP),AUTOSAR Adaptive Platform (AP), TIMEX (AUTOSAR Timing Extensions), ARTI (AUTOSAR/ASAM Run-Time Interface), Timing Analysis

Unit V

Intelligent Transportation Systems : Intelligent Transportation System Concepts, Vehicular Networks, Smart Vehicle, Vehicular Networks, Vehicle-to-Infrastructure Communication Concepts, Vehicle-to-Vehicle Communication Concepts, Vehicular Cloud Concepts

Reference Books:

1. WilliamB.Ribbens,"Understanding Automotive Electronics", 6th Edition,SAMS/Elsevier Publishing
2. 2.NicolasNavet, "Automotive Embedded Systems Handbook", Industrial
3. Information Technology Series, CRC press.
4. Robert Bosch GmbH, "Automotive Electrics Automotive Electronics", 5th edition,

5. Wiley publications.
6. Ronald K Jurgen, "Automotive Electronics Handbook", McGraw-Hill, Inc, 2nd edition.
7. Electric and Hybrid Vehicles, Iqbal Husain, CRC Press, 3rd Ed, 2021
8. Embedded Software Timing Methodology, Analysis and Practical Tips with a Focus on Automotive, Peter Gliwa, Springer 2021
9. Intelligent Transport System in Smart Cities Aspects and Challenges of Vehicular Networks and Cloud, Rodolfo I. Meneguette, Robson E. De Grande, Antonio A. F. Loureiro, Springer 2021

E-Resources:

1. Intro to Traffic Flow Modeling and Intelligent Transport Systems – edx thro'classcentral.com
2. An Introduction to Intelligent Transportation Systems – MIT OCW
3. Intelligent transportation systems https://www.engineeringonline.ncsu.edu/

Course Title	Cryptography And Network Security				
Course Code	MLEL216E	Credits	3	L-T-P	3:0:0
CIE	50 Marks	SEE		50 Marks	

Prerequisites:
A combination of mathematical concepts (modular, algebra), computer science proficiency, and a solid understanding of security principles is necessary to delve into cryptography and network security.

Course outcomes:

CO1	Acquire knowledge in Cryptography and Network Security Concepts	PO3
CO2	Ability to identify, analyse and implement classical models and algorithms related to data security in various scenarios.	PO3
CO3	Analyse the advantages and limitations of different stream ciphers, hash functions and network Security.	PO3
CO4	Involve in independent learning on contemporary issues in Cryptography and Network Security technologies, communicate effectively and prepare a report	PO3

Unit I
Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple
XOR, One-Time Pads, Computer Algorithms
SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data Encryption Standard (DES), The
AES Structure, AES Key Expansion.

Unit II
More Number Theory: Prime Numbers, Fermat's and Euler's theorem, Testing for Primality, The Chinese Remainder theorem, Discrete Logarithms Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve arithmetic, Elliptic Curve Cryptography

Unit III

Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP

Unit IV

One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA], One-way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme.

Unit V

E-mail Security: Pretty Good Privacy-S/MIME.
IP Security: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP)
Web Security: Web Security Considerations, SSL

Textbooks:

1. "Cryptography and Network Security Principles and Practice", William Stallings, Pearson Education Inc., ISBN: 978-93325-1877-3, 6th Edition, 2015.
2. "Applied Cryptography Protocols, Algorithms, and Source code in C", Bruce Schneier,
   Wiley Publications ISBN: 9971-51348-X, 2nd Edition

Reference Books:

1. "Cryptography and Network Security", Behrouz A. Forouzan, TMH, 2007
2. "Cryptography and Network Security", Atul Kahate, TMH, 200

E-Resources:

1. Cryptography and Network by Dr. Kulothungan - This book covers a wide range of topics, including modern cryptography, key management, digital signatures, and network security models. It's available under a Creative Commons license.

2. Cryptography and Network Security: Principles and Practices by William Stallings - A comprehensive guide that introduces both the principles and practices of cryptography and network security. It includes topics like cloud security, IoT network security, and post-quantum cryptography.
3. Cryptography and Network Security: Principles and Practice, 8th Edition by William Stallings - This updated edition explores innovations in cryptography and network security, with expanded coverage of lightweight cryptography and trustworthiness in computer systems

MOOC/Online courses:

1. Cryptography and Network Security by NPTEL: This course, offered by IIT Kharagpur, covers a wide range of topics, including classical cryptosystems, block ciphers, public key cryptography, and modern advancements like blockchain and post-quantum cryptography.
2. Cryptography I by Coursera: Taught by Dan Boneh, this course dives into the fundamentals of cryptographic systems, stream ciphers, and public-key techniques. It also explores real-world applications and common mistakes in cryptographic protocols.
3. MOOC List - Cryptography Courses: This platform provides a variety of courses related to cryptography, including blockchain security, quantum algorithms, and advanced data structures.

Course Title	**VLSI Testing and Verification Lab**				
Course Code	**MLELL209**	**Credits**	**2**	**L-T-P**	**0:0:2**
CIE	**50 Marks**	**SEE**		**50 Marks**	

Course Outcomes

CO1	Able to design and verification using System Verilog	PO3
CO2	Able to Insert faults and perform fault simulation	PO3
CO3	Able to insert scan chain and verify for scan cycle	PO3

PART -A

Testing

1. Synthesize the given design using 45nm with few area and timing constraints.
(i) 10 bit counter (ii) FSM design (iii) Open cores mini projects

2. Write code and simulate for scan flip-flop to understand its functionality.

3. Insert the scan and stich it for the taken design using given technology based scan flip-flop.

4. Model the faults for the given combinational circuit and Introduce modelled faults in the Design. Simulate and check whether fault introduced in the circuit.

5. Perform the Fault simulation of taken circuits in experiment (4) with the ATPG generated for the modelled fault using different algorithm.

6. Construct a BIST structure for a 10 bit synchronous counter design.

PART- B

Verification

1. To Design and perform Verification of D-Flip-flop using SV

2. Design a JK Flip Flop with active low asynchronous reset using SV.

3. Design a mod-6 synchronous up/down counter and test the design using SV test bench architecture with interface and modport.

4. Design a mod-9 synchronous up/down counter and test the design using SV test bench architecture with interface and modport.

5. Design Asynchronous counter (sequence is 010 - 011--100--101--110) using D-Flop and test the design using SV test bench architecture with interface and modport.

6. To study the concepts of Classes, Extended classes, Virtual task and function and Polymorphism And Assertions, code/functional coverage, Fork join/join_none/Join_any

7. Design a Moore machine which detects an overlapping sequence of 1011 and write a System Verilog test bench using only Interface with Code Coverage.

8. To design a Mealy machine which detects an overlapping sequence of 1011 and write a System Verilog test bench using only Interface and Mod ports.

9. For a 4-bit Shift Register, Randomize the following Inputs-Serial input, parallel load and Direction pins using the transactor class. Use virtual Interface to drive the inputs to the design Using driver class and thus develop the system Verilog test bench environment.

10. To write concurrent assertions for 4-bit ALU with Code Coverage.

Third and Fourth Semester Detailed Scheme

III Semester A / IV Semester A

III Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits	CIE	SEE	Total Marks
1	PEC /MDC	MISS311x	(Online Courses) 12 weeks duration	3	50	50	100
2	PEC /MDC	MISS312x	(Online Courses) 12 weeks duration	3	50	50	100
3	PEC /MDC	MISS313x	(Online Courses) 12 weeks duration	3	50	50	100
4	INT	MINT384	Research Internship /Industry-Internship leading to project work/ Startup	3	50	50	100
Total				12			

IV Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits	CIE	SEE	Total Marks
1	INT	MINT481	Research Internship /Industry-Internship leading to project work/ Startup	12	50	50	100
2	PROJ	MPRJ482	Project	16	50	50	100
Total				28			

INT: Industry/Research Internship leading to the project work/startup PROJ: Project work outcome of Internship (Project Phase-II is Viva voce SEE) Taking up a two-semester Industry/Research Internship that leads to project work or a start-up can be a highly rewarding experience for students. It allows them to apply theoretical knowledge in practical settings, gain valuable industry or research experience, and potentially develop innovative solutions or business ideas. Here are some key steps and considerations for students pursuing such an internship.

Industry Internship: The main objective of the industry internship is to ensure that the intern is exposed to a real-world environment and gains practical experience. Often, it may be a practical exposure to the theory that has been learned during the academic period. The industry internship helps students understand analytical concepts and tools, hone their skills in real-life situations, and build confidence in applying the skills learned.

Research Internship: A research internship is an opportunity for students or early career professionals to gain hands-on experience in conducting research under the guidance of a mentor or within a research team. These internships can take place in academic institutions, research organizations, government agencies, or private companies.

Research/Industry Internship: In the third semester, students have to be in touch with a guide/mentor/coordinator and regularly submit the report referred to the progress of the internship. Based on the progress report, the guide/mentor/coordinator has to enter the CIE marks at the end of the 3rd semester. At the beginning of the 4th semester, students have to define the project topic out of the learning due to the internship. Upon completion of the project work, he/she has to attend the SEE at the parent institute.

Internship Leading to Start-up: An internship that leads to a startup is an exciting pathway, blending real-world experience with entrepreneurial ambition. Here's a comprehensive guide to transitioning an internship experience into launching your startup:

1. Maximize your internship experience
2. Identifying viable business ideas
3. Research and validation
4. Building a business plan
5. Networking and mentorship

6. Securing funding
7. Establishing startup
8. Launching and marketing

By following these steps, you can effectively transition from an internship to launching a successful startup. This journey requires dedication, resilience, and a willingness to learn and adapt.

MXXX301/401 to 303/403: MOOC courses of 12 weeks duration are the courses suggested by the Board of Studies of the University and will be displayed on www.online.vtu.ac.in. The online courses selected should not be the same as those studied in the first and second semesters of the program. The student will not be eligible to get their degree if they unintentionally select online courses that match previously finished courses. These courses are not considered for the vertical progression; however, qualifying for these courses and earning the credits is a must for the award of the degree. It is permitted to complete these online MOOC courses either in the 3rd semester or in the 4th semester.

III Semester B / IV Semester B

III Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits	CIE	SEE	Total Marks
1	PEC /MDC	MISS311x	(Online Courses) 12weeks duration	3	50	50	100
2	PEC /MDC	MISS312x	(Online Courses) 12weeks duration	3	50	50	100
3	PEC /MDC	MISS313x	(Online Courses) 12weeksduration	3	50	50	100
4	INT	MINT384	Industry-Internship	11	50	50	100
Total				20			

IV Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits	CIE	SEE	Total Marks
1	Project	MPRJ481	Project work	20	50	50	100
Total				20			

Industry Internship: The main objective of the industry internship is to ensure that the intern is exposed to a real-world environment and gains practical experience. Often, it may be a practical exposure to the theory that has been learned during the academic period. The industry internship helps students understand of analytical concepts and tools, hone their skills in real-life situations, and build confidence in applying the skills learned. The students who take up a one-semester Internship in the Industry have to appear SEE at the institute at the end of the semester as per the examination calendar.

Project Work: Students in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare a synopsis, and narrate the methodology to carry out the project work. Each student, under the guidance of a faculty, is required to

- Present the seminar on the selected project orally and/ or through PowerPoint slides.
- Answer the queries and be involved in debate/ discussion.
- Submit two copies of the typed report with a list of references.
- The participants shall take part in discussions to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident

CIE marks for the project report (20 marks), seminar (20 marks) and question and answer (10 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Principal. The committee shall consist of internal guide and a faculty from the department with the senior most acting as the Chairperson.

Semester End Examination SEE marks for the project report (30 marks), seminar (10 marks) and question and answer session (10 marks) shall be awarded (based on the quality of the report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.

Mxxx301/401 to 303/403: MOOC courses of 12 weeks duration are the courses suggested by the Board of Studies of the University and will be displayed on www.online.vtu.ac.in. The online courses selected should not be the same as those studied in the first and second semesters of the program. The student will not be eligible to get their degree if they unintentionally select online courses that match previously finished courses. These courses are not considered for the vertical progression; however, qualifying for these courses and earning the credits is a must for the award of the degree. It is permitted to complete these online MOOC courses either in 3rd semester or in 4th semester.

III Semester C / IV Semester C

III Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits	CIE	SEE	Total Marks
1	PEC/IP CC/MD	MISS311x	(Online Courses) 12weeks duration	3	50	50	100
2	PEC/IP CC/MD C/PEC	MISS312x	(Online Courses) 12weeks duration	3	50	50	100
3	PEC/IP CC/MD C/PEC	MISS313x	(Online Courses) 12weeks duration	3	50	50	100
4	PEC/IP CC/MD C/PEC	MISS314x	(Online Courses) 12weeks duration	3	50	50	100
5	PROJ	MPRJ385	Project Phase-1	6	50	50	100
Total				18			

IV Semester **CREDIT BASED**

Sl. No	Course Type	Course Code	Course Title	Credits	CIE	SEE	Total Marks
1	Project	MPRJ481	Project work	22	50	50	100
Total				22			

The research section of the university has to announce the number of seats for M.Tech. students who are seeking PhD (research study) admission through a project leading to the publication of the paper in Q1/Q2/Q3 journals. Only full-time research work will be permitted in the university department or approved research centers of the affiliated colleges of the university (guidelines need to be setup). Based on seat availability, the students are permitted to register for project work leading to the publication of papers in Q1/Q2/Q3 journals and admission to research (PhD) in their 3rd semester of the M.Tech. program.

Project Phase-1

Project Phase-I, typically the initial phase in any project, is crucial as it lays the foundation for the entire project. This phase involves defining the project's scope, objectives, and initial planning. Here's a structured approach to effectively carry out Project Phase-I:

- **Project Charter:** Outlines the project's purpose, objectives, and stakeholders.
- **Scope Statement:** Defines the project boundaries and deliverables.
- **Requirements Document:** Captures all project requirements.
- **Project Plan:** Details the approach, timeline, and resource allocation.
- **Risk Management Plan:** Identifies and plans for potential risks.
- **Feasibility Study Report:** Assesses technical, economic, and operational feasibility.

Students in consultation with the guide shall carry out literature survey/visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare a synopsis, and narrate the methodology to carry out the project work. Each student, under the guidance of a faculty, is required to:

- Present the seminar on the selected project orally and/or through PowerPoint slides.
- Answer the queries and be involved in debate/discussion.
- Submit two copies of the typed report with a list of references.
- The participants shall take part in discussions to foster a friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

Continuous Internal Evaluation (100 Marks):

CIE marks for the project report (60 marks), seminar (20 marks), and question and answer (20 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Principal. The committee shall consist of an internal guide and a faculty from the department with the senior most acting as the Chairperson.

Project Work Phase-II:

Each student shall be involved in carrying out the project work jointly in constant consultation with internal guide and external guide and prepare the project report as per the norms of the university to avoid plagiarism. Phase II of a project typically involves the detailed execution of the planned activities, continuous monitoring and control of the project's progress, and making necessary adjustments to ensure the project stays on track. Keep detailed records of all project activities, decisions, and changes. Ensure all project documentation is organized and accessible. Conduct a final project review to evaluate overall performance, achievements, and lessons learned. Document best practices and areas for improvement for future projects.

Paper Publication Process: Publishing a research paper based on your project in a Q1/Q2/Q3 journal involves several key steps, from writing the manuscript to navigating the peer review process. Here’s a comprehensive guide.

Writing the Manuscript: Choose a clear and concise title that accurately reflects the content. Write an abstract summarizing the research question, methods, results, and conclusions.

Literature Review: Review relevant existing research to establish the foundation of your study. Identify gaps that your research aims to fill.

Methodology: Describe the research design, methods, and procedures in detail. Include information on data collection, analysis, and any tools or software used.

Results: Present the findings of your research clearly and logically. Use tables, figures, and charts to illustrate key results.

Discussion: Interpret the results and explain their implications. Compare your findings with existing research and discuss any discrepancies or new insights.

Conclusion: Summarize the main findings and their significance. Suggest potential future research directions.

References: Cite all sources used in your research following the journal's citation style.

Journal Selection: Choose a journal that aligns with the scope and focus of your research. Consider the journal's impact factor (Q1, Q2, Q3) and audience.

Review Journal Guidelines: Carefully read the journal's submission guidelines and ensure your manuscript adheres to them.

Prepare Your Manuscript: Format your manuscript according to the journal's guidelines. Include all required sections and supplementary materials.

Cover Letter: Write a cover letter to the journal editor highlighting the significance of your research and why it fits the journal.

Submit the Manuscript: Use the journal's online submission system to submit your manuscript. Ensure all required information and documents are included.

Semester End Examination: SEE marks for the project report (60 marks), seminar (20 marks), and question and answer session (20 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.