VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELGAUM

SCHEME OF TEACHING AND EXAMINATION FOR

M.Tech. Electronics

I Semester **CREDIT BASED**

Subject Code	Name of the Subject	Teaching hours/week		Duration of Exam in Hours	Marks for		Total Marks	CREDITS
		Lecture	Practical / Field Work / Assignment/ Tutorials		I.A.	Exam		
14ELD11	Advanced Mathematics	4	2	3	50	100	150	4
14EVE12	Digital VLSI Design	4	2	3	50	100	150	4
14EVE13	Advanced Embedded Systems	4	2	3	50	100	150	4
14ELD14	Digital Circuits and Logic Design	4	2	3	50	100	150	4
14ELD15X	Elective - I	4	2	3	50	100	150	4
14ELD16	Digital Electronics Lab -1	--	3	3	25	50	75	2
14ELD17	Seminar on Advanced topics from refereed journals	--	3	--	25	--	25	1
	Total	**20**	**16**	**18**	**300**	**550**	**850**	**23**

Elective-1

14 ELD 151	Digital System Design using Verilog	14 EVE 154	ASIC Design
14 ELD 152	Automotive Electronics	14 ELD 155	Simulation, Modeling and Analysis
14 ELD 153	NanoElectronics		

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II Semester **CREDIT BASED**

Subject Code	Name of the Subject	Teaching hours/week		Duration of Exam in Hours	Marks for		Total Marks	CREDITS
		Lecture	Practical / Field Work / Assignment/ Tutorials		I.A.	Exam		
14ELD21	Modern DSP	4	2	3	50	100	150	4
14ELD22	Coding Theory	4	2	3	50	100	150	4
14ELD23	Digital Signal Compression	4	2	3	50	100	150	4
14ELD24	Real Time Operating Systems	4	2	3	50	100	150	4
14ELD25X	Elective-2	4	2	3	50	100	150	4
14ELD26	Digital Electronics Lab -2		3	3	25	50	75	2
14ELD27	Seminar on Advanced topics from refereed journals	--	3	--	25	--	25	1
**Project Phase-I(6 week Duration)								
	Total	**20**	**16**	**18**	**300**	**550**	**850**	**23**

Elective -2:

14 ELD 251	VLSI Design and Verification	14 ECS 254	Multimedia Communication
14 ELD 252	Synthesis & Optimization of Digital Circuits	14 ECS 255	Spread Spectrum Communication
14 ELD 253	MEMS		

**** Between the II Semester and III Semester, after availing a vocation of 2 weeks.**

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M.Tech. Electronics

III Semester: INTERNSHIP # **CREDIT BASED**

Course Code	Subject	Teaching hours/week		Duration of the Exam in Hours	Marks for		Total Marks	CREDITS
		Lecture	Practical / Field Work		I.A.	Exam		
14ELD31	Midterm Presentation on Internship (After 8 weeks from the date of commencement) *	-	-	-	25	-	25	1
14ELD32	Report on Internship (After 16 weeks from the date of commencement)	-	-	-	75		75	15
14ELD33	Evaluation and Viva-voce	-	-	3	–	50	50	4
	Total	**-**	**-**	**-**	**100**	**50**	**150**	**20**

* The student shall make a midterm presentation of the activities undertaken during the first 8 weeks of internship to a panel comprising Internship Guide, a senior faculty from the department and Head of the Department.

\# The College shall facilitate and monitor the student internship program.

The internship report of each student shall be submitted to the University.

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M.Tech. Electronics

IV Semester **CREDIT BASED**

Subject Code	Subject	Teaching hours/week		Duration of Exam in Hours	Marks for		Total Marks	CREDITS
		Lecture	Practical / Field Work / Assignment/ Tutorials		I.A.	Exam		
14ELD41	Advanced Computer Architecture	4	2	3	50	100	150	4
14ELD42X	Elective-3	4	2	3	50	100	150	4
14ELD43	Evaluation of Project Phase-I	-	-	-	25	-	25	1
14ELD44	Phase-II : Midterm evaluation of Project	-	-	-	25	-	25	1
14ELD45	Evaluation of Project Work and Viva-voce	–	-	3	-	100+100	200	18
Total		**8**	**04**	**09**	**150**	**400**	**550**	**28**
Grand Total (I to IV Sem.) : 2400 Marks; 94 Credits								

Elective -3:

14 EVE 421	Advances in VLSI Design	14 ELD 424	Cryptographic Systems
14 ELD 422	Image and Video Processing	14 ELD 425	Advanced Microcontrollers
14 ECS 423	RF and Microwave Circuit Design		

Note:

1) Project Phase – I**:** 6 weeks duration shall be carried out between II and III Semesters. Candidates in consultation with the guides shall carryout literature survey / visit to Industries to finalize the topic of dissertation.
2) Project Phase – II**:** 16 weeks duration during III Semester. Evaluation shall be taken during the Second week of the IV Semester. Total Marks shall be 25.
3) Project Evaluation: 24 weeks duration in IV Semester. Project Work Evaluation shall be taken up at the end of the IV Semester. Project Work Evaluation and Viva-Voce Examinations shall be conducted. Total Marks shall be 250 (Phase I Evaluation: 25 Marks, Phase –II Evaluation: 25 Marks, Project Evaluation marks by Internal Examiner (guide): 50, Project Evaluation marks by External Examiner: 50, marks for external and 100 for viva-voce).

   Marks of Evaluation of Project:

   - The I.A. Marks of Project Phase – I & II shall be sent to the University along with Project Work report at the end of the Semester.

4) During the final viva, students have to submit all the reports.
5) The Project Valuation and Viva-Voce will be conducted by a committee consisting of the following:

   a) Head of the Department (Chairman)
   b) Guide
   c) Two Examiners appointed by the university. (Out of two external examiners at least one should be present).

Advanced Mathematics

Subject Code	: 14ELD11	IA Marks	: 50
No. of Lecture Hours / Week	: 04	Exam. Hours	: 03
Total No. of Lecture Hours	: 50	Exam. Marks	: 100

Matrix Theory

QR EL Decomposition – Eigen values using shifted QR algorithm- Singular Value EL Decomposition - Pseudo inverse- Least square approximations

Calculus of Variations

Concept of Functionals- Euler's equation – functional dependent on first and higher order derivatives – Functionals on several dependent variables – Iso perimetric problems- Variational problems with moving boundaries

Transform Methods

Laplace transform methods for one dimensional wave equation – Displacements in a string – Longitudinal vibration of a elastic bar – Fourier transform methods for one dimensional heat conduction problems in infinite and semi infinite rod.

Elliptic Equation

Laplace equation – Properties of harmonic functions – Fourier transform methods for laplace equations. Solution for Poisson equation by Fourier transforms method

Linear and Non Linear Programming

Simplex Algorithm- Two Phase and Big M techniques – Duality theory- Dual Simplex method. Non Linear Programming –Constrained extremal problems- Lagranges multiplier method- Kuhn- Tucker conditions and solutions

Reference Books:

1. Richard Bronson, **"Schaum's Outlines of Theory and Problems of Matrix Operations"**, McGraw-Hill, 1988.
2. Venkataraman M K, **"Higher Engineering Mathematics"**, National Pub. Co, 1992.
3. Elsgolts, L., **"Differential Equations and Calculus of Variations"**, Mir, 1977.
4. Sneddon,I.N., **"Elements of Partial differential equations"**, Dover Publications, 2006.
5. Sankara Rao, K., **"Introduction to partial differential equations"**, Prentice – Hall of India, 1995
6. Taha H A, **"Operations research - An introduction"**, McMilan Publishing co, 1982.

Digital VLSI Design

Subject Code	: 14EVE12	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.

MOS Inverters: Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load, CMOS Inverter.

MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Esimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

Dynamic Logic Circuits : Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM).

Low-Power CMOS Logic Circuits: Introduction, Overview of Power Consumption, Low-Power Design Through Voltage Scaling, Estimation and Optimization of Switching Acivity, Reduction of Switched Capacitance, Adiabatic Logic Circuits.

BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.

Design for Manufacturability : Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modelling, Parametric Yield Esimation, Parametric Yield Maximization, Worst-Case Analysis, Performance Variability Minimization.

Reference Books:

1. Sung Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition.
2. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.

Advanced Embedded Systems

Subject Code	: 14EVE13	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components.

Characteristics and Quality Attributes of Embedded Systems: Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software Trade-offs.

Embedded Hardware Design and Development :EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement, PCB track routing.

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture.

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Reference Books:

1. Shibu K V, **"Introduction to Embedded Systems"**, Tata McGraw Hill Education Private Limited, 2009
2. Joseph Yiu, **"The Definitive Guide to the ARM Cortex-M3"**, Newnes, (Elsevier), 2008.
3. James K Peckol, "Embedded Systems – A contemporary Design Tool", John Weily, 2008.

Digital Circuits and Logic Design

Subject Code	: 14ELD14	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks

Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic

Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities and Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, ELDompositions, Synthesis of Multiple Machines.

State—Identifications and Fault-Detection Experiments: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault-Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection Experiments for Machines which have no Distinguishing Sequences.

Reference Books:

1. Zvi Kohavi, "**Switching and Finite Automata Theory**", 2nd Edition. Tata McGraw Hill Edition
2. Charles Roth Jr., "**Digital Circuits and logic Design**",
3. Parag K Lala, "**Fault Tolerant And Fault Testable Hardware Design**", Prentice Hall Inc. 1985
4. E. V. Krishnamurthy, "**Introductory Theory of Computer**", Macmillan Press Ltd, 1983
5. Mishra & Chandrasekaran, "**Theory of computer science – Automata, Languages and Computation**", 2nd Edition, PHI,2004

Digital System Design Using Verilog

Subject Code	: 14 ELD151	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Introduction and Methodology: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.

Combinational Basics: Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.

Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers.

Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology.

Memories: Concepts, Memory Types, Error Detection and Correction.

Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.

Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory.

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.

Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test.

REFERENCE BOOKS:

1. Peter J. Ashenden, **"Digital Design: An Embedded Ssytems Approach UsingVERILOG"**, Elesvier, 2010.

Automotive Electronics

Subject Code	: 14ELD152	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System, Battery, Starting System

Air/Fuel Systems – Fuel Handling, Air Intake System, Air/ Fuel Management

Sensors – Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor

Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator

Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control

Communication – Serial Data, Communication Systems, Protection, Body and Chassis Electrical Systems, Remote Keyless Entry, GPS

Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension

Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters

Integrated Body – Climate Control Systems, Electronic HVAC Systems, Safety Systems – SIR, Interior Safety, Lighting, Entertainment Systems

Automotive Diagnostics – Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems

Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System

Reference Books:

1. William B. Ribbens, “Understanding Automotive Electronics”, 6th Edition, SAMS/Elsevier Publishing
2. Robert Bosch Gambh, Automotive Electrics Automotive Electronics Systems and Components, 5th edition, John Wiley& Sons Ltd., 2007.

NanoElectronics

Subject Code	: 14ELD153	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores law and continued miniaturization., Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giantmolecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometerlength scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems.

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantumwells, quantum wires, quantum dots, super-lattices, band offsets, electronicdensity of states.

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edgeover growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonanttunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantumconfined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural.

Methods of measuring properties-structure:atomic,crystallography,microscopy,spectroscopy. Properties of nanoparticles: metalnano clusters, semiconducting nanoparticles, rare gas and molecularclusters, methods of synthesis(RF, chemical, thermolysis, pulsed laser methods) Carbon nanostructures and its applications(field emission and shielding, computers, fuelcells, sensors, catalysis).Self assembling nanostructured

molecular materials and devices: building blocks, principles of self assembly, methods to prepare and pattern nanoparticles, template dnanostructures, liquid crystal mesophases. Nanomagnetic materials and devices: magnetism, materials, magnetoresistance, nanomagnetism intechnology, challenges facing nanomagnetism.

Applications: Injectionlasers, quantumcascadelasers, singlephotonsources, biologicaltagging, opticalmemories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS.

Reference Books:

1. Ed Robert Kelsall,IanHamley,MarkGeoghegan, **" Nanoscale science and technology"** ,John wiley and sons,2007.
2. Charles P Poole,Jr,Frank J owens, **"Introduction to Nanotechnology"** ,John wiley,copyright 2006,Reprint 2011.
3. Ed William A Goddard III,Donald W Brenner,Sergey EdwardLyshevski,Gerald J Lafrate, **" Hand Book of Nanoscience Engineering and Technology"** ,CRC press,2003

ASIC Design

Subject Code	: 14EVE154	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Note: All Designs Will Be Based On VHDL

Introduction: Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channelled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, SIC cell libraries.

Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers

ASIC Library Design: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.

Low-Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation.

Programmable ASIC: programmable ASIC logic cell, ASIC I/O cell.

A Brief Introduction to Low Level Design Language: an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation.

ASIC Construction Floor Planning and Placement And Routing: Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

Reference Books:

1. M.J.S .Smith, **"Application - Specific Integrated Circuits",** Pearson Education, 2003.
2. Jose E.France, YannisTsividis, **"Design of Analog-Digital VLSICircuits for Telecommunication and signal processing"**, Prentice Hall, 1994.

3. MalcolmR.Haskard; Lan. C. May, **“Analog VLSI Design - NMOSand CMOS”**, Prentice Hall, 1998.
4. Mohammed Ismail and Terri Fiez, **“Analog VLSI Signal andInformation Processing”**, McGraw Hill, 1994.

Simulation Modelling and Analysis

Subject Code	: 14ELD155	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Basic simulation modeling: nature of simulation, system models, discrete event simulation, single server simulation, alternative approaches, other types of simulation.

Building valid, credible and detailed simulation models. Techniques for increasing model validity and credibility, comparing real world observations

Selecting input probability distributions. Useful probability distributions, assessing sample independence, activity I, II and III. Models of arrival process.

Random numbers generators: linear congruential, other kinds, testing random number generators. Random variate generation: approaches, continuous random variates, discrete random variates, correlated random variates.

Output data analysis. Statistical analysis for terminating simulations, analysis for steady state parameters. Comparing alternative system configurations. Confidence intervals. Variance reduction techniques. Antithetic and Control variates.

Reference Books:

1. Jerry Banks, "**Discrete event system simulation"**, Pearson, 2009
2. Averill Law "**Simulation modeling and analysis"**, MGH 4th edition, 2007
3. Seila, Ceric, Tadikamalla, "**Applied simulation modeling",** Cengage, 2009.
4. George S. Fishman, "**Discrete event simulation"**, Springer, 2001
5. N. Viswanadham, Y. Narahari, "**Performance modeling of automated manufacturing systems"**, PHI, 2000
6. Frank L. Severance, "**System modeling and simulation"**, Wiley, 2009
7. K. S. Trivedi, "**Probability and stastistics with reliability queuing and computer science applications",** PHI, 2007.

Digital Electronics Lab -1

Subject Code	: 14ELD16	IA Marks	: 25
No. of Lecture Hours /week	: 03	Exam Hours	: 03
Total no. of Lecture Hours	: 42	Exam Marks	: 50

Design Using Cadence ORCAD

1. Design of 3½ Digit Digital Voltmeter
2. Design of Monolithic function Generator.
3. Design of Regulator Power supplies.
4. Design of Batch counter using TTL ICs.
5. Design of DAC and ADC.
6. Design of Electronic P, PI, PID and ON/OFF controllers.
7. Design of Programmable Timers.
8. Design of filters and resonance circuits.

VLSI DIGITAL DESIGN

FPGA DIGITAL DESIGN

VLSI Front End Design programs:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels and logic analyzer)/Chipscope pro apart from verification by simulation with any of the front end tools

1. Write Verilog code for the design of 8-bit
    i. Carry Ripple Adder
    ii. Carry LookAhead adder
    iii. Carry Skip Adder

iv. BCD Adder &Subtracter

2. Write Verilog Code for 8-bit

i. Array Multiplication (Signed and Unsigned)

ii. Booth Multiplication (Radix-4)

3. Write Verilog code for 4/8-bit

i. Magnitude Comparator

ii. LFSR

iii.Parity Generator

iv.Universal Shift Register

4. Write Verilog Code for 3-bit Arbitary Counter to generate 0,1,2,3,6,5,7 and repeats.

5. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.

Eg 11101 (with and without overlap) any sequence can be specified

6. Design a FIFO and LIFO buffers in Verilog and Verify its Operation.

7. Design a coin operated public Telephone unit using Mealy FSM model with following operations

i. The calling process is initiated by lifting the receiver.

ii. Insert 1 Rupee Coin to make a call.

iii. If line is busy, placing the receiver on hook should return a coin

iv. If line is through, the call is allowed for 60 seconds at the 45th second prompt another 1 Rupee coin to be inserted, to continue the call.

v. If user doesn't insert the coin within 60 seconds the call should be terminated.

vi. The system is ready to accept new call request when the receiver is placed on the hook.

vii. The FSM goes 'out of order' state when there is a Line Fault.

Note: Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits

Modern DSP

Subject Code	: 14ELD21	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Goal of the course – Advances in Digital Signal Processing involve variable sampling rates and thus the multirate signal processing and hence their applications in communication systems and signal processing. It is intended to introduce a basic course in multirate signal processing especially meant for students of branches eligible for M Tech courses in EC related disciplines.

Introduction and Discrete Fourier Transforms: Signals, Systems and Processing, Classification of Signals**,** The Concept of Frequency in Continuous-Time and Discrete-Time Signals**,** Analog-to-Digital and Digital-to-Analog Conversion**,** Frequency-Domain Sampling: The Discrete Fourier Transform**,** Properties of the DFT**,** Linear Filtering Methods Based on the DFT (Ref.1 Chap. 1 & 7)

Design of Digital Filters: General Considerations, Design of FIR Filters, Design of IIR Filters from Analog Filters, Frequency Transformations. (Ref.1Chap.10)

Multirate Digital Signal Processing: Introduction, EL Dimation by a factor 'D', Interpolation by a factor 'I', Sampling rate Conversion by a factor 'I/D', implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion, Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank. (Ref.1 Chap.11)

Adaptive Filters: Applications of Adaptive Filters, Adaptive Direct Form FIR Filters- The LMS Algorithm, Adaptive Direct Form Filters-RLS Algorithm. (Ref.1 Chap.13)

Reference Books:

1. Proakis and Manolakis, "**Digital Signal Processing**", Prentice Hall 1996. (Fourth Edition).

2. Roberto Cristi, "**Modern Digital Signal Processing**", Cengage Publishers, India, (Erstwhile Thompson Publications), 2003.

3. S.K. Mitra, "**Digital Signal Processing: A Computer Based Approach"**, III Ed, Tata McGraw Hill, India, 2007.

4. E.C. Ifeachor and B W Jarvis, "**Digital Signal Processing, a practitioners approach**," II Edition, Pearson Education, India, 2002 Reprint.

Coding Theory

Subject Code	: 14ELD22	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Information and Entropy: Sources of information, DMS and Markov. Properties of Entropy. Entropy of information sources, Extension of a DMS. Information channels, probability relations in a channel, A Priori, A Posteriori Entropies, Equivocation, Mutual information, Capacity of BSC, BEC, Noiseless and deterministic channels.

Source coding: Uniquely EL Dodable codes, Instantaneous codes and its construction, Average length of a code, Bounds for Average Length,Kraft'sInequality. R-ary compact codes. Code efficiency, Redundancy. Shannon-Fano and Huffman code.

Algebra: Groups, rings and fields, properties of finite fields, Galois field arithmetic and its realization, Vector spaces, Matrices.

Channel Coding: Block codes, Minimum distance of a block code, Singleton bound. Performance of Codes. Hamming codes. Cyclic codes, Golay Codes BCH codes, R-S codes. Convolutional codes. Viterbi Algorithm. LDPC Codes.

Reference Books:

1. S. Lin and D. J. Costello Jr, **"Error Control Coding"**, *Pearson Prentice Hall*, 2004
2. T. K. Moon, **"Error Correction Coding: Mathematical Methods And Algorithms"**, Student Edition, *John Wiley & Sons*, 2005

Digital Signal Compression

Subject Code	: 14ELD23	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Introduction: Compression techniques, Modeling & coding, Distortion criteria, Differential Entropy, Rate Distortion Theory, Vector Spaces, Information theory, Models for sources, Coding – uniquely ELDodable codes, Prefix codes, Kraft McMillan Inequality

Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm, Tree structured VQ, Structured VQ, Variations of VQ – Gain shape VQ, Mean removed VQ, Classified VQ, Multistage VQ, Adaptive VQ, Trellis coded quantization

Differential Encoding: Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation, Speech coding – G.726, Image coding.

Transform Coding: Transforms – KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression – JPEG, Application to audio compression.

Sub-band Coding: Filters, Sub-band coding algorithm, Design of filter banks, Perfect reconstruction using two channel filter banks, M-band QMF filter banks, Poly-phase ELDomposition, Bit allocation, Speech coding – G.722, Audio coding – MPEG audio, Image compression

Wavelet Based Compression: Wavelets, Multiresolution analysis & scaling function, Implementation using filters, Image compression – EZW, SPIHT, JPEG 2000

Analysis/Synthesis Schemes: Speech compression – LPC-10, CELP, MELP, Image Compression – Fractal compression

Video Compression: Motion compensation, Video signal representation, Algorithms for video conferencing & videophones – H.261, H. 263, Asymmetric applications – MPEG 1, MPEG 2, MPEG 4, MPEG 7, Packet video

Lossless Coding: Huffman coding, Adaptive Huffman coding, Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding, Arithmetic coding, Algorithm implementation, Applications of Arithmetic coding, Dictionary techniques – LZ77, LZ78, Applications of LZ78 – JBIG, JBIG2, Predictive coding – Prediction with partial match, Burrows Wheeler Transform, Applications – CALIC, JPEG-LS, Facsimile coding – T.4, T.6.

Reference Books:

1. K. Sayood**,** "**Introduction to Data Compression**," Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.
2. N. Jayant and P. Noll, **"Digital Coding of Waveforms: Principles and Applications to Speech and Video**," Prentice Hall, USA, 1984.
3. D. Salomon, "**Data Compression: The Complete Reference**", Springer, 2000.
4. Z. Li and M.S. Drew**,** "**Fundamentals of Multimedia**," Pearson Education (Asia) Pte. Ltd., 2004.

Real Time Operating Systems

Subject Code	: 14ELD24	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Reentrant Functions.

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonicleast upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.

I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.

Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components: Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging.

Performance Tuning: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.

High availability and Reliability Design: Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.

Design of RTOS – PIC microcontroller. (Chap 13 of book MykePredko)

Reference Books:

1. Sam Siewert, **"Real-Time Embedded Systems and Components"**, Cengage Learning India Edition, 2007.
2. MykePredko, **"Programming and Customizing the PIC microcontroller"**, 3rd Ed, TMH, 2008.
3. Dreamtech Software Team, **"Programming for Embedded Systems"**, Jhon Wiley, India Pvt. Ltd., 2008.

VLSI Design and Verification

Subject Code	: 14ELD251	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Note: Today, the complexity of the VLSI integrated circuits that are being designed is so large that pre-silicon verification presents a major challenge to the design team. The fact that IP from multiple sources are integrated todayto create a system-on-chip design further complicates the matter. Simulationbased verification techniques that were developed in the past are considered inadequate to-day, since they require too many test cases and require too much development time and run-time. Raising the level of abstraction to design can help bring down the simulation cost. Formal specification and verification techniques are another way to address the challenge of design verification.

Importance of Design Verification: What is verification? What is attest bench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification.[Ref1- Chapter1]

Functional verification approaches: Black box verification, white box verification, grey box verification. Testing versus verification: scan based testing, design for verification. Verification reuse. The cost of verification.[Ref1- Chapter1]

Verification Tools: Linting tools: Limitations of linting tools, linting verilog source code, linting VHDL source code, linting OpenVera and e-source code, code reviews. Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.[Ref1-Chapter2]

Code Coverage: statement coverage, path coverage, expression coverage, FSM coverage, what does 100%coverage mean? Functional coverage: Item Coverage, cross coverage, Transition coverage , what does 100% functional mean? Verification languages: Assertions: simulation based assertions, formal assertions proving. Metrics: Code related metrics, Quality related metrics, interpreting metrics.[Ref1-Chapter2]

The verification plan: The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. [Ref1-Chapter3]

From specification to features: component level feature, system level features, Error types to look for?, prioritise, design for verification. Directed test bench approaches group into test cases, from test cases to test benches, measuring progress. Coverage driven random based approach: Measuring progress, From features to functional coverage, from features to test bench, From features to generators, directed test cases. [Ref1-Chapter3]

Static Timing Verification: Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, falsepaths, Timing models. [Ref2 Chapter 1, 2, 3, 8]

Physical Design Verification: Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, Crosstalk and Noise**:** Cross talk glitch analysis, crosstalk delayanalysis, timing verification [Ref4 Chapter 8]

IP-Reuse in modern-day SoC: SoC Integration and the problem of verification of IP-based designs. Verification IP and their importance, Formal Verification: SAT BDDs, Symbolic Model Checking with BDDs, Model Checking using SAT, Equivalence Checking. [Ref 5, Ref3 Chapter 1, 2]

Reference Books:

1. JanickBergeron, **"Writing testbenches: functional verification of HDL models"**, 2nd edition ,Kluwer Academic Publishers,2003
2. JayaramBhasker,RakeshChadha ,**"Static Timing Analysis for Nanometer Designs"** A practical approach, Springer publications
3. S.Minato **"Binary Decision diagram and applications for VLSICAD"**, Kulwer Academic pub November 1996
4. PrakashRashinkar, PeterPaterson,Leena Singh **"System on a Chip Verification"**, Kulwer Publications.
5. http://www.cse.psu.edu/~vijay/verify/instructors.html

Synthesis and Optimization of Digital Circuits

Subject Code	: 14ELD252	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioural hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, dataflow and sequencing graphs, compilation and optimization techniques.

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Schedule Algorithms: A model for scheduling problems, Scheduling wither source and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Anti fuse based F.P.G.As), rule based library binding.

Testing: Simulation, Types of simulators, basic components of a simulator, fault simulation Techniques, Automatic test pattern generation methods (ATPG), design for Testability (DFT) Techniques.

Reference Books:

1. Giovanni De Micheli, **"Synthesis and Optimization of Digital Circuits"**, Tata McGraw-Hill, 2003.
2. SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer, **"Logic Synthesis"**, McGraw-Hill, USA, 1994.
3. NeilWeste and K. Eshragian, **"Principles of CMOS VLSI Design: A System Perspective",** 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
4. KevinSkahill, **"VHDL for Programmable Logic",** Pearson Education(Asia) Pvt. Ltd., 2000

MEMS

Subject Code	: 14ELD253	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Overview of MEMS & Microsystems: MEMS & Microsystems, Typical MEMS and Micro system products — features of MEMS, The multidisciplinary nature of Microsystems design and manufacture, Applications of Microsystems in automotive industry, health care industry, aerospace industry, industrial products, consumer products and telecommunications.

Scaling Laws in Miniaturization: Introduction to scaling, scaling in geometry, scaling in rigid body dynamics, scaling electrostatic forces, electromagnetic forces, electricity, scaling in fluid mechanics & heat transfer.

Transduction Principles in MEMS & Microsystems: Introduction, Micro sensors — thermal, radiation, mechanical, magnetic and bio — sensors, Micro actuation, MEMS with micro actuators.

Microsystems Fabrication Process: Introduction, Photolithography, Ion-implantation, diffusion, oxidation, CVD, PVD, etching and materials used for MEMS, Some MEMS fabrication processes: surface micro-machining, bulk micromachining, LIGA process, LASER micro machining, MUMPS, FAB-less fabrication.

Micro System Design and Modeling: Introduction, Design considerations: Process design, Mechanical design, Modeling using CAD tools: ANSYS / Multiphysics or Intellisuite or MEMS CAD, Features and Design considerations of RF MEMS, Design considerations of Optical MEMS (MOEMS), Design and Modeling: case studies - i) Cantilever beam ii) Micro switches iii) MEMS based SMART antenna in mobile applications for maximum reception of signal in changing communication conditions and iv) MEMS based micro mirror array for control and switching in optical communications.

Micro system packaging: Over view of mechanical packaging of micro electronics micro system packaging, Interfaces in micro system packaging, Packaging technologies.

Reference Books:

1. Tai Ran Hsu, **"MEMS and Micro Systems : Design and Manufacture"**, Tata McGraw Hill, 2002
2. Boca Raton, **"MEMS and NEMS: Systems, Devices and Structures"**, CRC Press, 2002
3. J. W. Gardner and V. K. Vardan, **"Micro Sensors MEMS and SMART Devices"**, John Wiley, 2002
4. N. Maluf, **"Introduction to Micro Mechanical Systems Engineering, Artech House"**, Norwood, MA, 2000.

Multimedia Communication

Subject Code	: 14ECS254	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Multimedia Communications: multimedia information representation, multimedia networks, multimedia applications, network QoS and application QoS.

Information Representation: text, images, audio and video, Text and image compression, compression principles, text compression, image compression. Audio and video compression, audio compression, video compression, video compression principles, video compression standards: H.261, H.263, P1.323, MPEG 1, MPEG 2, Other coding formats for text, speech, image and video.

Detailed Study of MPEG 4: coding of audiovisual objects, MPEG 4 systems, MPEG 4 audio and video, profiles and levels. MPEG 7 standardization process of multimedia content description, MPEG 21 multimedia framework, Significant features of JPEG 2000, MPEG 4 transport across the Internet.

Synchronization: notion of synchronization, presentation requirements, reference model for synchronization, Introduction to SMIL, Multimedia operating systems, Resource management, process management techniques.

Multimedia Communication Across Networks: Layered video coding, error resilient video coding techniques, multimedia transport across IP networks and relevant protocols such as RSVP, RTP, RTCP, DVMRP, multimedia in mobile networks, multimedia in broadcast networks.

Reference Books:

1. Fred Halsall, **"Multimedia Communications**", Pearson education, 2001
2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, **"Multimedia Communication Systems"**, Pearson education, 2004
3. Raif steinmetz, Klara Nahrstedt, **"Multimedia: Computing, Communications and applications"**, Pearson education, 2002
4. Tay Vaughan, "**Multimedia: Making it work"**, 6th edition, Tata McGraw Hill, 2004
5. John Billamil, Louis Molina, **"Multimedia: An Introduction"**, PHI, 2002
6. Pallapa Venkataram, **"Multimedia Information Systems"**, Pearson education (In Press), 2005

Spread Spectrum Communication

Subject Code	: 14ECS255	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Review of digital communication concepts, direct sequence and frequency hop spread spectrum systems.

Hybrid direct sequence/frequency hop spread spectrum. Complex envelop representation of spread spectrum signals.

Sequence generator fundamentals, Maximum length sequences. Gold and Kasami codes, Nonlinear Code generators.

Spread spectrum communication system model, Performance of spread spectrum signals in jamming environments, Performance of spread spectrum communication systems with and without forward error correction.

Diversity reception in fading channels, Cellular radio concept, CDMA cellular systems. Examples of CDMA cellular systems. Multicarrier CDMA systems. CDMA standards

Reference Books:

1. R. L. Peterson, R. E. Zeimer and D. E. Borth, **"Introduction to Spread Spectrum Communications"**, Pearson, 1995.
2. J. D. Proakis and M. Salehi, **"Digital Communication"**, McGraw Hill, 2008
3. A. J. Viterbi, **"CDMA: Principles of Spread Spectrum Communications",** Addision Wesley, 1995.
4. S. Verdu, **"Multiuser Detection"**, Cambridge University Press, 1998

Digital Electronics Lab -2

Subject Code	: 14ELD26	IA Marks	: 50
No. of Lecture Hours /week	: 03	Exam Hours	: 03
Total no. of Lecture Hours	: 42	Exam Marks	: 100

Graphical Programming using LabVIEW

Design of 4 bit Adders (CLA, CSA, CMA, Parallel adders)

Design of Binary Subtractors

Design of Encoder (8X3), ELDoder(3X8)

Design of Multiplexer (8X1), and Demultiplexer (1X8)

Design of code converters & Comparator

Design of FF (SR, D, T, JK, and Master Slave with delays)

Design of registers using latches and flip-flops

Design of 8 bit Shift registers

Design of Asynchronous & Synchronous Counters

ARM-CORTEX M3

[Programming to be done using Keiluvision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U].

Write an Assembly language program to calculate 10+9+8+.....+1

Write a Assembly language program to link Multiple object files and link them together.

Write a Assembly language program to store data in RAM.

Write a C program to Output the "Hello World" message using UART.

Write a C program to Design a Stopwatch using interrupts.

Write an Exception vector table in C

Write an Assembly Language Program for locking a Mutex.

Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stacked PC location and the stacked register values.

Advanced Computer Architecture

Subject Code	: 14ELD41	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Introduction and Review of Fundamentals of Computer Design: Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design; Performance and Price-Performance; Fallacies and pitfalls; Case studies.

Some topics in Pipelining, Instruction –Level Parallelism, Its Exploitation and Limits on ILP: Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining; Basic concepts and challenges of ILP; Case study of Pentium 4, Fallacies and pitfalls. Introduction to limits in ILP; Performance and efficiency in advanced multiple-issue processors.

Memory Hierarchy Design, Storage Systems: Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy; Fallacies and pitfalls in the design of memory hierarchies. Introduction to Storage Systems; Advanced topics in disk storage.

Definition and examples of real faults and failures ; I/O performance, reliability measures, and benchmarks; Queuing theory; Crosscutting issues; Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls.

Hardware and Software for VLIW and EPIC Introduction: Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism, Hardware Support for Exposing

Parallelism: Predicated Instructions, Hardware Support for Compiler Speculation, The Intel IA-64 Architecture and Itanium Processor, Concluding Remarks.

Large-Scale Multiprocessors and Scientific Applications Introduction, Interprocessor Communication: The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications, Implementing Cache Coherence, The Custom Cluster Approach: Blue Gene/L, Concluding Remarks.

Computer Arithmetic: Introduction, Basic Techniques of Integer Arithmetic, Floating Point, Floating-Point Multiplication, Floating-Point Addition, Division and Remainder, More on Floating-Point Arithmetic, Speeding Up Integer Addition, Speeding Up Integer Multiplication and Division, Fallacies and Pitfalls.

Reference Books:

1. Hennessey and Patterson, **"Computer Architecture A Quantitative Approach"**, 4th Edition, Elsevier, 2007.

2. Kai Hwang, **"Advanced Computer Architecture - Parallelism, Scalability, Programmability"**, 2nd Edition

Advances in VLSI Design

Subject Code	: 14EVE421	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Review of MOS Circuits: MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.

MESFETS: MESFET and MODFET operations, quantitative description of MESFETS.

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nanotubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic. Defect tolerant computing,

Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks -NMOS and CMOS functional blocks.

Special Circuit Layouts and Technology Mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module layout.

System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom design.

Reference Books:

1. Kevin F Brennan "**Introduction to Semi Conductor Device**", Cambridge publications
2. Eugene D Fabricius "**Introduction to VLSI Design**", McGraw-Hill International publications
3. D.APucknell "**Basic VLSI Design**", PHI Publication

4. Wayne Wolf, "**Modern VLSI Design**" Pearson Education, SecondEdition , 2002

Image and Video Processing

Subject Code	: 14ELD422	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Introduction: 2D systems, Mathematical preliminaries – Fourier Transform, Z Transform, Optical & Modulation transfer function, Matrix theory, Random signals, Discrete Random fields, Spectral density function.(Ref.1,Chap.2)

Image Perception: Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelitycriteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision. (Ref.1, Chap.3)

Image Sampling and Quantization: Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization. (Ref.1, Chap.4)

Image Transforms: Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, DFT, DCT, DST, Hadamard, Haar, Slant, KLT, SVD transform. (Ref.1, Chap.5)

Image Representation by Stochastic Models: Introduction, one dimensional Causal models, AR models, Non-causal representations, linear prediction in two dimensions. (Ref.1, Chap.6)

Image Enhancement: Point operations, Histogram modeling, spatial operations, Transform operations, Multi-spectral image enhancement, false color and Pseudo-color, Color Image enhancement. (Ref.1, Chap.7)

Image Filtering & Restoration: Image observation models, Inverse &Wiener filtering, Fourier Domain filters, Smoothing splines and interpolation, Least squares filters, generalized inverse, SVD and Iterative methods, Maximum entropy restoration, Bayesian methods, Coordinate transformation& geometric correction, Blind de-convolution. (Ref.1, Chap.8)

Image Analysis & Computer Vision: Spatial feature extraction, Transform features, Edge detection, Boundary Extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification Techniques. (Ref.1, Chap.9)

Image Reconstruction from Projections: Introduction, Radon Transform, Back projection operator, Projection theorem, Inverse Radon transform, Fourier reconstruction, Fan beam reconstruction, 3D tomography. (Ref.1,Chap.10)

Image Data Compression: Introduction, Pixel coding, Predictive techniques, Transform coding, Inter-frame coding, coding of two tone images, Image compression standards. (Ref.1, Chap.11)

Video Processing: Fundamental Concepts in Video – Types of video signals, Analog video, Digital video, Color models in video, Video Compression Techniques – Motion compensation, Search for motion vectors, H.261,H.263, MPEG I, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing. (Ref.4)

Reference Books:

1. Anil K. Jain, **"Fundamentals of Digital Image Processing,"** Pearson Education (Asia) Pte. Ltd./Prentice Hall of India, 2004.
2. Z. Li and M.S. Drew, **"Fundamentals of Multimedia"** Pearson Education (Asia) Pte. Ltd., 2004.
3. R. C. Gonzalez and R. E. Woods, **"Digital Image Processing"** 2nd edition, Pearson Education (Asia) Pte. Ltd/Prentice Hall of India, 2004.
4. M. Tekalp, **"Digital Video Processing",** Prentice Hall, USA, 1995.

RF and Microwave Circuit Design

Subject Code	: 14ECS423	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Wave Propagation in Networks: Introduction to RF/Microwave Concepts and applications; RF Electronics Concepts; Fundamental Concepts in Wave Propagation; Circuit Representations of two port RF/MW networks

Passive Circuit Design: The Smith Chart, Application of the Smith Chart in Distributed and lumped element circuit applications, Design of Matching networks.

Basic Considerations in Active Networks: Stability Consideration in Active networks, Gain Considerations in Amplifiers, Noise Considerations in Active Networks.

Active Networks: Linear and Nonlinear Design: RF/MW Amplifiers Small Signal Design, Large Signal Design, RF/MW Oscillator Design, RF/MW Frequency Conversion Rectifier and Detector Design, Mixer Design, RF/MW Control Circuit Design, RF/MW Integrated circuit design.

Reference Books:

1. Matthew M. Radmanesh**,** "**Radio Frequency and Microwave Electronics Illustrated,**" Pearson Education (Asia) Pte. Ltd., 2004.
2. Reinhold Ludwig and Pavel Bretchko, "**RF Circuit Design: Theory and Applications**," Pearson Education (Asia) Pte. Ltd., 2004.

Cryptographic Systems

Subject Code	: 14 ELD424	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Overview: Services, Mechanisms and attack models, Model for network security, Symmetric cipher model, Substitution techniques, Transposition techniques, Rotor machine, Steganography.

Block Ciphers and DES: Block cipher design principles, Block cipher modes of operation. Differential and Linear cryptanalysis 3DES, Rijndael system, AES, IDEA Fermat's and Euler's theorem, Big-O notation, Chinese Remainder Theorem, Fields, Group- isomorphism, Discrete Logarithm, Pohlig-Hellman algorithm, Pollard's p-1 factorization, pollard rho factorization algorithm.

Public Key Cryptography and RSA: Principles of public key cryptosystems, RSA algorithm, Integer Factorization and RSA, Miller-Rabin Test, Massey-Omura, ElGamal crypto systems, Knapsack problem.

Other Public Key Crypto Systems and Key Management: Key management, Diffie-Hellman key exchange, DH with multiple participants, Elliptic curve arithmetic, Elliptic curve cryptography, Analog of Massey –Omura, Analog of ElGamal crypto systems. Elliptic curve factorization - pollard's p-1 method, Lenstra's elliptic curve factorization algorithm, Hyper elliptic curve cryptography.

Message Authentication and Hash Functions: Authentication requirements, Authentication functions, Message authentication codes, Hash functions, Security of hash functions and MAC.

Digital Signature and Authentication Protocol: Digital signature, Authentication protocols, Digital signature standard, RSA digital signatures, ElGamal digital signatures and DSA, ECDSA Zero-knowledge proofs, Secret sharing schemes, Identification schemes.

Reference Books:

1. Neal Koblitz, **"A Course in Number Theory and Cryptography"**, -2nd Edition, Springer Verlag
2. Jeffrey Hoffstein,JillPipher,Joseph H. Silverman ,**"An Introduction to Mathematical Cryptography"** -Springer 2008
3. Behrouz A .Forouzan, DebdeeepMukhopadhyay, "**Cryptography and Network Security",** 2nd Edition, McGraw Hill
4. William Stallings, **"Cryptography and Network Security"**, 4thEdition, Pearson Education PHI.

Advanced Microcontrollers

Subject Code	: 14 ELD425	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 50	Exam Marks	: 100

Note: Microcontrollers have become prevalent in a number of applications such as instrumentation, industrial electronics, automotive electronics, robotics, etc. Advances in VLSI technology permit the integration of not only the processor but also the analog electronics, memory and peripherals necessary for system implementation; this allows low-cost system implementation. Some microcontrollers used in industrial electronics also provide some digital signal processing capability to further reduce the system cost.

Power dissipation is often a consideration in many systems and modern microcontrollers address it through the support of several low-power modes of operation. The aim of the course is to introduce advanced microcontrollers (16-bit and 32-bit).

Motivation for advanced microcontrollers – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Examples of applications.

MSP430 – 16-bit Microcontroller family. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus – architecture. The assembly language and „C" programming for MSP-430 microcontrollers. On-chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts.

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 – General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture.

Applications – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.

Reference Books:

1. Joseph Yiu " **The Definitive Guide to the ARM Cortex-M3,** , Newnes, (Elsevier), 2008.
2. John Davies, " **MSP430 Microcontorller Basics**", Newnes (Elsevier Science), 2008.

3. **MSP430 Teaching CD-ROM**, Texas Instruments, 2008.
4. **Sample Programs for MSP430** downloadable from msp430.com
5. David Patterson and John L. Henessay, "**Computer Organization and Design**", (ARM Edition), Morgan Kauffman.