LINEAR ALGEBRA

Subject Code	: **12EC046**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Linear Equations: Fields; system of linear equations, and its solution sets; elementary row operations and echelon forms; matrix operations; invertible matrices, LU-factorization. (Ref.2 Chap.1)

Vector Spaces: Vector spaces; subspaces; bases and dimension; coordinates; summary of row-equivalence; computations concerning subspaces. (Ref.1 Chap.2)

Linear Transformations: Linear transformations; algebra of linear transformations; isomorphism; representation of transformations by matrices; linear functionals; transpose of a linear transformation. (Ref.2 Chap.3)

Canonical Forms: Characteristic values; annihilating polynomials; invariant subspaces; direct-sum decompositions; invariant direct sums; primary decomposition theorem; cyclic bases; Jordan canonical form. Iterative estimates of characteristic values. (Ref.1 Chap.8)

Inner Product Spaces: Inner products; inner product spaces; orthogonal sets and projections; Gram-Schmidt process; QR-factorization; least-squares problems; unitary operators. (Ref.2 Chap.1)

Symmetric Matrices and Quadratic Forms: Digitalization; quadratic forms; constrained optimization; singular value decomposition. (Ref.2 Chap.7)

REFERENCE BOOKS:

1.David. C. Lay, "**Linear Algebra and its Applications**," 3rd edition, Pearson Education (Asia) Pte. Ltd, 2005.

2.Kenneth Hoffman and Ray Kunze, "**Linear Algebra**," 2nd edition, Pearson Education (Asia) Pte. Ltd/ Prentice Hall of India, 2004. .

3.Bernard Kolman and David R. Hill, "**Introductory Linear Algebra with Applications**," Pearson Education (Asia) Pte. Ltd, 7th edition, 2003.

4.Gilbert Strang**,** "**Linear Algebra and its Applications**," 3rd edition, Thomson Learning Asia, 2003.

DIGITAL CIRCUITS AND LOGIC DESIGN

Subject Code	: **12EC029**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks.

Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic

Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities and Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, Decompositions, Synthesis of Multiple Machines.

State—Identifications and Fault-Detection Experiments: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault-Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection Experiments for Machines which have no Distinguishing Sequences.

REFERENCE BOOKS:

1.Zvi Kohavi, "**Switching and Finite Automata Theory**", 2nd Edition. Tata McGraw Hill Edition

2.Charles Roth Jr., "**Digital Circuits and logic Design**",

3.Parag K Lala, "**Fault Tolerant and Fault Testable Hardware Design**", Prentice Hall Inc. 1985.

4.E. V. Krishnamurthy, "**Introductory Theory of Computer**", Macmillan Press Ltd, 1983

5.Mishra & Chandrasekaran, "**Theory of Computer Science – Automata, Languages and Computation**", 2nd Edition, PHI,2004

Laboratory Experiments:

I. Digital Circuits & Logic Design

1.Devise a minimal-length binary code to represent the state of a phone: no-work, dial-tone, dialing, busy, connected, disconnected, and ringing.
2. Write Boolean equation for a BCD decoder, that is, a decoder that has a BCD code word as input and that has outputs yo through y9. Draw a circuit that uses AND and OR gates and inverters to implement the decoder.
3. Test the circuit diagram for a multiplexer that selects amoung four sources of data, each of which is encoded with three bits. The circuit should be implemented 4-to-1 multiplexers.
4. Design circuit that has as input, a transmit clock and an NRZ serial data signal and htat generates a Manchester encoded serial data signal as output.
5. Develop a circuit of a 4-bit Gray code to unsigned binary converter implemented using a combinational ROM.
6. Develop a circuit that calculates the average of 16-bit 2s-complement signed numbers, without checking for overflow.
All the above experiments are to be tested with any suitable simulator or a HDL.
Any experiments can be included the supports the theory.

AUTOMOTIVE ELECTRONICS

Subject Code	:**12EC117**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System, Battery, Starting System. **s**
Air/Fuel Systems – Fuel Handling, Air Intake System, Air/ Fuel Management.

Sensors – Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor
Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator
Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control
Communication – Serial Data, Communication Systems, Protection, Body and Chassis Electrical Systems, Remote Keyless Entry, GPS

Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension
Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters.

Integrated Body – Climate Control Systems, Electronic HVAC Systems, Safety Systems – SIR, Interior Safety, Lighting, Entertainment Systems
Automotive Diagnostics – Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems

Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System

References: -

1.William B. Ribbens: Understanding Automotive Electronics, 6th Edition, SAMS/Elsevier Publishing

2.Robert Bosch GmbH: Automotive Electrics Automotive Electronics Systems and Components, 5th edition, John Wiley& Sons Ltd., 2007

CMOS VLSI DESIGN

Subject Code	: **12EC021**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03

MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter.

CMOS Process Technology: Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect) , Circuit elements, resistor , capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

Basics of Digital CMOS Design: Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits - Introduction, Behavior of hi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuits techniques, Dynamic CMOS circuit techniques

CMOS Analog Design: Introduction, Single Amplifier. Differential Amplifier, Current mirrors, Band gap references, basis of cross operational amplifier.

Dynamic CMOS and Clocking: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS., static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements.

REFERENCE BOOKS:

1.Neil Weste and K. Eshragian, "**Principles of CMOS VLSI Design: A System Perspecti**", 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.

2. Wayne, Wolf, "**Modern VLSI Design: System on Silicon**", Pearson Education, Second Edition

3.Douglas A Pucknell & Kamran Eshragian , "**Basic VLSI Design**" PHI 3rd Edition (original Edition – 1994)

4.Sung Mo Kang & Yosuf Lederabic Law, "**CMOS Digital Integrated Circuits: Analysis and Design**", McGraw-Hill (Third Edition)

CMOS VLSI DESIGN LAB:
(Should use Cadence/Synopsis/Menta-graphics Tools)

DIGITAL DESIGN

ASIC-DIGITAL DESIGN FLOW

1. Write Verilog Code for the following circuits and their Test Bench for **verification**, observe the waveform and **synthesize** the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

1.An inverter
2.Circular Buffer
3.Transmission Gate
4.Basic/universal gates
5.Flip flop -RS, D, JK, MS, T
6.Serial & Parallel adder
7.4-bit counter [Synchronous and Asynchronous counter]
8.Successive approximation register [SAR]

** An appropriate constraint should be given*

PART - B
ANALOG DESIGN

Analog Design Flow

1. Design an **Inverter** with given specifications*, completing the design flow mentioned below:
   a. **Draw the schematic** and verify the following
      i) DC Analysis
      ii) Transient Analysis
   b. **Draw the Layout** and verify the DRC, ERC
   c. Check for LVS

d. Extract RC and back annotate the same and verify the Design
e. Verify & Optimize for Time, Power and Area to the given constraint***

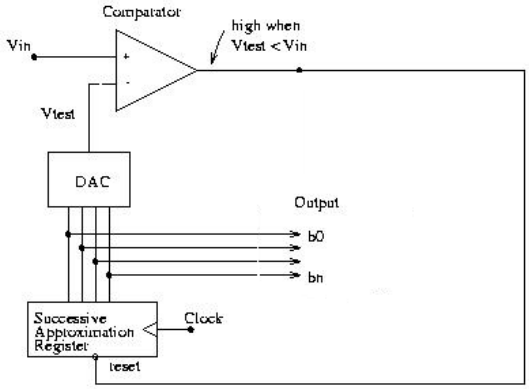
2. Design the following circuits with given specifications*, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.
      i) A Single Stage differential amplifier
      ii) Common source and Common Drain amplifier

3. Design an **op-amp** with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii). AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

4. Design a **4 bit R-2R based DAC** for the given specification and completing the design flow mentioned using given op-amp in the library**.
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

5. For the **SAR based ADC** mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.

[Specifications to GDS-II]



***** Appropriate specification should be given.
** Applicable Library should be added & information should be given to the Designer.
*** An appropriate constraint should be given

(***Any other appropriate experiments supportive to the course can be added)***

ELECTIVE – I

ADVANCED MICROCONTROLLERS

Subject Code	: **12EC116**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Microcontrollers have become prevalent in a number of applications such as instrumentation, industrial electronics, automotive electronics, robotics, etc. Advances in VLSI technology permit the integration of not only the processor but also the analog electronics, memory and peripherals necessary

for system implementation; this allows low-cost system implementation. Some microcontrollers used in industrial electronics also provide some digital signal processing capability to further reduce the system cost.
Power dissipation is often a consideration in many systems and modern microcontrollers address it through the support of several low-power modes of operation. The aim of the course is to introduce advanced microcontrollers (16-bit and 32-bit).

Motivation for advanced microcontrollers – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Examples of applications. 3 hours

MSP430 – 16-bit Microcontroller family. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus –architecture. The assembly language and 'C' programming for MSP-430 microcontrollers. On-chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts. 15 hours

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 – General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture.
15 hours

Applications – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.
7 hours.

References Books:

1.Joseph Yiu " **The Definitive Guide to the ARM Cortex-M3,** , Newnes, (Elsevier), 2008.
2.John Davies, " **MSP430 Microcontorller Basics**", Newnes (Elsevier Science), 2008.
3.**MSP430 Teaching CD-ROM**, Texas Instruments, 2008.
4.**Sample Programs for MSP430** downloadable from msp430.com
5.David Patterson and John L. Henessay, "**Computer Organization and Design**", (ARM Edition), Morgan Kauffman.

DIGITAL SYSTEM DESIGN USING VERILOG

Subject Code	: **12EC121**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction and Methodology:
Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.

Combinational Basics:
Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.

Number Basics:
Unsigned and Signed Integers, Fixed and Floating-point Numbers.

Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology.

Memories: Concepts, Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.

Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory.

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.
Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test,

Reference Books:

1.“**Digital Design: An Embedded Ssytems Approach Using VERILOG”,** Peter J. Ashenden, Elesvier, 2010.

DIGITAL SIGNAL COMPRESSION

Subject Code	: **12EC030**	IA Marks	: 50

No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction: Compression techniques, Modeling & coding, Distortion criteria, Differential Entropy, Rate Distortion Theory, Vector Spaces, Information theory, Models for sources, Coding – uniquely decodable codes, Prefix codes, Kraft McMillan Inequality.(Ref.1 Chap.1 & 2.)

Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm, Tree structured VQ, Structured VQ, Variations of VQ – Gain shape VQ, Mean removed VQ, Classified VQ, Multistage VQ, Adaptive VQ, Trellis coded quantization(Ref.1 Chap.9 & 10.)

Differential Encoding: Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation, Speech coding – G.726, Image coding.(Ref.1 Chap.11)

Transform Coding: Transforms – KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression – JPEG, Application to audio compression. (Ref.4 Chap.13)

Sub-band Coding: Filters, Sub-band coding algorithm, Design of filter banks, Perfect reconstruction using two channel filter banks, M-band QMF filter banks, Poly-phase decomposition, Bit allocation, Speech coding – G.722, Audio coding – MPEG audio, Image compression. (Ref.1 Chap.14)

Wavelet Based Compression: Wavelets, Multiresolution analysis & scaling function, Implementation using filters, Image compression – EZW, SPIHT, JPEG 2000. (Ref.4 Chap. 8)
Analysis/Synthesis Schemes: Speech compression – LPC-10, CELP, MELP, Image Compression – Fractal compression. (Ref.1 Chap.17)

Video Compression: Motion compensation, Video signal representation, Algorithms for video conferencing & videophones – H.261, H. 263, Asymmetric applications – MPEG 1, MPEG 2, MPEG 4, MPEG 7, Packet video. (Ref.4 Chap.10,11,12)

Lossless Coding: Huffman coding, Adaptive Huffman coding, Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding,

Arithmetic coding, Algorithm implementation, Applications of Arithmetic coding, Dictionary techniques – LZ77, LZ78, Applications of LZ78 – JBIG, JBIG2, Predictive coding – Prediction with partial match, Burrows Wheeler Transform, Applications – CALIC, JPEG-LS, Facsimile coding – T.4, T.6.(Ref.4 Chap.7.)

REFERENCE BOOKS:

1.K. Sayood**,** "**Introduction to Data Compression**," Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.

2.N. Jayant and P. Noll, **"Digital Coding of Waveforms: Principles and Applications to Speech and Video**," Prentice Hall, USA, 1984.

3.D. Salomon, "**Data Compression: The Complete Reference**", Springer, 2000.

4.Z. Li and M.S. Drew**,** "**Fundamentals of Multimedia**," Pearson Education (Asia) Pte. Ltd., 2004.

SEMESTER II

ADVANCES IN VLSI DESIGN

Subject Code	: **12EC009**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Review of MOS Circuits: MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.

MESFETS: MESFET and MODFET operations, quantitative description of MESFETS.

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological

computing Mole electronics-molecular Diode and diode- diode logic .Defect tolerant computing,

Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

Special Circuit Layouts and Technology Mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out.

System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

REFERENCE BOOKS:

1.Kevin F Brrnnan "**Introduction to Semi Conductor Device**", Cambridge publications
2.Eugene D Fabricius "**Introduction to VLSI Design**", McGraw-Hill International publications
3.D.A Pucknell "**Basic VLSI Design**", PHI Publication
4.Wayne Wolf, "**Modern VLSI Design**" Pearson Education, Second Edition, 2002

NANOELECTRONICS

Subject Code	: **12EC054**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction: Overview of nanoscience and engineering,Development milestones in microfabrication and electronic industry,Moores law and continued miniaturization,Classification of Nano structures,Electronic properties of atoms and solids: Isolated atom, Bonding between atoms,Giant molecular solids,Free electron models and energy bands,crystalline solids, Periodicity of crystal lattices, Electronic conduction,effects of nanometer length scale,Fabrication methods: Top down processes,Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems.

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk ,surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Inorganic semiconductor nanostructures: overview of semiconductor physics,Quantum confinement in semiconductor nanostructures:quantum wells,quantum wires,quantum dots,superlattices,band offsets,electronic density of states.

Fabrication techniques: requirements of ideal semiconductor,epitaxial growth of quantum wells, lithography and etching,cleaved edge overgrowth,growth of vicinal substrates,strain induced dots and wires,electrostatically induced dots and wires,Quantum well width fluctuations,thermally annealed quantum wells,semiconductor nanocrystals,collidal quantum dots,self-assembly techniques.

Physical processes: modulation doping,quantum hall effect,resonant tunneling,charging effects,ballistic carrier transport,Inter band absorption, intraband absorption,Light emission processes,phonon bottleneck, quantum confined stark effect,nonlinear effects,coherence and dephasing, characterization of semiconductor nanostructures:optical electrical and structural.

Methods of measuring properties:structure:
atomic,crystallography,microscopy,spectroscopy. Properties of nanoparticles: metal nano clusters, semiconducting nanoparticles, rare gas and molecular clusters, methods of synthesis(RF, chemical, thermolysis,pulsed laser methods) Carbon nanostructures and its applications(field emission and shielding,computers,fuel cells,sensors,catalysis).Self assembling nanostructured molecular materials and devices: building blocks,principles of self assembly, methods to prepare and pattern nanoparticles,templated nanostructures,liquid crystal mesophases.Nanomagnetic materials and devices:magnetism,materials,magneto resistance,nanomagnetism in technology,challenges facing nano magnetism.

Applications: Injection lasers,quantum cascade lasers,singe photon sources,biological tagging,optical memories,coulomb blocade devices,photonic structures,QWIP's,NEMS,MEMS.

References:

1.Ed Robert Kelsall,Ian Hamley,Mark Geoghegan, " **Nanoscale science and technology**" ,John wiley and sons,2007.

2.Charles P Poole,Jr,Frank J owens "**Introduction to Nanotechnology**" ,John wiley,copyright 2006,Reprint 2011.

3.Ed William A Goddard III,Donald W Brenner,Sergey Edward Lyshevski,Gerald J Lafrate, " **Hand Book of Nanoscience Engineering and Technology**" ,CRC press,2003

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Subject Code	: **12EC077**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Schedule Algorithms: A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

Testing: Simulation, Types of simulators, basic components of a simulator, fault simulation Techniques, Automatic test pattern generation methods (ATPG), design for Testability (DFT) Techniques.

REFERENCE BOOKS:

1.Giovanni De Micheli, "**Synthesis and Optimization of Digital Circuits**", Tata McGraw-Hill, 2003.

2.Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer, "**Logic Synthesis**", McGraw-Hill, USA, 1994.

3.Neil Weste and K. Eshragian, **"Principles of CMOS VLSI Design: A System Perspective",** 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.

4.Kevin Skahill, "**VHDL for Programmable Logic**," Pearson Education (Asia) Pte. Ltd., 2000.

ADVANCED EMBEDDED SYSTEM

Subject Code	: **12EC118**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Typical Embedded System : Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components Characteristics and Quality Attributes of Embedded Systems

Hardware Software Co-Design and Program Modelling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modelling Language, Hardware Software Trade-offs

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages Real-Time Operating System (RTOS) based Embedded System Design.

Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Trends in the Embedded Industry : Processor Trends in Embedded System, Embedded OS Trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks.

Reference Books:

1.Introduction to Embedded Systems, Shibu K V, Tata McGraw Hill Education Private Limited, 2009

2.Embedded Systems – A contemporary Design Tool, James K Peckol, John Weily, 2008.

Advanced Embedded System Lab:

Lab Experiments :-

1. Use the EDA (Electronic Design Automation) tools to learn the Embedded Hardware Design and for PCB design.
2. Familiarize the different entities for the circuit diagram design.
3. Familiarize with the layout design tool, building blocks, component placement, routings, design rule checking etc.

Embedded Programming Concepts (RTOS):

4. Create 'n' number of child threads. Each thread prints the message " I'm in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
5. Implement the multithread application satisfying the following :
    1. Two child threads are crated with normal priority.
    2. Thread 1 receives and prints its priority and sleeps for 50ms and then quits.
    3. Thread 2 prints the priority of the thread 1 and rises its priority to a bove normal and retrieves the new priority of thread 1,

prints it and then quits.

4. The main thread waits for the child thread to complete its job and quits.

6.Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.

7. Test the program below using multithread application-
   1. The main thread creates a child thread with default stack size and name 'Child_Thread'.
   2. The main thread sends user defined messages and the message 'WM_QUIT' randomly to the child thread.
   3. The child thread processes the message posted by the main thread and quits when it receives the 'WM_QUIT' messge.
   4. The main thread checks the termination of the child thread and quits when the child thread complete its execution.
   5. The main thread continues sending the random messages to the child thread till the 'WM_QUIT' message is sent to child thread.
   6. The messaging mechanism between the main thread and child thread is synchronous.

8.Test the program application for creating an anonymous pipe with 512 bytes of size and pass the 'Read Handle' of the pipe to a second process using memory mapped object. The first process writes a message ' Hi from Pipe Server'. The 2nd process reads the data written by the pipe server to the pipe and displays it on the console. Use event object for indicating the availability of data on the pipe and mutex objects for synchronizing the access in the pipe.

9. Create a POSIX based message queue for communicating between two tasks as per the requirements given below:-
   a.Use a named message queue with name 'MyQueue'.
   b.Create two tasks(Task1 & Task2) with stack size 4000 & priorities 99 & 100 respectively.
   c.Task 1 creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console.
   d.Task2 open the message queue and posts the message 'Hi from Task2'.
   e.Handle all possible error scenarios appropriately.

Any other experiments can be included to support the theory.

ELECTIVE II

ASIC DESIGN

Subject Code	: **12EC012**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Note : All Designs Will Be Based On VHDL

Introduction: Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, ASIC cell libraries

Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers

ASIC Library Design: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.

Low-level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation

Programmable ASIC: programmable ASIC logic cell, ASIC I/O cell

A Brief Introduction to Low Level Design Language: an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation;

ASIC Construction Floor Planning and Placement and Routing: Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

REFERENCE BOOKS:

1.M.J.S .Smith, - "**Application - Specific Integrated Circuits**" – Pearson Education, 2003

2.Jose E.France, Yannis Tsividis, "**Design of Analog-Digital VLSI Circuits for Telecommunication and Signal Processing**", Prentice Hall, 1994.

3. Malcolm R.Haskard; Lan. C. May, "**Analog VLSI Design - NMOS and CMOS**" Prentice Hall, 1998.

4.Mohammed Ismail and Terri Fiez, "**Analog VLSI Signal and Information Processing"**, McGraw Hill, 1994.

SPEECH AND AUDIO PROCESSING

Subject Code	: **12EC075**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

INTRODUCTION: The speech signal, signal processing, digital signal processing, digital speech processing, digital transmission and storage of speech, speech synthesis systems, speaker verification and identification, speech recognition systems, aids-to-the-handicapped, enhancement of signal quality (Ref.1 Chap.1)

Digital Models for the Speech Signal: Process of speech production, the mechanism of speech production. (Ref.1 Chap.3)

Time Domain Models For Speech Processing: Time dependent processing of speech, Short time energy and average magnitude, Short time average zero crossing rate, Speech vs silence discrimination using energy & zero crossings. (Ref.1 Chap.4)

Digital Representations of the Speech Waveform: Sampling speech signals, Review of statistical model for speech, Instantaneous quantization, Uniform quantization, Instantaneous companding, quantization for optimum SNR (Ref.1 Chap.5)

Short Time Fourier Analysis: Definitions and properties, Fourer transform interpretation, Linear Filtering interpretation, sampling rates, time and frequency, Filter bank summation method, Short time synthesis, Overlap addition method, short time synthesis (Ref.1 Chap.6)

Linear Predictive Coding of Speech: Basic principles of linear predictive analysis, autocorrelation method, covariance method, computation of gain (Ref.1 Chap.8)

Digital speech processing for man-machine communication by voice: Voice response systems, general considerations in the design of voice response systems, multiple output digital voice response systems, speech synthesis by concatenation of formant coded words, typical applications of computer voice response systems, speaker recognition systems, speaker verification systems, speaker identification systems (Ref.1 Chap.9)

Audio Processing: Basics of digital audio, digitization of sound, Nyquist theorem, signal to noise ratio, signal to quantization noise ratio, linear and nonlinear quantization, audio filtering, audio quality vs. data rate, synthetic sounds, MIDI, MIDI overview, hardware aspects of MIDI, structure of MIDI messages, general MIDI, MIDI to WAV conversion, quantization and transmission of audio, coding of audio, pulse code modulation, differential coding of audio, lossless predictive coding, DPCM, DM, ADPCM. (Ref.2 Chap.6)

REFERENCE BOOKS:

1.L. R. Rabiner and R. W. Schafer**,** "**Digital Processing of Speech Signals"**, Pearson Education (Asia) Pte. Ltd., 2004.

2.Z. Li and M.S. Drew**,** "**Fundamentals of Multimedia"**, Pearson Education (Asia) Pte. Ltd., 2004

REAL TIME OPERATING SYSTEMS

Subject Code	: **12EC126**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Esecutive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Reentrant Functions.

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.

I/O Resources:
Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

Memory:
Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash filesystems.

Multi-resource Services:
Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services:
Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

Embedded System Components:
Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components:
Execptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging.

Performance Tuning:
Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.

High availability and Reliability Design:
Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design trade offs, Hierarchical applications for Fail-safe design.

Design of RTOS – PIC microcontroller. **(Chap 13 of book Myke Predko)**

Reference Books:

1. "**Real-Time Embedded Systems and Components" ,** Sam Siewert, Cengage Learning India Edition, 2007.
2. " **Programming and Customizing the PIC microcontroller" ,** Myke Predko, 3rd Ed, TMH, 2008.
3. "**Programming for Embedded Systems**", Dreamtech Software Team, Jhon Wiley, India Pvt. Ltd., 2008.

Real Time Operating Systems:
Laboratory Experiments -
(Reference Book 3 can be used to give Lab. Assignments)

USE LINUX/SOLARIS/QNX OS ONLY.

1. Implement simple IPC protocol.
2. Implement Semaphore and Mutex for any given applications.
3. Communicate between 2 PCs using Socket programming or message passing techniques (ie., MPI).
4. Create 'n' number of child threads. Each thread prints the message " I'm in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.

5. Implement the multithread application satisfying the following :
   i. Four child threads are crated with normal priority.
   ii. Thread 1& 2 receives and prints its priority and sleeps for 50ms and then quits.
   iii. Thread 3&4 prints the priority of the thread 1 &2 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.
   iv. The main thread waits for the child thread to complete its job and quits.
6. Implement the usage of send and receive primitives with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.

7. Test the program below using multithread application-
   1.The main thread creates a child thread with default stack size and name 'Child_Thread'.
   2.The main thread sends user defined messages and the message 'WM_QUIT' randomly to the child thread.
   3.The child thread processes the message posted by the main thread and quits when it receives the 'WM_QUIT' messge.
   4.The main thread checks the termination of the child thread and quits when the child thread complete its execution.
   5.The main thread continues sending the random messages to the child thread till the 'WM_QUIT' message is sent to child thread.
   6.The messaging mechanism between the main thread and child thread is synchronous.

8. Test the program application for creating an anonymous pipe with 512 bytes of size and pass the 'Read Handle' of the pipe to a second process using memory mapped object. The first process writes a message ' Hi from Pipe Server'. The 2nd process reads the data written by the pipe server to the pipe and displays it on the console. Use event object for indicating the availability of data on the pipe and mutex objects for synchronizing the access in the pipe. For synchronization semaphore/mutex can be used.

9. Create a POSIX based message queue for communicating between several tasks as per the requirements given below:-

i. Use a named message queue with name 'MyQueue'.
ii. Create N tasks with stack size 4000 & priorities (n-1) & n respectively. N can be any number but more than 4.
iii. Tasks creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console.
iv. Tasks open the message queue and posts the message 'Hi from Task(n-1)'.
i.Handle all possible error scenarios appropriately.

MINI PROJECTS: (optional)

1. Implement protocol converter (refer book 3 given in the RTOS theory)
2. Implement System Calls for the RTOS using RTLinux.
3. Implement an IP phone.
4. Implement Device Driver.

ANY EXPERIMETNS CAN BE ADDED TO SUPPLEMENT THE THEORY. ABOVE IS THE ONLY GUIDE LINES.

III – SEMESTER

RF AND MICROWAVE CIRCUIT DESIGN

Subject Code	: **12EC071**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Wave Propagation in Networks: Introduction to RF/Microwave Concepts and applications; RF Electronics Concepts; Fundamental Concepts in Wave Propagation; Circuit Representations of two port RF/MW networks

Passive Circuit Design: The Smith Chart, Application of the Smith Chart in Distributed and lumped element circuit applications, Design of Matching networks.

Basic Considerations in Active Networks: Stability Consideration in Active networks, Gain Considerations in Amplifiers, Noise Considerations in Active Networks.

Active Networks: Linear and Nonlinear Design: RF/MW Amplifiers Small Signal Design, Large Signal Design, RF/MW Oscillator Design, RF/MW Frequency Conversion Rectifier and Detector Design, Mixer Design, RF/MW Control Circuit Design, RF/MW Integrated circuit design.

REFERENCE BOOKS:

1. Matthew M. Radmanesh**, "Radio Frequency and Microwave Electronics Illustrated"**, Pearson Education (Asia) Pte. Ltd., 2004.
2. Reinhold Ludwig and Pavel Bretchko, "**RF Circuit Design: Theory and Applications",** Pearson Education (Asia) Pte. Ltd., 2004.

ELECTIVE - III

PROCESS CONTROL INSTRUMENTATION

Subject Code	: **12EC066**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction to Process Control, objects and benefits, mathematical modeling;

Principles, Modeling Analysis for Process Control; Dynamic behavior of typical process systems;

PID Controller tuning for dynamic performance, stability analysis and controller tuning;

Digital Implementation of process control;

Temperature Measurement using IC temperature sensor, thermocouple & RTD; Measurement of strain, force, displacement weight, flow and pressure;

Signal Conditioning & Transmission, 4-20mA current transmitter for LVDT, signal conditioning for low level DC & AC signals, concept of shielding, grounding & EMI

REFERENCE BOOKS:

1.Thomas E Marlin, "**Designing Process & Control Systems for Dynamic Performance",**2-ed – 2000

2.Anvekar & Sonde, "**Electronic Data Converters**", TMH

MODERN DSP

Subject Code	: **12EC123**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Goal of the course – Advances in Digital Signal Processing involve variable sampling rates and thus the multirate signal processing and hence their applications in communication systems and signal processing. It is intended to introduce a basic course in multirate signal processing especially meant for students of branches eligible for M Tech courses in EC related disciplines.

Introduction and Discrete Fourier Transforms: Signals, Systems and Processing, Classification of Signals**,** The Concept of Frequency in Continuous-Time and Discrete-Time Signals**,** Analog-to-Digital and Digital-to-Analog Conversion**,** Frequency-Domain Sampling: The Discrete Fourier Transform**,** Properties of the DFT**,** Linear Filtering Methods Based on the DFT.(Ref.1 Chap. 1 & 7)

Design of Digital Filters: General Considerations, Design of FIR Filters, Design of IIR Filters from Analog Filters, Frequency Transformations.(Ref.1 Chap. 10)

Multirate Digital Signal Processing: Introduction, Decimation by a factor 'D', Interpolation by a factor 'I', Sampling rate Conversion by a factor 'I/D', implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion, Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank.(Ref.1 Chap. 11)

Adaptive Filters: Applications of Adaptive Filters, Adaptive Direct Form FIR Filters- The LMS Algorithm, Adaptive Direct Form Filters-RLS Algorithm. (Ref.1 Chap. 13)

References:

1. Proakis and Manolakis, "**Digital Signal Processing**", Prentice Hall 1996. (third edition).

2. Roberto Cristi, "**Modern Digital Signal Processing**", Cengage Publishers, India, (erstwhile Thompson Publications), 2003.

3. S.K. Mitra, "**Digital Signal Processing: A Computer Based Approach"**, III Ed, Tata McGraw Hill, India, 2007.

4. E.C. Ifeachor and B W Jarvis, "**Digital Signal Processing, a practitioners approach**," II Edition, Pearson Education, India, 2002 Reprint.

ADVANCED CONTROL SYSTEMS

Subject Code	: **12EC005**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Digital Control Systems: Review of difference equations and Z — transforms, Z- transfer function (Pulse transfer function), Z.-. Transforms analysis sampled data systems, Stability analysis (Jury's Stability Test and Bilinear Transformation), Pulse transfer functions and different configurations for closed loop Discrete-time control systems

Modern Control Theory: I, State model for continuous time and discrete time systems, Solutions of state equations (for both continuous and discrete systems), Concepts of controllability and observability (For both continuous and discrete systems), Pole Placement by state feedback (for both continuous and discrete systems), Full order and reduced order observes (for both continuous and discrete systems), Dead beat control by state feedback, Optimal control problems using state variable approach, State Regulator and output regulator, Concepts of Model reference control systems, Adaptive Control systems and design

Non Linear Control Systems: Common nonlinearities, Singular Points, Stability of nonlinear systems - Phase plane analysis and describing function analysis, Liapunoy's stability criterion, Popov's criterion

REFERENCE BOOKS:

1.Ogata. K. "**Modern Control Engineering**", PHI

2.Ogata K "**Discrete time Control Systems**", Pearson Education

3.Nagarath and Gopal, "**Control Systems Engineering**", Wiley Eastern Ltd

4.M Gopal "**Modem Control System Theory**"; Wiley Eastern Ltd.

5.M. Gopal, "**Digital Control & State Variable Methods**", TMH, 2003.

ELECTIVE – IV

LOW POWER VLSI DESIGN

Subject Code	: **12EC047**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction : Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

REFERENCE BOOKS:

1.Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**" Wiley, 2000

2.Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002

3.Rabaey, Pedram, "**Low Power Design Methodologies**" Kluwer Academic, 1997

ADVANCED COMPUTER ARCHITECTURE

Subject Code	: **12EC003**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Parallel Computer Models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and Network Properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

Principles of Scalable Performance: Performance Metrics and Mesaures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approches.

Advanced Processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor Architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,

Multithread and Dataflow Architecure: Principles of Multithreading, Scalable and Multithreaded Architecure, Dataflow Architecture

REFERENCE BOOKS:

1.Kai Hwang, "Advanced computer architecture"; TMH.
2.Kai Hwang and Zu, "Scalable Parallel Computers Architecture"; MGH.
3.M.J Flynn, "Computer Architecture, Pipelined and Parallel Processor Design"; Narosa Publishing.
4.D.A.Patterson, J.L.Hennessy, "Computer Architecture :A quantitative approach"; Morgan Kauffmann feb,2002.

IMAGE AND VIDEO PROCESSING

Subject Code	: **12EC043**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction: 2D systems, Mathematical preliminaries – Fourier Transform, Z Transform, Optical & Modulation transfer function, Matrix theory, Random signals, Discrete Random fields, Spectral density function.(Ref.1, Chap.2)

Image Perception: Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision.(Ref.1, Chap.3)

Image Sampling and Quantization: Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization.(Ref.1, Chap.4)

Image Transforms: Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, DFT, DCT, DST, Hadamard, Haar, Slant, KLT, SVD transform.(Ref.1, Chap.5)

Image Representation by Stochastic Models: Introduction, one-dimensional Causal models, AR models, Non-causal representations, linear prediction in two dimensions. (Ref.1, Chap.6)

Image Enhancement: Point operations, Histogram modeling, spatial operations, Transform operations, Multi-spectral image enhancement, false color and Pseudo-color, Color Image enhancement.(Ref.1, Chap.7)

Image Filtering & Restoration: Image observation models, Inverse & Wiener filtering, Fourier Domain filters, Smoothing splines and interpolation, Least squares filters, generalized inverse, SVD and Iterative methods, Maximum entropy restoration, Bayesian methods, Coordinate transformation & geometric correction, Blind de-convolution. (Ref.1, Chap.8)
Image Analysis & Computer Vision: Spatial feature extraction, Transform features, Edge detection, Boundary Extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification Techniques. (Ref.1, Chap.9)

Image Reconstruction from Projections: Introduction, Radon Transform, Back projection operator, Projection theorem, Inverse Radon transform, Fourier reconstruction, Fan beam reconstruction, 3D tomography.(Ref.1, Chap.210)

Image Data Compression: Introduction, Pixel coding, Predictive techniques, Transform coding, Inter-frame coding, coding of two tone images, Image compression standards. (Ref.1, Chap.11)

Video Processing: Fundamental Concepts in Video – Types of video signals, Analog video, Digital video, Color models in video, Video Compression Techniques – Motion compensation, Search for motion vectors, H.261, H.263, MPEG I, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing. Ref 4.

REFERENCE BOOKS:

1.K. Jain**,** "**Fundamentals of Digital Image Processing**," Pearson Education (Asia) Pte. Ltd./Prentice Hall of India, 2004.

2.Z. Li and M.S. Drew**, "Fundamentals of Multimedia**," Pearson Education (Asia) Pte. Ltd., 2004.

3.R. C. Gonzalez and R. E. Woods, "**Digital Image Processing**," 2nd edition, Pearson Education (Asia) Pte. Ltd/Prentice Hall of India, 2004.

4. M. Tekalp, "**Digital Video Processing**," Prentice Hall, USA, 1995.