# B.M.S. COLLEGE OF ENGINEERING
# IEEE SSCS

IEEE Solid-State Circuit Society
BMSCE IEEE Student Branch Chapter

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| Name of the event | VERILOG-Synthesis Workshop |
| Date | 25-11-2025 |
| Time | 2 PM – 5 PM |
| Venue | L303, COE Lab, 3rd Floor, ECE Department |

## *OBJECTIVE OF THE SESSION*

The workshop aimed to introduce students to the fundamentals of Verilog synthesis and develop a practical understanding of the synthesis flow. The session focused on gate-level interpretation, the impact of coding style on hardware efficiency, and improving students' confidence in digital design workflows.

## *BRIEF SUMMARY*

The IEEE SSCS BMSCE Chapter conducted the *Verilog-Synthesis Workshop* on 15th November 2025 at the COE Lab, ECE Department. The event was fully handled by the IEEE SSCS club members and saw participation from 18 students.

The session covered the essentials of Linux, Verilog, and the Synopsys synthesis flow, giving students a complete overview of the digital design pipeline. Participants were introduced to basic Linux commands, key Verilog concepts, and the use of Synopsys tools to perform RTL synthesis and interpret gate-level outputs. The workshop emphasized understanding how coding style affects area, timing, and power.

Students also explored example designs, viewed synthesis reports, and engaged in interactive discussions that clarified practical implementation challenges. The focused batch size enabled smooth guidance and active participation.

Overall, the workshop provided valuable exposure to industry-relevant tools and strengthened the participants' foundation in digital and VLSI design.

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Fig 1.

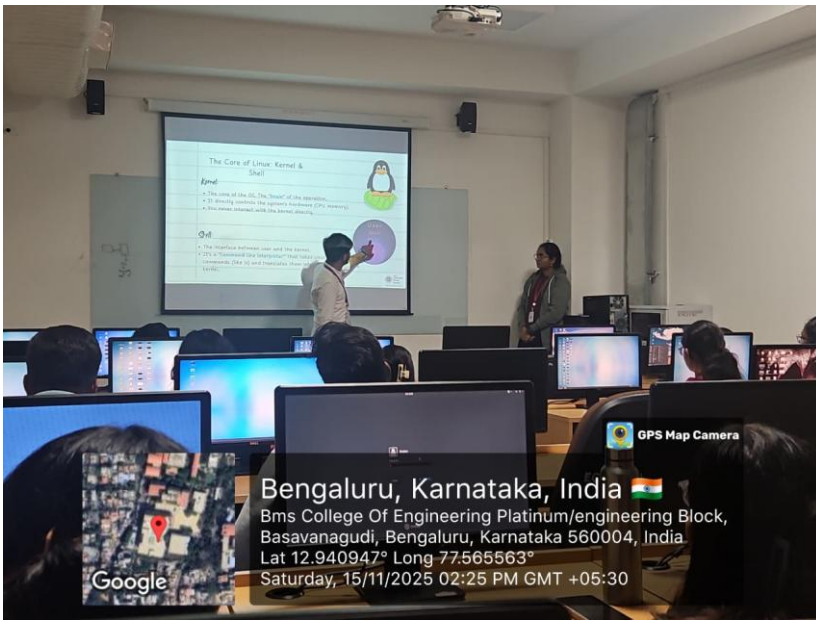


Fig 2.