Department of Electronics and Communication Engineering

B.M.S COLLEGE OF ENGINEERING

(Autonomous College Affiliated to Visvesvaraya Technological University, Belgaum)

Bull Temple Road, Basavanagudi, Bangalore-560019.

2022 - 2023

Report on

"Timeline of events of IEEE Solid State Circuits Society Chapter"

1. Inauguration of IEEE Antennas and Propagation Society and IEEE Solid-state Circuits Society Student Branch chapters - 13th May, 2023.

The inauguration of IEEE Antennas and Propagation Society and IEEE Solid-state Circuits Society student branch chapters took place on May 13, 2023, at 10:00 AM in the ECE Seminar Hall. The event was a success, co-hosted by ELSOC BMSCE and Ninaad BMSCE, with around 100 attendees including students, professors, and guests from Synopsys Inc.

The Chief Guest, Smt. Suman Dwivedi, a senior manager at Synopsys Inc. with extensive experience in the semiconductor industry, and Guest of Honour, Dr. Chandrashekar B U, a principal engineer at Synopsys Inc. with 30 years of industry experience, were recognized. They both have strong affiliations with IEEE and shared their insights.

The event featured introductions to the IEEE APS and SSCS Student Chapters, including their objectives and plans, as well as welcome speeches. Dr. Bheemsha emphasized the importance of these student chapters for holistic development. The Chief Guest delivered an informative talk on semiconductor chip physical design, highlighting industry advancements and the role of Synopsys. She also discussed the significance of Artificial Intelligence and Machine Learning in chip design, encouraging aspiring designers to familiarize themselves with these concepts.

Fig 1. Lighting of the Lamp

Fig 2. Group picture

2. RISC-V and VLSI Roadshow – 10th August 2023

The VLSI System Design (VSD) and India Electronics Semiconductor Association (IESA) recently organized a highly successful state-level RISC-V and VLSI roadshow, hosted by ELSOC and BMSCE IEEE SSCS. Drawing in 100 participants from across Karnataka, the event aimed to provide hands-on experience and practical insights into RISC-V architecture and VLSI design. The comprehensive curriculum covered a range of topics including converting high-level programming languages to RISC-V machine code, programming RISC-V development boards, and transforming Verilog RTL to GDS using open-source EDA tools.

The roadshow commenced with insightful talks by industry experts from VSD and IESA, shedding light on the importance of RISC-V architecture and VLSI design in the technology landscape. A midday break allowed participants to network and engage in discussions, followed by an afternoon of immersive lab sessions. The Vsdsquadron development board, a

creation of VSD, played a crucial role in providing participants with practical hands-on experience. Beyond the event day, participants left with enhanced skills, a deeper understanding of RISC-V architecture and VLSI design, and a valuable network of industry contacts. This event significantly contributed to the growth and advancement of the tech ecosystem in Karnataka, fostering enthusiasm and knowledge-sharing among tech enthusiasts and learners.

Fig 3. Talk by industry experts

Fig 4. Attendees of the workshop

3. SynthoSphere

BMSCE IEEE SSCS and ELSOC, Electronics Society at BMS College of Engineering, joined forces to organize SynthoSphere: A VeriLog Designathon on the 24th August, 2023. With the valuable support of Mr. Kunal Ghosh, co-founder at VLSI System Design, the event kicked off with an opening call at 8:30 AM. During this session, judges outlined the competition rules, judging criteria, and emphasized the importance of thorough documentation.

The 48-hour online competition officially commenced at 9:00 AM, tasking participants with selecting a design and meticulously working towards building and synthesizing it. They had to document the design, along with the results. Slack was utilized for seamless doubt clarification, aiding participants in their progress. Impressively, a significant number of participants successfully completed their designs within the allocated time frame. Following the competition's conclusion at 9 AM on the 26th of August, a closure call was held, expressing the vote of thanks. The prompt announcement of results within two days marked the culmination of a highly successful Designathon, providing participants with valuable exposure to open-source tools and showcasing their technical prowess in Verilog design.

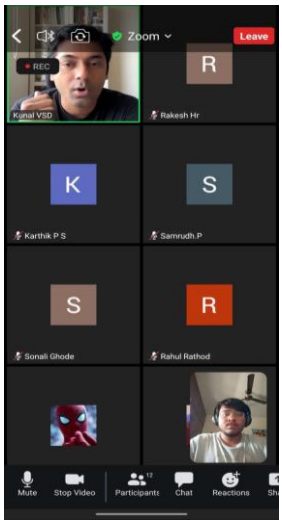

Fig 1: Opening call

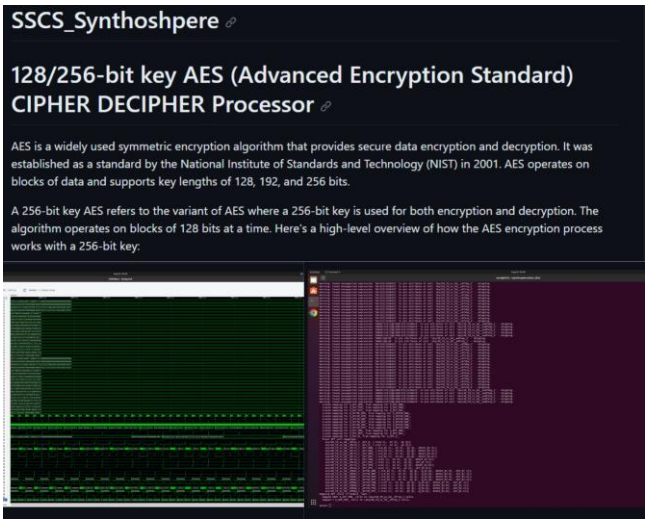

Fig 2: Repository snips of Winner