Report on VLSI Analog Layout Value Added Course

Value-Added Course on VLSI Analog Layout Design Using Cadence Virtuoso

Four Saturdays, Hands-On Session Report

11TH April to 2nd May 2026

Course Area	Focus
Domain	VLSI Analog Layout Design
Tool Used	Cadence Virtuoso
Course Type	Value-Added Course
Learning Mode	Theory supported by hands-on layout experiments
Major Outcomes	CMOS layout basics, layout generation, routing, DRC and LVS verification

Introduction

A value-added course on VLSI Analog Layout Design was conducted with the objective of giving students practical exposure to CMOS layout design, industry-standard layout tools, and physical verification techniques. The seminar focused on bridging the gap between theoretical CMOS concepts and their real-world implementation in integrated circuit design.

The course was conducted in a hands-on manner using Cadence Virtuoso, a widely used software tool in the VLSI industry for schematic entry, layout design, and verification. Over three days, participants learned CMOS basics, layout creation, device matching techniques, and verification methods such as DRC and LVS.

Day 1: CMOS Basics, Cadence Virtuoso Introduction, and Layout Fundamentals

The first day began with an introduction to the basics of CMOS technology and its equivalent representation in layout design. Students were introduced to the structure and working of NMOS and PMOS devices and how these devices are physically represented in layout form.

A detailed explanation was given on the importance of different wells used in CMOS layouts, including Deep N-Well, and how these wells help in device isolation and noise reduction. The role of wells, diffusion

regions, polysilicon, contacts, vias, and metal layers was explained with respect to physical layout implementation.

The session then moved to the basics of Cadence Virtuoso. Students were introduced to the software environment and its different working views, such as cell view, schematic view, and layout view.

View Type	Purpose
Cell View	Represents the design cell in the library
Schematic View	Used to create the circuit-level representation
Layout View	Used to create the physical layout of the circuit

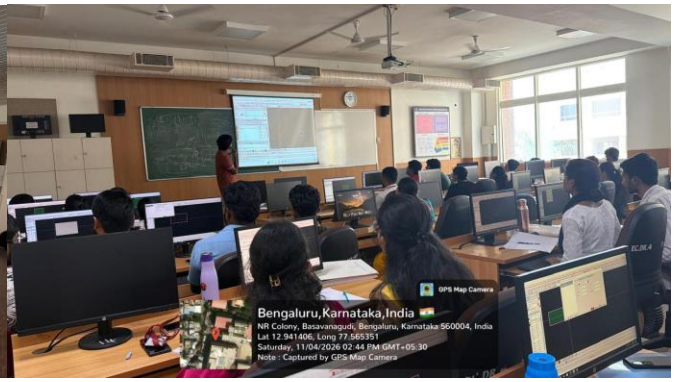
Students were taught how to use Cadence Virtuoso in layout mode. Basic layout operations such as drawing shapes, moving objects, measuring distances, stretching shapes, querying object properties, and instantiating components were demonstrated. Various useful layout features and commands such as move, measure, stretch, query, instantiate, and other editing options were introduced.

A flowchart-based explanation was also given to show the real-world process involved in chip design and fabrication. This included the overall flow from circuit design to schematic creation, layout generation, physical verification, tape-out, fabrication, and final chip testing.

Students were also introduced to stick diagrams, which help in understanding the simplified layout representation of CMOS circuits. The different layers used in layout views, such as diffusion, polysilicon, contacts, vias, and metal layers, were explained in detail.

Brief Learning Summary of Day 1

Through the hands-on session, students learned how CMOS devices are translated into physical layouts. They became familiar with the Cadence Virtuoso layout environment, basic layout commands, different design views, layout layers, and the overall chip design process used in the semiconductor industry.



Day 2: Layout Generation, Fingers, Multipliers, NAND Layout, and Verification Basics

The second day focused on generating layout views from source designs and understanding device sizing concepts such as multipliers and finger width. Students learned the meaning of fingers in CMOS devices and why fingered structures are used in practical layout design.

The concept of multipliers and fingers was explained with examples. Students learned how a large MOS device can be broken down into smaller unit devices and then arranged as repeated copies to create the complete transistor structure. This approach helps in improving layout compactness, matching, routing convenience, and performance.

A major hands-on activity of the day involved creating the schematic of a 2-finger NAND gate and then generating its corresponding layout view. Students applied the knowledge from the previous day to draw shapes, create device regions, connect terminals, and route signals. During the activity, several commonly found layout issues and errors were identified and debugged.

Students also learned how to draw paths for making proper electrical connections between devices. The difference between detached body and integrated body structures was discussed, along with their importance in CMOS layout design.

Additional shortcuts and layout-mode techniques in Cadence Virtuoso were introduced to improve design speed and accuracy. The placement of vias and the method of moving between different metal layers were demonstrated. Students learned how metal layers are used for routing and how vias allow interconnection between these layers.

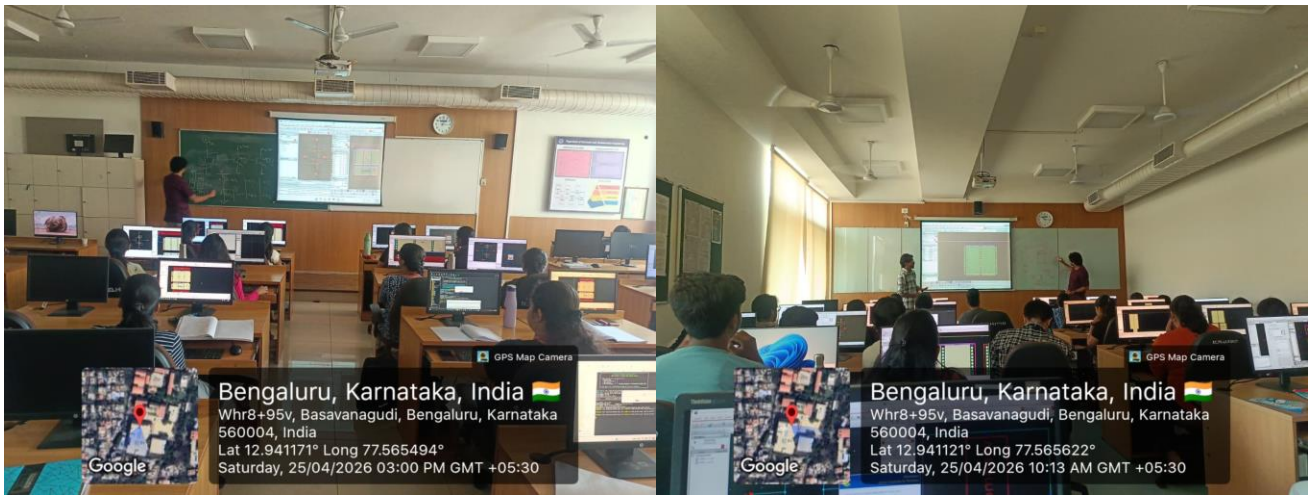
The session concluded with an introduction to DRC and LVS verification. Students were taught that DRC ensures that the layout follows foundry manufacturing rules, while LVS ensures that the layout electrically matches the schematic.

Verification Method	Meaning	Importance
DRC	Design Rule Check	Ensures layout follows foundry manufacturing rules
LVS	Layout Versus Schematic	Ensures layout electrically matches the schematic

The importance of these checks in the semiconductor industry was explained, along with where they are used in the real-world chip design flow.

Brief Learning Summary of Day 2

Through hands-on practice, students learned how to create layouts from schematics, use fingers and multipliers, build a 2-finger NAND layout, make proper routing connections, place vias, move between metal layers, and understand the importance of DRC and LVS verification in industrial VLSI design.



Day 3: Current Mirror Layout, Matching Techniques, DRC, and LVS Debugging

The third day focused on applying the knowledge gained from the previous two days to design a more practical analog layout block: a current mirror. Students used unit NMOS and PMOS devices to construct the current mirror layout.

The concepts of fingers and multipliers were applied in a hands-on manner. Students learned how devices are divided into unit structures and arranged to achieve better matching and layout symmetry. This was especially important for analog circuits, where device mismatch can strongly affect performance.

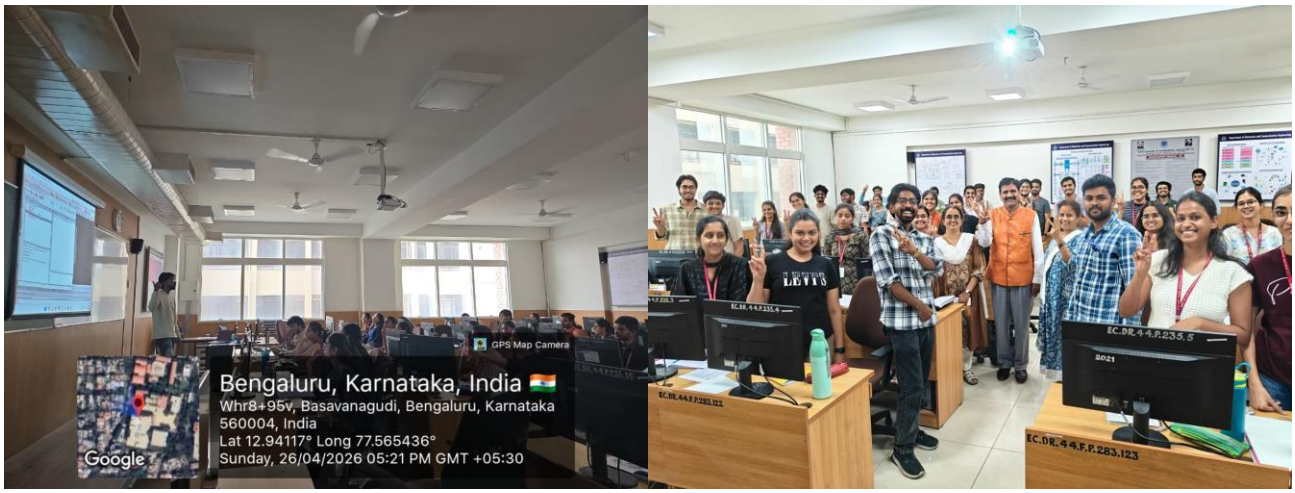
A key topic covered on the third day was pattern making and unit device arrangement. Students were introduced to the idea of placing unit devices in such a way that they experience nearly the same average process variation across the layout. This helped students understand the importance of matching techniques in analog layout design.

After completing the current mirror layout, students performed DRC and LVS scans. The DRC scan helped identify rule violations related to spacing, width, enclosure, and other layout design constraints. The LVS scan was used to check whether the final layout matched the intended schematic.

Students then debugged the reported violations, corrected the layout errors, and re-ran the verification checks. This process gave them practical experience in resolving layout issues and achieving a verified layout.

Brief Learning Summary of Day 3

Through the current mirror layout exercise, students learned how to apply layout matching techniques, use unit devices, arrange fingers and multipliers, perform DRC and LVS checks, debug violations, and complete layout verification for an analog circuit.



Day 4: Capstone Project - Operational Amplifier Layout Design

The fourth day was conducted as a capstone-based project in which students applied the complete knowledge gained during the previous sessions using Cadence Virtuoso. The main objective of this project was to design the layout of an operational amplifier using the same analog layout principles, device arrangement methods, and verification flow learned throughout the course.

Students worked on drawing the best possible patterns for the different configurations of the op-amp based on their multipliers. The devices were arranged carefully in the layout tool by considering proper sharing,

matching, symmetry, and placement. Special attention was given to the right distribution of devices so that the layout could achieve better device sharing and improved physical organization.

The session also focused on practical routing methods. Students learned how devices should be interconnected using suitable metal layers and routing strategies to achieve the final working system. DRC checks were performed on the op-amp layout, the reported errors were debugged, and corrections were made to satisfy the layout rules. Finally, a successful LVS check was achieved, confirming that the completed op-amp layout matched its schematic representation.

Brief Learning Summary of Day 4

Through the capstone project, students learned how to combine CMOS layout basics, fingers, multipliers, device placement, sharing, routing, DRC debugging, and LVS verification to complete a practical op-amp layout using Cadence Virtuoso.

Overall Learning Outcomes

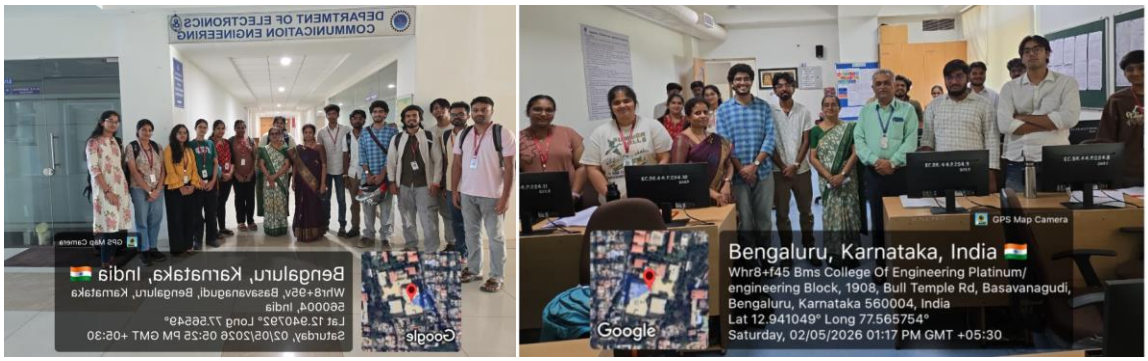
By the end of the value-added course, students gained practical knowledge of VLSI analog layout design and developed hands-on experience with Cadence Virtuoso. The course helped students understand how theoretical CMOS concepts are converted into real physical layouts used in chip design, and how complete analog blocks such as current mirrors and operational amplifiers are verified through industry-relevant DRC and LVS flows.

Area	Learning Outcome
CMOS Fundamentals	Understood CMOS devices and their physical layout equivalents

Area	Learning Outcome
Cadence Virtuoso	Learned basic layout operations and design views
Layout Layers	Understood wells, diffusion, polysilicon, contacts, vias, and metal layers
Stick Diagrams	Learned simplified layout planning techniques
Device Sizing	Understood fingers, multipliers, and unit device concepts
Digital Layout	Created and debugged a 2-finger NAND layout
Analog Layout	Designed a current mirror using NMOS and PMOS units
Verification	Performed DRC and LVS checks and debugged violations
Industry Relevance	Understood how layout design fits into the real-world chip design process
Capstone Project	Designed an op-amp layout by applying device patterning, placement, routing, DRC debugging, and LVS verification

Conclusion

The four-day VLSI Analog Layout seminar served as an effective value-added course by providing students with both theoretical understanding and practical exposure to layout design. The sessions helped participants understand the complete flow of physical design, from CMOS basics and layout creation to verification using DRC and LVS, ending with a capstone op-amp layout project.



The hands-on experiments using Cadence Virtuoso gave students valuable insight into how layouts are created, checked, corrected, and finalized in the semiconductor industry. Overall, the course strengthened the students' understanding of analog layout design and prepared them for further learning and practical work in the field of VLSI design.