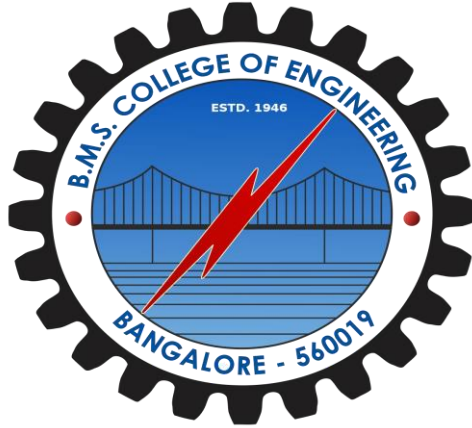


**BMS COLLEGE OF ENGINEERING    ELECTRONICS AND  
TELECOMMUNICATION**

**REPORT ON MULTISIM INTERNSHIP**



## **ACKNOWLEDGEMENT**

The satisfaction that accompanies the successful completion of this Multisim Internship would be incomplete without mention of the people who made it possible, without constant guidance and encouragement would have made efforts go in vain. We consider ourselves privileged to express gratitude and respect towards all from the completion of this internship.

We convey thanks to **professors Dr. Kanamani B mam, Prof. Gowra P S mam, Prof. Archana K mam, Prof. Ambika K mam** of Electronics and Telecommunication department for providing encouragement, constant support and guidance which was of a great help for completion of this internship successfully.

## **TWO WEEKS INTERNSHIP ON MULTISIM**

NI Multisim is an electronic schematic capture and simulation program which is part of a suite of circuit design programs, along with NI Ultiboard. Multisim Live is a web-based electronic schematic capture and simulation tool with built-in SPICE based simulation. NI Multisim and Multisim Live are developed and owned by National Instruments.

**B.M.S COLLEGE OF ENGINEERING  
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATIONS.**

# **TWO WEEK ONLINE INTERNSHIP ON MULTISIM**

(Circuit simulation tool from National Instruments)

**Date: 23-08-2021 TO 04-09-2021  
Duration : 10 A.M TO 12:30 P.M  
Fee: 300Rs**

**Mode of payment:**  
Account name : HOD,Telecommunications  
Account number: 20274184938.  
Indian Bank ; IFSC CODE: IDIB000B607

**Coverage: Analog and Digital circuit experiments from  
V.T.U syllabus.**

**Criteria to get certificate:**

- Minimum of 80% attendance.
- To implement a project.

**Resource Persons:**  
P.S Gowra  
Ambika.K  
Archana.K

**Student Co-ordinators: Sharanya.S  
8197212486  
Bhuvana Bharadwaj K  
9071366235**

**For students of 2nd and 3rd year  
(V.T.U or Autonomous or any other university)**

## **OBJECTIVE OF INTERNSHIP**

The main objective of this internship is that:

- Due to Pandemic situation, students were not able to attend colleges and didn't have a hands on experience with hardware lab implementations. Hence, this internship provided a platform for students to visualize hardware implementation using multi-sim simulation tool.
- In this multi-sim, students will be able to learn and implement the practical circuits and can observe and analyse the output.
- In this internship, Analog as well as Digital circuit implementation will be taught.
- Here, Students will be able to gain knowledge on Analog and Digital circuit theoretically and practically.
- In the final stage of this internship, student will be able to design & execute a mini project.

**Schedule for two weeks online internship on multi-sim**

**Date: 23/08/2021 – 03/09/2021**

<b>Date</b>	<b>Faculty handling</b>	<b>Concepts</b>
<b>Day-1 23/08/2021</b>	<b>Archana K</b>	<ul style="list-style-type: none"><li>● Introduction to multi-sim live tool</li><li>● Diode Characteristics</li><li>● Half wave rectifier (With &amp; Without filter)</li><li>● Bridge rectifier (With &amp; Without filter)</li></ul>
<b>Day-2 24/08/2021</b>	<b>Archana K</b>	<ul style="list-style-type: none"><li>● Full wave rectifier</li><li>● CE configuration – I/P &amp; O/P characteristics</li><li>● Basic gates – Truth table verification</li><li>● Half adder – Implementation using basic gates</li></ul>
<b>Day-3 25/08/2021</b>	<b>Archana K</b>	<ul style="list-style-type: none"><li>● Full adder using basic gates</li><li>● Half adder &amp; Full adder using Nor gates</li><li>● Half adder &amp; Full adder using NAND gates</li></ul>
<b>Day-4 26/08/2021</b>	<b>Ambika K</b>	<ul style="list-style-type: none"><li>● Op-amp as voltage follower</li><li>● Inverting &amp; Non-inverting amplifier</li><li>● Inverting &amp; Non-inverting summing amplifier</li><li>● Differentiator &amp; Integrator</li></ul>
<b>Day-5 27/08/2021</b>	<b>Ambika K</b>	<ul style="list-style-type: none"><li>● Precision Half wave &amp; Full wave rectifier</li><li>● Zero crossing detector &amp; Schmitt trigger</li><li>● First order low pass &amp; High pass filter</li><li>● Wein bridge oscillator</li></ul>
<b>Day-6 30/08/2021</b>	<b>P S Gowra</b>	<ul style="list-style-type: none"><li>● Clipping circuits (Single / Double ended)</li><li>● Clamping circuits (Positive/Negative)</li></ul>

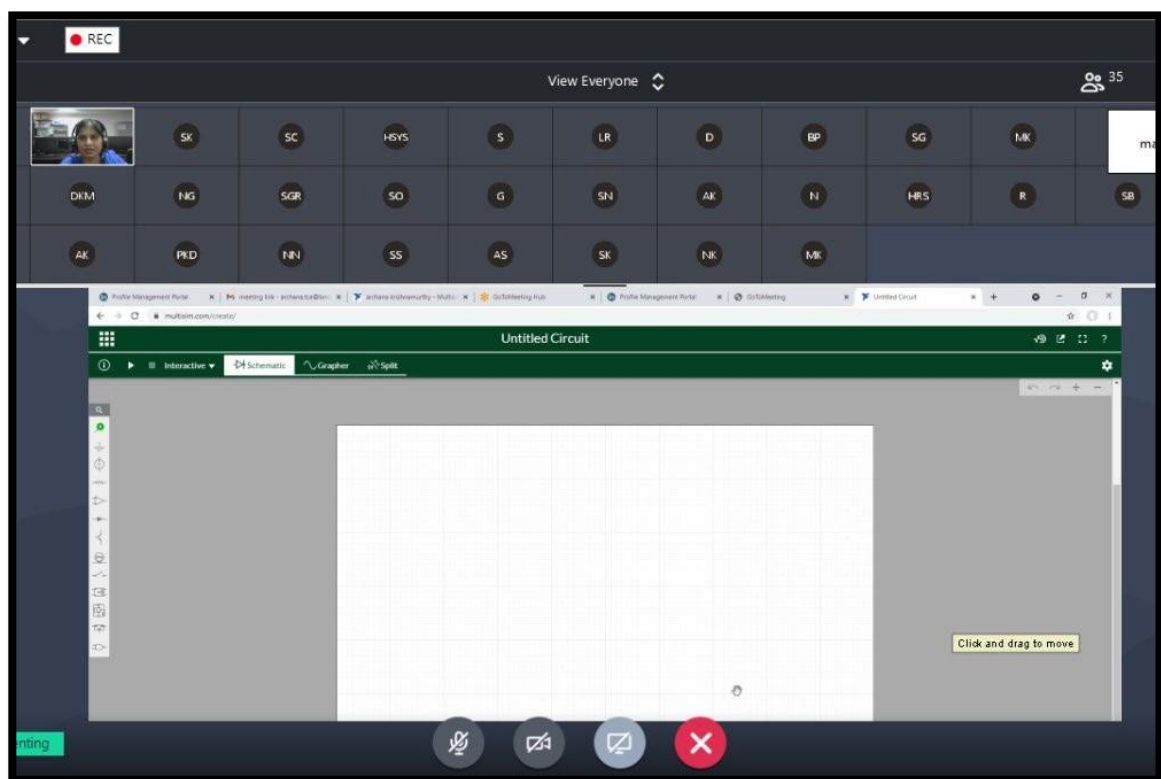
		<ul style="list-style-type: none"> <li>● Transistor as a Switch</li> <li>● Briefing about mini project and team formation</li> </ul>
<b>Day-7</b> <b>31/08/2021</b>	<b>P S Gowra</b>	<ul style="list-style-type: none"> <li>● Zener as voltage regulator to determine Line / Load regulation</li> <li>● RC coupled Amplifier using multi-sim and virtual lab</li> <li>● BJT as RC phase shift oscillator</li> </ul>
<b>Day-8</b> <b>01/09/2021</b>	<b>P S Gowra</b>	<ul style="list-style-type: none"> <li>● RC coupled amplifier with feedback</li> <li>● Drain &amp; Source characteristics of MOSFET</li> <li>● Finalizing projects and teams</li> </ul>
<b>Day-9</b> <b>02/09/2021</b>	<b>P S Gowra</b>	<b>Project Presentation</b>
<b>Day-10</b> <b>03/09/2021</b>	<b>P S Gowra</b>	<b>Project Presentation</b>

## DAY-1: 23/08/2021 – REPORT

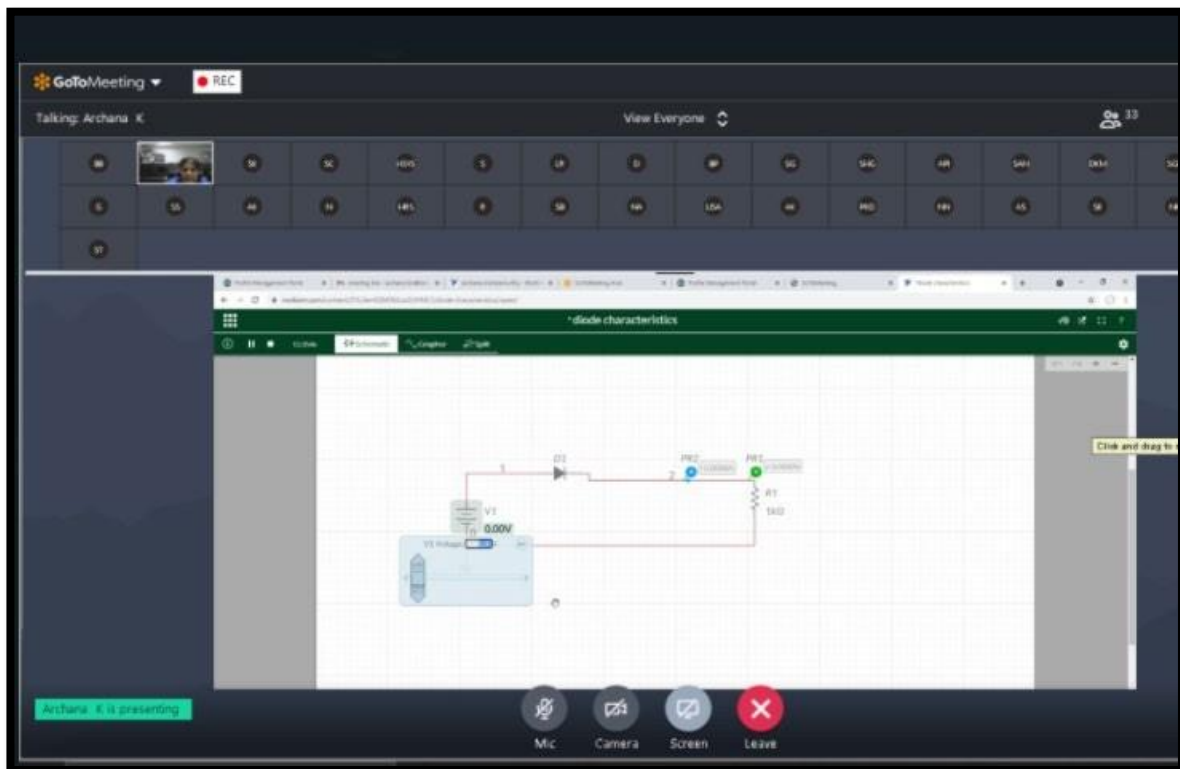
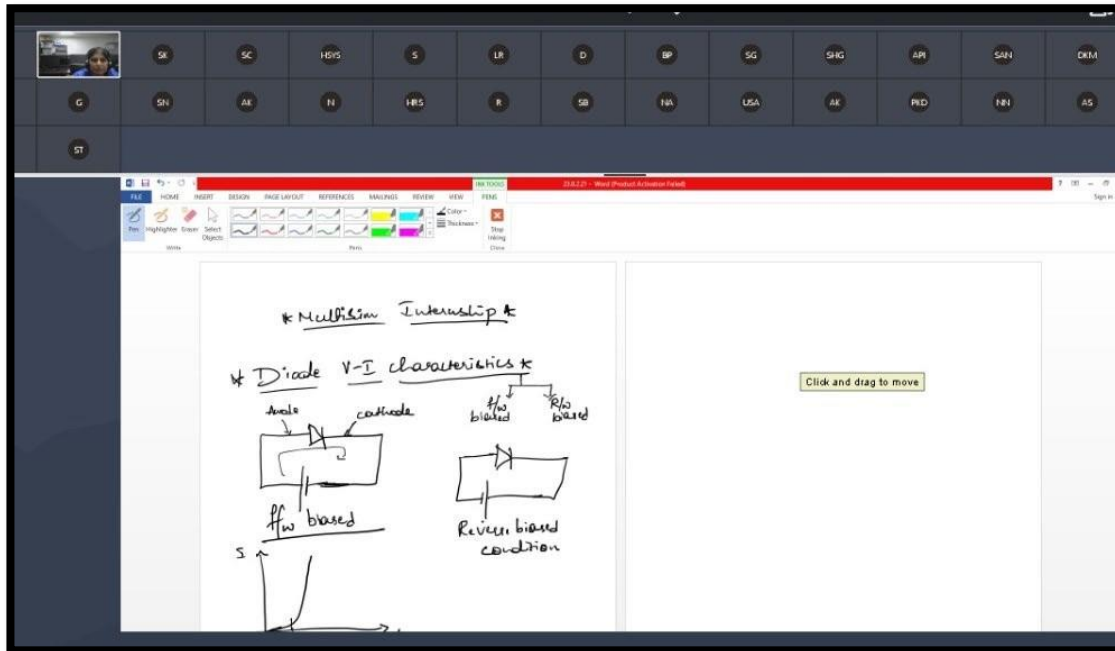
**Day -1:** The session started at 10:00 am. Faculty handled by Archana K . About 35 students were present for the first day training on multi-sim.

- **Topics Covered:**

- Introduction about Internship
- Introduction about Multi-sim platform
- VI Characteristics of diode
- Rectifiers: Bridge rectifier, half wave rectifier, Centre tapped rectifier.



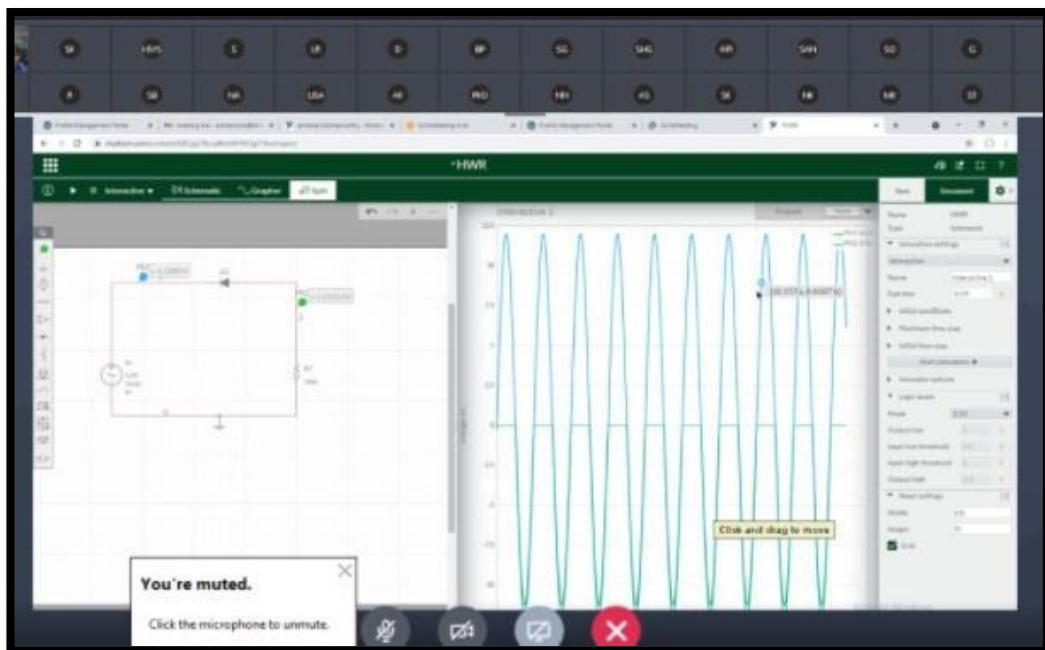
- VI characteristics Diode:** When the forward voltage exceeds the diodes P-N junction internal barrier voltage, which for silicon is about 0.7 volts, avalanche occurs and the forward current increases rapidly for a very small increase in voltage producing a non-linear curve.





- **Rectifiers:** A rectifier is an electrical device that converts alternating current (AC) into Pulsating DC, which flows in only one direction.

- **Half wave Rectifier:** In half-wave rectification of a single-phase supply, either the positive or negative half of the AC wave is passed, while the other half is blocked. Because only one half of the input waveform reaches the output, mean voltage is lower.
- **Full wave Rectifier:** A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output. Mathematically, this corresponds to the absolute value function. Full-wave rectification converts both polarities of the input waveform to pulsating DC (direct current), and yields a higher average output voltage. Two diodes and a centre tapped transformer, or four diodes in a bridge configuration and any AC source (including a transformer without centre tap), are needed.

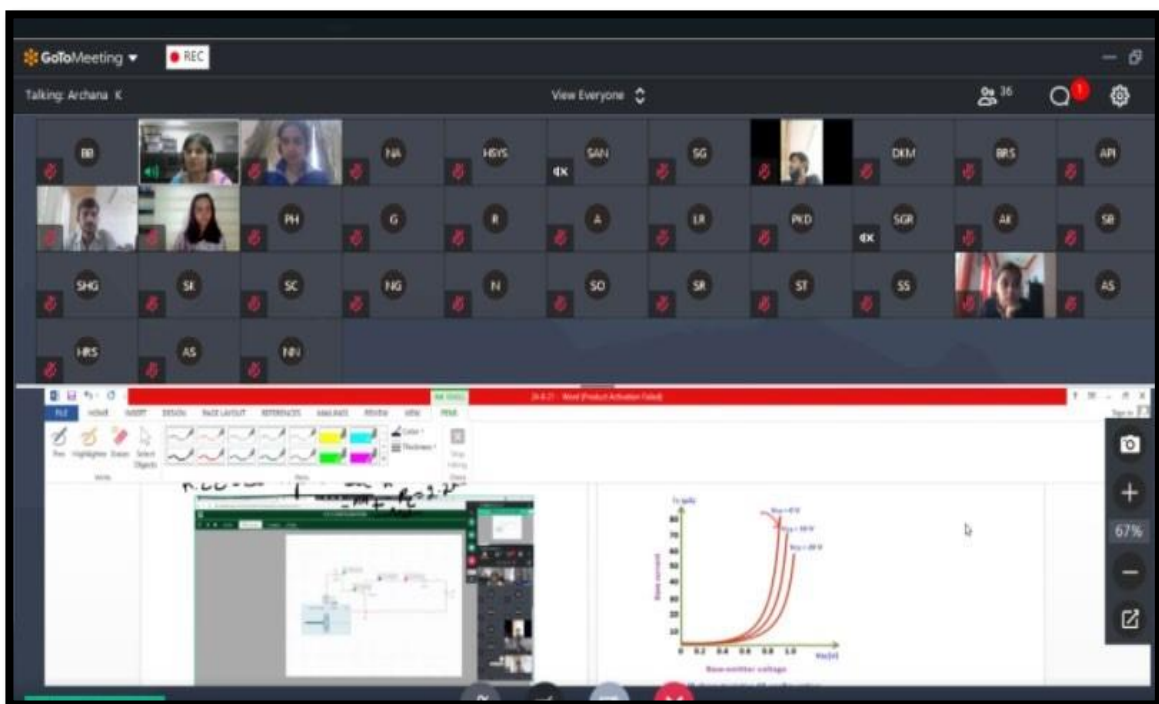


## OUTCOME

Students were able to implement the above mentioned content. They could analyze the practical aspects of the circuit using theoretical knowledge on multi-sim platform.

### DAY 2: 24-08-2021

The session started at 10:00 am. Faculty handled by Archana K . About 37 students were present for the second day training on multi-sim.



- **Topics Covered:**

- Common Emitter configuration of BJT transistor.
- Introduction about digital circuits.
- AND,OR,NOT NAND and NOR gates.
- Design and implementation of Half adder.

- **Common Emitter configuration of BJT transistor:**

The **common emitter** (CE) configuration is the most widely used transistor configuration. The common emitter (CE) amplifiers are used when large current gain is needed. The input signal is applied between the base and emitter terminals while the output signal is taken between the collector and emitter terminals.

View Everyone

I<sub>b</sub> characteristic -  $V_{ce} \rightarrow f_{in}$

$V_{be} \rightarrow V_{be}$  |  $I_{c} \rightarrow I_{c}$

Q-point characteristic -  $V_{be} \rightarrow f_{in}$ ,  $I_{c} \rightarrow f_{out}$

$V_{be} / V_{ce}$	$I_{c} (mA)$
0.7	0
0.7	20

GoToMeeting REC

Talking: View Everyone

\*CE-CONFIGURATION

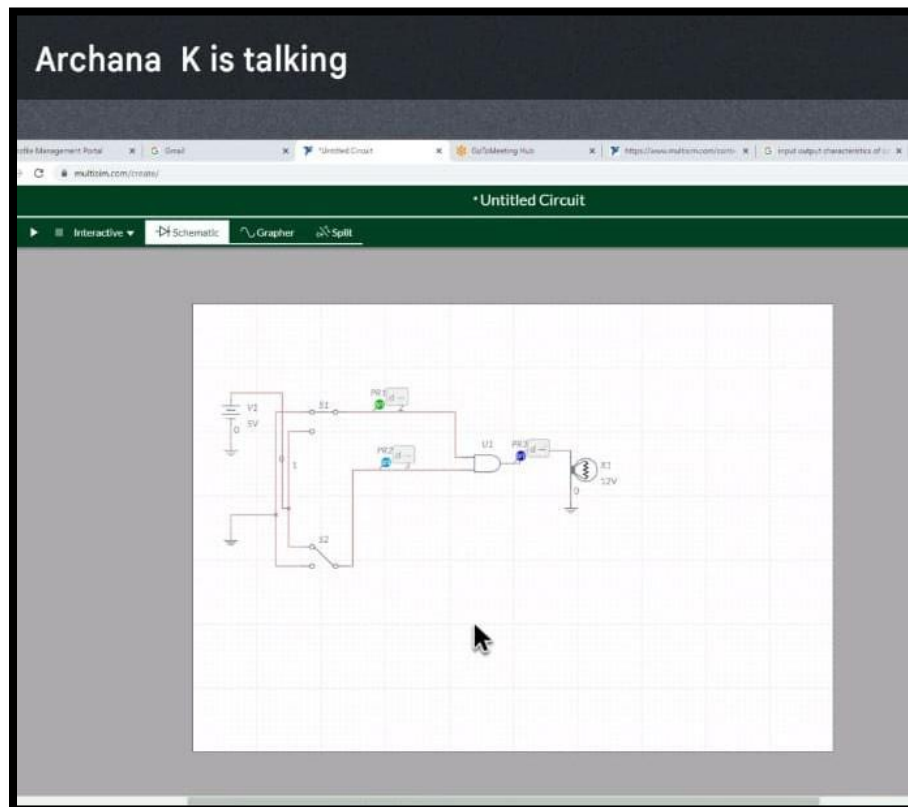
Interactive | Schematic | Grapher | Split

You're muted.

## **DIGITAL GATES:**

The basic digital electronic circuit that has one or more inputs and single output is known as **Logic gate**. Hence, the Logic gates are the building blocks of any digital system.

- **AND:** An AND gate is a digital circuit that has two or more inputs and produces an output, which is the **logical AND** of all those inputs. It is optional to represent the **Logical AND** with the symbol.
- **OR:** An OR gate is a digital circuit that has two or more inputs and produces an output, which is the logical OR of all those inputs. This **logical OR** is represented with the symbol '+’.
- **NOT:** A NOT gate is a digital circuit that has single input and single output. The output of NOT gate is the **logical inversion** of input. Hence, the NOT gate is also called as inverter.
- **NAND:** The NAND (Not – AND) gate has an output that is normally at logic level “1” and only goes “LOW” to logic level “0” when ALL of its inputs are at logic level “1”. The Logic NAND Gate is the reverse or “Complementary” form of the AND gate
- **NOR:** A NOR gate is a logic gate which gives a positive output only when both inputs are negative. Like NAND gates, NOR gates are so-called "universal gates" that can be combined to form any other kind of logic gate.



### **HALF ADDER:**

Half Adder is a combinational logic circuit which is designed by connecting one EX-OR gate and one AND gate. The half adder circuit has two inputs: A and B, which add two input digits and generates a carry and a sum. A half adder is used for adding together the two least significant digits in a binary sum.

The screenshot shows a digital logic simulation software interface. On the left, a circuit diagram is displayed with inputs A and B. Input A is connected to an AND gate and an OR gate. Input B is connected to an AND gate and an OR gate. The output of the AND gate is labeled  $A\bar{B}$ . The output of the OR gate is labeled  $A+B$ . The final output is labeled  $AB+AD$ . Below the circuit diagram is a truth table grid.

On the right, the Boolean algebra derivation is shown:

$$\begin{aligned}
 &= \bar{A}\bar{B}C + A\bar{B}C + A\bar{B} \\
 &= A\bar{B}C + B(A+\bar{A}C) \rightarrow (A+C) \\
 &= A\bar{B}C + B(A+C) \\
 &= A\bar{B}C + \bar{A}B + BC \\
 &= A(B+\bar{B}C) + BC \\
 &= A(B+C) + BC = AB + AC + BC
 \end{aligned}$$

### OUTCOME:

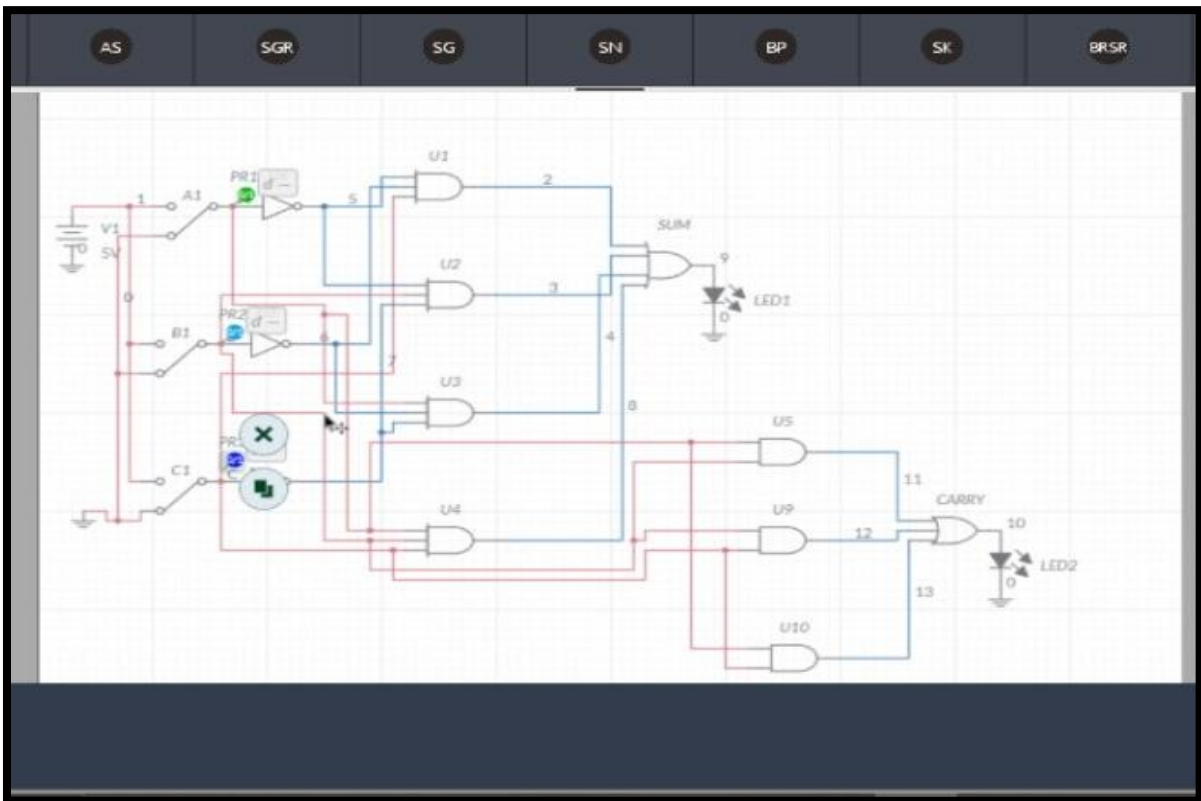
Students were able to implement the above mentioned content. They could analyze the practical aspects of the circuit using theoretical knowledge on multi-sim platform. Also they were able to learn, analyze and design digital circuits.

## DAY-3: 25/08/2021 – REPORT

**Day -3:** The session started at 10:00 am. Faculty handled by Archana K . About 37 students were present for the third day training on multi-sim.

- **Topics Covered:**

- Full adder using basic gates
- Half adder and Full adder using NOR gates.
- Half adder and Full adder using NAND gates



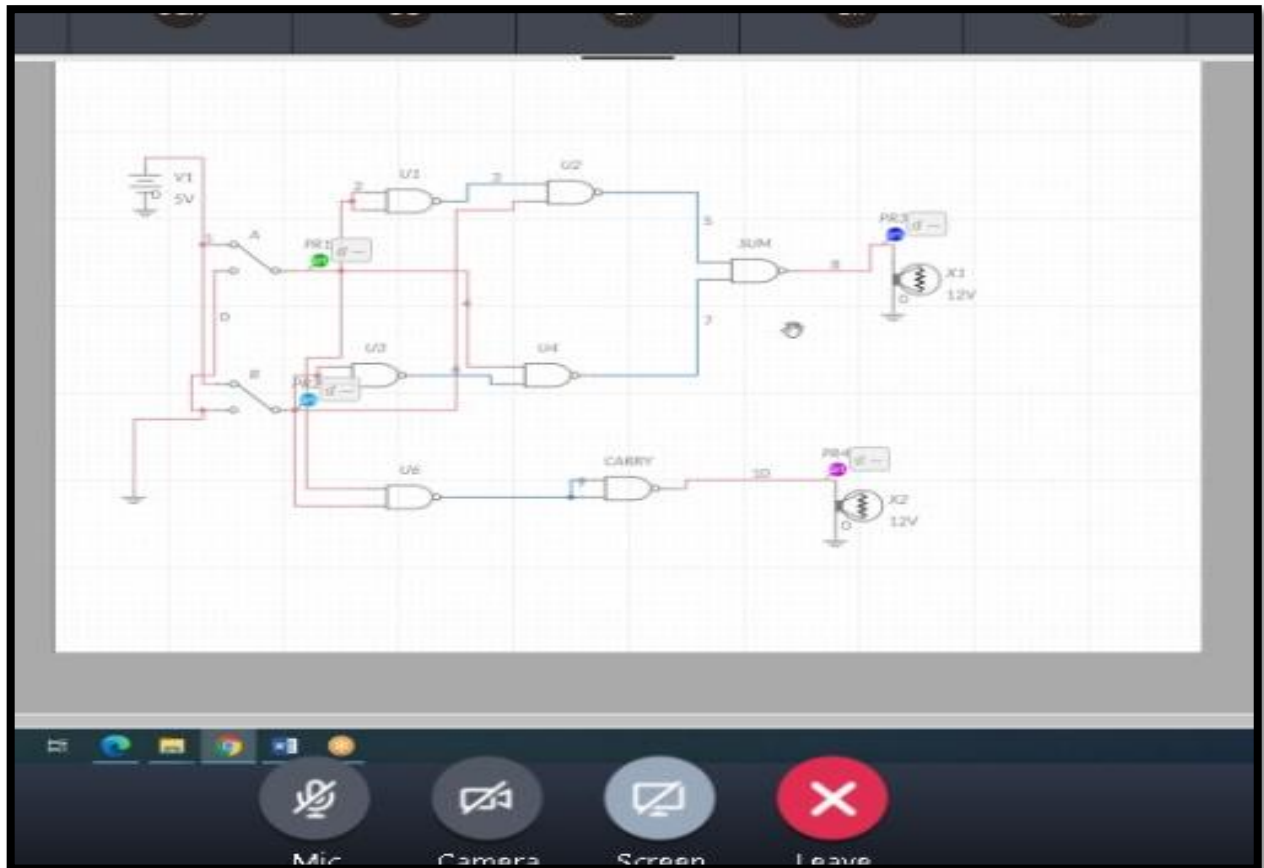
H.A. :-  
 $Sum = \bar{A}B + A\bar{B}$   
 $carry = AB$

20) place bubbles at o/p of AND gate & i/p of OR gates.  
21) place inverters in the lines where bubbles are added.  
22) cancel the even no. of bubbles appearing in each line.  
23) replace i/p bubbled OR gate by NAND gate & inverter by ~~NAND~~ Equivalant NAND gate.

$\bar{A}B$   
 $A\bar{B}$   
 $\bar{A}B + A\bar{B} = sum$   
 $AB = carry$

You're muted. Click the microphone to unmute.

→ **Full Adder:** Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another.



→ **Full Adder using NAND Gates:** a NAND gate is one of the universal gates and can be used to implement any logic design. The circuit of full adder using only NAND gates .Full adder is a simple 1-bit adder. If we want to perform n-bit addition, then we need 'n' number of 1-bit full adders should be used in the form of a cascade connection.



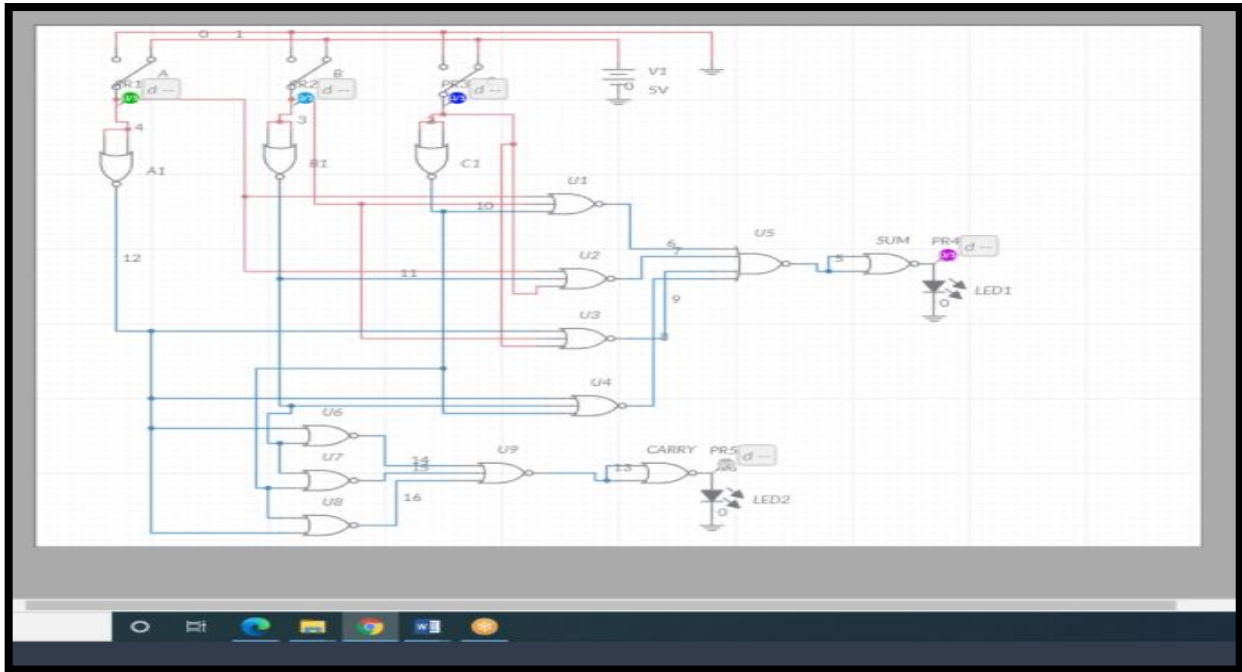
\*full adder Implementation\*  
using NOR: -

$$\text{Sum} = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$

$$\text{Carry} = AB + BC + AC$$

1) Implement the exp. using basic gates.  
 2) NOR Implementation! -  
 a) place bubbles at o/p of OR gates & p of AND gates  
 b) place inverters in each line, where bubb

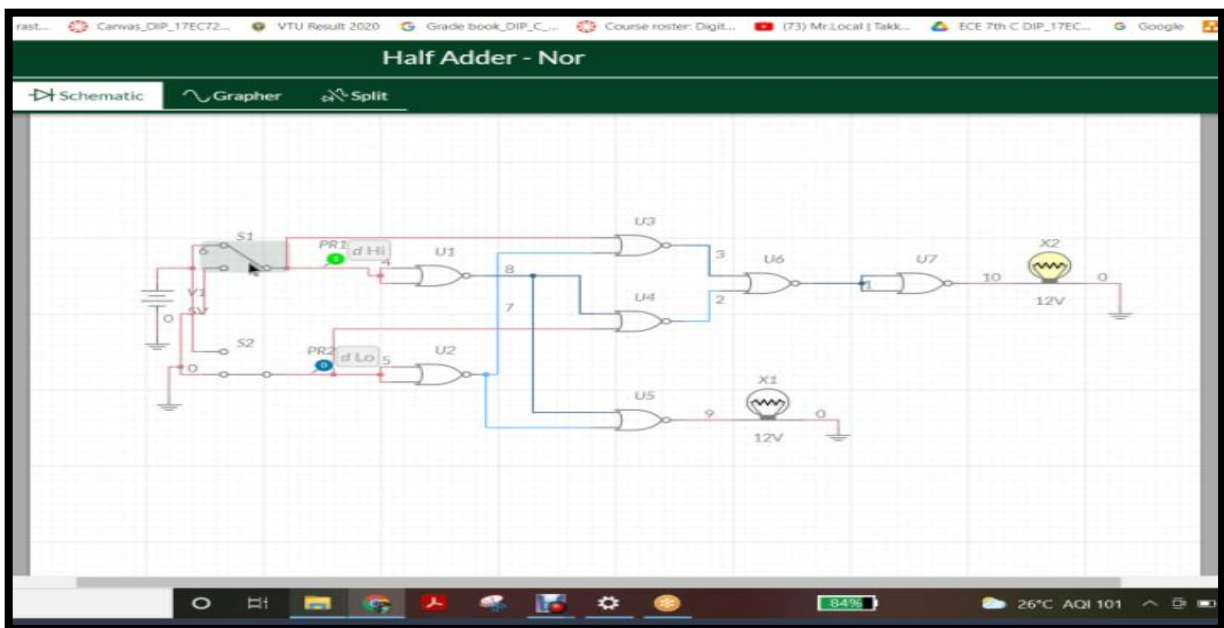
→ **Full adder using NOR gates:** a NOR gate is one of the universal gates and can be used to implement any logic design. The circuit of full adder using only NOR gates.



As we know that NAND and NOR are called universal gates as any logic system can be implemented using these two, the half adder circuit can also be implemented using them.

Five NAND gates are required in order to design a half adder.

→ **Half Adder using NOR gates:** Five NOR gates are required in order to design a half adder.



### **OUTCOME:**

Students were able to implement the above mentioned content. They could analyze the practical

aspects of the circuit using theoretical knowledge on multi-sim platform. They learnt to implement a Full adder & Half adder circuits, its Boolean Equations and also design of Full adder & Half adder using NAND and NOR gates.

### DAY-4: 26/08/2021 – REPORT

**Day -4:** The session started at 10:00 am. Faculty handled by Ambika K. About 37 students were present for the fourth day training on multi-sim.

- **Topics Covered:**

- Introduction to operational amplifiers (op-amp).
- Op-amp as voltage follower.
- Inverting and non-inverting amplifiers.
  - Inverting and non-inverting summing amplifiers.
  - Differentiator and integrator.

Talking: Ambika K View Everyone 26

BB SG SO SC NA SN N SAN AK N  
R M NK DKM D AS HRS SHG SGR HVS SS

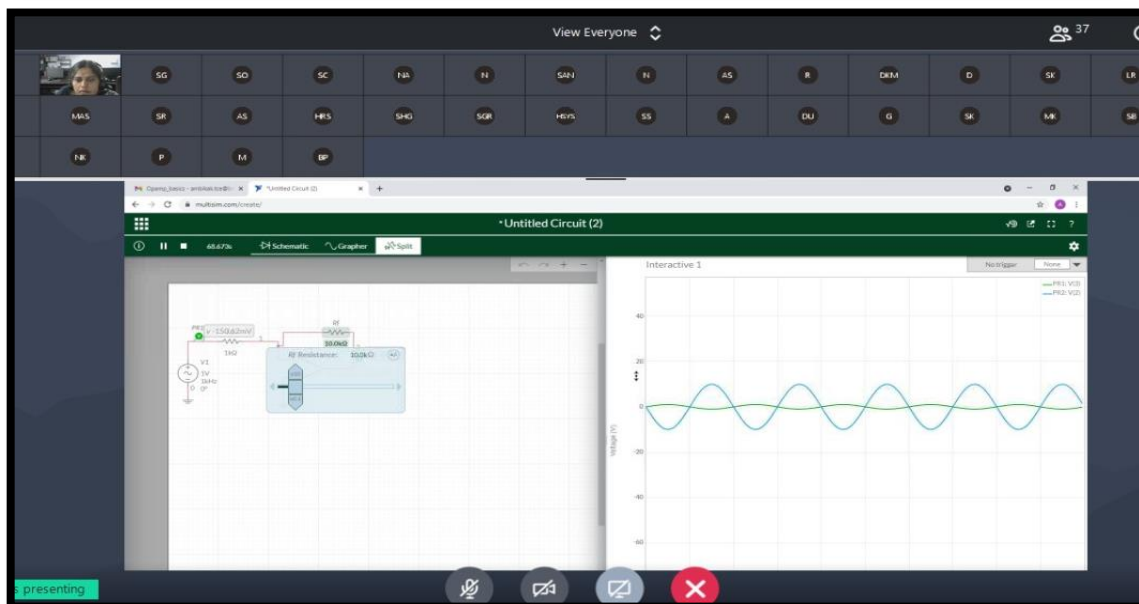
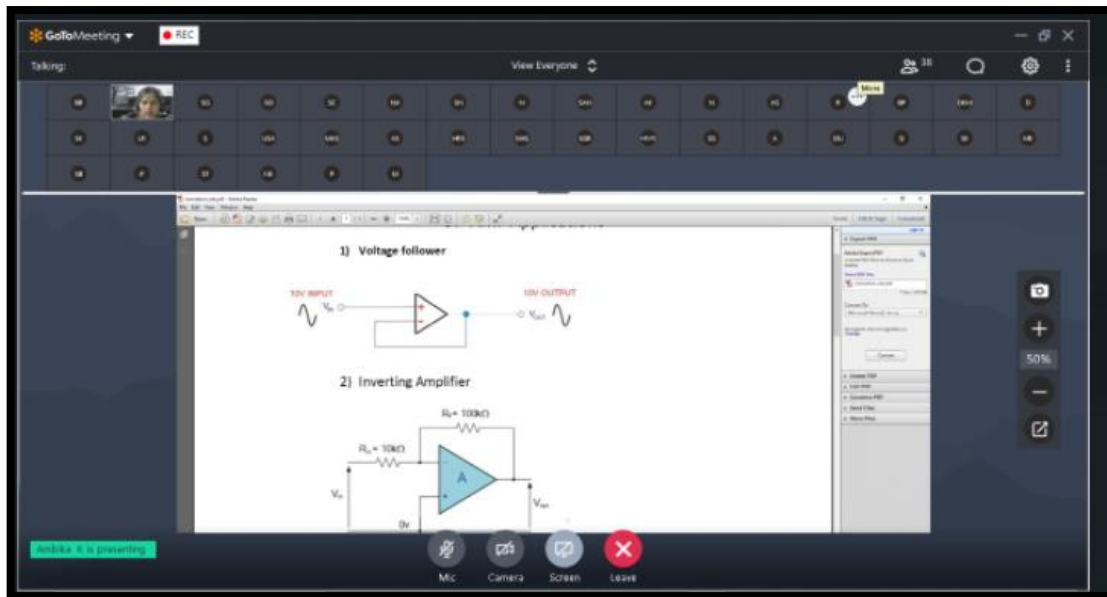
1. What is an Operational Amplifier (Op-amp)?

An operational amplifier has two input pins and one output pin. Its basic role is to amplify and output the voltage difference between the two input pins.

Non-inverting input  
Inverting input  
Negative power  
Output

→ **Op-amp as Voltage follower:**

Voltage Follower is simply a **circuit in which output follows the input**, means output voltage remains same as input voltage. It is also commonly known as Unity gain Opamp Amplifier or Opamp Buffer.

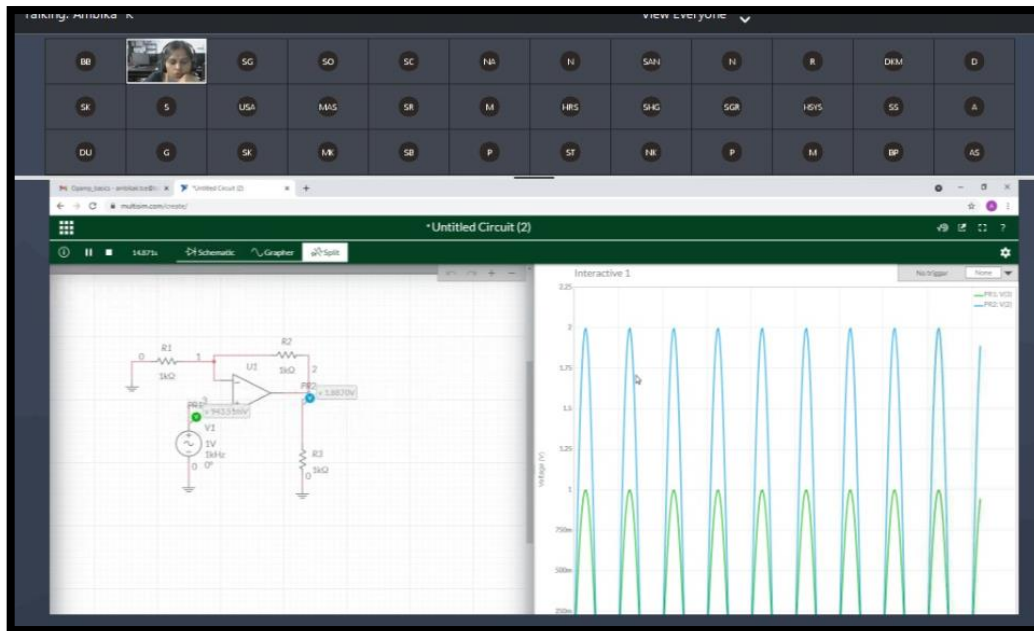


→ **Op-amp as Inverting Amplifier:**

An inverting amplifier (also known as an inverting operational amplifier or an inverting op-amp) is a type of **operational amplifier circuit** which produces an output which is out of phase with respect to its input by **180°**

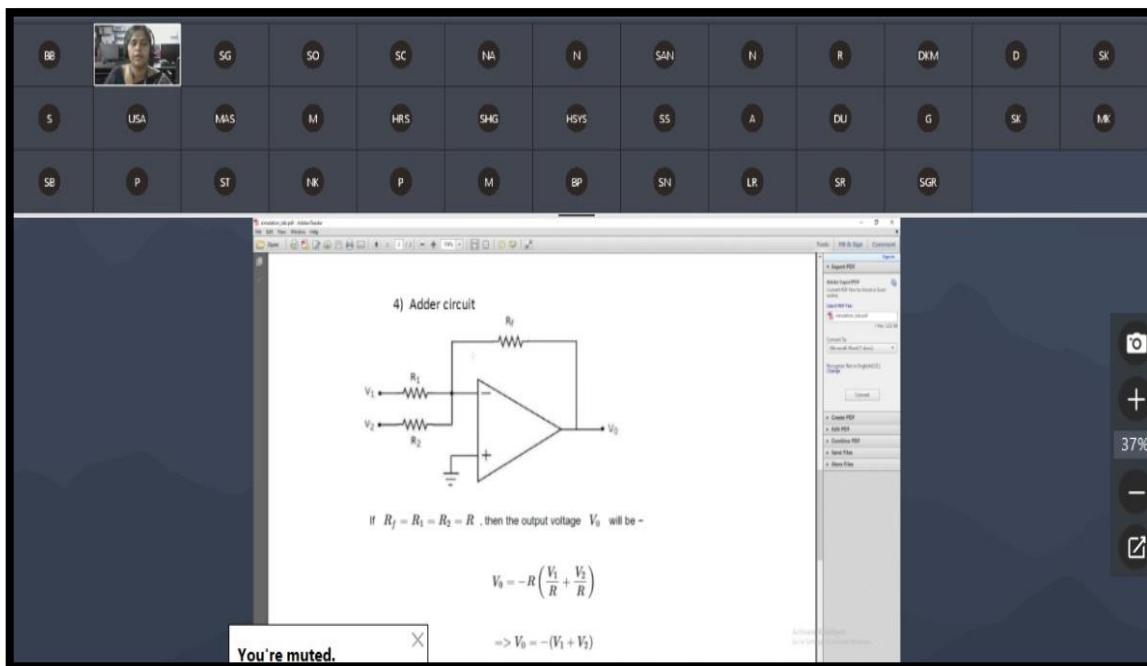
→ **Op-amp as non - Inverting Amplifier:**

A non-inverting amplifier is an **op-amp circuit configuration** that produces an **amplified output signal** and this output signal of the non-inverting op-amp is in-phase with the applied input signal. In other words, a non-inverting amplifier behaves like a voltage follower circuit.



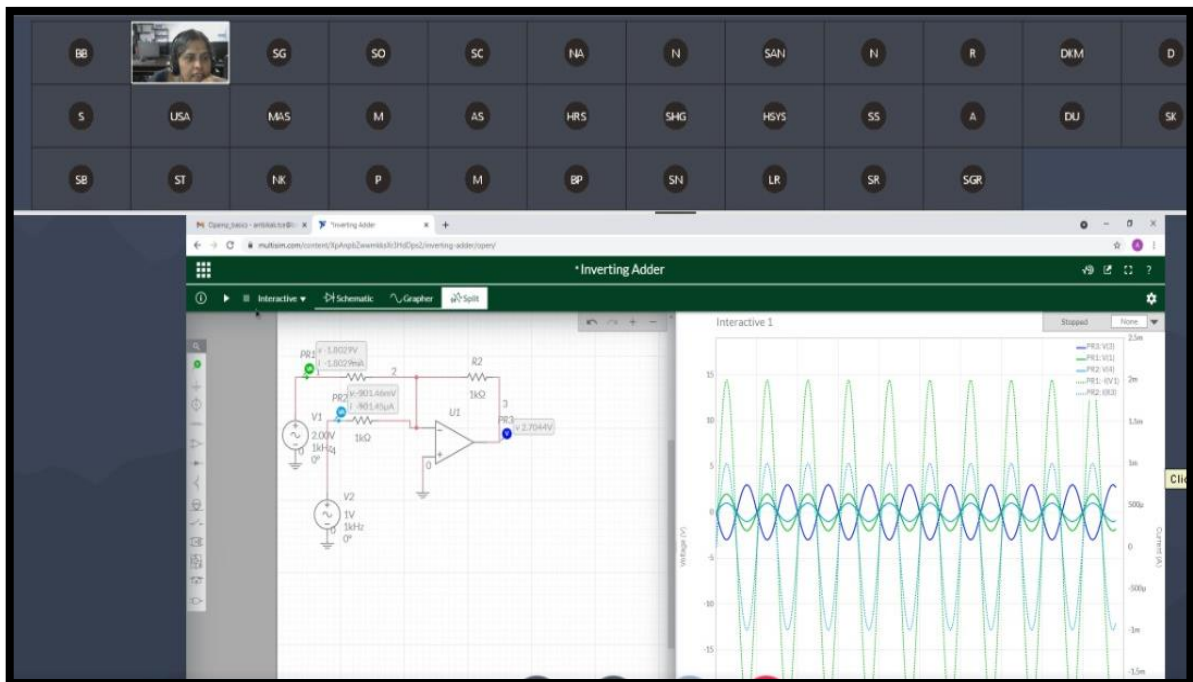
→ **Op-amp as Inverting summing Amplifier:**

The Summing Amplifier. The Summing Amplifier is another type of operational amplifier circuit configuration that is used to **combine the voltages present on two or more inputs** into a single output voltage.



→ **Op-amp as non - Inverting summing Amplifier:**

A Non-Inverting Summing Amplifier can also be constructed using the Non-Inverting Amplifier configuration of the Op Amp. Here, the input voltages are applied to the non-inverting input terminal of the Op Amp and a part of the output is fed back to the inverting input terminal, through voltage-divider-bias feedback.

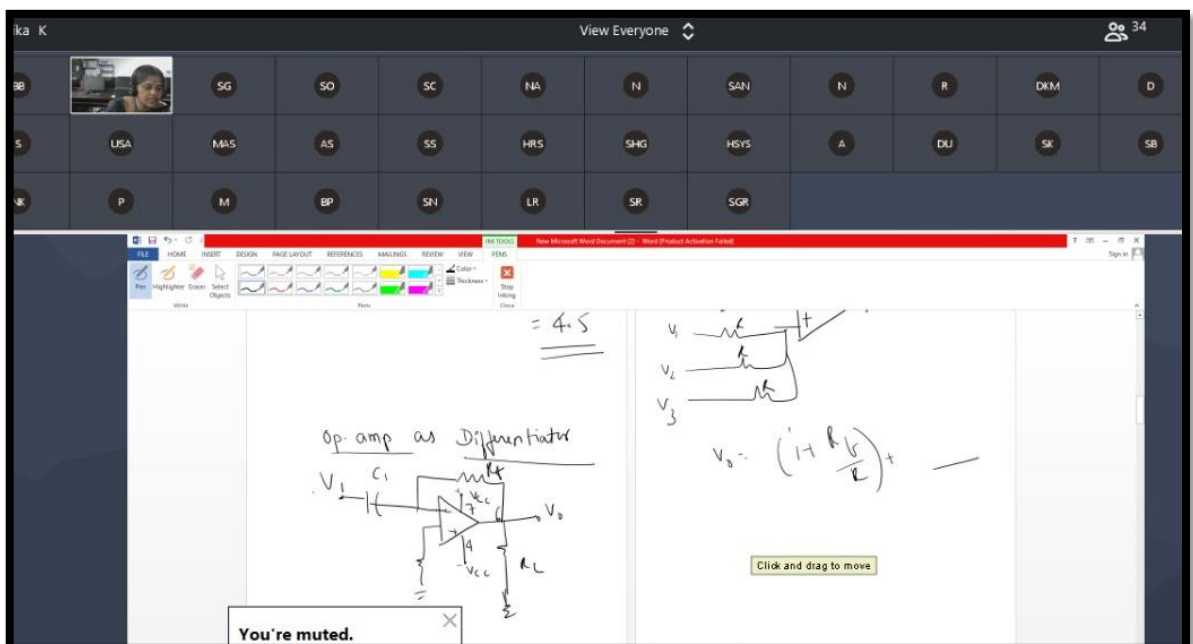


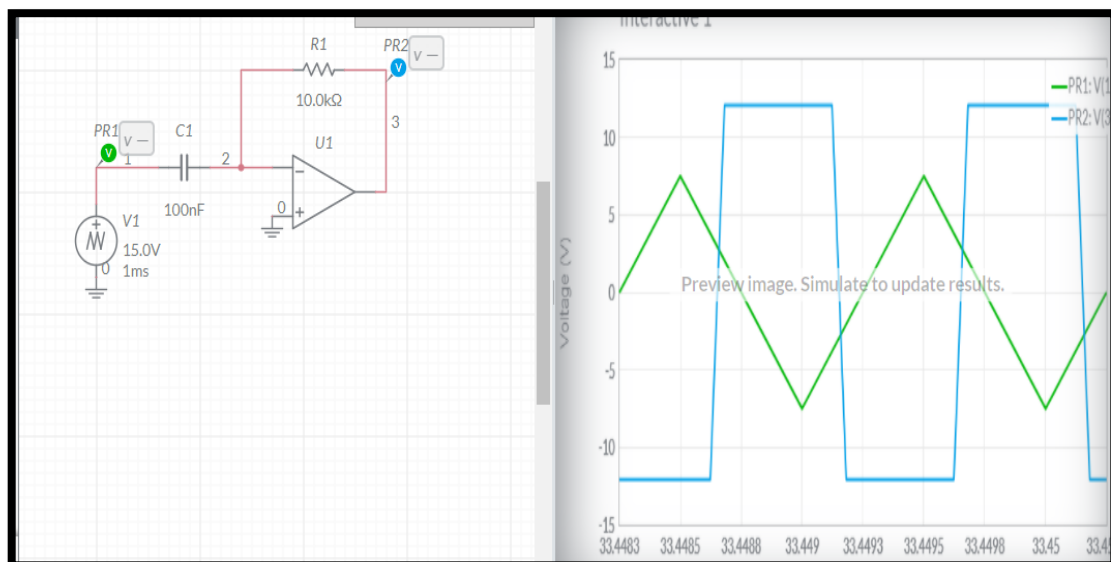
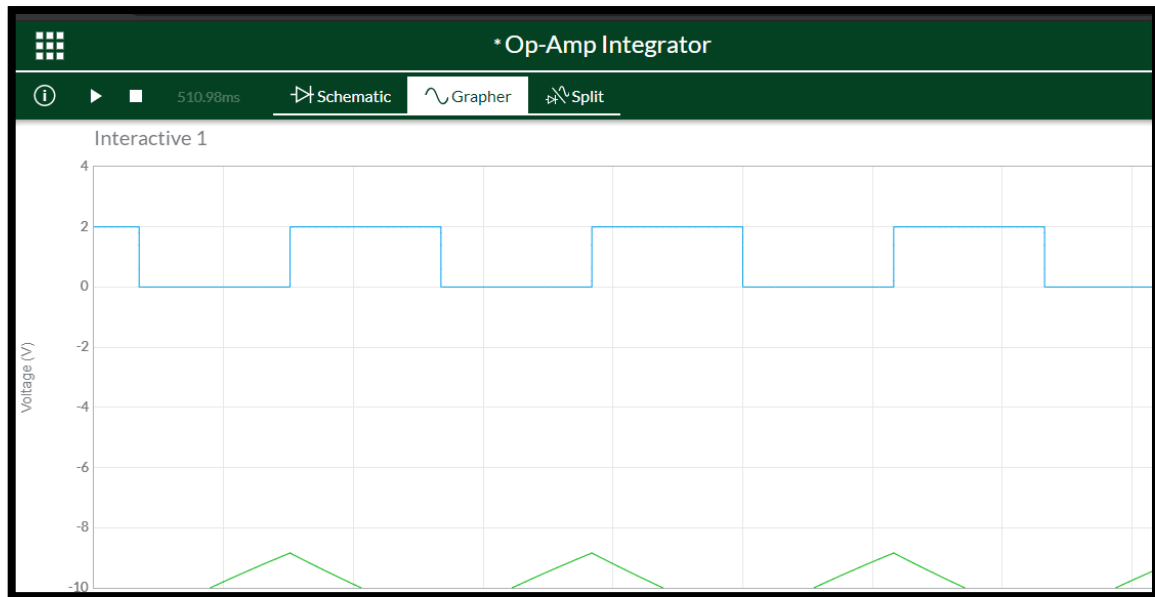
→ Op-amp as differentiator and integrator:

An op-amp differentiator or a differentiator amplifier is a **circuit configuration which is inverse of the integrator circuit**. It produces an output signal where the instantaneous amplitude is proportional to the rate of change of the applied input voltage.

→ Op-amp as differentiator and integrator:

An operational amplifier (op-amp) integrator is **an operational amplifier circuit that performs the mathematical operation of integration with respect to time**—this means the output voltage is proportional to the input voltage integrated over time.





### **OUTCOME:**

Students were able to learn operational amplifiers and their applications. They implemented and analyzed the mathematical functions such as summing, differentiation and integration using opamps.

### **DAY-5: 27/08/2021 – REPORT**

**Day -5:** The session started at 10:00 am. Faculty handled by Ambika K . About 37 students were present for the fifth day training on multi-sim.

- **Topics Covered:**

- Precision Half wave and Full wave rectifier.
- First order High & Low pass filter.

□ Zero crossing detector & Schmitt trigger.

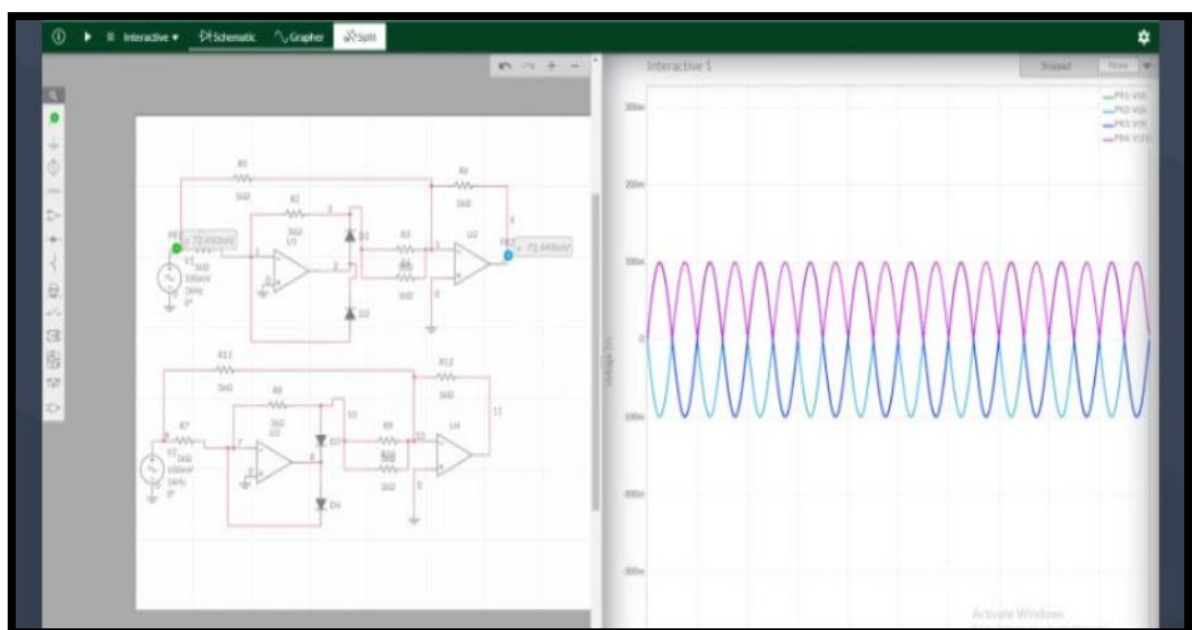
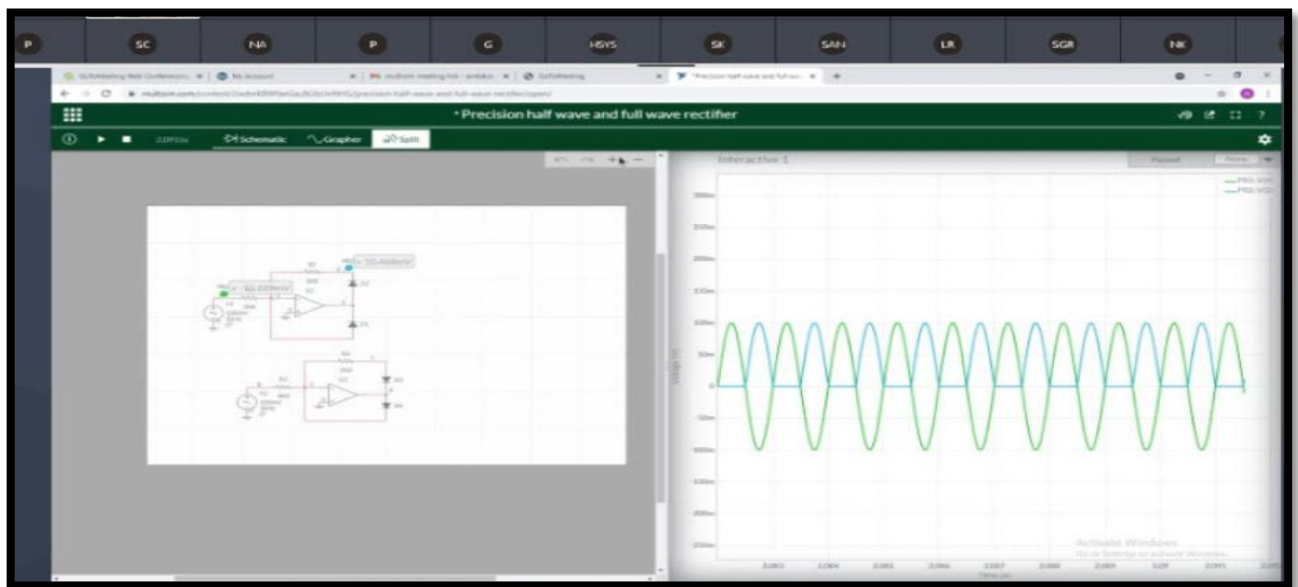
→ Wein bridge oscillator

→ Multisim installation

- **Precision Half wave and Full wave rectifier:**

→ Precision half-wave rectifiers are commonly used with other op amp circuits such as a peak-detector or bandwidth limited non-inverting amplifier to produce a DC output voltage. This configuration has been designed to work for sinusoidal input signals between 0.2mVpp and 4Vpp at frequencies up to 50 kHz.

→ The Precision Full Wave Rectifier circuits accept an Ac signal at the input, inverts either the negative or the positive half, and delivers both the inverted and non-inverted halves at the output.



- **First order High pass and Low pass filter:**

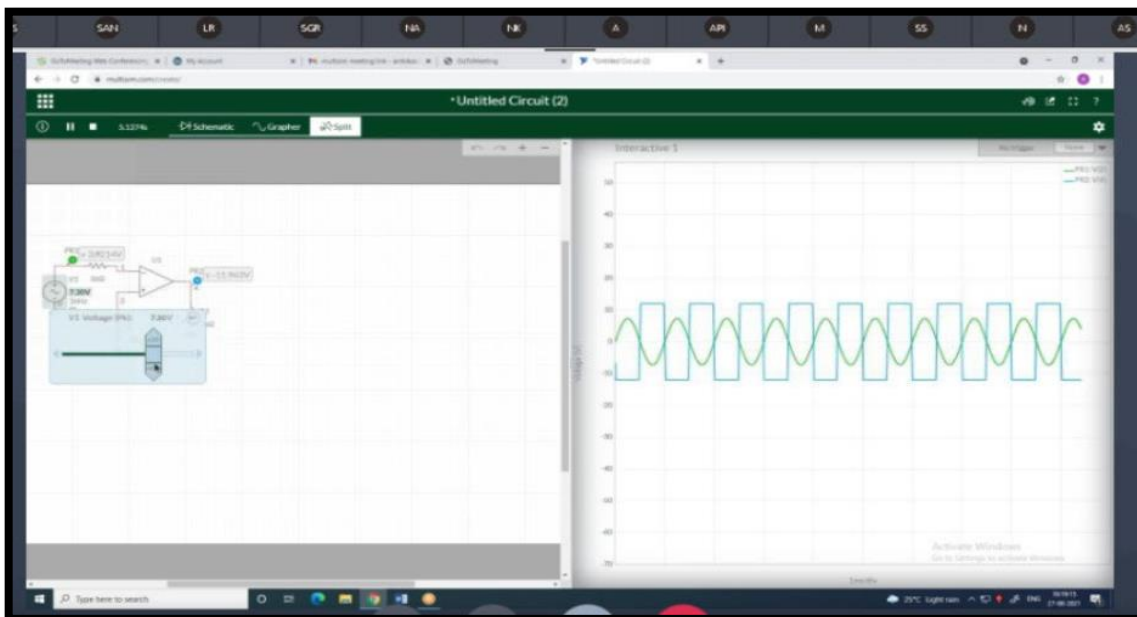
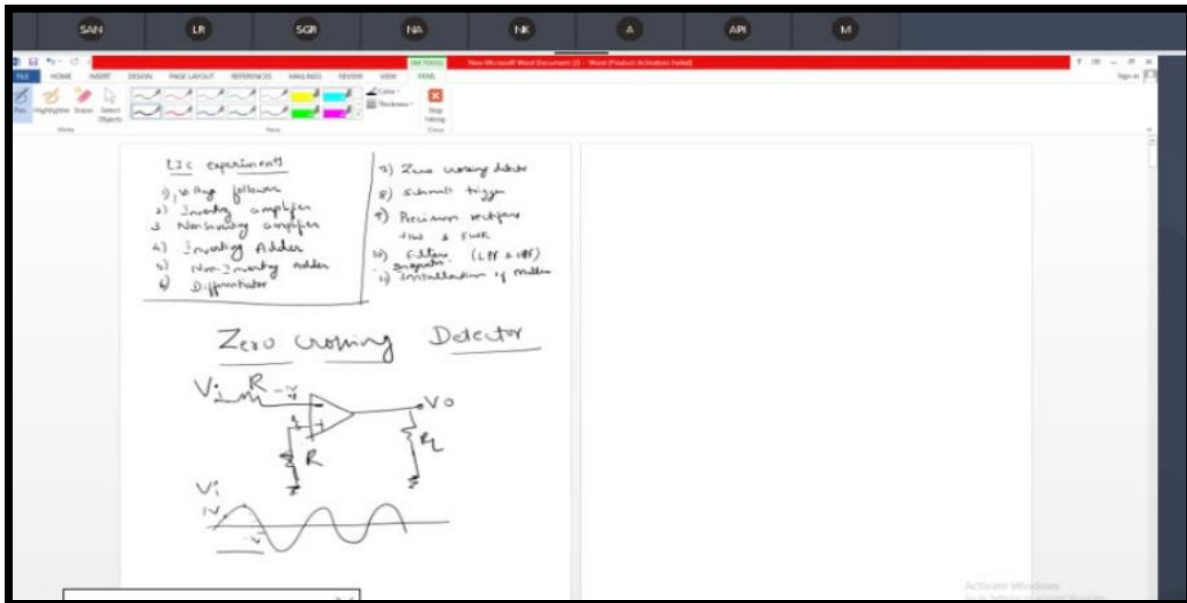
→ First-order high pass filter, consists simply of a passive filter followed by a non-inverting amplifier. The frequency response of the circuit is the same as that of the



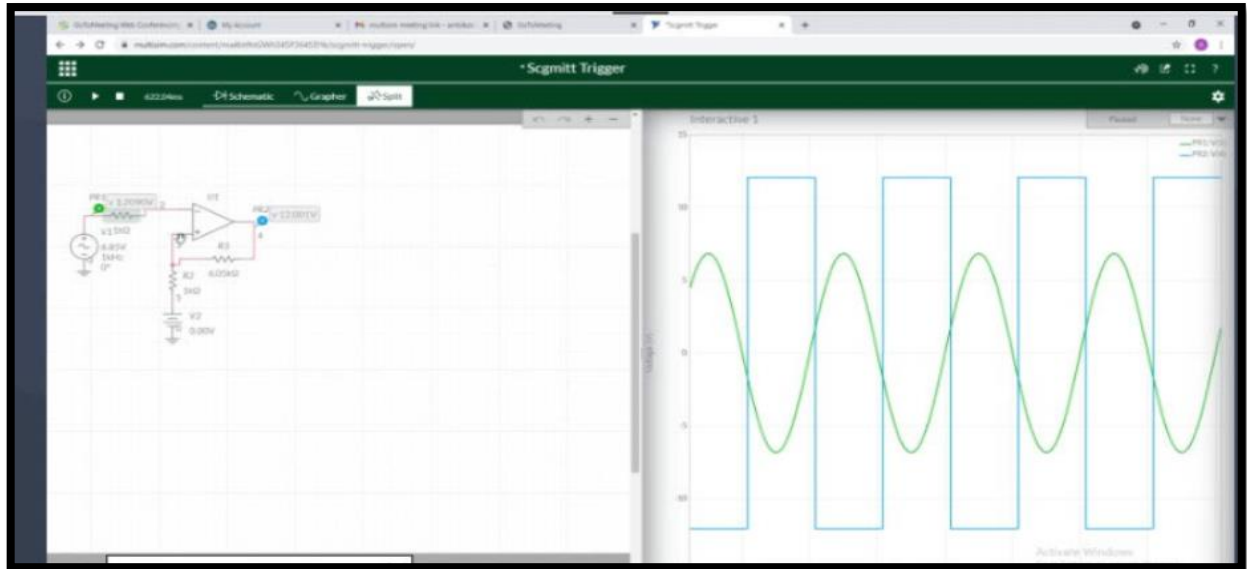
passive filter, except that the amplitude of the signal is increased by the gain of the amplifier.

→ First-order low pass active filter, consists simply of a passive RC filter stage providing a low frequency path to the input of a non-inverting operational amplifier. ... If a voltage gain greater than one is required we can use the following filter circuit.

- **Zero crossing detector:** A zero-crossing detector or ZCD is one type of voltage comparator, used to detect a sine waveform transition from positive and negative that coincides when the I/P crosses the zero voltage condition. The applications of the Zero Crossing Detector are phase meter and time marker generator.



- **Schmitt Trigger:** Schmitt trigger is a comparator circuit with hysteresis implemented by applying positive feedback to the noninverting input of a comparator or differential amplifier. It is an active circuit which converts an analog input signal to a digital output signal. The circuit is named a "trigger" because the output retains its value until the input changes sufficiently to trigger a change.



- **Wein Bridge Oscillator:** A Wien bridge oscillator is a type of electronic oscillator that generates sine waves. It can generate a large range of frequencies. The oscillator is based on a bridge circuit originally developed by Max Wien in 1891 for the measurement of impedances. The bridge comprises four resistors and two capacitors. The oscillator can also be viewed as a positive gain amplifier combined with a bandpass filter that provides positive feedback.

### **OUTCOME:**

Students were able to implement the above mentioned content. They could analyze the practical aspects of the circuit using theoretical knowledge on multi-sim platform. They were able to learn operational amplifiers and their applications. They learnt some application such as wein bridge oscillator, precision half wave & full wave, first order high pass & low pass filter.

### **DAY-6: 30/08/2021 – REPORT**

**Day -6:** The session started at 10:00 am. Faculty handled by P.S Gowra . About 30 students were present for the sixth day training on multi-sim.

- **Topics Covered:**

- Clipping circuits (single/double ended).
- Transistor as a Switch
- Briefing about mini project.

- **CLIPPING CIRCUITS:**

A clipper is a device that removes either the positive half (top half) or negative half (bottom half), or both positive and negative halves of the input AC signal. In other words, a clipper is a device that limits the positive amplitude or negative amplitude or both positive and negative amplitudes

of the input AC signal. In some cases, a clipper removes a small portion of the positive half cycle or negative half cycle or both positive and negative half cycles.

The clipping of a waveform is the most common technique that applies to the input signals to adapt them so that they may lie within the operating range of the electronic circuits. The clipping of waveforms can be done by eliminating the portions of the waveform which crosses the input range of the circuit.

Clippers can be broadly classified into two basic types of circuits. They are:

- Series Clippers
- Shunt or Parallel Clippers

Series clipper circuit contains a power diode in series with the load connected at the end of the circuit.

The shunt clipper contains a diode in parallel with the resistive load.

ting: P S Gowra View Everyone 28

You may be experiencing difficulties. To help, please close an application or switch to tel

Series Clippers-Biased Clipper Circuits 3 & 4 with +Vref  
**Always  $V_i(\text{peak})$  has to be greater than  $V_R$**   
Assume  $V_i = 10 \sin \omega t$ ,  $V_R = 4V$  for analysis purpose.

Prepared by P.S.Gowra, Department of ETE, BMSCE 44

Positive\_Series\_CL - Multisim - [Positive\_Series\_CL]

File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help

Design Toolbox

Positive\_Series\_CL

Positive\_Series\_CL

Function generator-XFG1

Waveforms

Signal options

Frequency: 1 kHz

Duty cycle: 50 %

Amplitude: 10 Vp

Offset: 0 V

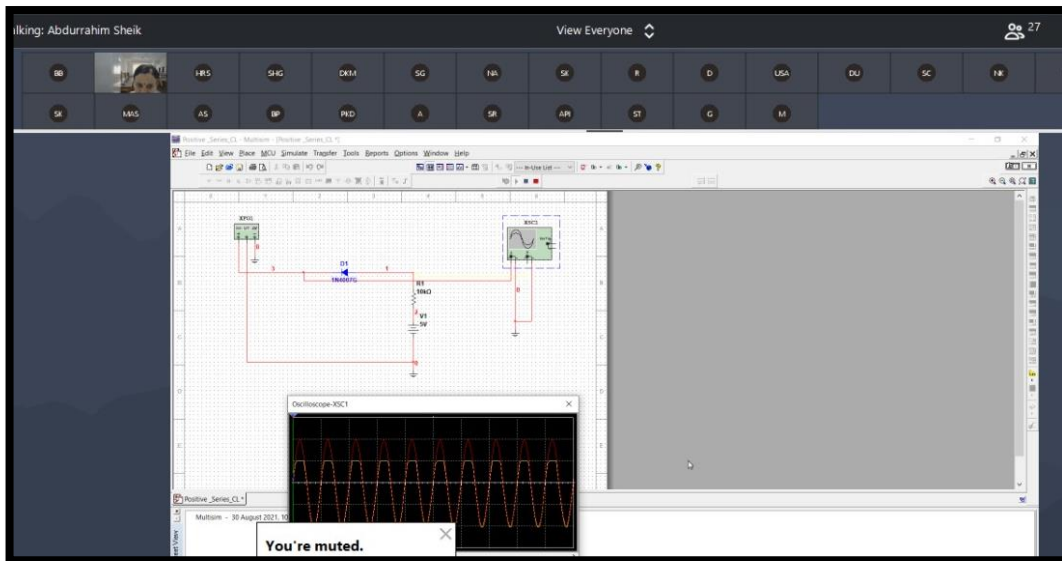
Set max/roll time

Common

You're muted.

Click the microphone to unmute.

P S Gowra is presenting



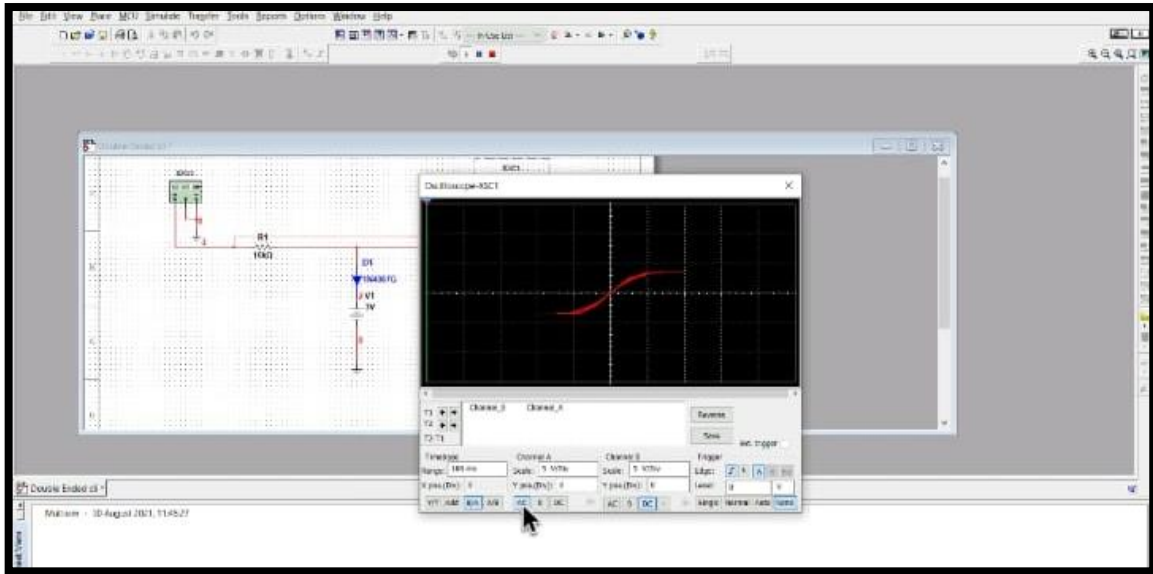
- **DOUBLE ENDED CLIPPERS:**

Sometimes it is desired to remove a small portion of both positive and negative half cycles. In such cases, the dual clippers are used.

The dual clippers are made by combining the biased shunt positive clipper and biased shunt negative clipper.

**Double Ended Clipper- Circuit I**  
 Assume  $V_i = 10\sin\omega t$ ,  $V_{R1} = 4V$ ,  $V_{R2} = 6V$  and Silicon diodes. For ideal diodes  $V_K = 0V$ .

Input voltage	Diode status	Output voltage	Slope
$v_i \leq V_{R1} - V_K$	$D_1$ on, $D_2$ off	$v_o = V_{R1} - V_K$	0
$V_{R1} - V_K < v_i < V_{R2}$	$D_1$ off, $D_2$ off	$v_o = v_i$	1
$v_i \geq V_{R2} + V_K$	$D_1$ off, $D_2$ on	$v_o = V_{R2} + V_K$	0



- **TRANSISTOR AS A SWITCH:**

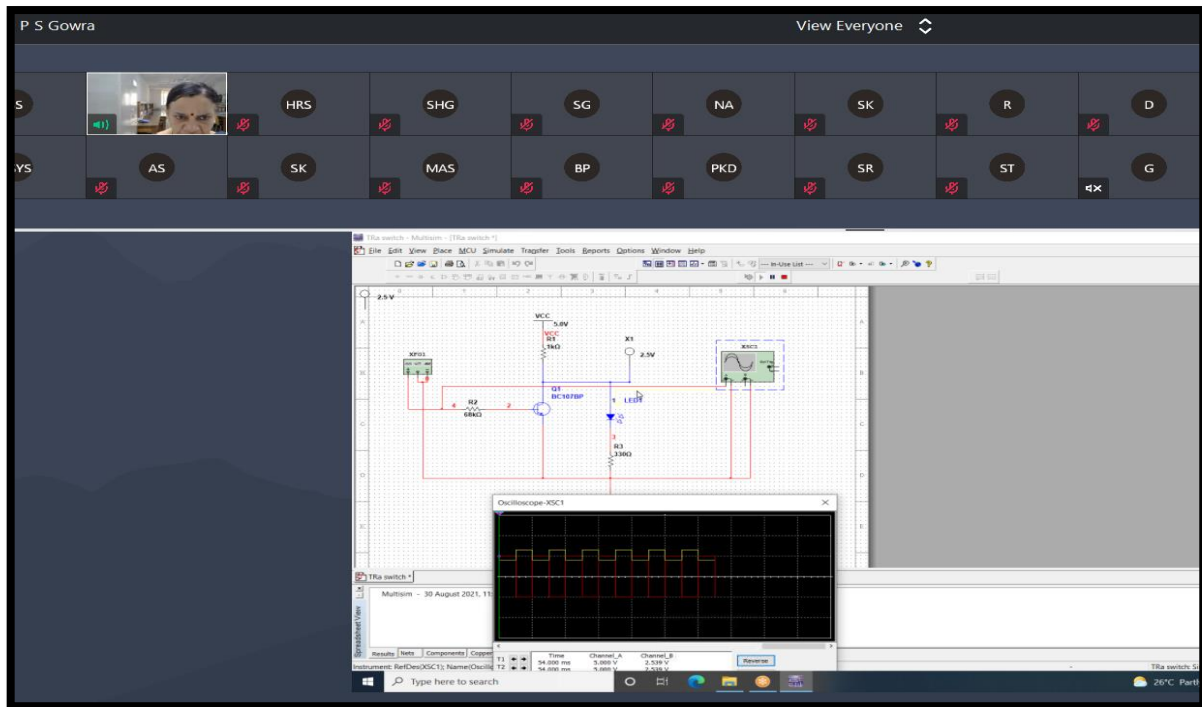
Using a transistor as a switch is the simplest application of the device. A transistor can be extensively used for switching operation either for opening or closing of a circuit. Meanwhile, the basic concept behind the operation of a transistor as a switch relies on its mode of operation. Generally, the low voltage DC is turned on or off by transistors in this mode.

Both PNP and NPN transistors can be utilized as switches. A basic terminal transistor can be handled differently from a signal amplifier by biasing both NPN and PNP bipolar transistors by an "ON / OFF" static switch. One of the main uses of the transistor to transform a DC signal "On" or "OFF" is solid-state switches.

 A screenshot of a Zoom meeting interface. The top part shows a grid of participants with their names and video thumbnails. Below the grid, a document titled "Analog Electronic Circuits Lab Manual [Compatibility Mode] - Word" is shared. The document content includes:
 

**Experiment No.1**  
**Transistor as a switch**  
**Aim:** To understand the working of transistor as a switch.  
**Components:** NPN Transistor BC107/147, Resistors 330Ω, 1KΩ, 68 KΩ, square wave generator, fixed power supply 5V, red LED.

 Below the text is a circuit diagram showing a square wave generator connected to the base of an NPN transistor (Q1, BC107BP) through a resistor (RB, 68K). The emitter is grounded. The collector is connected to a 5V supply (VCC) through a resistor (RC, 1K) and to an LED through a resistor (R, 330Ω). The LED is also connected to ground.



### **OUTCOME:**

Students were able to implement the above mentioned content. They could analyze the practical aspects of the circuit using theoretical knowledge on multi-sim platform. They were able to learn clipping circuits and transistors its working and applications and were also able to analyze transistor working as switch with respective waveforms.

### **DAY-7: 31/08/2021 – REPORT**

**Day -7:** The session started at 10:00 am. Faculty handled by P.S Gowra . About 30 students were present for the sixth day training on multi-sim.

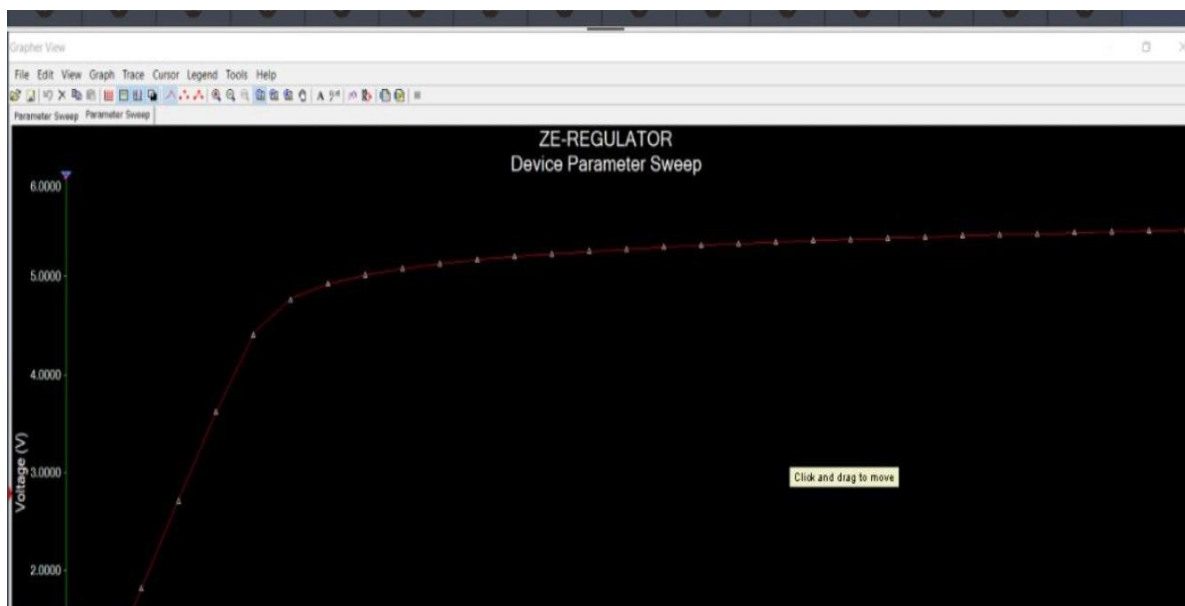
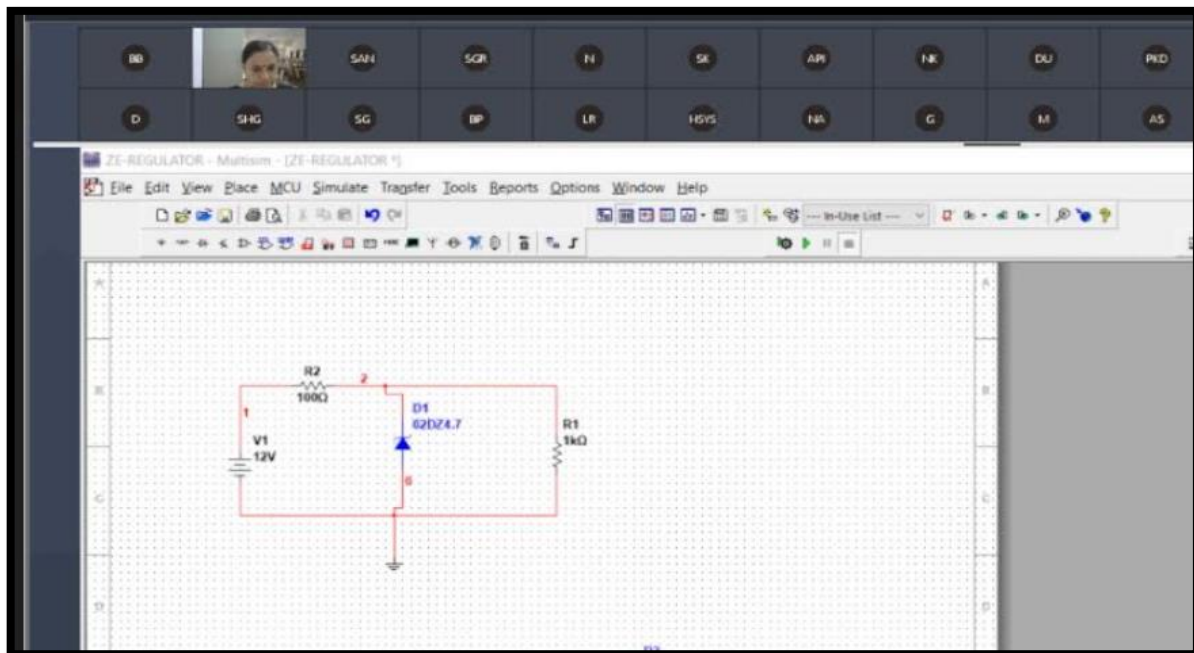
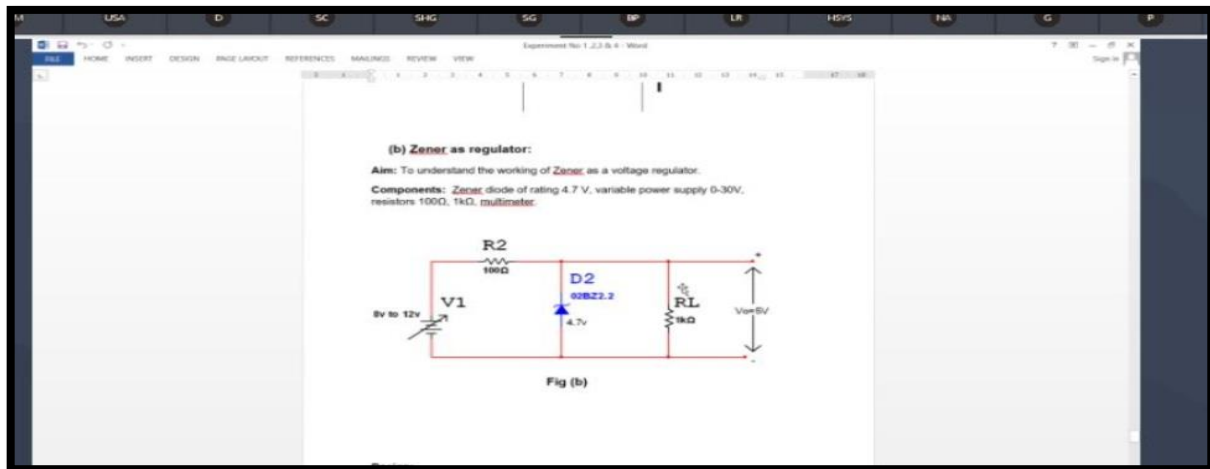
- **Topics Covered:**

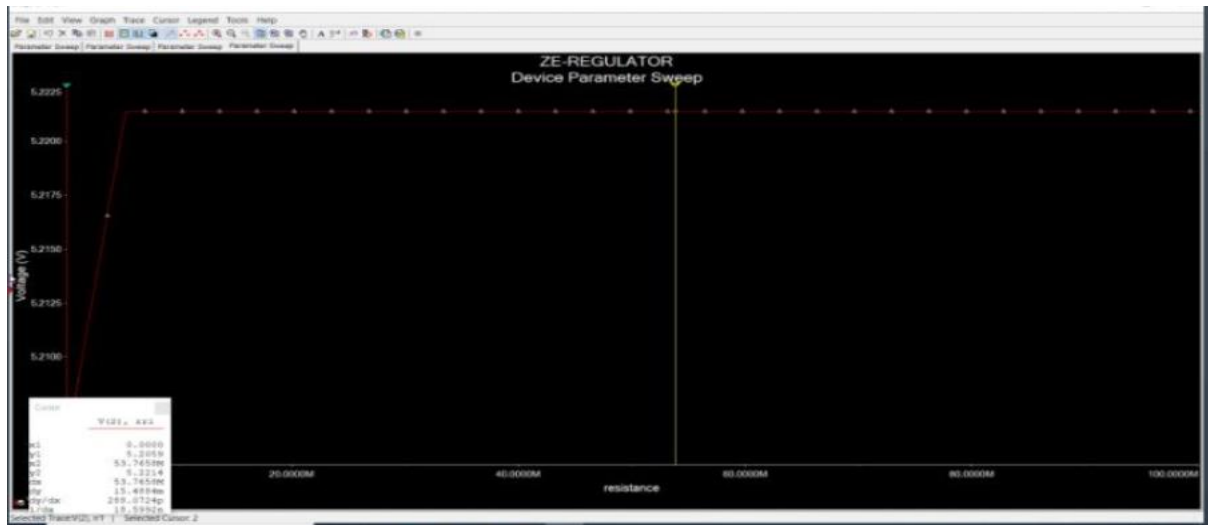
- Zener as Voltage regulator to determine Line/Load regulation.
  - Clippers
- RC coupled amplifier using multi-sim & virtual lab
  - BJT as RC phase shift oscillator.

- **Zener as Voltage regulator:**

- The Zener voltage regulator consists of a current limiting resistor  $R_S$  connected in series with the input voltage  $V_S$  with the Zener diode connected in parallel with the load  $R_L$  in this reverse biased condition. The stabilized output voltage is always selected to be the same as the breakdown voltage  $V_Z$  of the diode.
- Line regulation: Series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.

→ Load Regulation: Input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.





- **Clampers:**

Clampers can also be referred as DC restorers. Clamping circuits are designed to shift the input waveform either above or below a DC reference level without altering the shape of the waveform. This shifting of the waveform results in a change in the DC average voltage of the input waveform. The levels of peaks in the signal can be shifted using the clamper circuit, hence clampers can also be referred as level shifters.

**Types of Clampers**

- (1) Positive Peak Clamper ( Negative Clamper )
  - (a) With  $V_{ref} = 0V$
  - (b) With  $V_{ref} = +ve$
  - (c) With  $V_{ref} = -ve$
- (2) Negative Peak Clamper ( Positive Clamper )
  - (a) With  $V_{ref} = 0V$
  - (b) With  $V_{ref} = +ve$
  - (c) With  $V_{ref} = -ve$

Prepared by P.S.Gowri, Department of ETE, BPSCCE 62

Mic Camera Screen Leave



Three Positive Peak Clampers(-ve Clampers) and Three Negative Peak Clampers(+ve Clampers) with i/p and o/p waveforms

**Summary of Clamper Circuits**

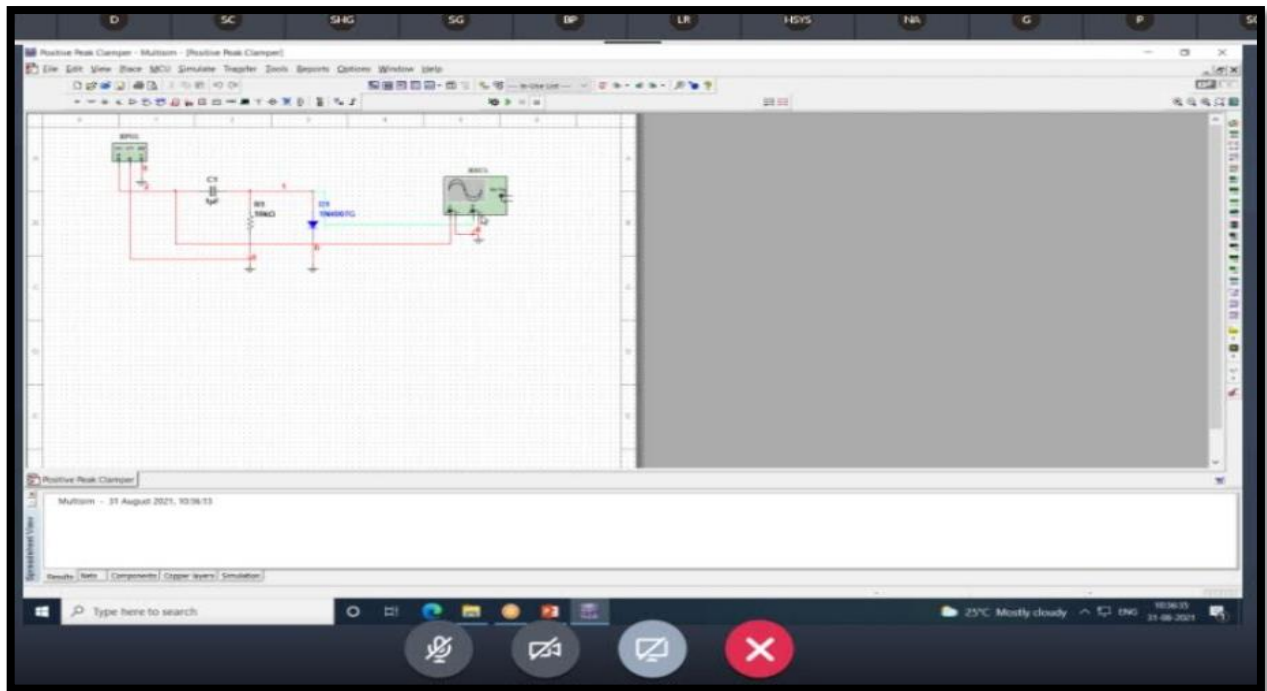
Prepared by PS Gowers, Department of ETE, BMSCE 65

Clampers can be broadly classified into two types. They are:

- Positive Clampers
- Negative Clampers

**Positive Clamper:** This type of clamping circuit shifts the input waveform in a positive direction, as a result the waveform lies above a DC reference voltage.

**Negative Clamper:** This type of clamping circuit shifts the input waveform in a negative direction, as a result the waveform lies below a DC reference voltage.

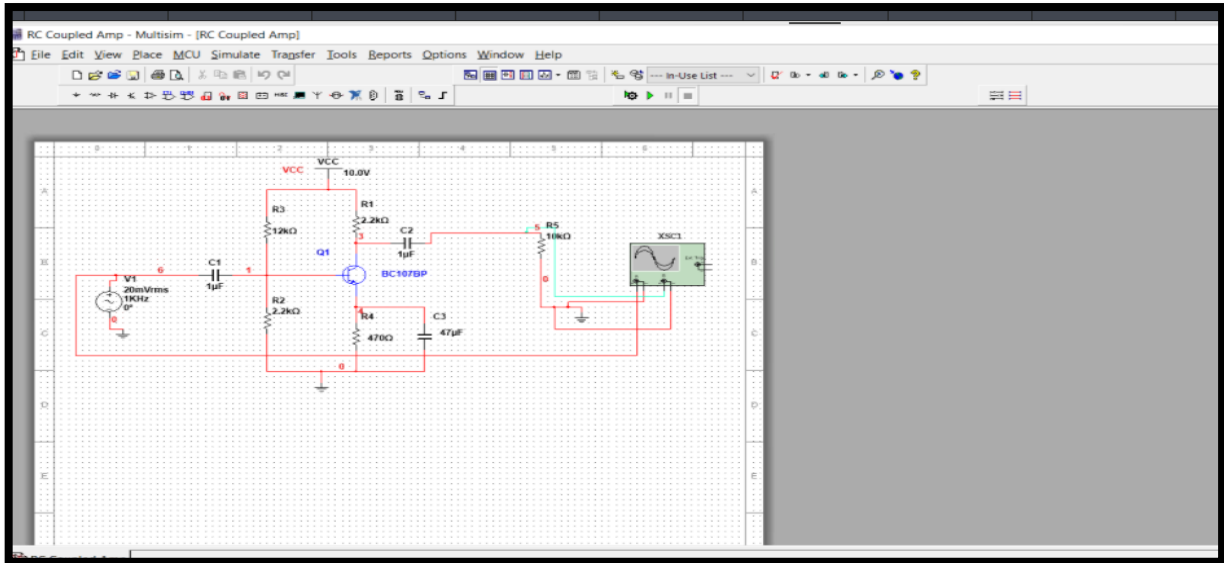


- **RC coupled amplifier:**

A Resistance Capacitance (RC) Coupled Amplifier is basically a multi-stage amplifier circuit extensively used in electronic circuits. Here the individual stages of the amplifier are connected together using a resistor–capacitor combination due to which it bears its name as RC Coupled. The design of individual stages of the RC coupled amplifiers is similar to that in the case of common emitter amplifiers in which the resistors  $R_1$  and  $R_2$  form the biasing network while the emitter resistor  $R_E$  form the stabilization network.

The  $C_E$  is also called bypass capacitor which passes only AC while restricting DC, which causes only DC voltage to drop across  $R_E$  while the entire AC voltage will be coupled to the next stage.

Further, the coupling capacitor  $C_C$  also increases the stability of the network as it blocks the DC while offers a low resistance path to the AC signals, thereby preventing the DC bias conditions of one stage affecting the other. In addition, in this circuit, the voltage drop across the collector-emitter terminal is chosen to be 50% of the supply voltage  $V_{CC}$  in order to ensure appropriate biasing point.



AC\_POWER

Label	Display	Value	Fault	Pins	User fields
Voltage (RMS):		20m			V
Voltage offset:		0			V
Frequency (F):		1K			Hz
Time delay:		0			s
Damping factor (1/s):		0			=
Phase:		0			=
AC analysis magnitude:		1			V
AC analysis phase:		0			=
Distortion frequency 1 magnitude:		0			V
Distortion frequency 1 phase:		0			=
Distortion frequency 2 magnitude:		0			V
Distortion frequency 2 phase:		0			=
Tolerance:		0			=

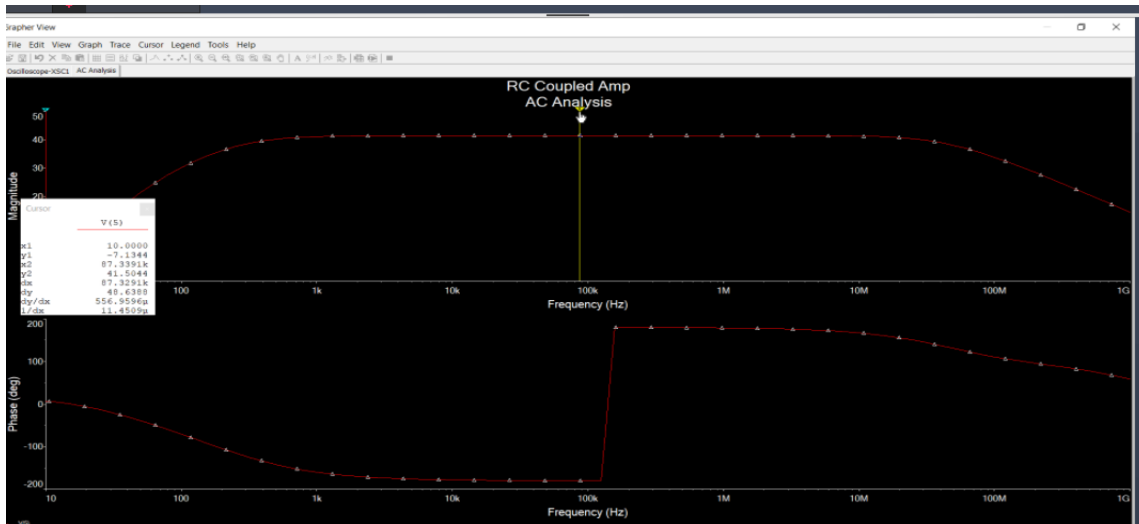
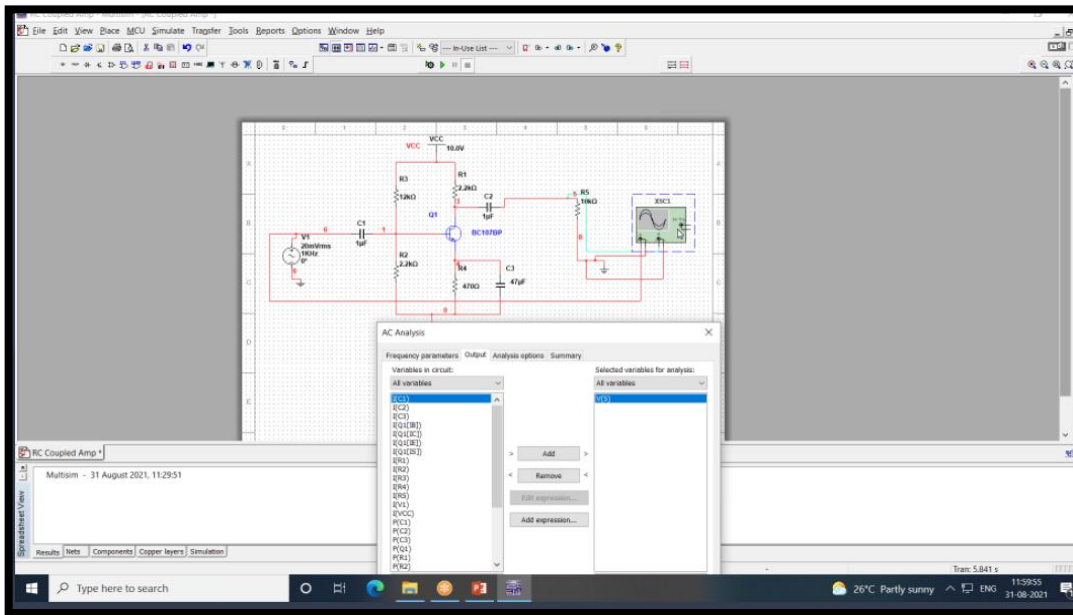
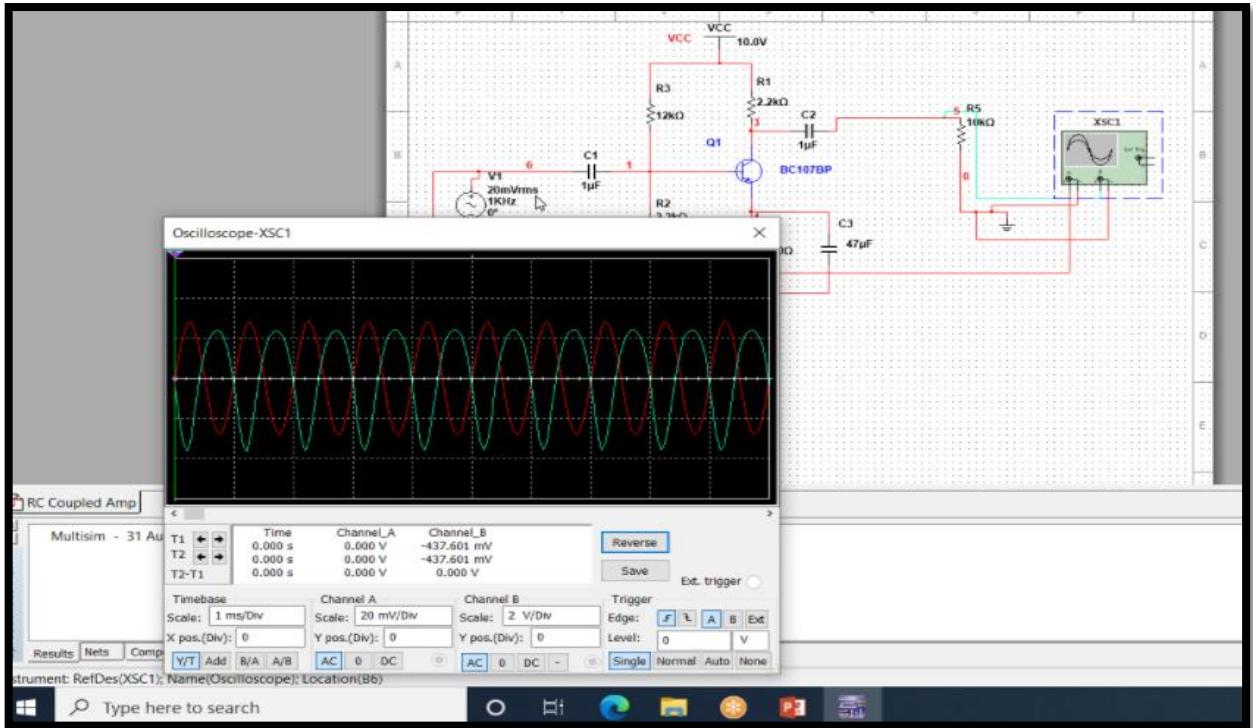
RC Coupled A

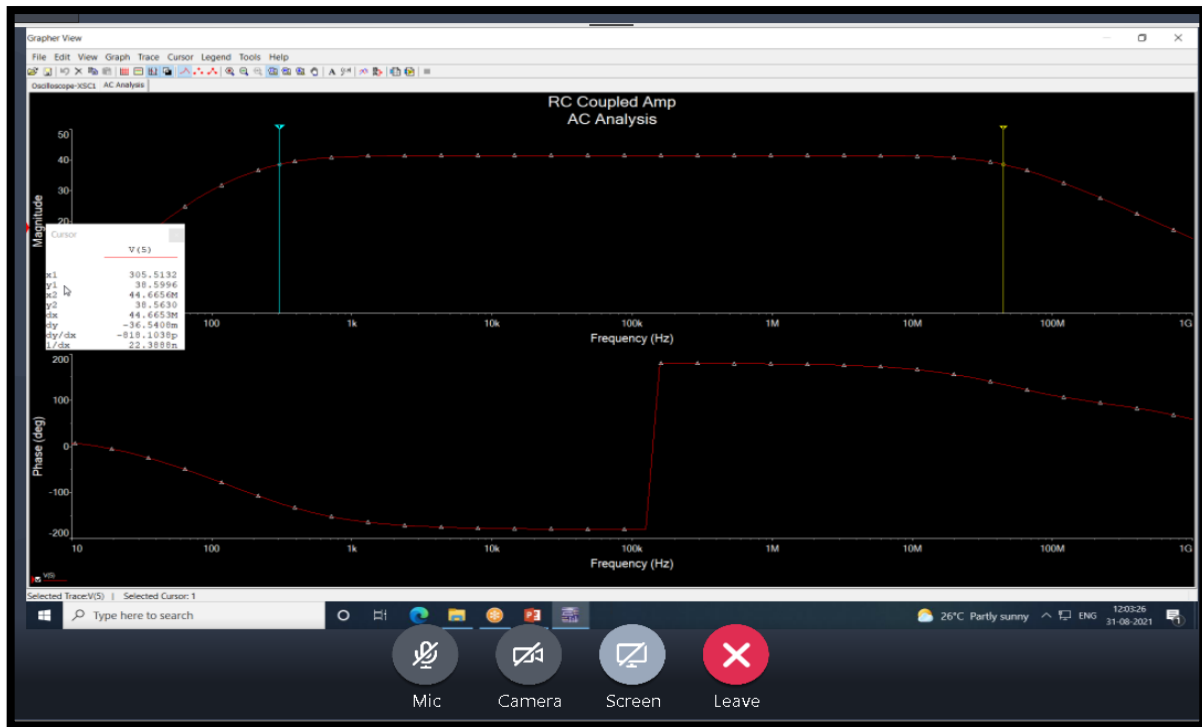
Multisim

Spreadsheet View

Results Nets

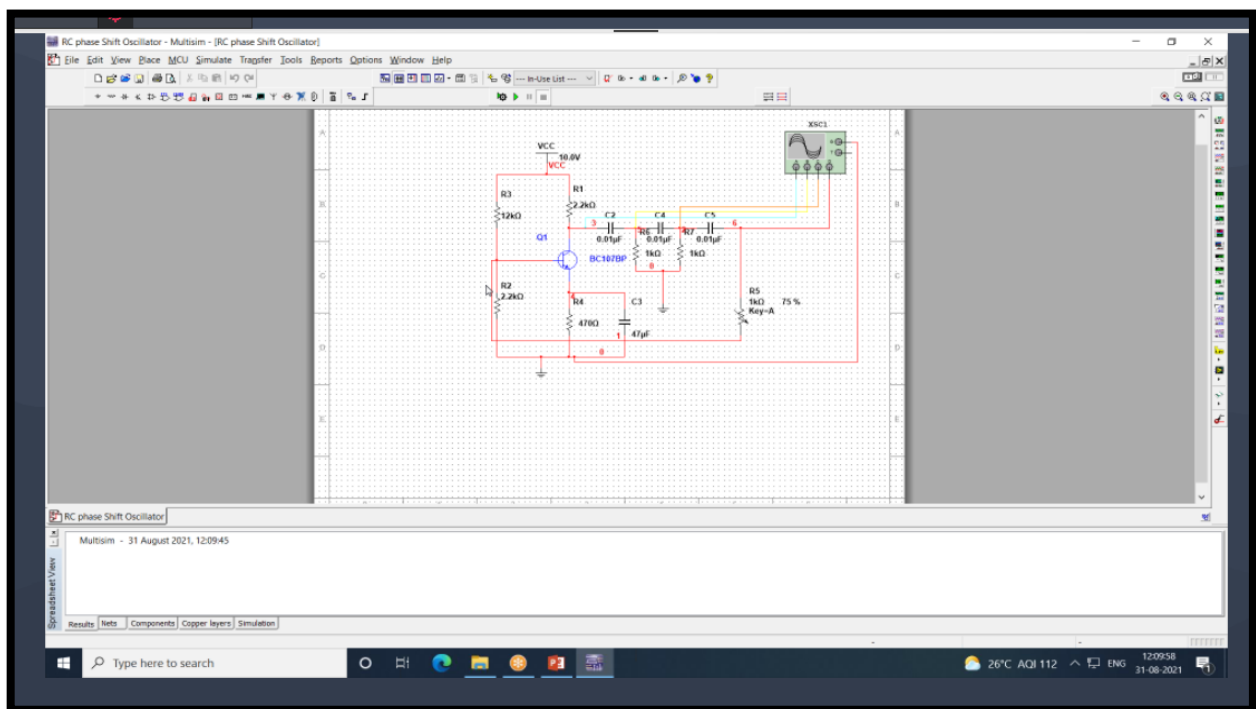
Type here to search

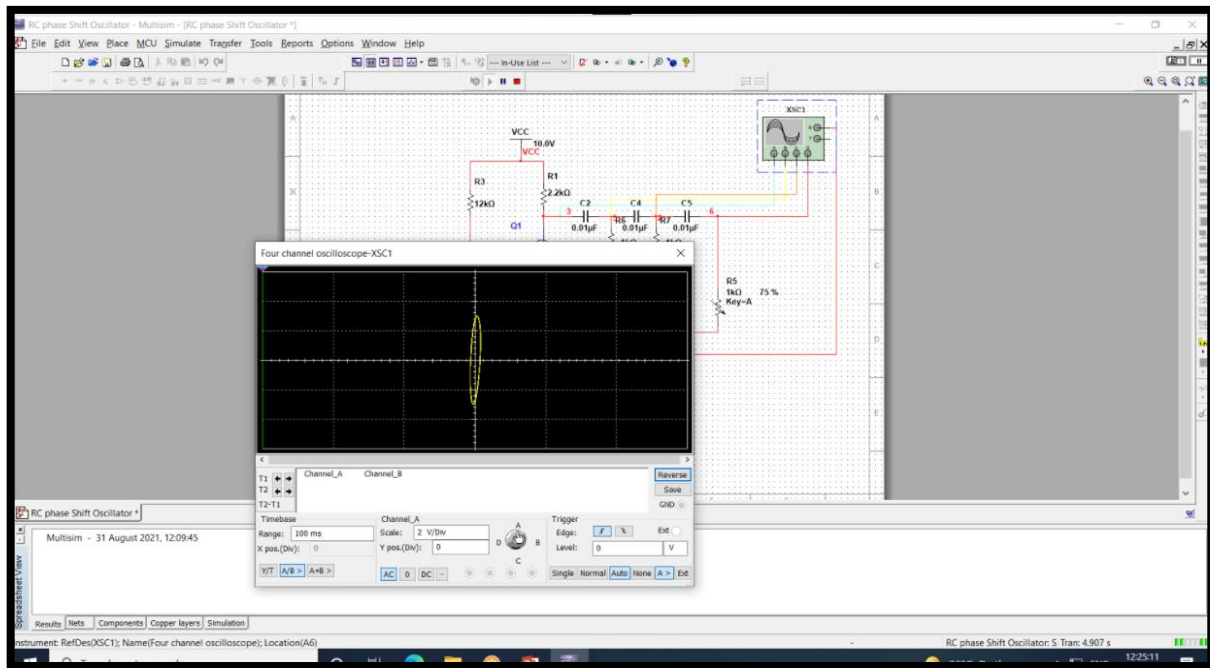
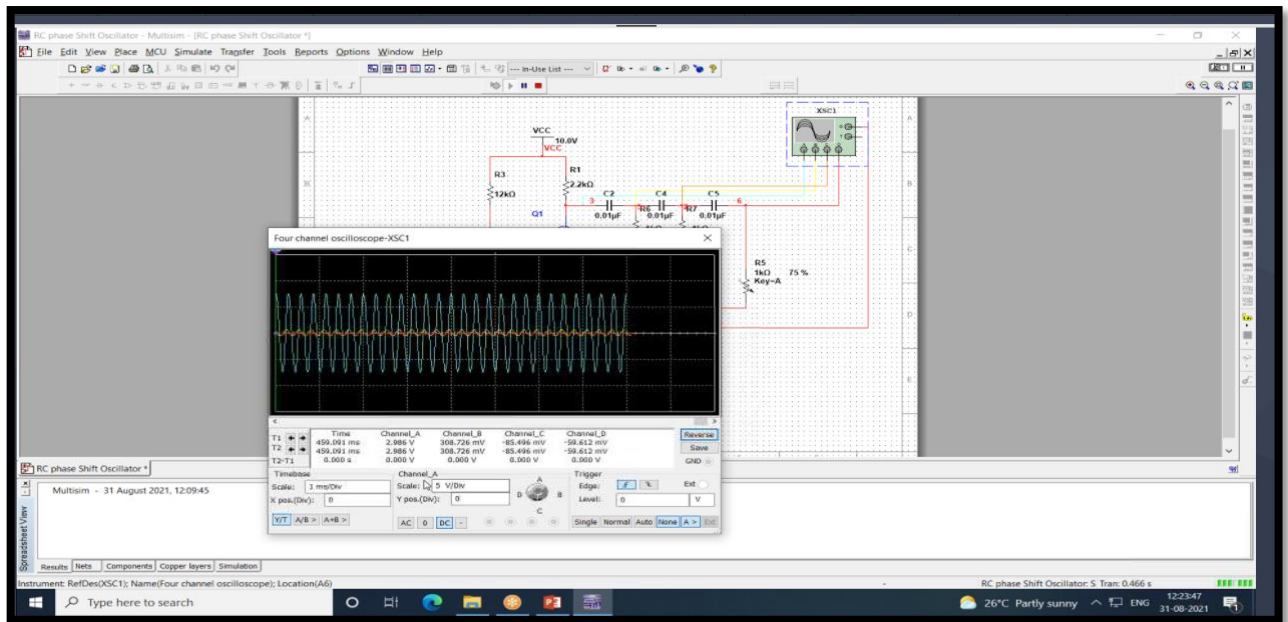




- **BJT as RC Phase shift oscillator:**

RC phase-shift oscillator circuit can be built with a resistor as well as a capacitor. This circuit offers the required phase shift with the feedback signal. They have outstanding frequency strength and can give a clean sine wave for an extensive range of loads. Preferably an easy RC network can be expected to include an o/p which directs the input with 90 degree. The following RC phase shift oscillator circuit using BJT can be built by cascading 3-RC phase shift networks; each provides a  $60^{\circ}$  phase shift. In the circuit, the RC which is known as the collector resistor stops the transistor's collector current.





### **OUTCOME:**

Students were able to implement the above mentioned content. They could analyze the practical aspects of the circuit using theoretical knowledge on multi-sim platform. They were able to learn Zener as voltage regulator and also determine it has line and load regulations. They also learnt RC coupled amplifier in multi-sim as well as in virtual lab. They learnt BJT as RC phase shift oscillator. Also clamping circuits were also taught to implement.

### **DAY-8: 01/09/2021 – REPORT**

**Day -8:** The session started at 10:00 am. Faculty handled by P.S Gowra . About 33 students were present for the sixth day training on multi-sim.

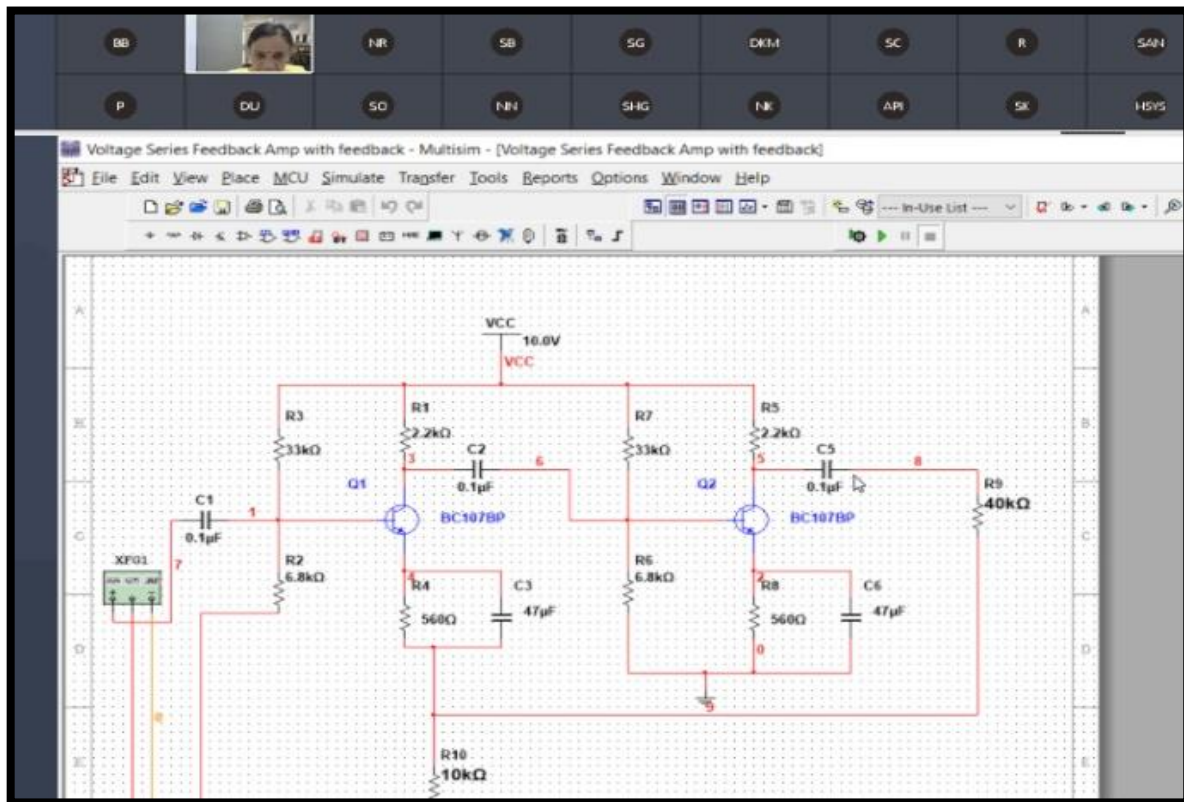
- **Topics Covered:**

- Voltage series with and without feedback.
- Drain and source characteristics of MOSFET.
- RC coupled circuits in Virtual lab.

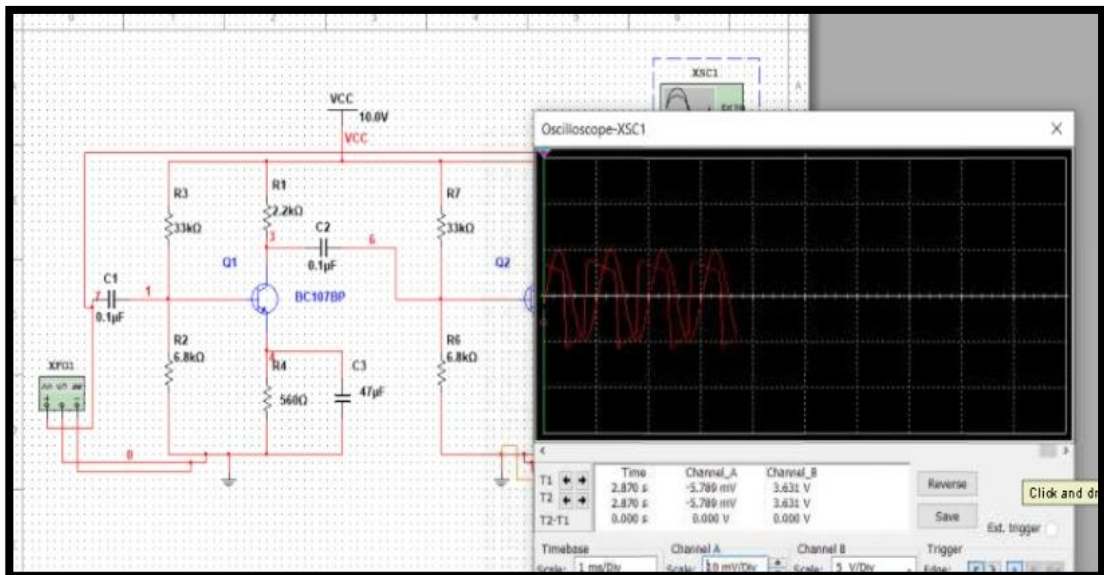
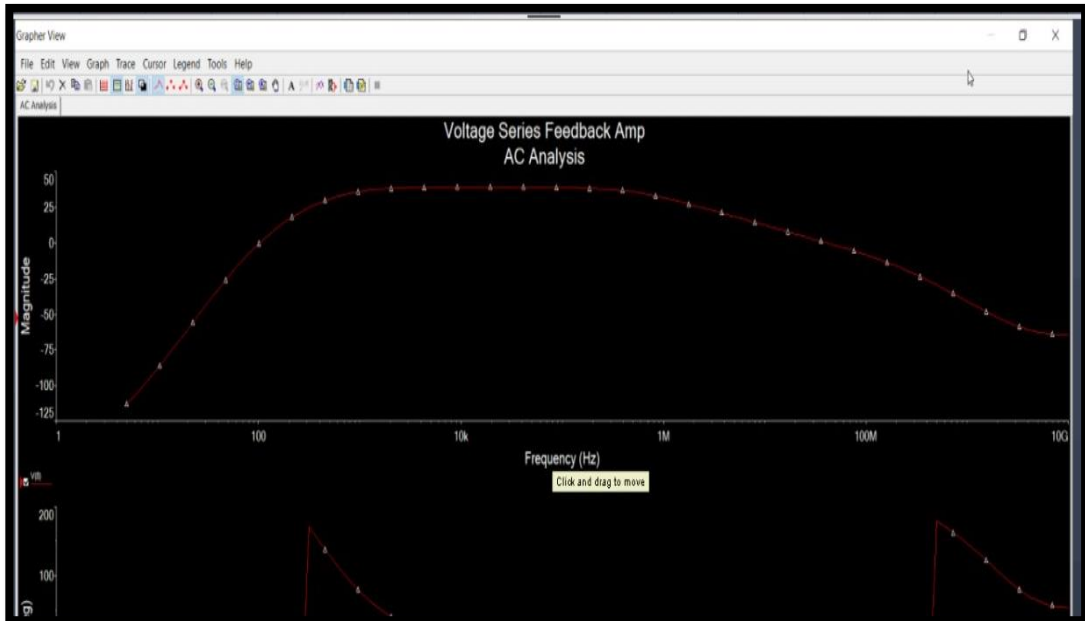
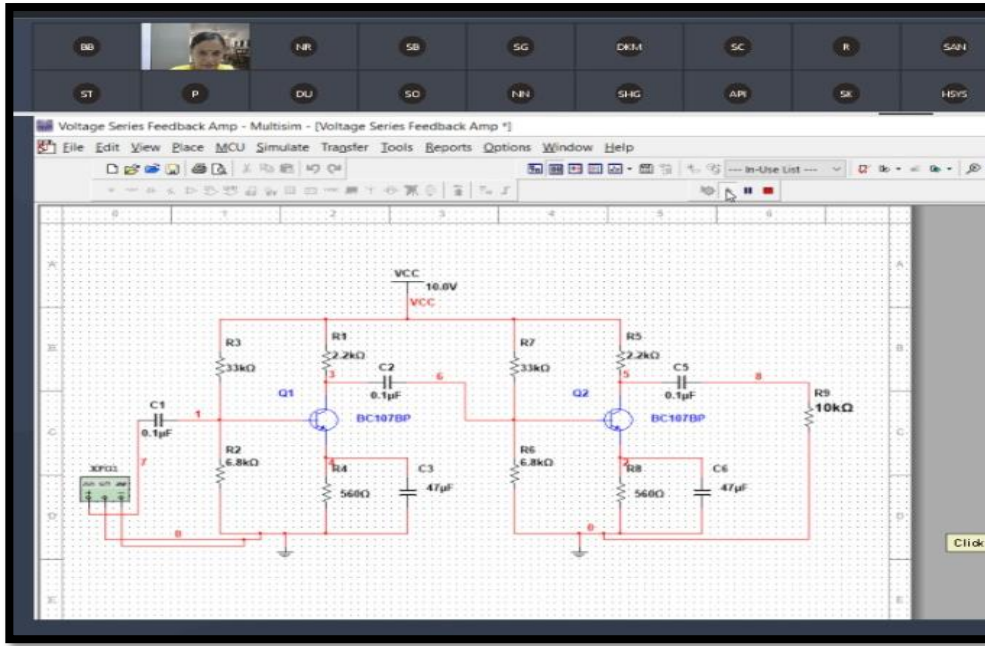
- **Voltage series feedback amplifier with feedback:**

When any increase in the output signal results into the input in such a way as to cause the decrease in the output signal, the amplifier is said to have negative feedback. The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that by proper use of this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative

feedback is that the voltage gain is decreased. In Voltage-Series feedback, the input impedance of the amplifier is increased and the output impedance is decreased. Noise and distortions are reduced considerably.



- **Voltage series feedback amplifier without feedback:**



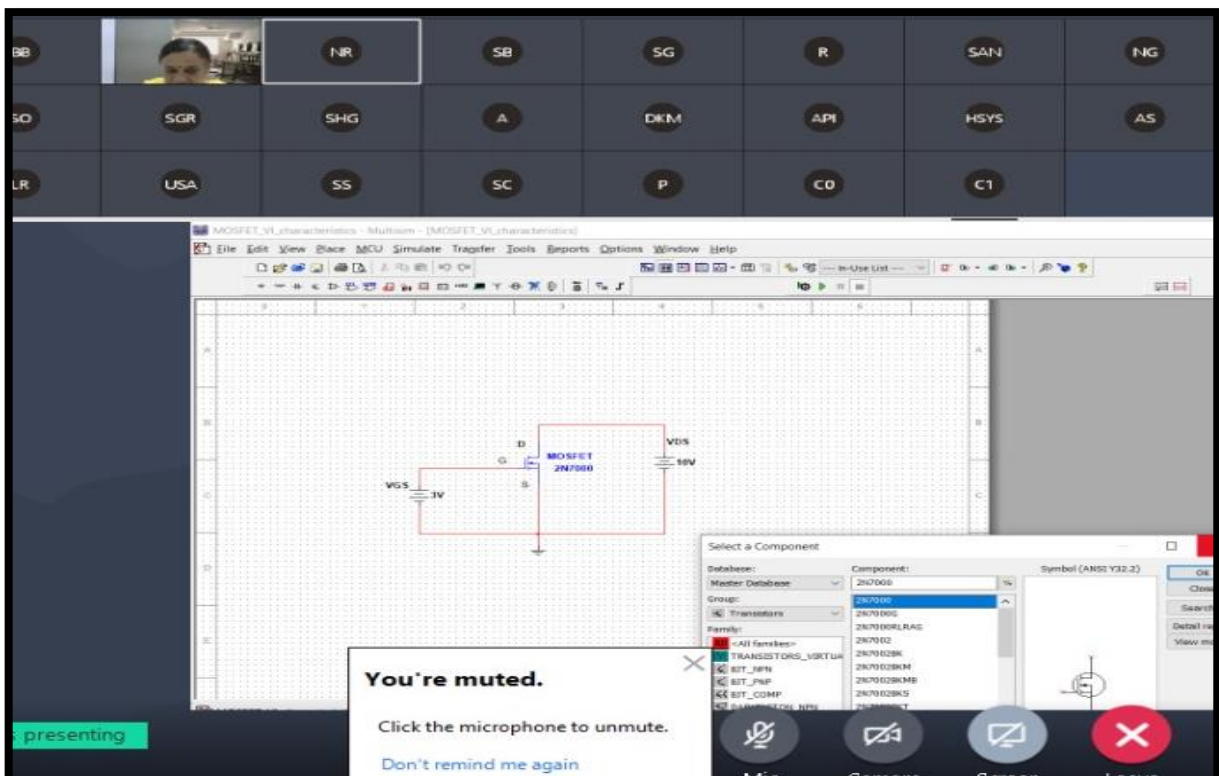
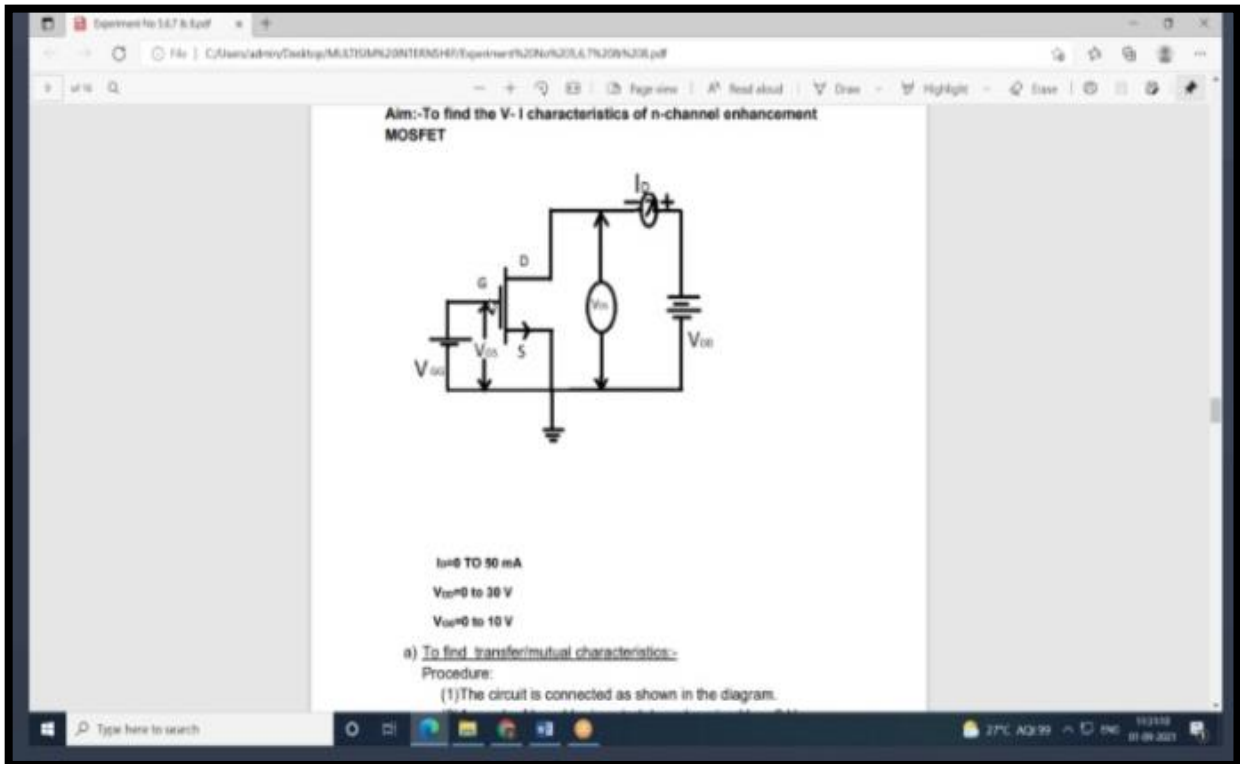


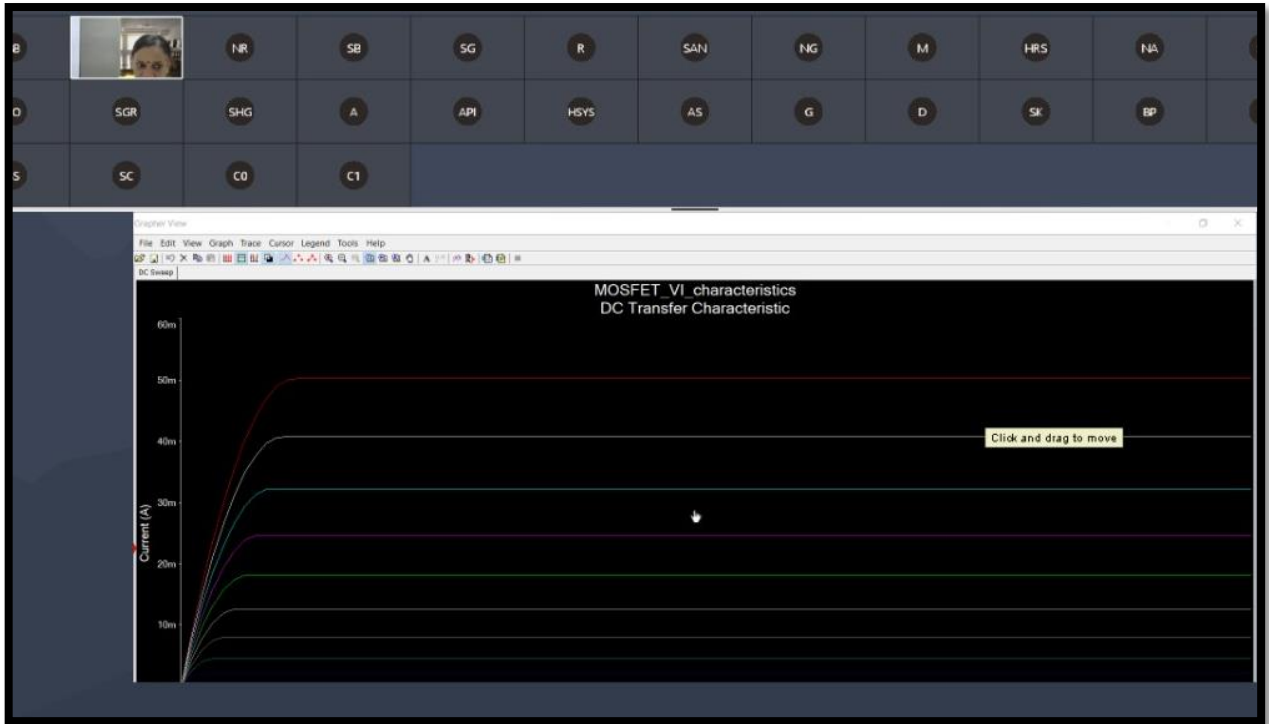
- Drain and source characteristics of MOSFET :

MOSFET stands for Metal Oxide Silicon Field Effect Transistor or Metal Oxide Semiconductor Field Effect Transistor.

The drain characteristics of a MOSFET are drawn between the drain current  $I_D$  and the drain source voltage  $V_{DS}$ . The characteristic curve is as shown below for different values of inputs.

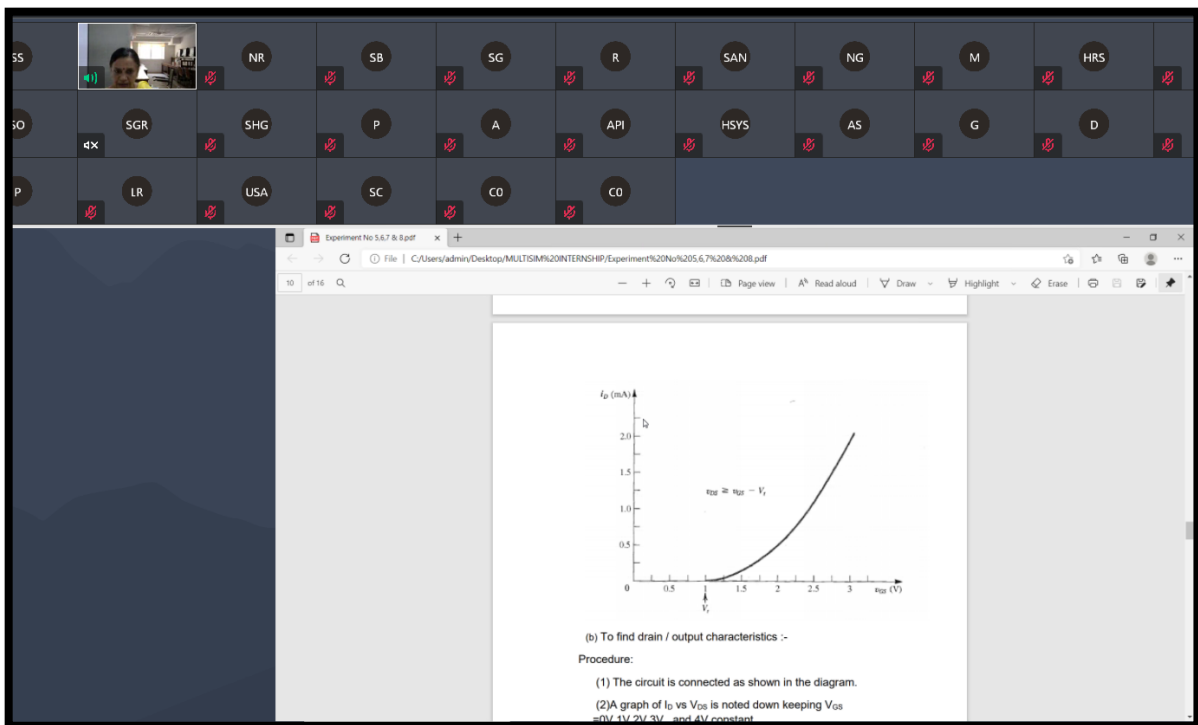
Actually when  $V_{DS}$  is increased, the drain current  $I_D$  should increase, but due to the applied  $V_{GS}$ , the drain current is controlled at certain level. Hence the gate current controls the output drain current.

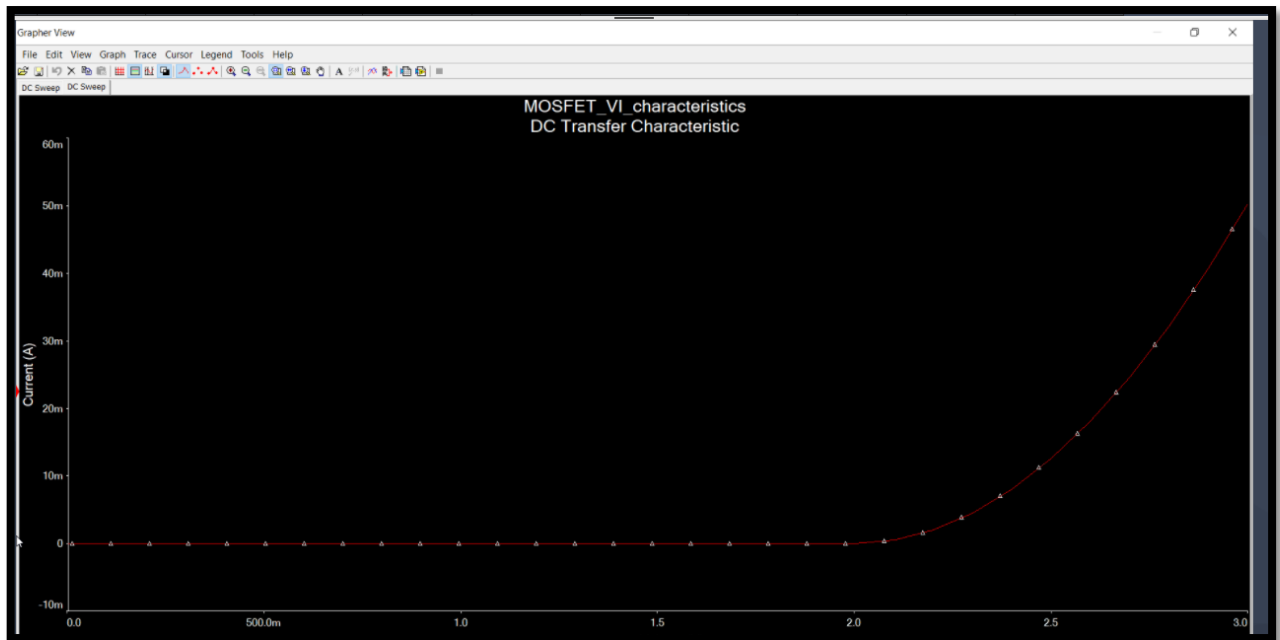




### Transfer Characteristics

Transfer characteristics define the change in the value of  $V_{DS}$  with the change in  $I_D$  and  $V_{GS}$  in both depletion and enhancement modes. The below transfer characteristic curve is drawn for drain current versus gate to source voltage.





- RC coupled circuits in Virtual lab:

Virtual Labs  
An MoE, Govt of India Initiative

### CE Amplifier

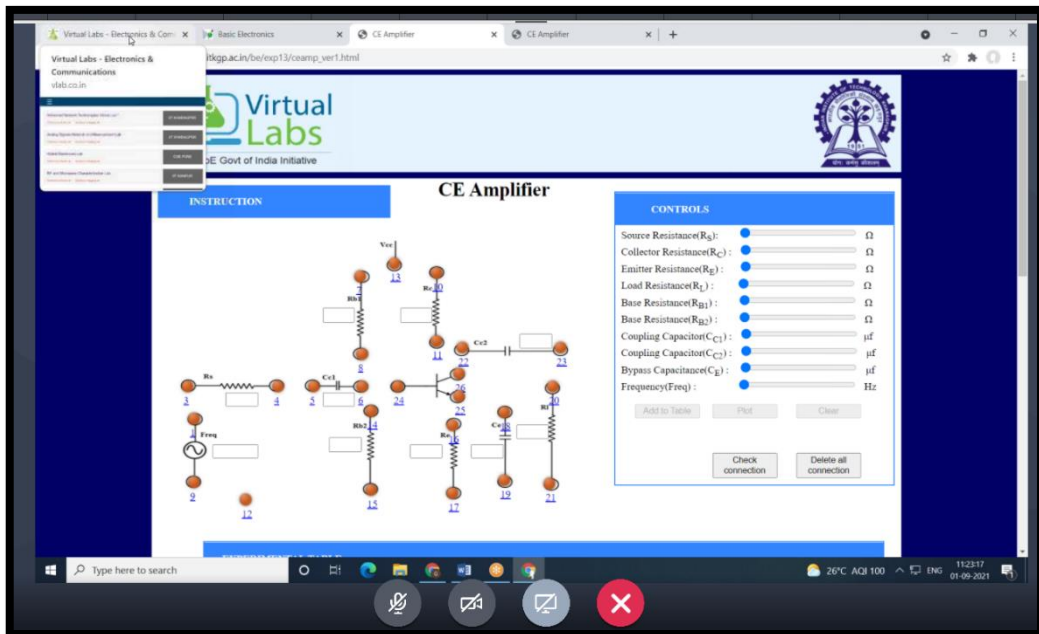
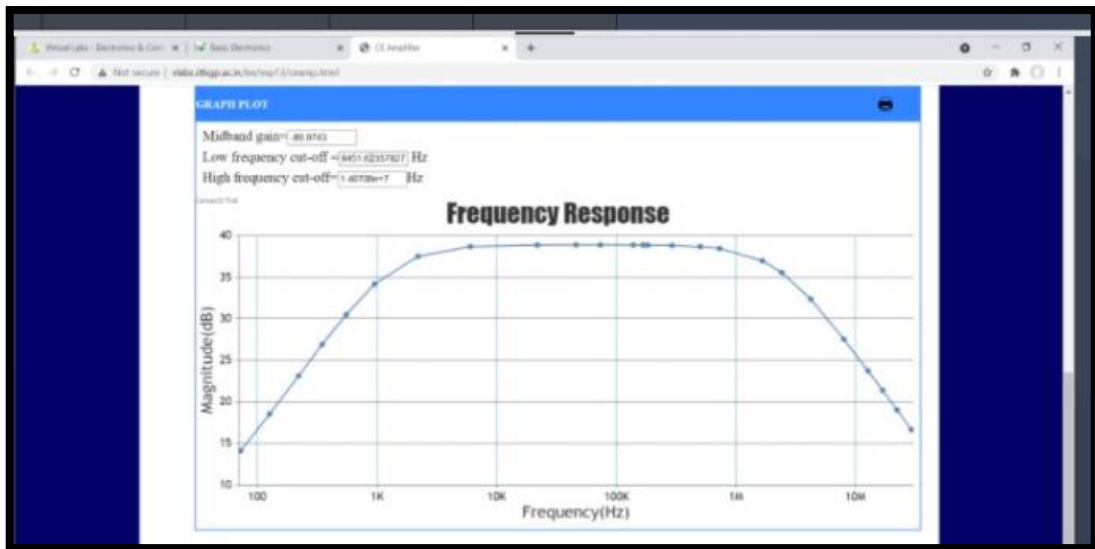
**INSTRUCTION**

**CONTROLS**

- Source Resistance( $R_S$ ):
- Collector Resistance( $R_C$ ):
- Emitter Resistance( $R_E$ ):
- Load Resistance( $R_L$ ):
- Base Resistance( $R_B$ ):
- Base Resistance( $R_{B2}$ ):
- Coupling Capacitor( $C_{C1}$ ):
- Coupling Capacitor( $C_{C2}$ ):
- Bypass Capacitor( $C_B$ ):
- Frequency(Freq):

**EXPERIMENTAL TABLE**

Serid |



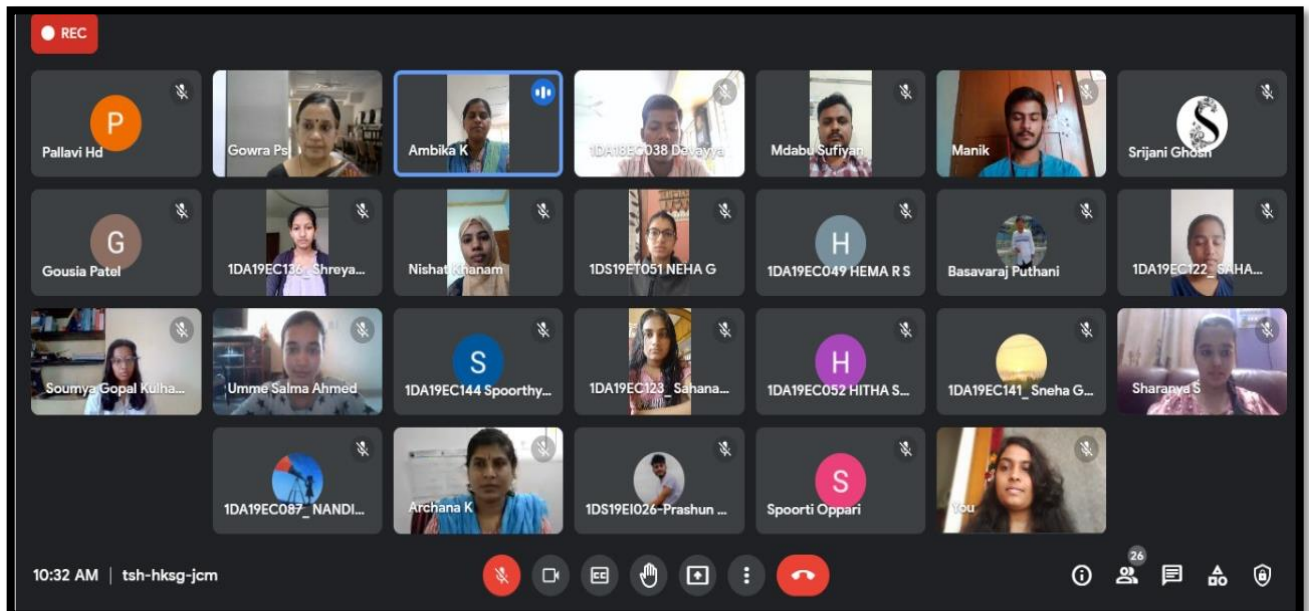
### OUTCOME:

Students were able to implement the above mentioned content. And they have learnt to rig up the circuit in both multisim and virtual labs.

Students also gained knowledge on DC and AC analysis, frequency responses as well as transfer characteristics of given circuit or IC.

## DAY-8,9,10: 02/09/2021-4/09/2021

As mentioned earlier in the schedule three days from 2<sup>nd</sup> September to 4<sup>th</sup> September students presented their project under the supervision of P.S.Gowra mam. Students at the end of the internship were able to design and implement mini-project using multisim and presented, executed and explained them in the meet.



## PROJECT TOPICS AND SCHEDULE

**BMS COLLEGE OF ENGINEERING  
ELECTRONICS AND TELECOMMUNICATION**

**Project Groups & Project Title**

**Schedule for Project presentation**

<b>DATE</b>	<b>Project Groups</b>	
<b>02/09/2021</b>	Srijani Ghosh	Function Generator
	Dinesh U	DC Regulated power supply
	Hema R S Hitha Shree Y S	Sine wave to Square wave converter
	Shashidhar S Suparna B K	Band pass filter
	Sahana K S Sneha G R Spoorthi H G	Hartley oscillator
	Nanditha A Sahana A N Shreya C	Automatic Door Bell
	Anusha T A Siri Ranganath	Password security Instrumentation amplifier
	Neha G Prashun Kumar Dash	Mobile phone charger
	Rashmi T	Low pass filter
	Adrian P Issac	Simple D to A converter using op-amp

<b>DATE</b>	<b>Project Groups</b>	
<b>03/09/2021</b>	<b>Nishat Khanam Maheshwari</b>	Traffic light controller with timers and counters
	<b>Spoorti Oppari Basavaraj Puthani</b>	Automatic Washroom light project
	<b>Avyukt Sharma Shirisha</b>	3 Phase sine wave generator
	<b>Divya Abdurrahim</b>	Op-Amp Transistor PWM
	<b>Umme Salma Ahmed</b>	PWM LED Dimmer using NE555 timer.
	<b>Soumya Kulhali Nimisha MR</b>	FM Listening bugger circuit
	<b>Sandeep T Likith P Reddy</b>	Mobile Detector circuit

<b>04/09/2021</b>	<b>Devayya Manik</b>	Mobile Jammer circuit
	<b>Gousia Begum Pallavi Md Abu Sufiyan</b>	Simple battery level indicat using op-amp

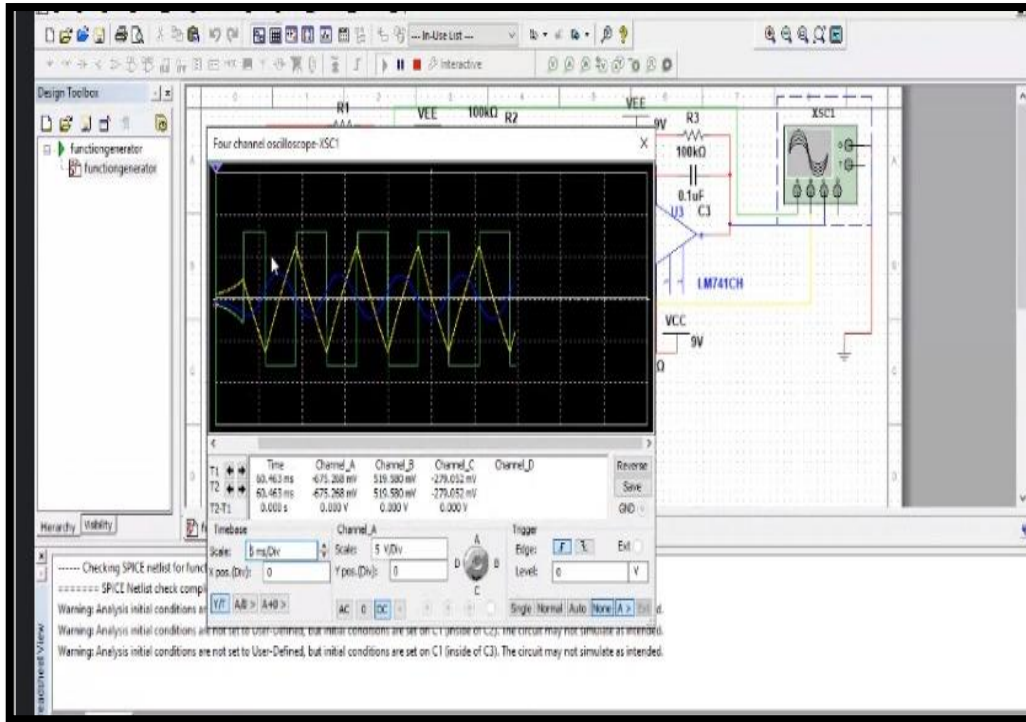
### OUTCOME

The students learnt to use the multisim software and bridge the gap between theory and real world. By working on project students gained knowledge on various real world applications on analog as well as digital electronics. And also they were able to analyze graphs, frequencies and other characteristics of the electronic components.

The session was very interactive as well as informative.

### PHOTO GALLERY OF THE PROJECT PRESENTATION

- Function generator:



- **Password security instrumentation amplifier:**

The image shows a screenshot of a video conference. The main window displays a circuit diagram titled 'PASSWORD SECURITY SYSTEM'. The diagram features a complex logic circuit with multiple logic gates (AND, OR, NOT) and a central component labeled 'PASSWORD SECURITY SYSTEM'. The circuit is connected to a 9V power source. On the right side of the video conference, there is a list of participants: 'Gowra Ps' (with a video thumbnail), '1DS19E1040 Siri/Rangana... ART' (with a video thumbnail), and '19 others' (with a profile icon).

- **DC regulated power supply:**

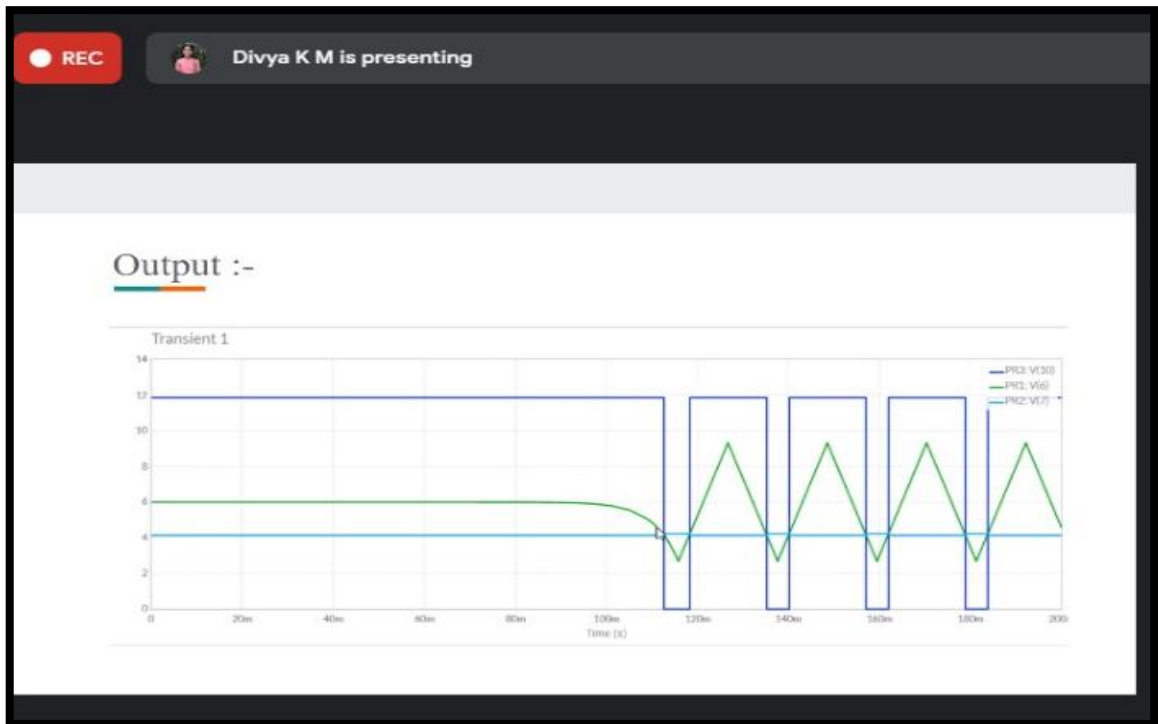


REC dinesh u is presenting

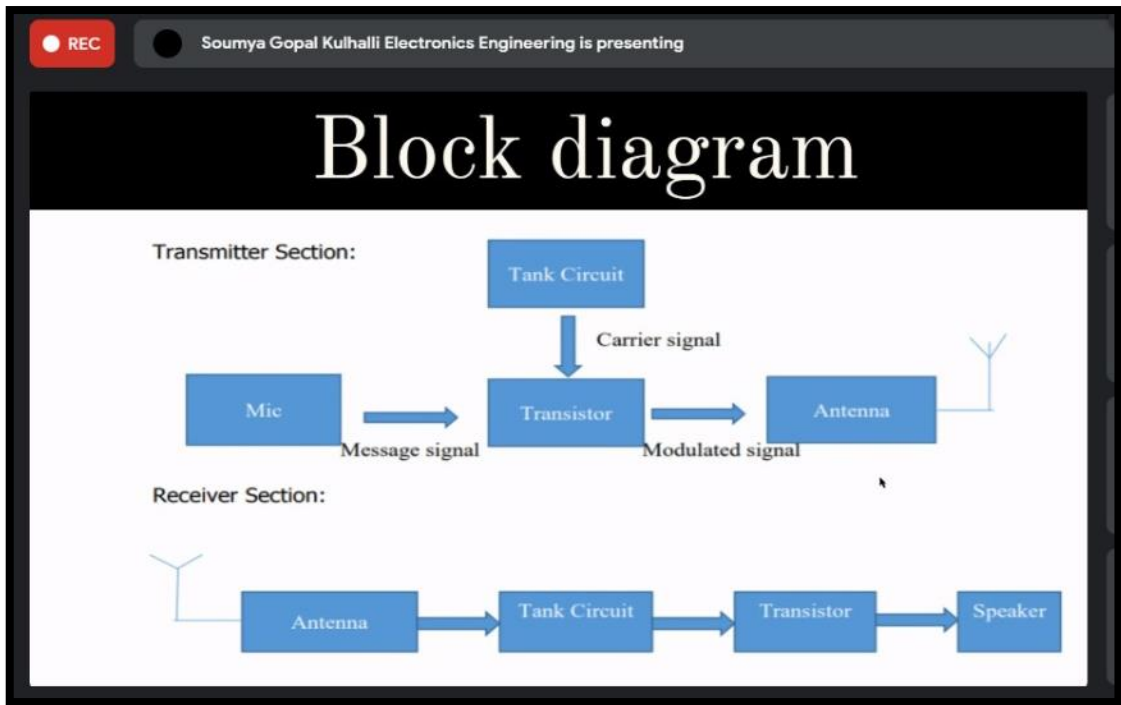
Output window showing:

- Multimeter-VMM1: 25.714 mV
- Multimeter-VMM2: 5.044 V

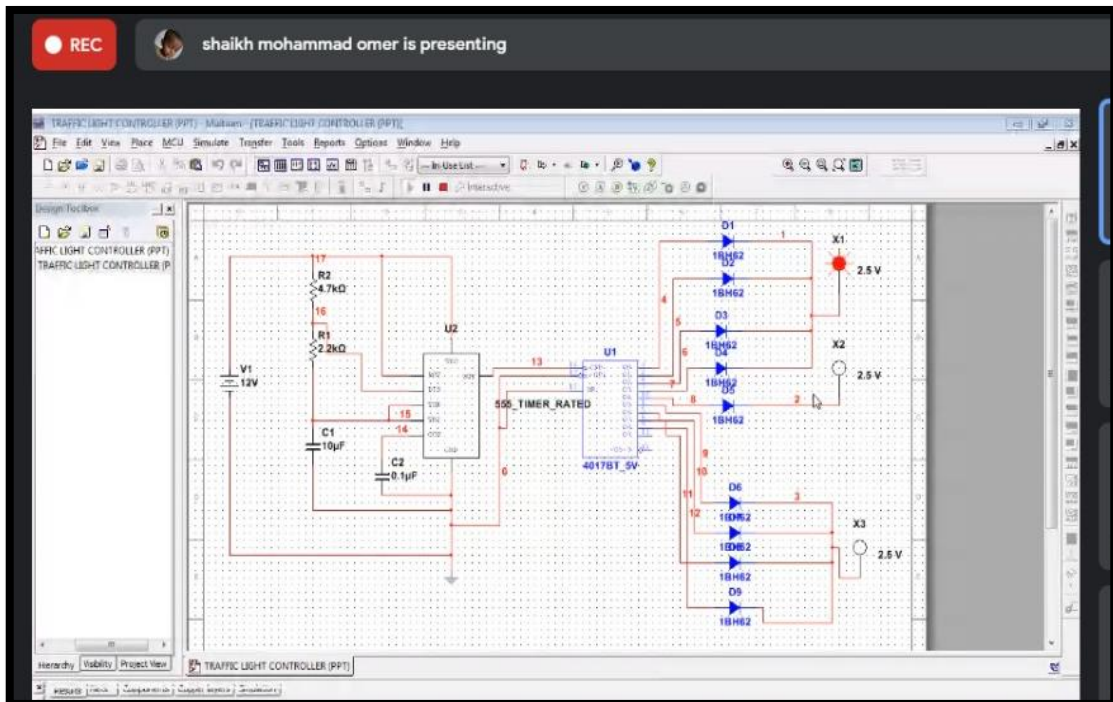
- **Pulse width modulation:**



- **FM listening bugger circuit:**



- **Traffic light controller with timers and counters:**



**ATTENDANCE LIST**

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
SLNO	NAME			23-Aug	24-Aug	25-Aug	26-Aug	27-Aug	30-Aug	31-Aug	01-Sep	02-Sep	03-Sep	04-Sep	Eligib	Percentage	
1	Abdurrahim sheik			AB	P	AB	P	P	P	P	P	P	P	P	YES	82%	
2	Abhijith k			P	P	P	AB	AB	AB	AB	AB	AB	AB	AB	NO	28%	
3	Adrian P Isaac			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
4	Aavyukt Sharma			P	P	P	P	P	P	AB	AB	AB	P	P		73%	
5	B R SPIRANGARAJU			AB	P	P	P	P	AB	AB	AB	P	AB	AB	NO	45%	
6	BASAVARAJ PUTHANI			P	P	P	P	AB	P	P	P	P	P	P	YES	91%	
7	Devassy			P	AB	P	P	AB	P	P	P	P	P	P	YES	82%	
8	Dinesh U			P	AB	AB	AB	P	P	P	P	P	P	P		73%	
9	Divya K M			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
10	Gousis			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
11	Hema R S			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
12	Hitha Shree Y S			P	P	P	P	P	AB	P	P	P	P	P	YES	91%	
13	Likhith P Reddy			P	P	P	P	P	AB	P	P	P	P	P	YES	91%	
14	Mheshwari M Birasore			AB	AB	AB	P	AB	AB	AB	AB	P	P	P	NO	36%	
15	Manik			AB	P	P	P	P	AB	P	P	P	P	P	YES	82%	
16	Manjiri Kulkarni			P	P	P	P	AB	AB	AB	AB	AB	AB	AB	NO	36%	
17	N Suraj Naik			AB	AB	P	P	AB	AB	AB	AB	AB	AB	AB	NO	18%	
18	Nandan.N			P	P	AB	AB	AB	P	P	P	AB	AB	AB	NO	46%	
19	Nanditha A			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
20	NEHA G			P	P	P	P	AB	P	P	P	P	P	P	YES	91%	
21	Nimicha MR			P	P	P	P	P	AB	P	P	P	P	P	YES	91%	
22	Nishat khanom			P	AB	P	P	P	P	P	P	P	P	P	YES	91%	
23	Prashun kumar Dash			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
24	Prashmi T			P	P	P	P	AB	P	P	P	P	P	P	YES	91%	
25	Sahana KS			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
26	Sahana.A.N.			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
27	Sandeep T			P	P	P	P	P	AB	P	P	P	P	P	YES	91%	
28	Shashidhar S			AB	P	P	P	P	P	P	P	P	P	P	YES	91%	
29	Shrisha B N			P	P	P	P	AB	AB	AB	AB	P	P	P		64%	
31	Shreya C			P	P	P	P	P	P	AB	P	P	P	P	YES	91%	
33	Sneha GR			AB	P	P	P	P	AB	P	P	P	P	P	YES	82%	
34	Soumya Kulkali			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
35	Spoorthu.H.G			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
36	Spoorti oppari			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
37	Srijani ghosh			P	P	P	P	P	P	P	P	P	P	P	YES	100%	
38	Suparna bk			P	P	P	P	P	AB	AB	AB	P	P	P		73%	
39	Umme Salma Ahmed			P	AB	P	P	AB	P	P	P	P	P	P	YES	82%	
40	ANUSHA TA			AB	P	P	P	P	P	P	P	P	P	P	YES	91%	
41	Siri Ranganath			AB	P	P	P	P	P	P	AB	P	P	P	YES	82%	
42	MD ABUSUFYAN			AB	AB	P	P	P	P	P	AB	P	P	P		73%	
42	PALLAWIHD			-	P	P	P	P	AB	P	AB	P	P	P	YES	80%	

**PERMISSION LETTER**

8/16/2021

Two week online Internship program - to\_office@bmsce.ac.in - BMS College of Engineering Mail

Hod Tce

To Principal, Viceprincipal, Faculties TCE, me

2:43 PM (4 m)

Dear Principal and Viceprincipal Sir

Pleased to inform that Three of our faculty:

P S Gowra

Ambika

Archana

would like to offer a Two Week online Internship program for students from 2nd and 3rd year students from any college, including our college. The event brochure is attached.

We plan to charge a nominal amount of Rs 300/- towards the Internship

We would like to share 30 % of the amount collected with college, and use the 70% towards department IRG (to be used for funding procurement of academic accessories for online teaching or any other expenditure)

The faculty would not like to claim any honorarium for this activity.

Thanking you

with regards

B Kanmani

B Kanmani  
16/8/21

Approved  
Officer  
16/8/21

## STUDENT DETAILS

A	B	C	D	E	F
				<b>List Of Students attending Multisim Internship</b>	
	<b>Sl.No</b>	<b>Name</b>		<b>College Name</b>	
	1	Abdurrahim sheik		St.Joseph College of Engineering	
	2	Abhijith k		BMS College of Engineering	
	3	Adrian P Isaac		University Visvesvaraya College of Engineering	
	4	Avyukt Sharma		BMS College of Engineering	
	5	BR SRIRANGARAJU		Atria Institute of Technology	
	6	BASAVARAJ PUTHANI		University Visvesvaraya College of Engineering	
	7	Devayya		Dr.Ambedkar Institute of Technology	
	8	Dinesh u		Govt. Sri Krishnarajendra Silver Jubilee Technology Institute	
	9	Divya K M		BMS College of Engineering	
	10	Gousia		PDA college of Engineering kalaburgi	
	11	Hema R S		Dr.Ambedkar Institute of Technology	
	12	Hitha Shree Y S		Dr.Ambedkar Institute of Technology	
	13	Likhith P Reddy		BMS College of Engineering	
	14	Maheshwari M Birapure		PDA college of Engineering kalaburgi	
	15	Manik		University Visvesvaraya College of Engineering	
	16	Manjiri Kulkarni		Dayananda Sagar College Of Engineering	
	17	N Suraj Naik		Dayananda Sagar College Of Engineering	
	18	Nandan.N		Dayananda Sagar Academy of Technology and Management	
	19	Nanditha A		Dr. Ambedkar Institute of Technology	
	20	NEHA G		Dayananda Sagar College Of Engineering	
	21	Nimisha MR		BMS College of Engineering	
	22	Nishat khanam		Poojya Doddappa Appa College of Engineering Kalaburagi	
	23	Prashun kumar Dash		Dayananda Sagar College Of Engineering	
	24	Rashmi T		CMR Institute of Technology	
	25	Sahana KS		Dr Ambedkar Institute of Technology	
	26	Sahana.A.N.		Dr. Ambedkar Institute of Technology	
	27	Sandeep T		BMS College of Engineering	
	28	Shashidhar S		Dr. Ambedkar Institute of Technology	
	29	Shirisha B N		BMS College of Engineering	
	30	Shreya. C		Dr. Ambedkar Institute of Technology	
	31	Sneha G R		Dr. Ambedkar Institute of Technology	
	32	Soumya Gopal Kulkali		BMS College of Engineering	
	33	Spoorthy.H.G		Dr. Ambedkar Institute of Technology	
	34	SPOORTI.OPPARI		SDM College of Engineering and Technology	
	35	Srijani ghosh		BMS College of Engineering	
	36	Suparna bk		Dr. Ambedkar Institute of Technology	
	37	Umme Salma Ahmed		Dayananda Sagar College Of Engineering	
	38	ANUSHA TA		Dayananda Sagar College Of Engineering	
	39	Siri Ranganath		Dayananda Sagar college of Engineering	
	40	MD ABU SUFIYAN		PDA Engineering College,kalaburagi	
	41	PALLAVI HD		PDA College of Engineering kalaburgi	

## ACCOUNT DETAILS

<b>College Name</b>	<b>Amount Received</b>
BMS College of Engineering	Rs 200/-
<b>Total Students : 9</b>	<b>Rs 1800/-</b>

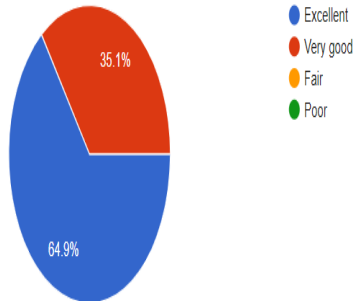
<b>College Name</b>	<b>Amount Received</b>
Other Colleges	Rs 300/-
<b>Total Students : 32</b>	<b>Rs 9600/-</b>

<b>Total Amount Received:</b> Rs 11,400/-
<b>Revenue for College:</b> Rs 3420/-
<b>Revenue for Department:</b> Rs 7980

**FEEDBACK RESPONSES**

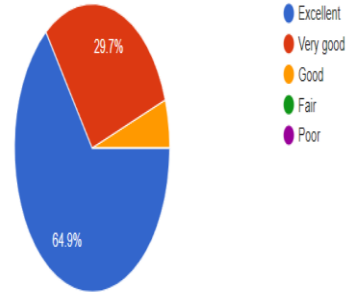
Speaker 1: Archana K- 1) knowledge about the topic

37 responses



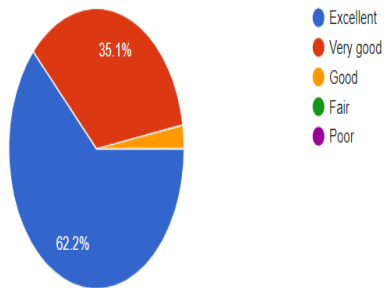
Speaker 1: Archana K- 2)Confidence level of teaching

37 responses



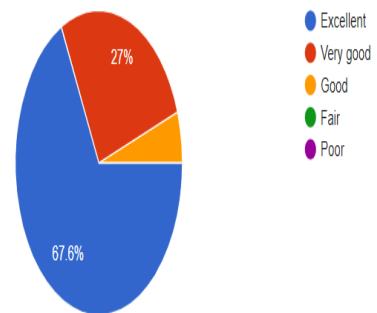
Speaker 1: Archana K- 3)Ability to make you understand the concepts?

37 responses



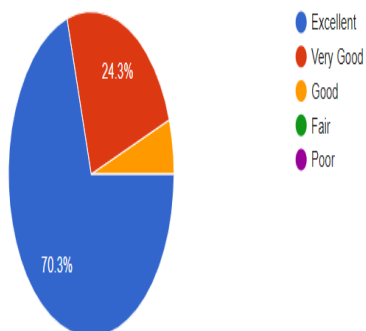
Speaker 2: Ambika K- 1)knowledge about the topic

37 responses



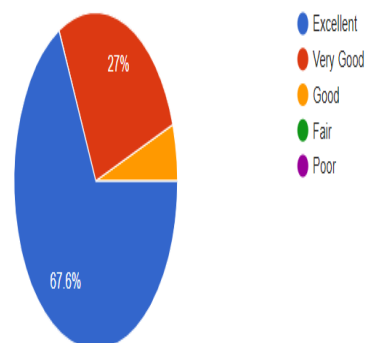
Speaker 2: Ambika K- 2)Confidence level of teaching

37 responses



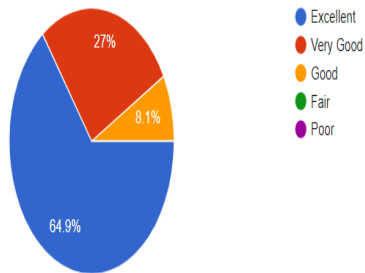
Speaker 2: Ambika K- 3)Ability to make you understand the concepts?

37 responses



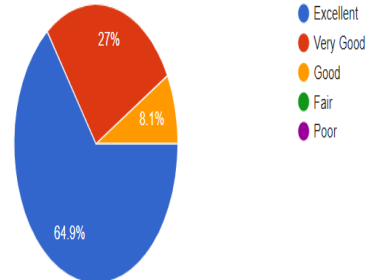
Speaker 3: P S Gowra- 1) knowledge about the topic

37 responses



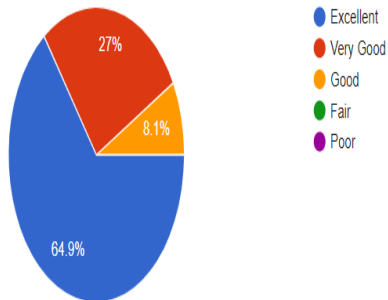
Speaker 3: P S Gowra- 2)Confidence level of teaching

37 responses



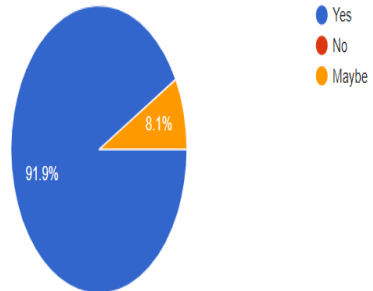
Speaker 3: P S Gowra-3)Ability to make you understand the concepts?

37 responses



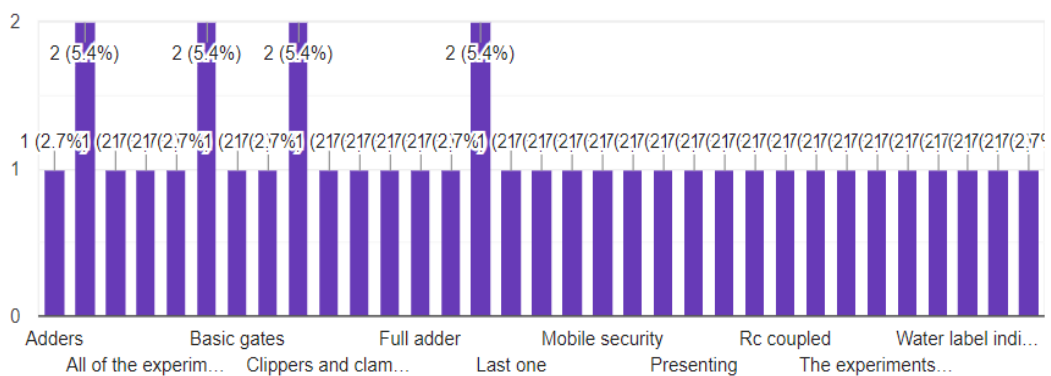
Would you like to recommend this type of internship to your friends?

37 responses



Which experiment you like the most?

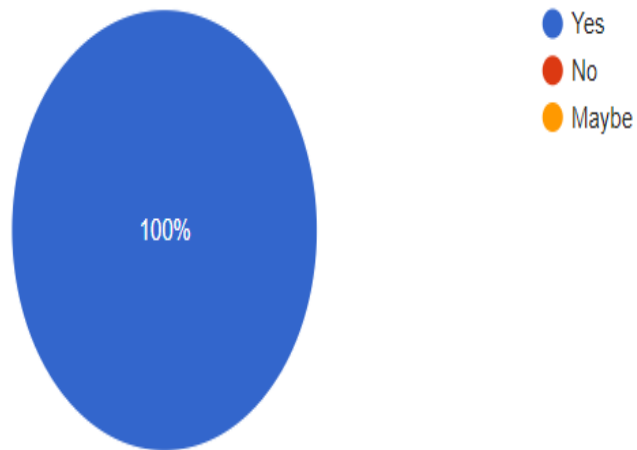
37 responses





### Was the project presentation helpful in your learning

37 responses



### Overall feedback about program

37 responses

