Linear Integrated Circuits Laboratory Manual

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2021

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Get the facts, **or** the facts will get you.

And when you get them, get them right.

Or they will get you wrong.

- Thomas Fuller

EXPERIMENT NO. 1 Date:-

BASIC OP-AMP APPLICATIONS

Aim: To design and study the basic applications of Op-amp as amplifiers and Summing Amplifiers.

Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1	Op-amp	μA 741	2
2.	Resistors	1K, 10K	2 each
3.	Base board (IC and Spring)		1 each
4.	Adopters		2
5.	DMM and Probes		1+2 set
6.	Connecting wires		
7.	Power supply	0-5 V & + /-15V	1

Procedure :-

I. Amplifiers:

1. Connections are made as shown in the circuit diagram of figure (1).

2. Input voltage V_i is increased in steps of 0.1 V and at each step the output voltage V_o is noted down.

3. Readings are tabulated and a graph of V_o Vs V_i is plotted.

4. The input DC supply is replaced with an ASG and a sinusoidal input of adequate amplitude (to cause output saturation) @ a frequency of 1 KHz is applied. The input and output are simultaneously fed to a CRO and the transfer curve is observed and traced.

5. The above procedure is repeated for circuit of figure (2).

II. Adders/Subtractors :- [In Inverting and Non-inverting modes]

1. Connections are made as shown in the circuit diagram of figure (3).

2. Different input voltages (V_1 and V_2) are applied and the output voltage is measured using a multimeter.

3. The readings are tabulated and the measured values are compared with the theoretical values.

4. The above procedure is repeated for circuits of figures (4), (5).

III. Buffer/ Voltage Follower:-

1. Connections are made as shown in the circuit diagram of figure (6).
2. The input voltage is varied in steps and the output voltage is noted to be approximately equal to input.

Circuit diagrams and designs:-

1) Inverting Amplifier :-

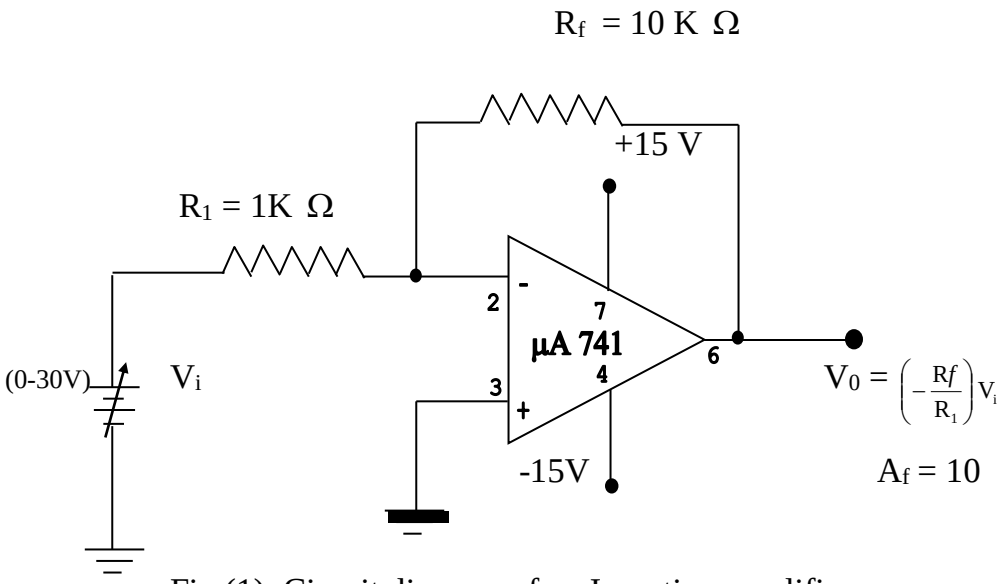

Fig (1) :Circuit diagram of an Inverting amplifier:

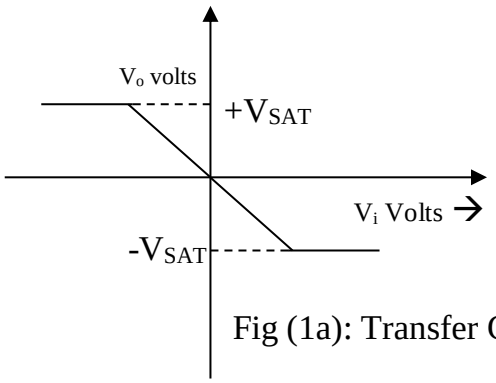

Fig (1a): Transfer Characteristics of Inv.Amp

Design Example:

Let $|A_v| = 10$. Choose $R_1 = 1\ k\Omega$

$$|A_v| = \frac{R_f}{R_1}$$ Therefore $R_f = 10\ k\Omega$

Tabular Column:-

Sl. No.	V_i Volts	V_o (Theoretical) Volts	V_o (Practical) Volts

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2) Non- Inverting Amplifier:-

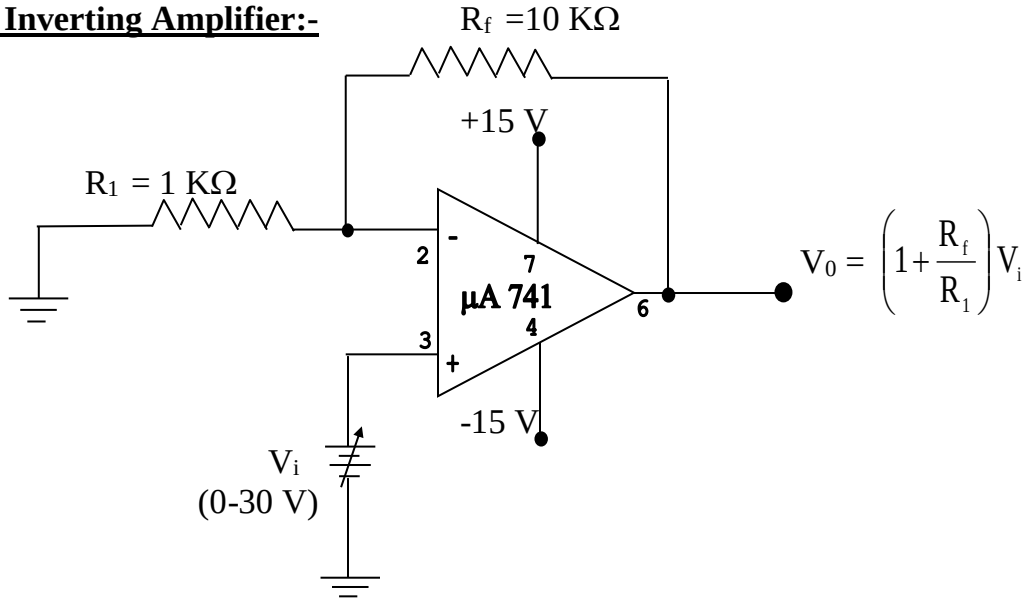

Fig (2): Circuit Diagram of a Non –inverting amplifier

Design Example :

Let $|A_v| = \frac{R_f}{R_1} = 11$. Let $R_1 = 1\ K\Omega$.== > $R_f = 10\ k\Omega$

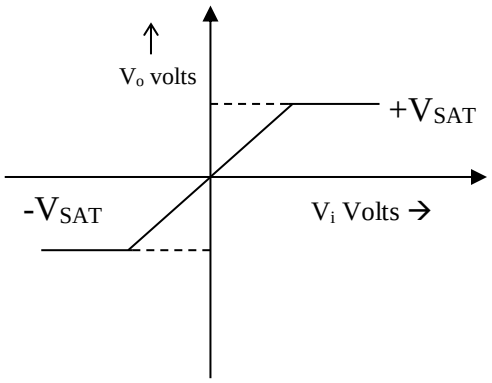

Fig (2a) :Transfer Characteristics of Non-inv Amp

Tabular Column :-

Sl. No.	V_i Volts	V_o (Theoretical)	V_o (Practical)
	0.0 0.1 0.2 -0.3 -0.65 3.0 -3.0		

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3) Inverting adder :-

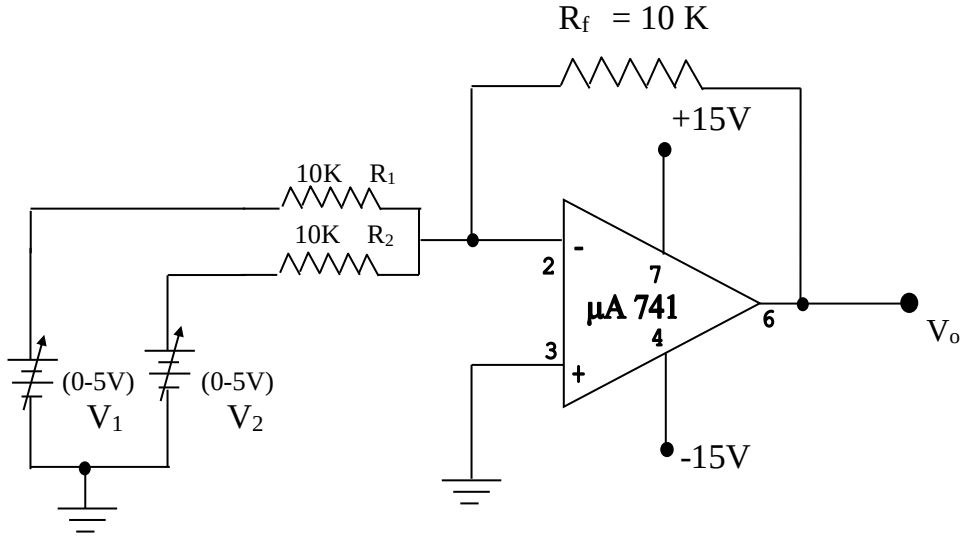

Fig (3): Circuit diagram of an Inverting adder

Design Example: $V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2\right]$

If $R_f = R_1 = R_2 = 10$ K . Then $V_0 = -[V_1 + V_2]$

Tabular Column :-

Sl. No.	V_1 (volts)	V_2 (Volts)	V_o (volts)

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5) Differential Amplifier as Subtractor ;-

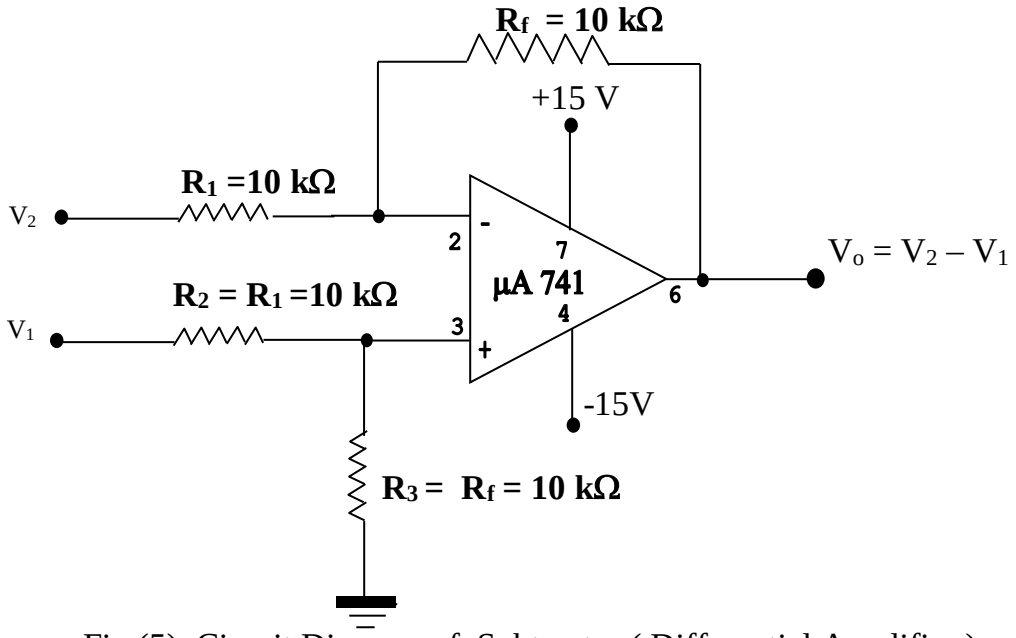


Fig (5): Circuit Diagram of Subtractor (Differential Amplifier)

Design Example:-

$$\mathbf{V_o} = -\frac{R_f}{R_1}(V_2 - V_1)$$

$R_1 = R_2 = R_f = 10\ \text{k}\Omega \Rightarrow V_o = [V_1 - V_2]$

Tabular Column :-

Sl. No.	V_1 Volts	V_2 Volts	Vo(practical) Volts	V_o (theoritical) Volts

---

6) Buffer/Voltage Follower ;-

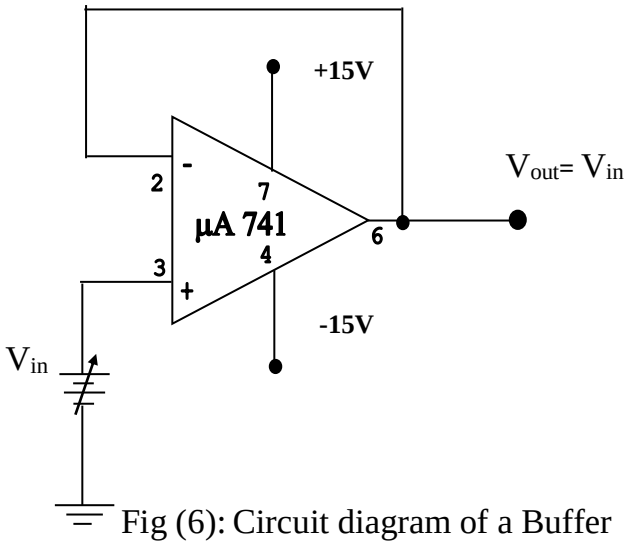


Fig (6): Circuit diagram of a Buffer

TABULAR COLUMN:-

Sl. No.	V_{in} Volts	V_{out} Volts

Experiment No. 2 Date:

VOLTAGE TO CURRENT CONVERTER

AIM : To design and test I to V and V to I converters for the given specifications.

APPARATUS REQUIRED:

Sl. No.	Particulars	Range	Quantity
1	IC μA 741		1
2	Milli ammeters	0-100 mA	1
		0-50 mA	1
		0-10 mA	1
3	Power supply	0-30 volts	1
4.	Power supply	+15 / –15 V	1
5.	Resistors	470 Ω	2
		1 k Ω	2
6	IC base board		1
	Base board		1
7	Multimeter and probes		1 set
8	Connecting wires		

PROCEDURE :-

I. Voltage to Current converter:-

1. The connections are made as shown in the circuit of figure (1).

2. The load resistor R_L a constant value (say R_L = 200 Ω)

3. The input voltage V_i is varied in steps and corresponding values of I_f are noted. The theoretical values of I_f are computed and compared.

4. All the readings are tabulated in table (1).

5. The i/p voltage V_i is kept at a constant value (at 2 Volts) and the load resistance is varied from around 50 ohms to 10 kohms and at each step the corresponding values of $\mathbf{I_L}$ & $\mathbf{V_L}$ are noted down and recorded in table (2).

6. The above procedure is repeated for circuit of figure (2). The readings are tabulated in tables (3) and (4).

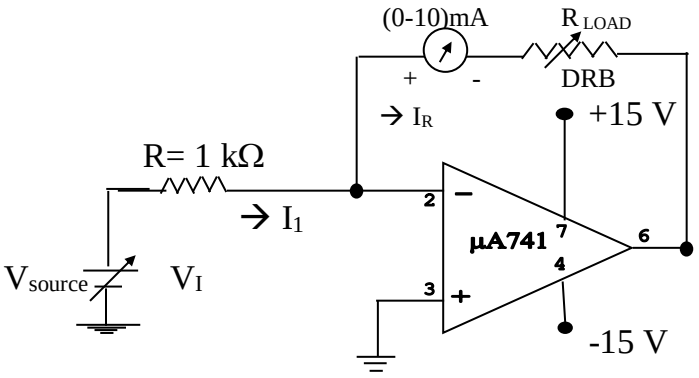


Fig (1): V TO I CONVERTERS FOR FLOATING LOAD

Design Example: $I_1 = I_R = \frac{V_i}{R}$ because of virtual ground .

Therefore $I_L = \frac{1}{R} V_I$

Here I_L is independent of R_{LOAD} within specified limits.
Choose R = 1 k Ω

Therefore $I_L = (10^{-3} V_I)$ Amperes. Where V_I is in volts.

Tabular Column (1):-

For R_L = 200 Ω constant

V_i Volts	I_L (Practical)	I_L (Theoretical)

Tabular Column (2):-

V_i = 2 V constant

R_L	I_L

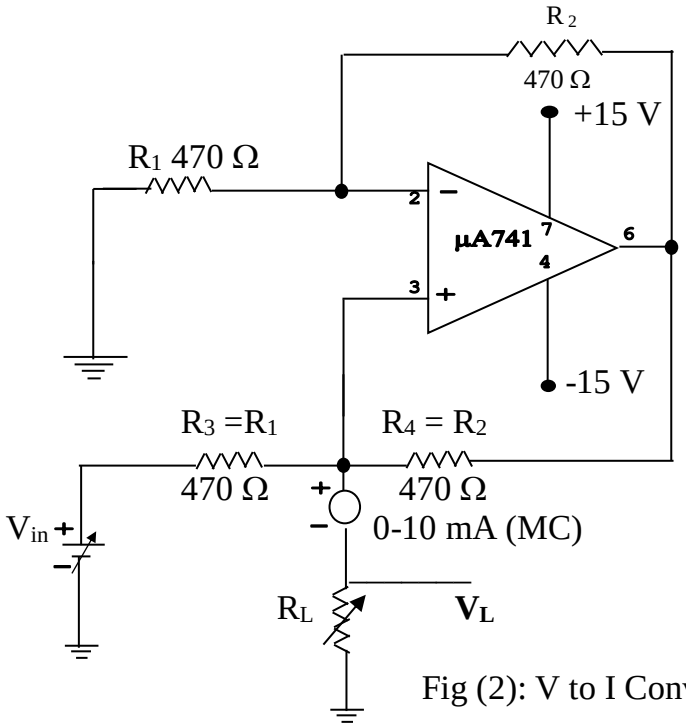


Fig (2): V to I Converter for grounded Load

[Also called Howland Current Generator]

Design Example :-

$I_o = \frac{1}{R_3} V_i$

Let $R_3 = 470\ \Omega$

Then $I_o = 0.0021$ x V_i volts

$I_o =$ _____Amps

Tabular Column(3):-

$R_L = 500\ \Omega$ constant

V_i in volts	I_L (Theoretical)	I_L (Practical)

Tabular Column(4):-

V_i = 5 volts (constant)

R_L	I_L	V_L

Experiment No. 3 Date :

INSTRUMENTATION AMPLIFIER

AIM : To design and test an instrumentation amplifier for the given gain and to determine CMRR.

APPARATUS REQUIRED :

Sl. No.	Particulars	Range	Quantity
1.	IC μA 741		3
2.	Resistors	10 k Ω	7
3.	Power supply	+15 / –15 V	1
		0-30 volts	2
4.	Multimeter and probes		1 set
5.	Connecting wires		1 set
6.	IC base board		1
7.	Base board		1

PROCEDURE :

1. Circuit connections are made as shown in figure (1) for the differential mode .
2. Inputs V_1 and V_2 are varied in steps and V_o is measured using a Multimeter and tabulated.
3. The Differential gain is calculated and verified with the designed gain.
4. For the common mode, connections are made as per circuit diagram (2), and V_{in} is varied in steps (2 V, 3V etc.,) .V_o is measured using a multimeter and recorded at each step.
4. The Common mode gain is calculated and recorded.
5. The CMRR in calculated and recorded.

CIRCUIT DIAGRAMS AND DESIGN:-

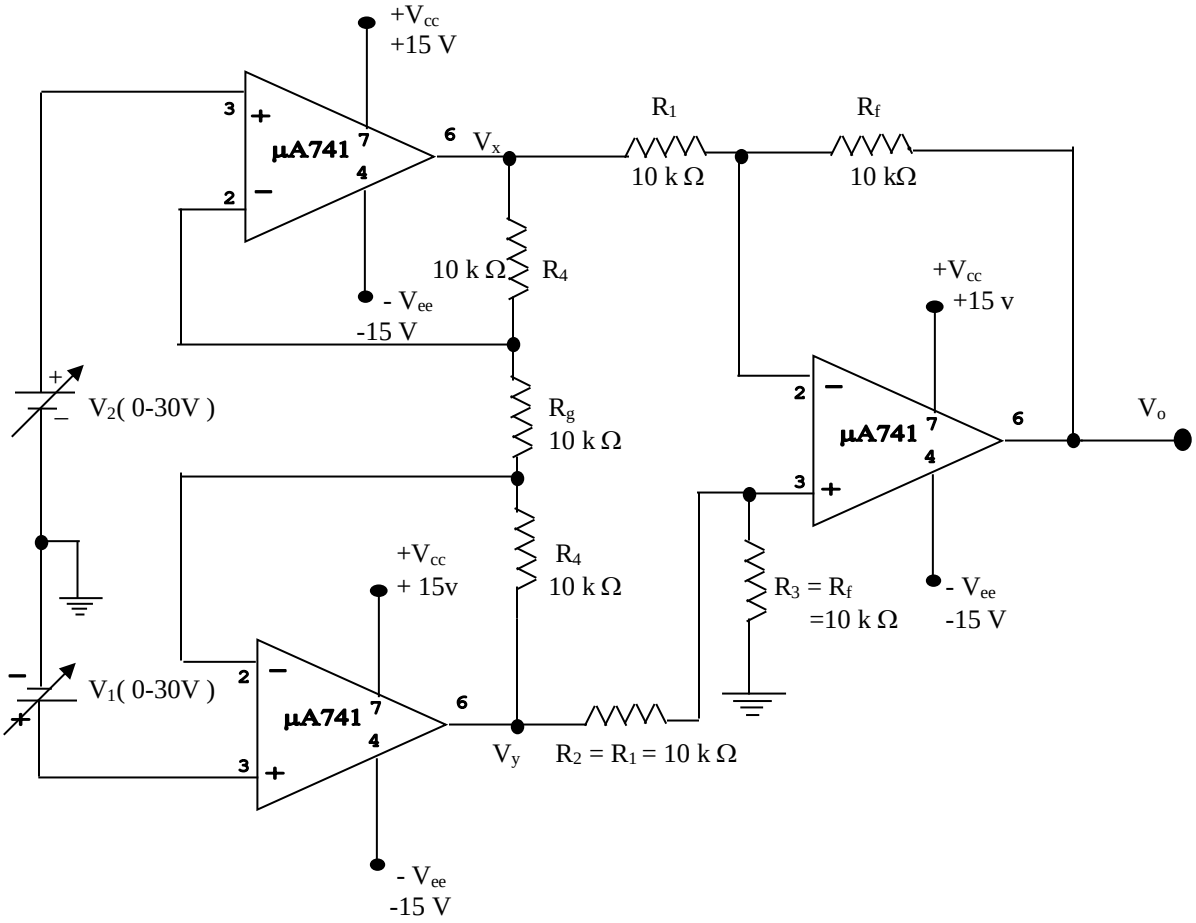


Fig (1) : INSTRUMENTATION AMPLIFIER IN DIFFERENTIAL MODE

Design Example:-

$$V_o = -\frac{R_f}{R_1}\left[1+\frac{2R_4}{R_g}\right](V_1 - V_2)$$

$$A_{vf} = \frac{V_o}{V_1 - V_2} = -\frac{R_f}{R_1}\left(1+\frac{2R_4}{R_g}\right)$$

For $R_f = R_1 = R_4 = R_g = 10\ K\Omega$

$V_o = -3\ (V_1 - V_2)$ i.e. $V_o = -3\ V_d$

Tabular Column (1):-

V_1 in volts	V_2 in volts	V_o (Theoretical) in volts	V_o (measured) in volts	$A_d = \frac{V_o}{V_1 - V_2}$ diff. gain
0.0	0.5			
1.5	0.8			
2.0	2.6			
2.2	2.55			
5.4	4.4			
6.4	7.4			
4.6	6.8			

Average A_d =

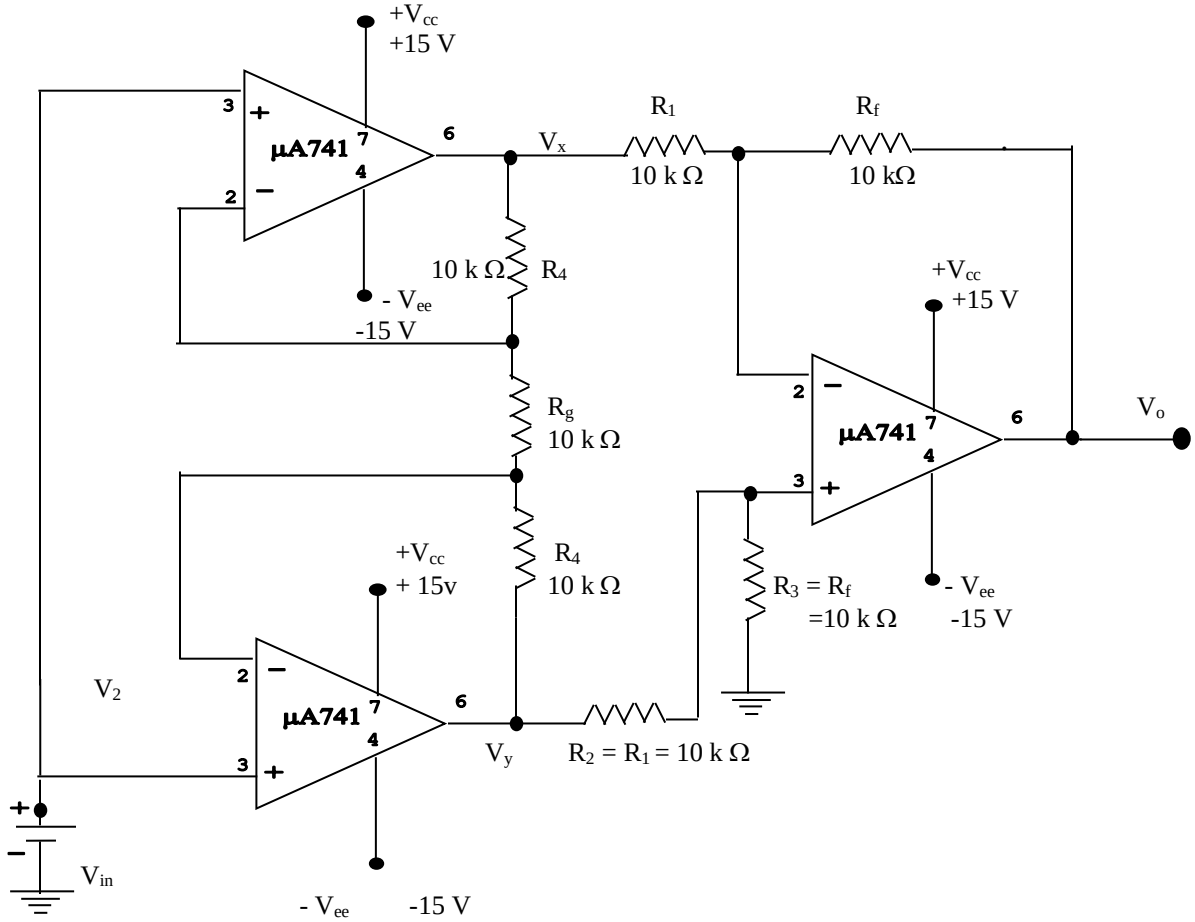


Fig (2):- INSTRUMENTATION AMPLIFIER IN COMMON MODE

Tabular Column

V*in* in volts	V_o in volts	$A_c = \frac{V_o}{Vin}$ Common mode gain
2.0 3.0 5.6 12.0		

Average A_c =

$$CMRR = 20 \log \frac{A_d}{A_c} \text{ ----------(in dBs)}$$

Results:-

Exercise : *Design and test an Instrumentation Amplifier for different gains like 30 and 100. Calculate the CMRR and comment on the results.*

Experiment No. 4 Date:

WEIN BRIDGE AND RC PHASE-SHIFT OSCILLATORS.

AIM : To design and test Op-amp based Weinbridge and RC -Phase Shift Oscillators.

APPARATUS REQUIRED :

Sl. No.	Particulars	Range	Quantity
1.	OP-Amp	LM 741 or OP 07	1
2	Resistors		2
3.	Capacitors		2
4.	Dual Power Supply	+ / –15 volts	1
5.	IC Base board		1
6.	Multimeter and probes		1 set
7.	Connecting wires		

PROCEDURE :-

1. The Wein bridge oscillator is designed for a given value of frequency (say 1 kHz) and the connections are made as shown in figure (1).
2. The dual power supply is verified to be +/- 15 V and then switched ON.
3. The feed-back resistor R_f is adjusted to get sustained oscillations.
4. The output waveform is observed on the CRO. The frequency and amplitude of oscillations are measured and recorded.
5. The measured frequency is compared with the designed frequency.
6. Steps 1-5 are repeated for different frequencies.
7. The above procedure is repeated for the RC Phase-shift oscillator circuit shown in figure (2).

Circuit diagrams and designs:-

I. WEINBRIDGE OSCILLATOR :-

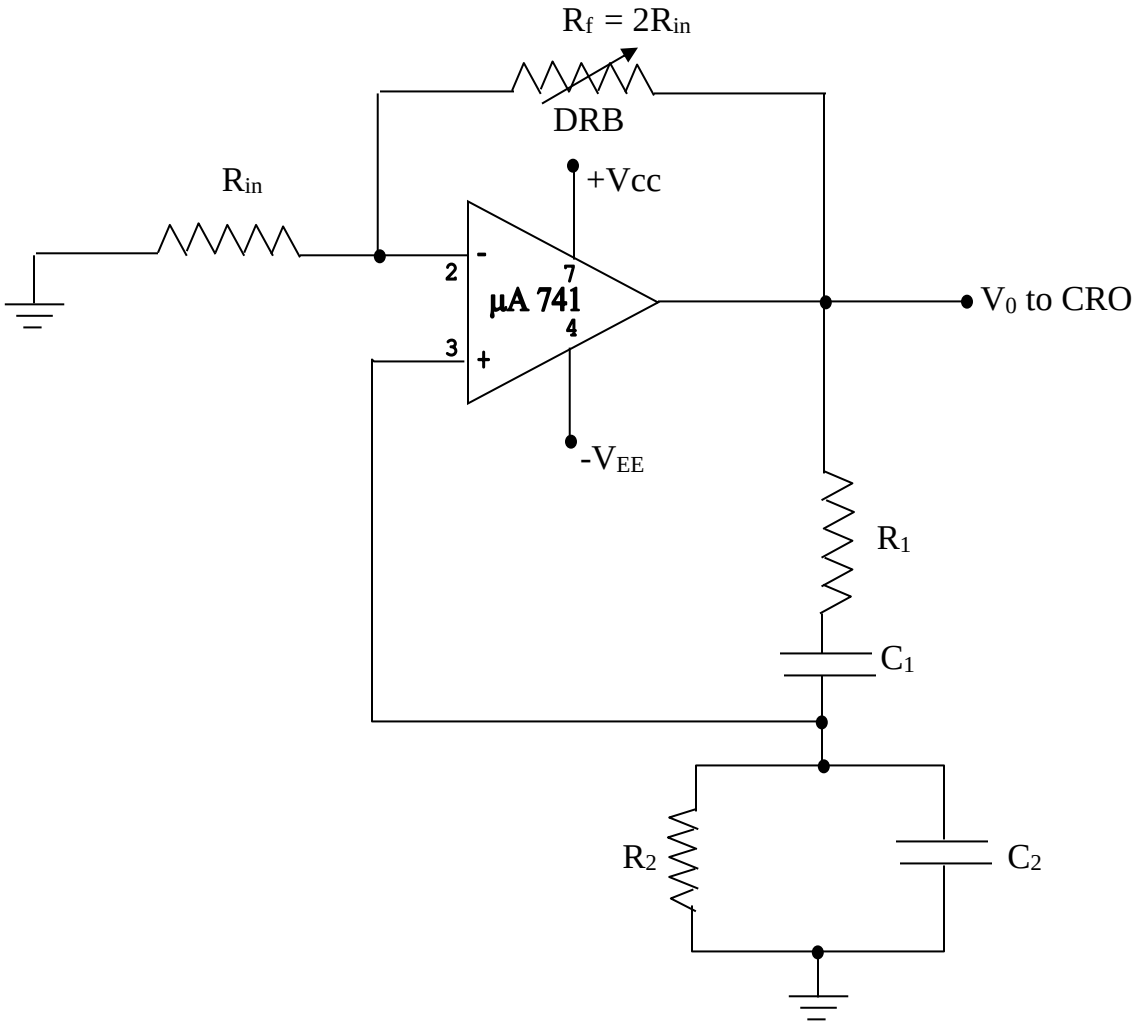


Fig (1): CIRCUIT DIAGRAM OF WEINBRIDGE OSCILLATOR

DESIGN EXAMPLE : The expression for frequency is :

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$ Assuming $R_1 = R_2$ & $C_1 = C_2$, we have $f = \frac{1}{2\pi RC}$

Let f = 1 kHz.

Assume C = 0.1 μF

$$f = \frac{1}{2\pi RC} \quad \text{or} \quad R = \frac{1}{2\pi fc}$$

$$\therefore \; R = \frac{1}{2\pi \text{ x } 1K \text{ x } 0.1\,\mu} = 1.591\,k\Omega$$

R_{cal} =1.59 k Ω, Use R = 1.6 kΩ

The condition for sustained oscillations is :

$$1 + \frac{R_f}{R_{in}} = 3$$

$$\text{i.e. } \frac{R_f}{Rin} = 2 \quad \text{or} \quad R_f = 2\,R_{in}$$

Use R_{in} = 1 K Ω . R_f = 2 K Ω [Use a DRB and trim R_f to get sustained oscillations]

TABULAR COLUMN :-

Sl. No.	R Ω	C μF	f_{cal} in Hz	T_{meas} Msec	f_{meas} Hz	V_o (p-p) Volts	R_f Ω

II. RC-PHASE SHIFT OSCILLATOR:-

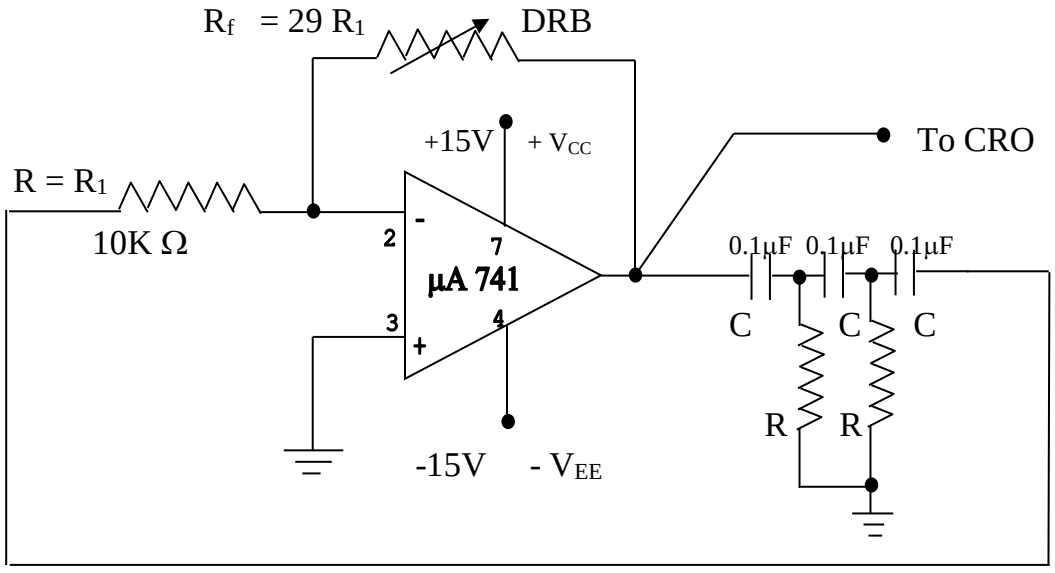


Fig (2): CIRCUIT DIAGRAM OF RC-PHASE SHIFT OSCILLATOR

DESIGN EXAMPLE :- To design for a frequency of f = 1 KHz

The frequency of oscillations is given by $f = \frac{1}{2\pi\sqrt{6}RC}$

Let f = 1 kHz. Assuming C = 0.1 μF

$f = \frac{1}{2\pi\sqrt{6}RC}$ ==> $R = \frac{1}{2\pi\sqrt{6}\, f\, C}$

$R = \frac{1}{2\pi\sqrt{6} \text{ x } 1K \text{ Hz x } 0.1\mu F} = 649.747\ \Omega$ [Use R = 660 Ω]

The Necessary condition to get sustained oscillations is $\frac{R_f}{R_1} = 29$

Therefore $R_f = 29\ R_1$

Assuming R_1 , R_f can be found [$R_1 \geq 10$ R]

Let R_1 = 10 K Ω ==> R_f = 290 K Ω

TABULAR COLUMN:-

Sl. No.	R Ω	C μF	f_{cal} Hz	T_{meas} m sec	f_{meas} Hz	V_o (P-P) volts	R_f Ω
1	660	0.1	984				

Experiment No. 5 **Date:**

ZCD AND VOLTAGE LEVEL DETECTORS.

AIM : To design and test the operation of ZCDs and voltage level detectors.

APPARATUS REQUIRED :

Sl. No.	Particulars	Range	Quantity
1.	IC μA 741		1
2.	Power supply	+15 v to –15 v	1
3.	ASG and probes		1 set
4.	Adapters, CRO		3+1
5.	Multimeter and Probes		1 set
6.	IC base board, base board		
7.	Connecting wires		

PROCEDURE :

1. Circuit connections are made as shown in figure (1)
2. Sinusoidal input signal of is applied from an ASG.
3. V_o is observed on CRO . The Transfer characteristics is observed and the switching points at the Zero Crossing of the input are noted.
4. The circuit of figure (1) is modified to detect the input-crossing at specific positive and negative voltage levels == > Voltage Level detectors of figure (2) & (3) are tested.

Circuit diagrams, Waveforms and Transfer Characteristics :-

(1) ZCD

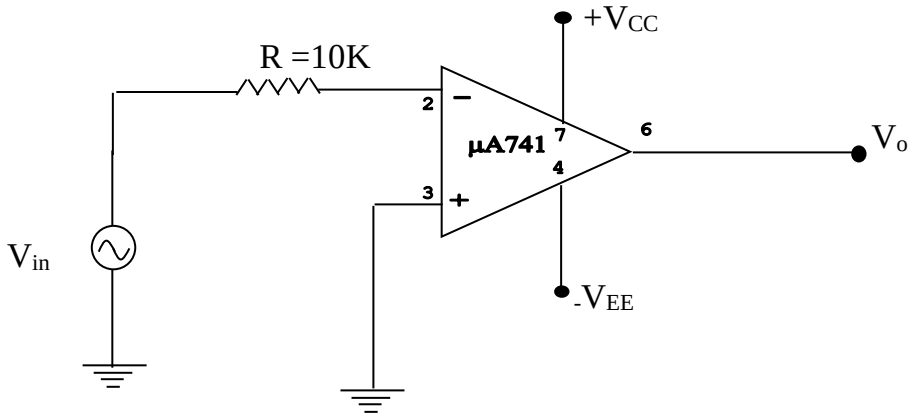


Fig (1): ZCD CIRCUIT

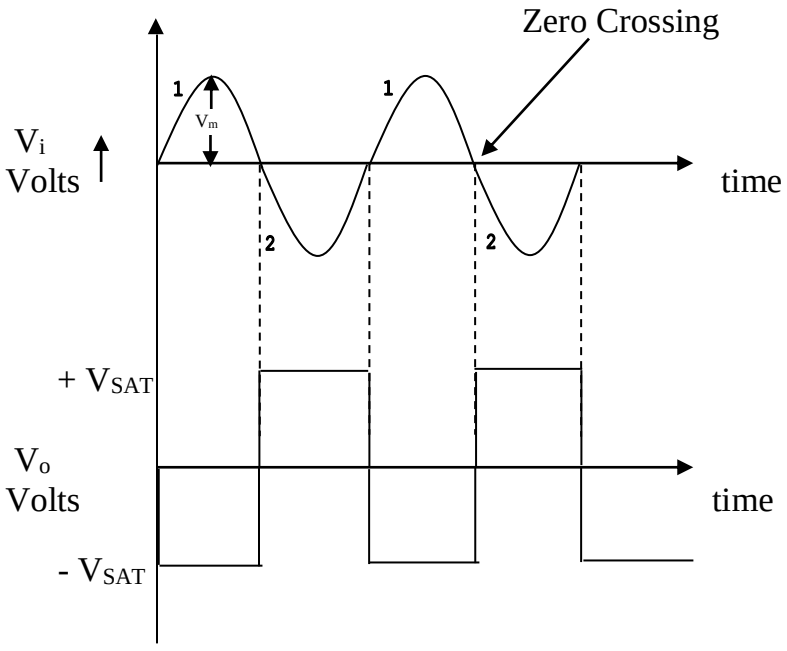


Fig (1a): *INPUT- OUTPUT WAVEFORMS of a ZCD*

(2) Positive Voltage Level Detector

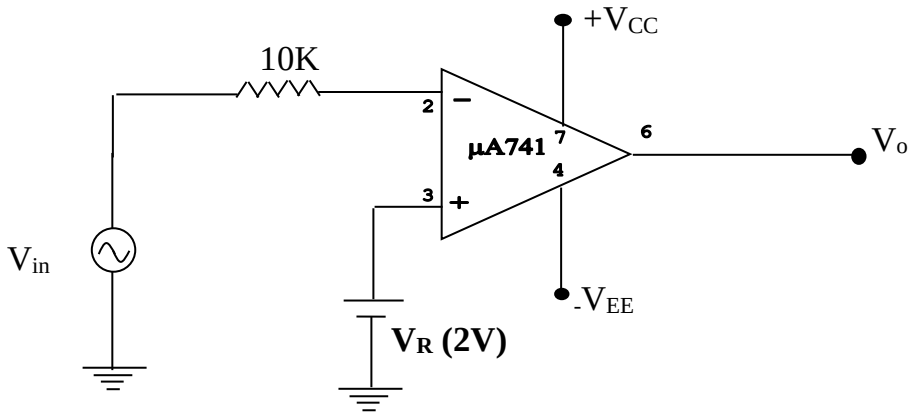


Fig (2): Positive Voltage Level Detector CIRCUIT

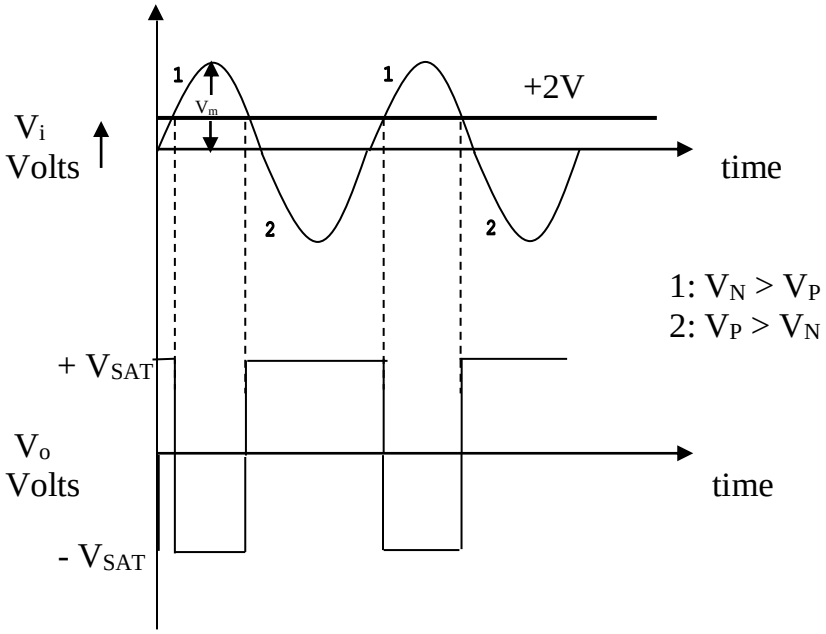


Fig (2a): *INPUT- OUTPUT WAVEFORMS of a* Positive Voltage Level Detector

(3) Negative Voltage Level Detector

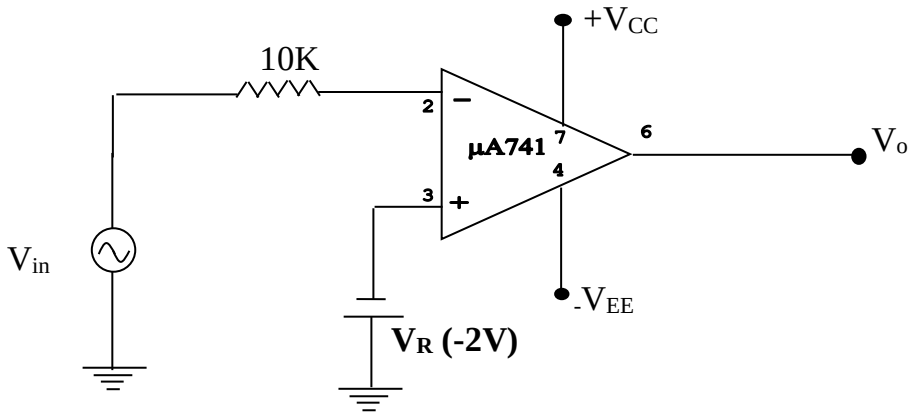


Fig (3): Negative Voltage Level Detector CIRCUIT

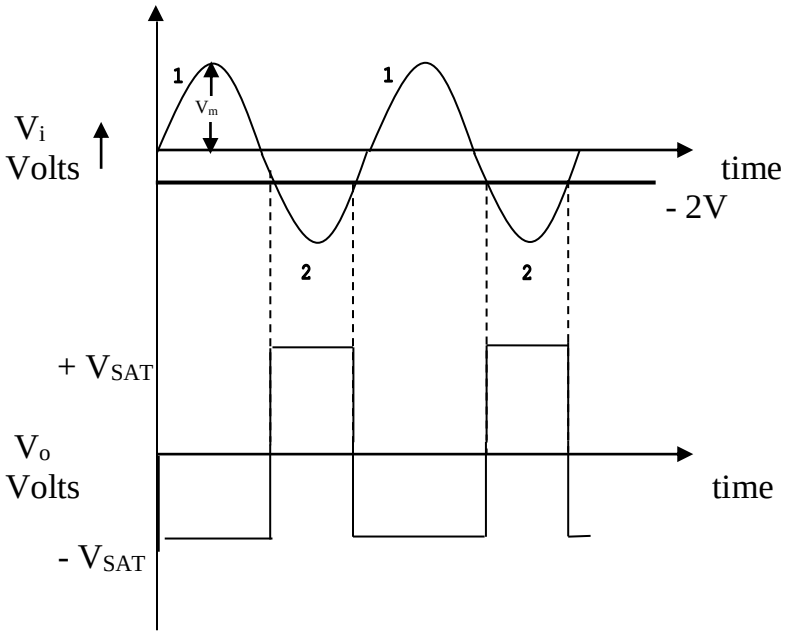


Fig (3a): *INPUT- OUTPUT WAVEFORMS of a* Positive Voltage Level Detector

Experiment No. 6 **Date:-**

SCHMITT TRIGGER CIRCUIT

AIM : To design and test an inverting Schmitt trigger circuit for a given value of Hysterisis or UTP and LTP points.

APPARATUS REQUIRED:

Sl. No.	Particulars	Range	Quantity
1.	IC μA 741		1
2.	Resistors		
3.	Power supply	+15 v to –15 v	1
4.	ASG and probes		1 set
5.	Adapters, CRO		3+1
6.	Multimeter and Probes		1 set
7.	IC base board, base board		
8.	Connecting wires		

PROCEDURE:

1. Circuit connections are made as shown in figure (2)
2. Sinusoidal input signal of adequate amplitude (more than the UTP & LTP values) is applied from an ASG.
3. V_o is observed on CRO . The Transfer characteristics is observed and the switching points [UTP & LTP] are verified and noted.
4. The circuit is designed for a different value of hysterisis and tested.

Circuit diagrams, Waveforms and Transfer Characteristics :-

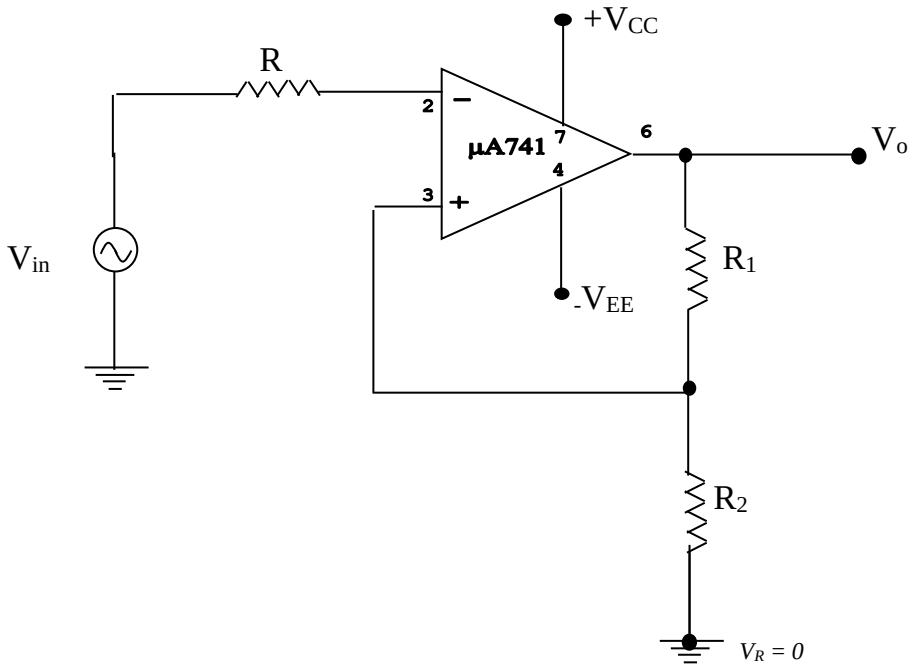


Fig (1) :SCHMITT TRIGGER CIRCUIT

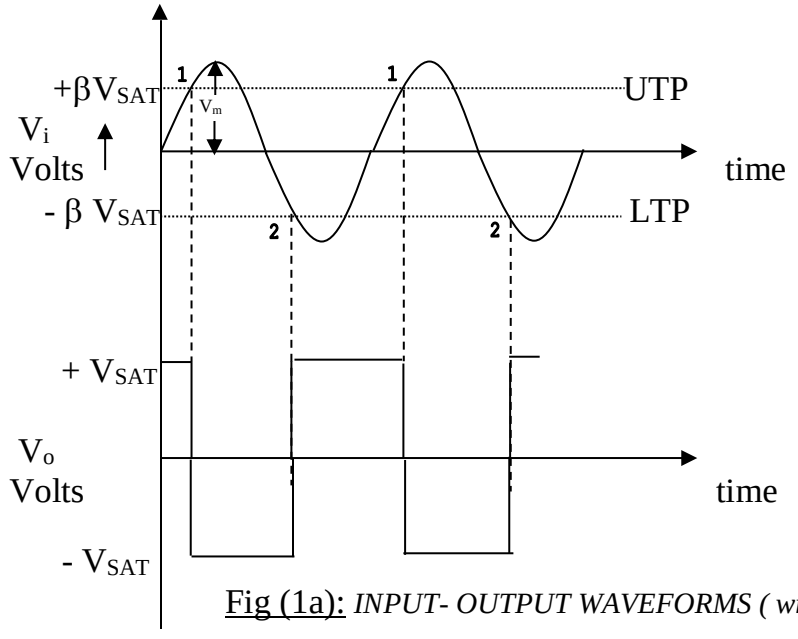
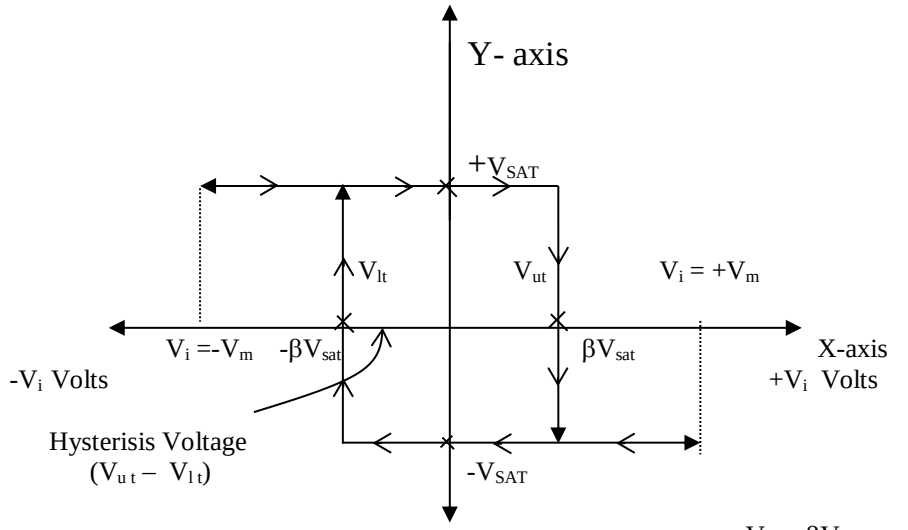


Fig (1a): *INPUT- OUTPUT WAVEFORMS (with $V_R = 0$)*



$V_{ut} = \beta V_{cc}$ = Upper trip point / UTP

$V_{lt} = -\beta V_{cc}$ = Lower trip point / LTP

Fig (1b) : **TRANSFER CHARACTERISTICS (With $V_R = 0$)**

Design Example : To design a Schmitt trigger circuit using op-amp for an UTP of +5 volts and LTP of +2 volts . Assume $+V_{SAT}$ = +14 volts and $-V_{SAT}$ = -14 V.

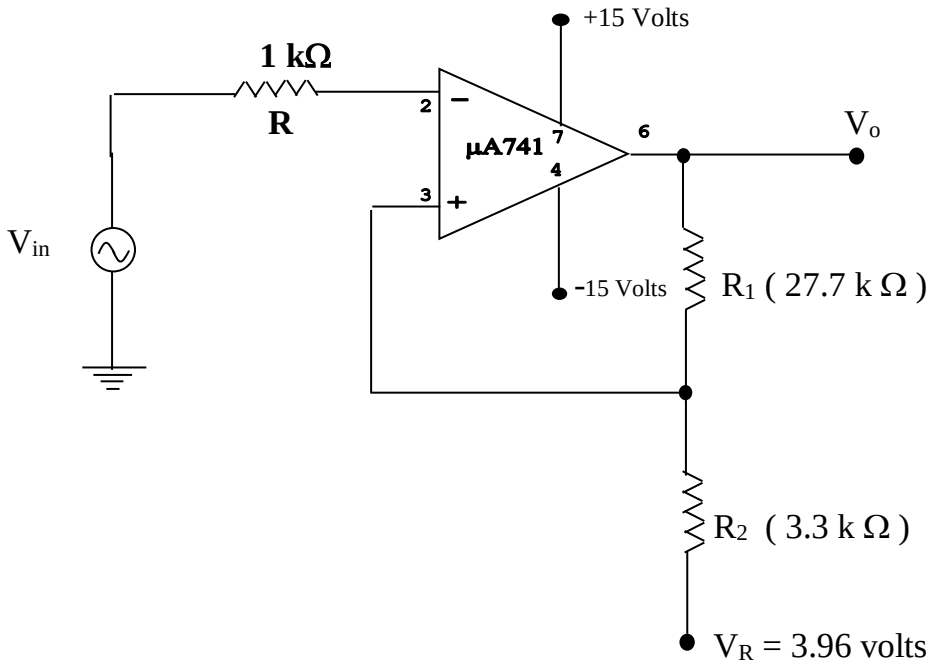


Fig (2): Circuit diagram of Schmitt trigger for design example (1)

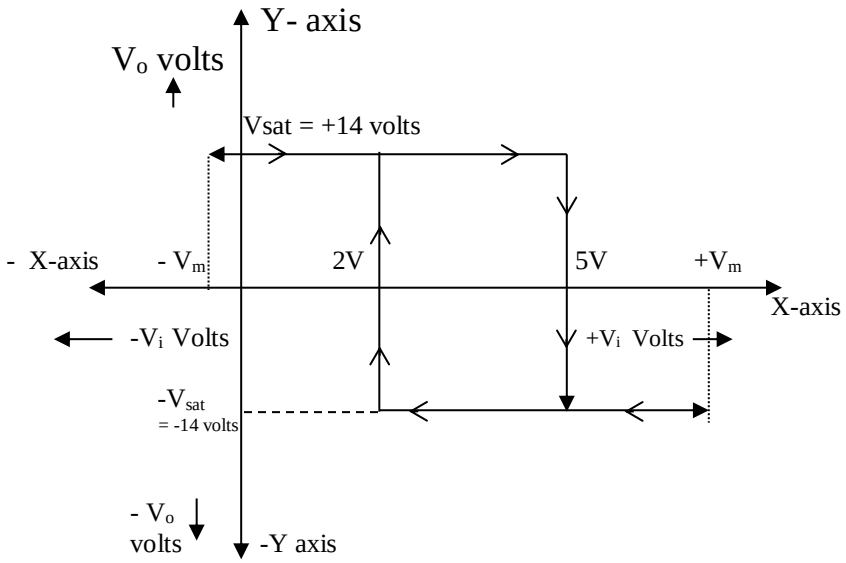


Fig (1b) : TRANSFER CHARACTERISTICS (With $+^{ve}$ V_R)

WKT : UTP = βV_{SAT} + $K V_R$ --- (1)

LTP = - βV_{SAT} + $K V_R$ --- (2)

& V_H = UTP – LTP ---(3)

Given : $V_H = 5 - 2 = 3$

Step (1)

Eqn(1)-Eqn(2)= Eqn (3) yields

$2 \beta V_{SAT} = 3$

$$\beta = \frac{3}{28} = 0.1071428$$

$$\frac{R_2}{R_1 + R_2} = 0.1071428$$

or $R_1 = 8.333 R_2$

for $R_2 = 3.3$ k Ω

we get $R_1 = 27.7$ k Ω

Step(2) : To find V_R :

UTP = $\beta V_{cc} + KV_R$

i.e. $\beta V_{SAT} = 1.5$

We can write

$5 = 1.5 + KV_R$

$$3.5 = \frac{R_1}{R_1 + R_2} V_R$$

$3.5 = 0.8935483 V_R$

or V_R = + 3.92 volts

Experiment No.7 Date:

PRECISION HW & FW RECTIFIERS

Aim : To rig up and test Half wave and Full wave Precision Rectifiers.

Apparatus Required :

Sl. No.	Apparatus	Range	Quantity
1.	IC μA 741		2
2.	Diodes	BY 127	2
3.	Resistors	10 k Ω 1 k Ω	5 2
4.	Multi meter		1
5.	Adopters		3
6.	IC base board, Base board		1 set
7.	ASG, Power supply, CRO		1 set
8.	Connecting wires		1 set

Procedure :

1) Connections are made as shown in the circuit of figure (1).
2) The bias supply is switched ON.
3) Sinusoidal input voltage of amplitude less than 0.7 V at a frequency of 1 kHz is applied and the output waveform is observed.
4) The input and output waveform are observed together on the CRO. The CRO is then set to X-Y mode and its transfer characteristic is observed.
5) The Values of Ra and / or Rb are changed and the change in the slope of the transfer curve is observed.
6) The above procedure is repeated for circuits of figure (2), (3)and (4).

Circuit Diagrams and Waveforms:-

Sl.No 1.

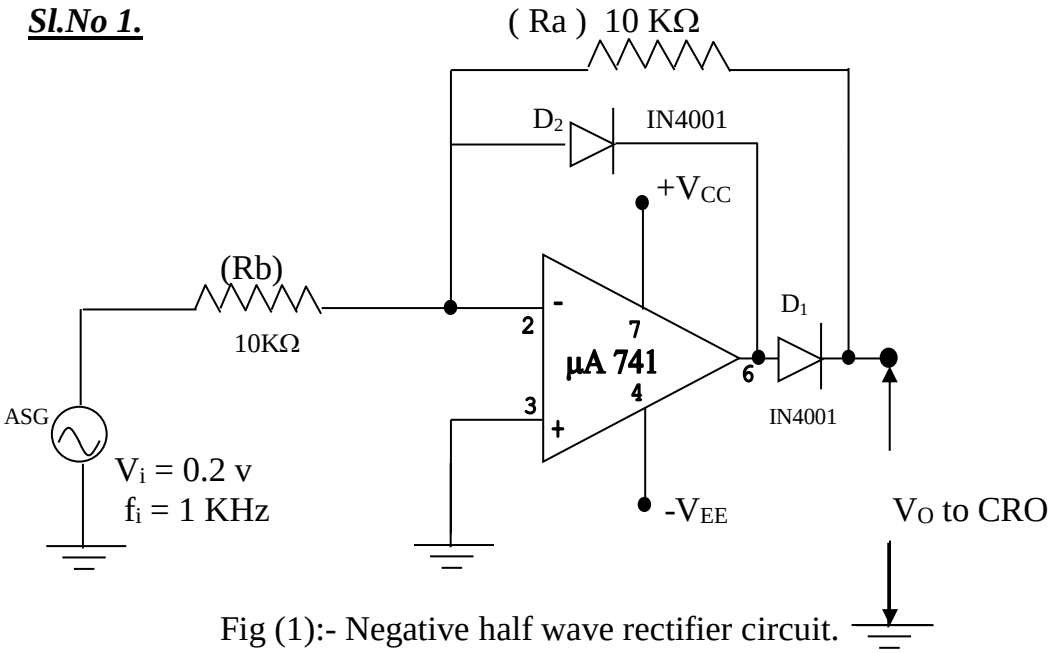


Fig (1):- Negative half wave rectifier circuit.

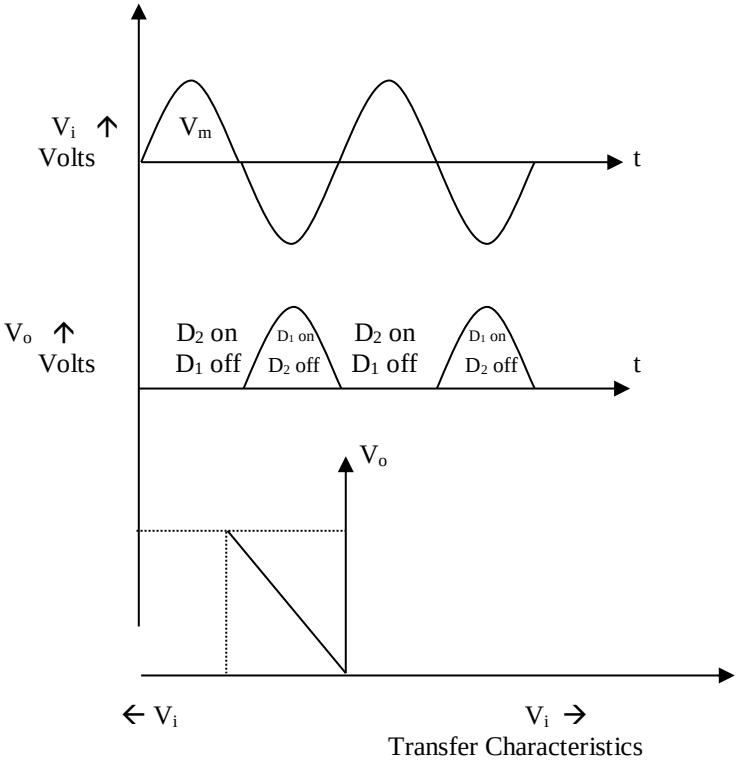


Fig (1a): WAVEFORMS & TRANSFER CURVE

Sl.No 2.

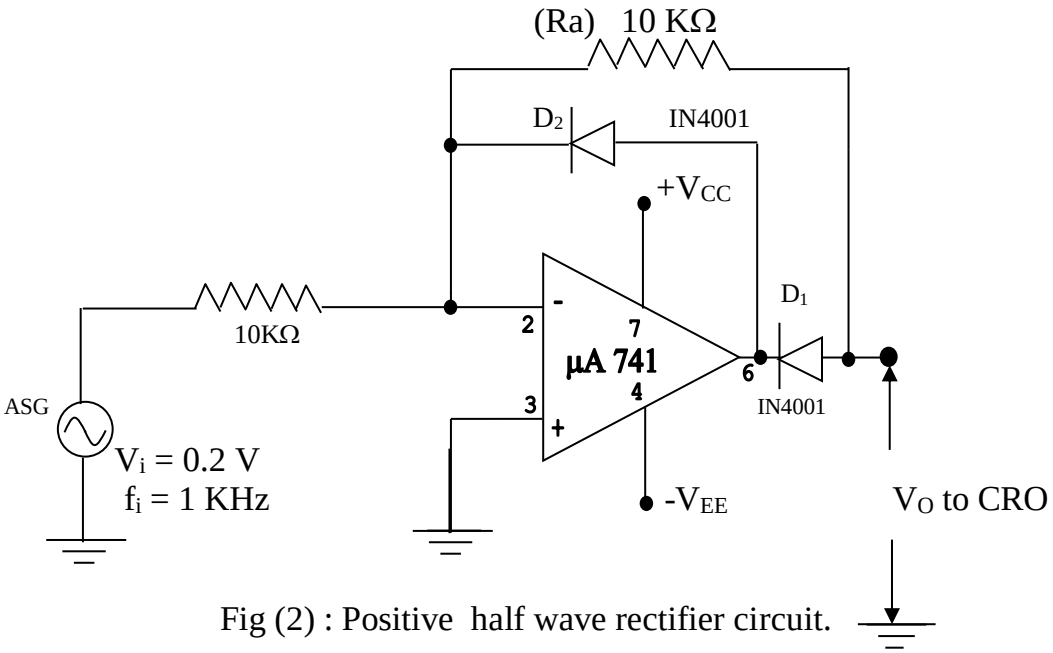


Fig (2) : Positive half wave rectifier circuit.

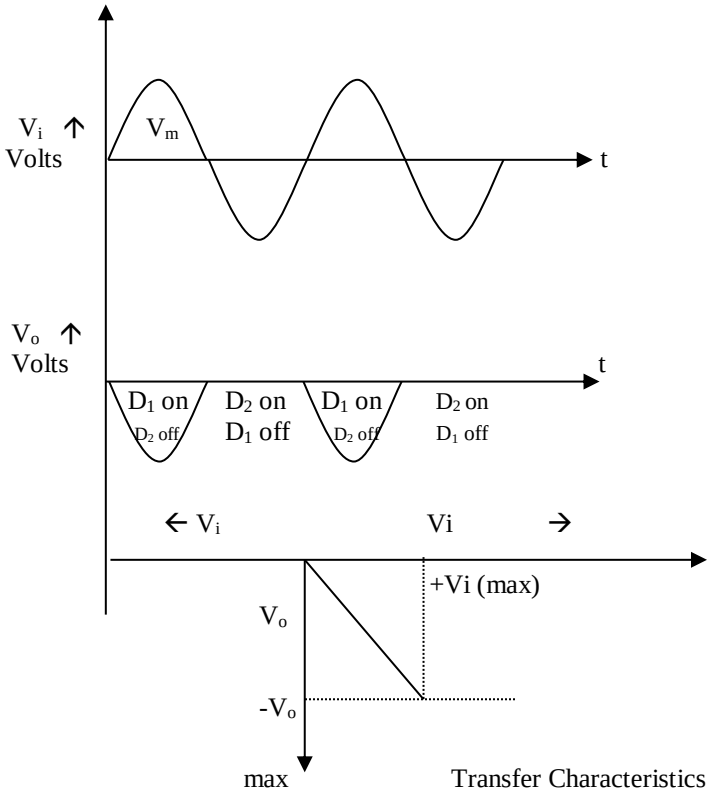


Fig (2a) : WAVEFORMS & TRANSFER CURVE

Sl.No 3.

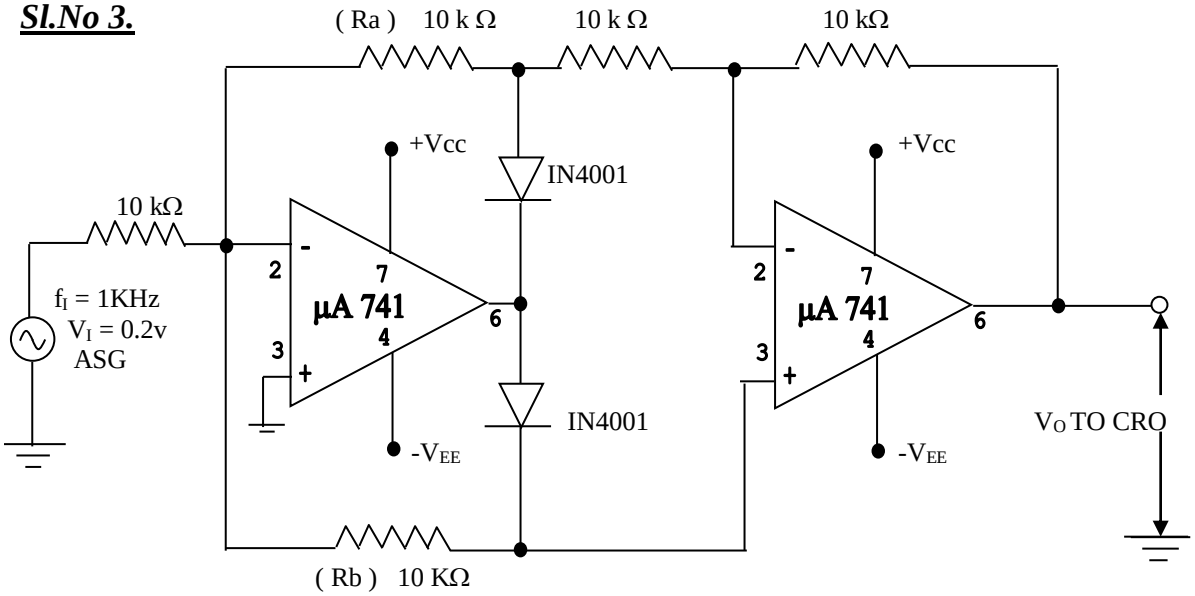


Fig (3) : Positive Full Wave Rectifier Circuit

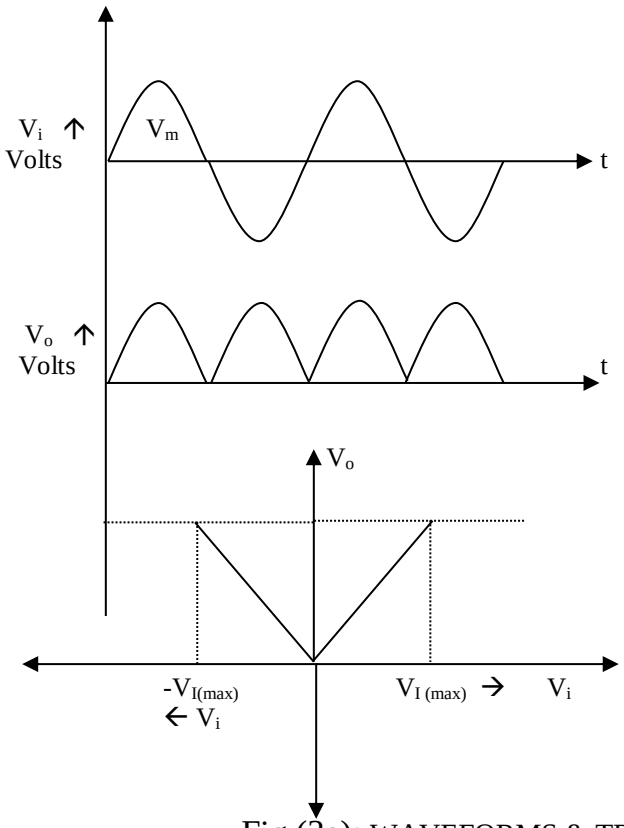


Fig (3a): WAVEFORMS & TRANSFER CURVE

Sl.No 4.

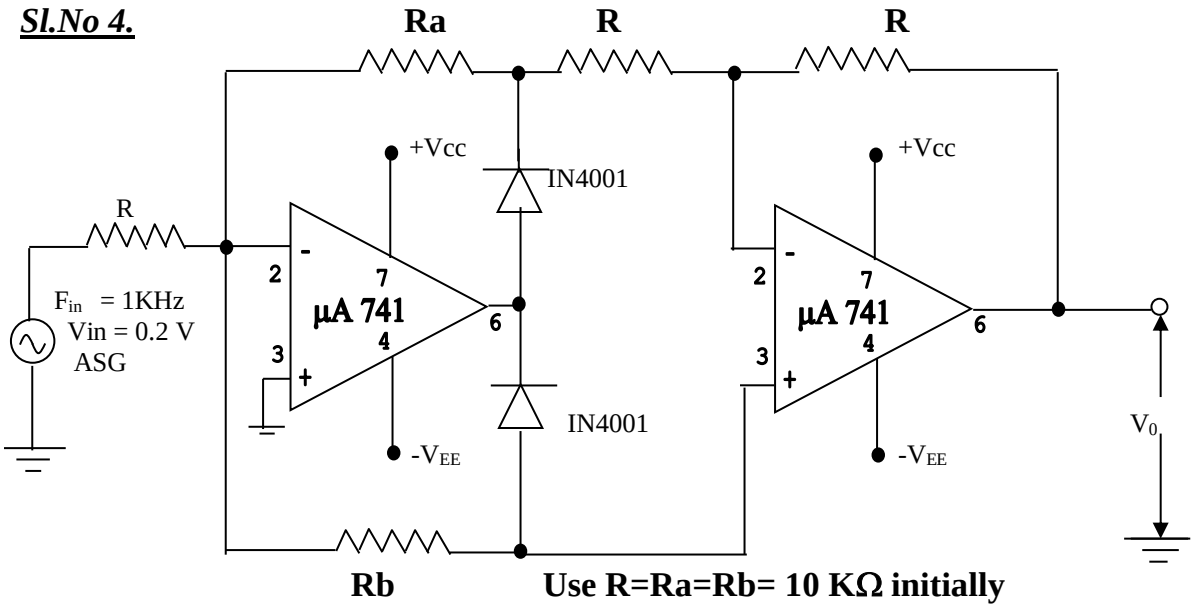


Fig (4) : Negative Full Wave Rectifier Circuit

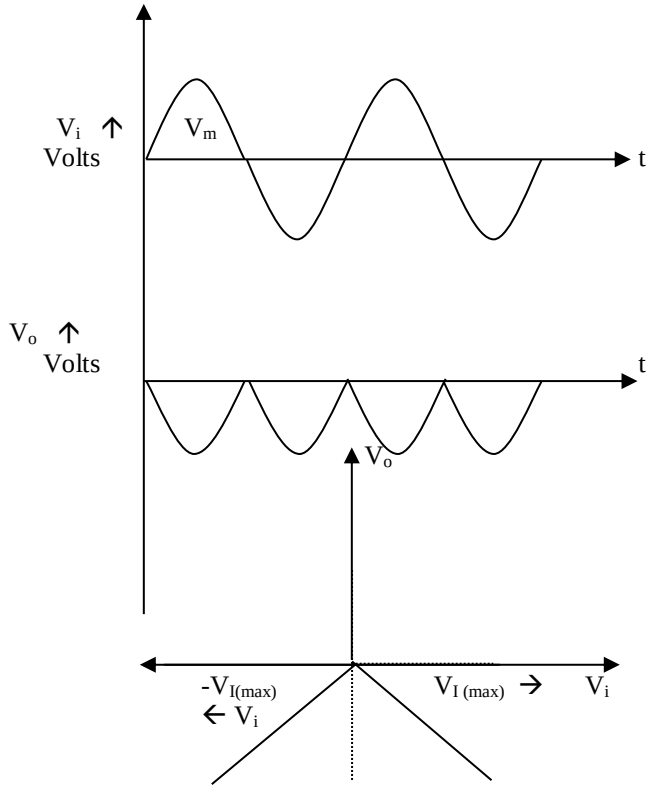


Fig (4a): WAVEFORMS & TRANSFER CURVE

Experiment No. 8 Date:

FIRST AND SECOND ORDER ACTIVE LOW PASS FILTERS

AIM : To design and test I and II order ACTIVE LOW pass filters, and to obtain the frequency responses.

APPARATUS REQUIRED:

Sl. No.	Particulars	Range	Quantity
1.	OP amp μA 741		
2.	Resistors	10 k Ω	3
3.	Capacitors	0.01 μF	2
4.	ASG, CRO		
5.	Adopters		2
6.	Power supply	+/-15V	1
7.	Multimeter and probes		1 + 2 set
8.	IC base board base board		1 1
9.	Connecting wires		

PROCEDURE :

1. The first order LPF is designed for a given cut-off frequency $\mathbf{f_h}$, say 5 KHz .
2. Connections are made as shown in figure(1) as per the design.
3. The input voltage is kept at a constant value (say 2 V) and the frequency is varied from 10 Hz to 100 KHz in steps, and at each step the output voltage is measured using a CRO and recorded.
4. The readings are tabulated and the gains in dB are calculated.
5. A graph of frequency Vs. gain in dB is plotted and the actual cut-off frequency (f_h) and the slope in the stop band (Roll-off rate) are determined from the graph plotted.
6. The above procedure is repeated for a II order LPF shown in figure (2).

Circuit Diagrams , Ideal Graphs and Designs :-

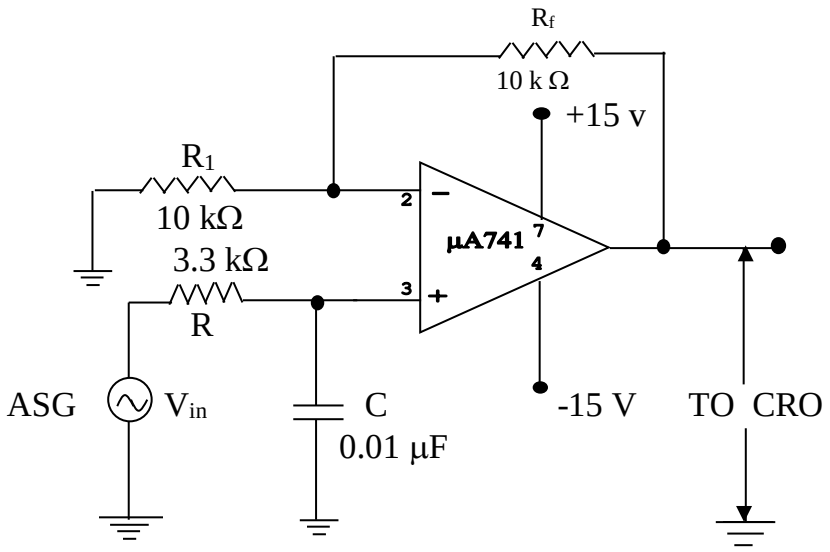


Fig (1): FIRST ORDER LOW PASS FILTER

Design Example:-

Let the filter's PB gain $A_f = 2$
Choose $R_f = R_1 = 10\ k\Omega$

WKT, $f_h = \frac{1}{2\pi RC}$. Given $f_h = 5$ KHz

If $C = 0.01\ \mu F$ then ., $R = \frac{1}{2\pi \times 0.01\mu \times 5k} = 3.183\ k\Omega.$

[Use 2.2 K + 1 K]

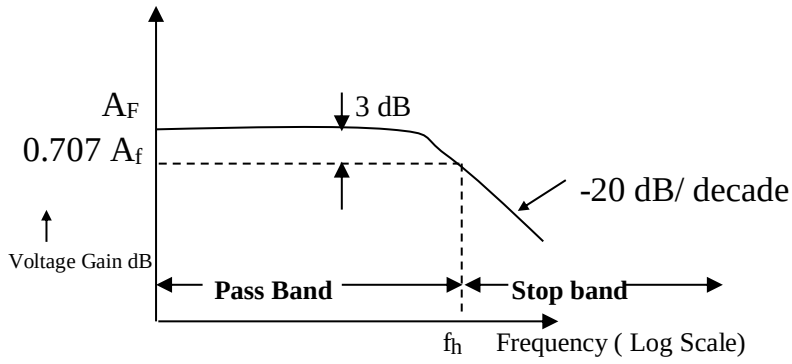


Fig (1a) : Frequency response curve

Tabular column :-

Constant V_{in} = 2.0 volts

Sl. No.	Frequency (Hz)	V_o volts	$A_v = \frac{V_o}{V_i}$	20 logA_v (Gain in dBs)

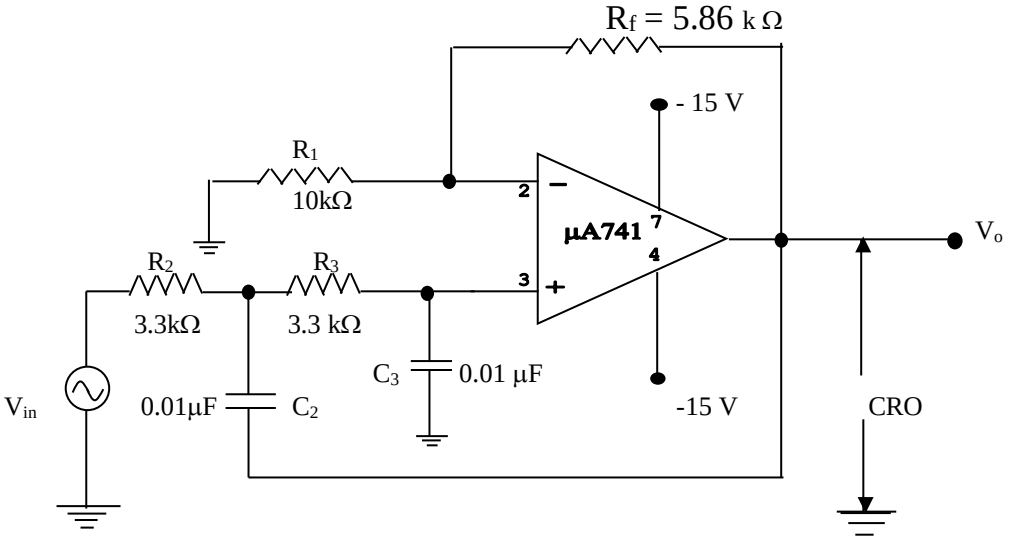


Fig (2) : Circuit Diagram of Second order low pass filter

Design Example:

For Butterworth response (Flat Pass band), $A_f = 1.586$

But $A_f = 1 + \frac{R_f}{R_1}$

let $R_1 = 10\ k\Omega$, therefore $R_f = 5.80\ k\Omega$

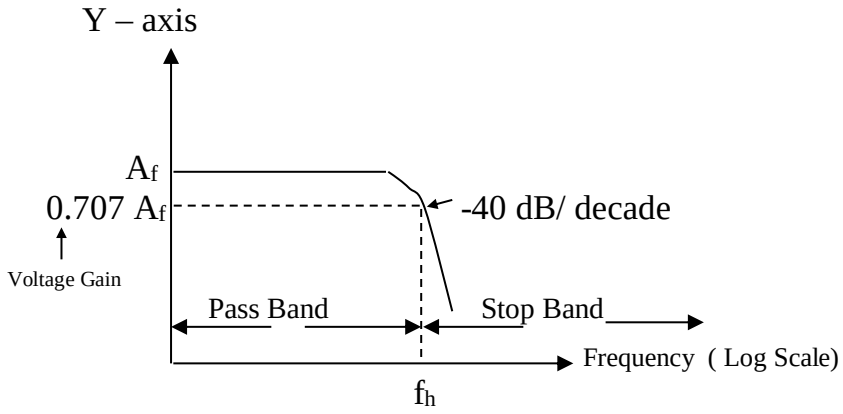
Now $f_h = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$ Assuming $R_2 = R_3 = R$ and $C_2 = C_3 = C$,

We have $f_h = \frac{1}{2\pi RC}$ Given $f_h = 5$ kHz.

Assuming $C = 0.01\ \mu F$,

$R = \frac{1}{2\pi \text{ x } 0.01\mu \text{ x } 5\text{ k}} = 3.183$ K [Use 2.2 K + 1 K]

Frequency response curve



Fig(2a) : Frequency response curve

TABULAR COLUMN :-

Constant $V_{in} = 4$ volts

Sl. No.	Frequency (Hz)	V_o volts	$A_v = \frac{V_o}{V_i}$	20 logA_v (Gain in dBs)

Experiment No. 9 Date:

FIRST AND SECOND ORDER ACTIVE HIGH PASS FILTERS

AIM: To design and obtain the frequency responses of I and II order active high pass filters :

APPARATUS REQUIRED:

Sl. No.	Particulars	Range	Quantity
1.	Op amp μA 741 IC		1
2.	Resistors		
3.	Capacitors	0.01 μF	1
4.	ASG, CRO		1
5.	Adopters		2
6.	Power supply	+/– 15 V	1
7.	Multimeter with probes		1+ 2 set
8.	Base board , IC Base board		1 set
9.	Connecting wires		1 set

PROCEDURE :-

7. The I order HPF is designed for a particular cut-off frequency (f_L) (say 5 KHz) by choosing proper values of R and C .
8. Connections are made as shown in figure(1) as per the design.
9. The input voltage is kept at a constant value (say 2 V) and the frequency is varied from 10 Hz to 100 KHz in steps, and at each step the output voltage is measured using a CRO and recorded.
10. All the readings are tabulated and the gain in dB is calculated.
11. A graph of frequency Vs. gain in dB is plotted and the actual cut-off frequency (f_L) and the slope in the stop band are determined from the graph plotted.
12. The above procedure is repeated for the circuit of a II order HPF shown in figure (2).

CIRCUIT DIAGRAMS,DESIGNS AND FREQUENCY RESPONSES:-

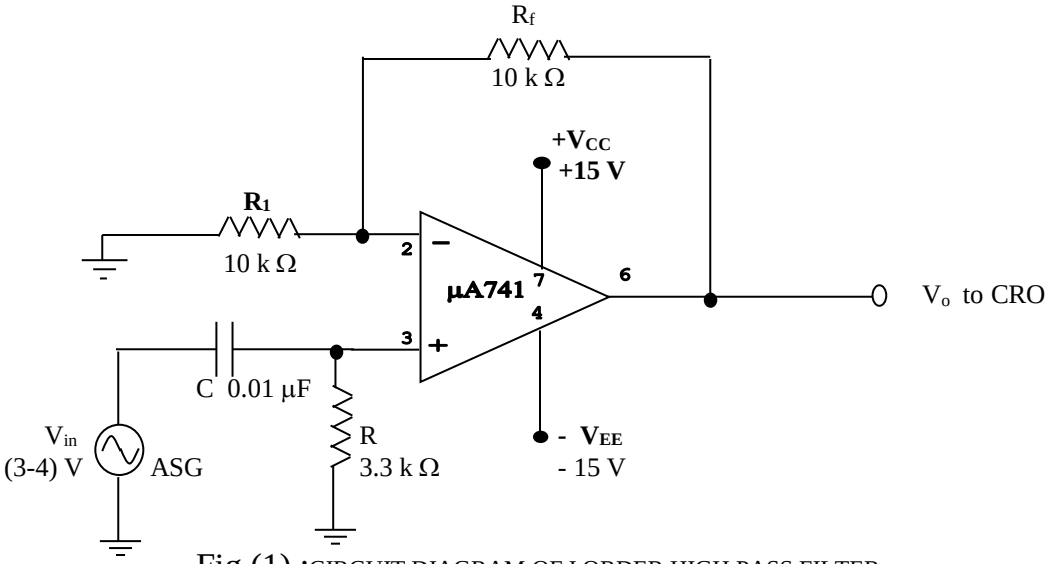


Fig (1) :CIRCUIT DIAGRAM OF I ORDER HIGH PASS FILTER

FREQUENCY RESPONSE:-

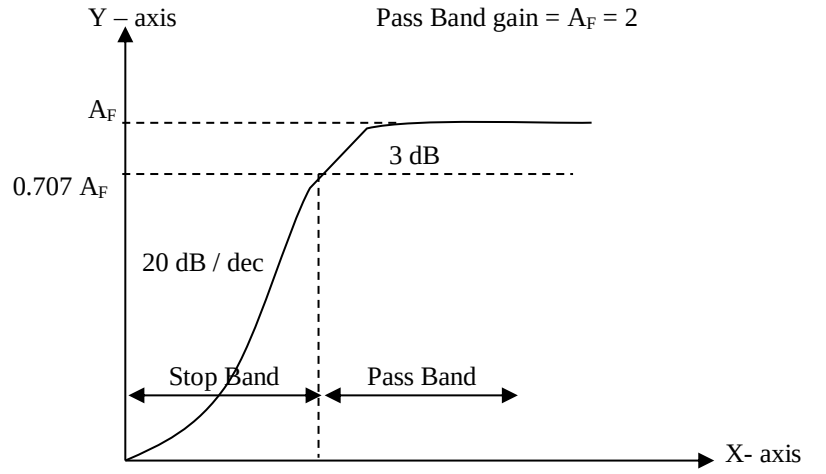


Fig (1a)

DESIGN EXAMPLE:-

The cut-off frequency $f_L = \frac{1}{2\pi RC}$

Let C = 0.01 µF

5 K = $\frac{1}{2\pi 0.01\mu * R}$ R = 3.18 k Ω { Use 2.2K and 1K in series }

Use $R_1 = R_f = 10$ k Ω → $A_F = 1 + \frac{R_f}{R_1}$ → A gain of 2.

TABULAR COLUMN:-

CONSTANT V_{in} = 4 volts

f in Hz	V_o Volts	$A_V = \frac{V_o}{V_i}$	A_V in dB

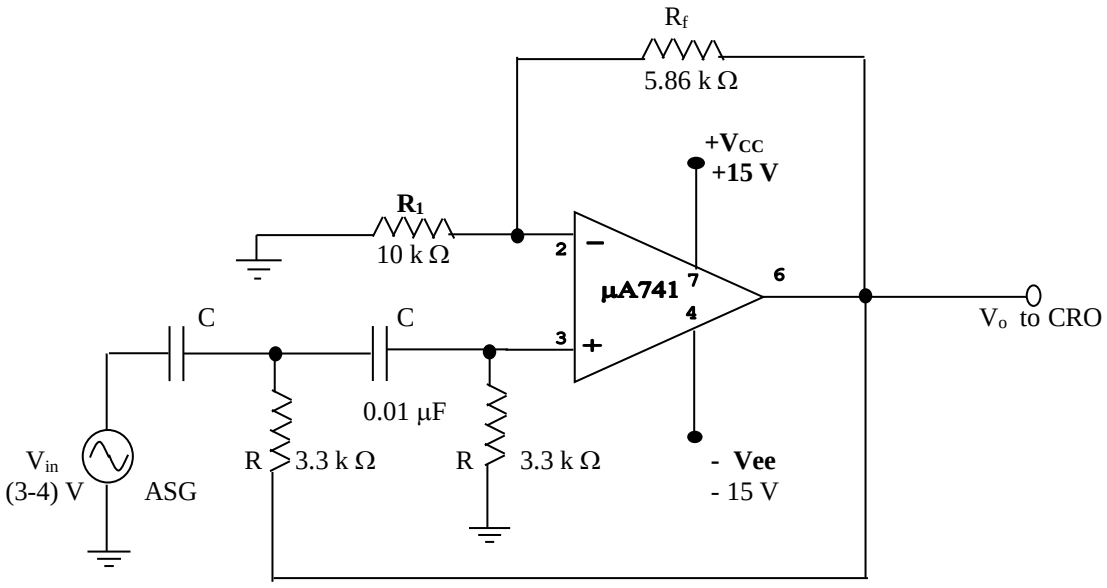


Fig (2) :CIRCUIT DIAGRAM OF II ORDER HIGH PASS FILTER

DESIGN EXAMPLE:-

For the Circuit, PB gain is $A_F = 1 + \frac{R_f}{R_1}$

For Butterworth response $A_F = 1.586$

Let $R_1 = 10\ k\Omega$,

$R_F = R_1 A_F - R_1 \quad = R_1 (1.586 - 1)$

$= 10\ K \times 0.586 = 5.86\ k\Omega$

for $f = 5$ kHz $\quad f_L = \frac{1}{2\pi RC}$

Let $C = 0.01\ \mu F \quad R = \frac{1}{2\pi \times 5\ k \times 0.01\ \mu}$

$R = 3.18\ k\Omega$

FREQUENCY RESPONSE:-

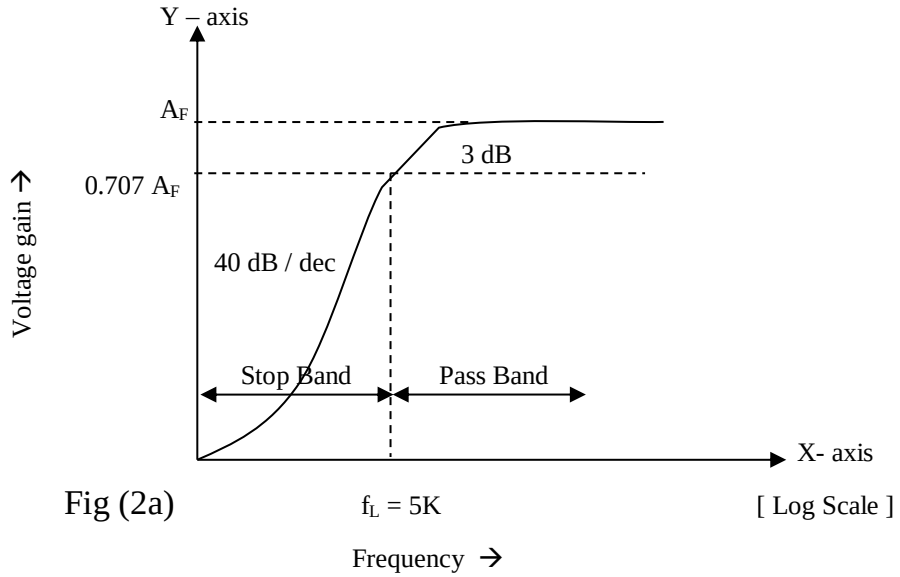


Fig (2a)

TABULAR COLUMN:-

CONSTANT V_{in} = 4 volts

f in Hz	V_o Volts	$A_V = \frac{V_o}{V_i}$	A_V in dB

Experiment No. 10 **Date:**

ASTABLE & MONOSTABLE MULTIVIBRATORS USING 555 TIMER

AIM : To design and test Astable and Monostable Multivibrators for the given specifications using 555 timer IC.

APPARATUS REQUIRED:

Sl. No.	Particulars	Range	Quantity
1.	IC 555		1
2.	Diodes IN 4001		2
3.	Capacitor	0.1 and 0.01 μF	1
4.	DCB, ASG, Base board		1
5.	DRB		
6.	Resistors		1
7.	Power supply	+ 5 V	1
8.	CRO and Probes		1 set
9.	Multimeter and probes		1 set
10.	Adopters & wires		3 sets

PROCEDURES :-

I . Astable Multivibrators (AMVs)

1. Connections are made as shown in the circuit of figure (1) and the power supply is switched ON.
2. The output voltage waveform and the voltage across the timing capacitor are observed and traced using a CRO.
3. All the relevant voltage levels like 1/3 Vcc , 2/3 Vcc are noted.

Ton and **Toff** are also measured and noted. The frequency of oscillation and the duty cycle are calculated and verified against the theoretical values.

5. The above procedure is repeated for different duty cycles as shown in circuits of figure (2) and (3).

II. <u>Monostable Multivibrator:-</u>

1. The MMV is designed for a particular 'Pulse width' as per the design shown and the connections are made as shown in circuit of figure(4).
2. The input trigger signal's frequency and duty cycle are set to appropriate values and the output waveform is observed and verified for the required pulse width.
3. The following combinations of waveforms are observed together on a CRO and traced. *a) Trigger signal and output signal*
   b) Output waveform and Capacitor voltage

1) The pulse width is measured and noted
2) The above procedure is repeated for a different value of pulse width.

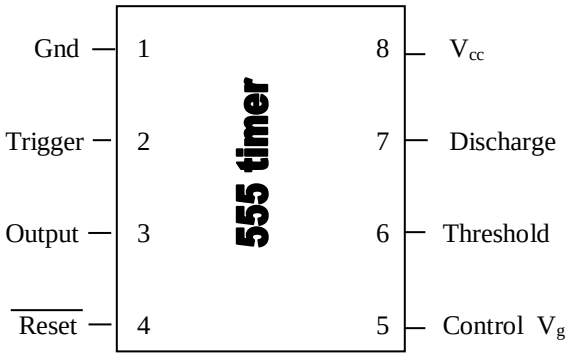


Fig (a) : PIN DIAGRAM OF 555 timer

<u>Note :</u>- In the circuit diagrams that follow, only pin numbers are marked. Referring to the pin diagram of Fig (a) , specify the pin functions accordingly for all the circuit diagrams.

Circuit Diagrams, Waveforms and Designs:-

Design Example 1 : To Design an Astable multivibrator circuit using 555 timer for f = 1 KHz, duty cycle = 70 % and V_{out} = 5 Volts.

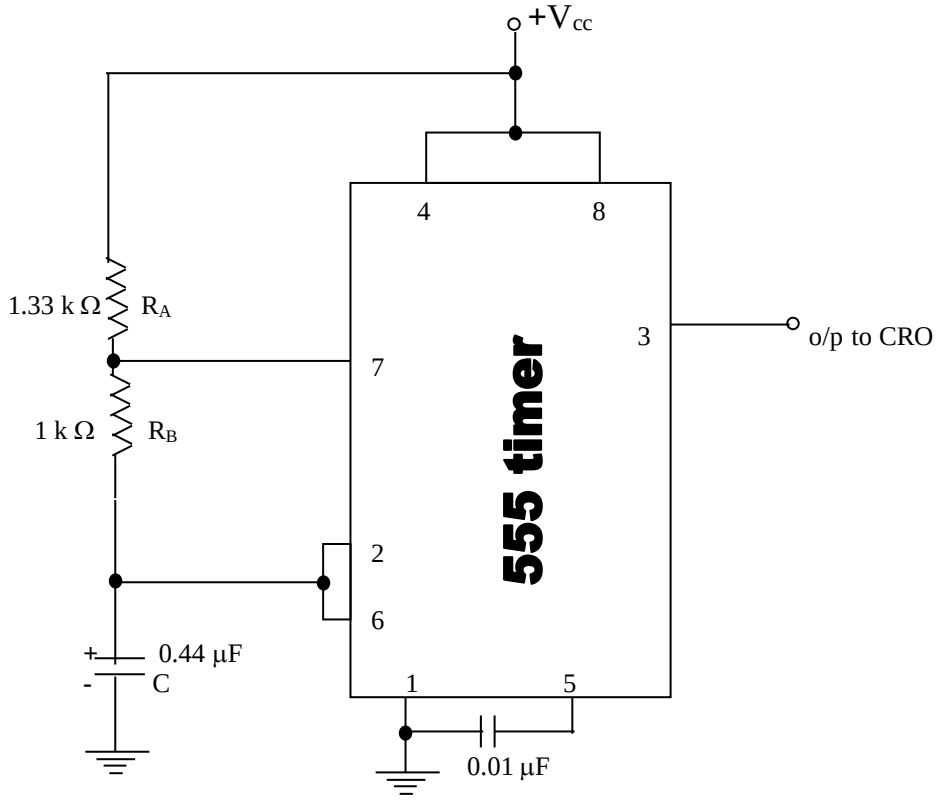


Fig (1) : Circuit of Astable Multivibrator for duty cycle > 50 %

We Know that

$T_1 = 0.69\ (R_A + R_B)\ C$ and $T_2 = 0.69\ R_B\ C$

and Duty Cycle $= \dfrac{T_1}{T_1 + T_2} = \dfrac{R_A + R_B}{R_A + 2R_B}$

Given duty cycle= 70 %

$$\therefore \frac{R_A + R_B}{R_A + 2R_B} = \frac{70}{100} = 0.7$$

or $R_A + R_B = 0.7\ R_A + 1.4\ R_B$

$0.3\ R_A = 0.4\ R_B$ or $R_A = 1.33\ R_B$

for $R_B = 1\ k\Omega$, $R_A = 1.33\ k\Omega$

$T = T_1 + T_2$ & $T = 0.69\ (R_A + 2R_B)\ C$

Given f = 1 KHz, therefore T = 1msec

1ms = 0.69 [1.33 K + (2 x 1 K)] x C

Therefore C = 0.44 μF (Use two numbers of 0.22 μF in parallel)

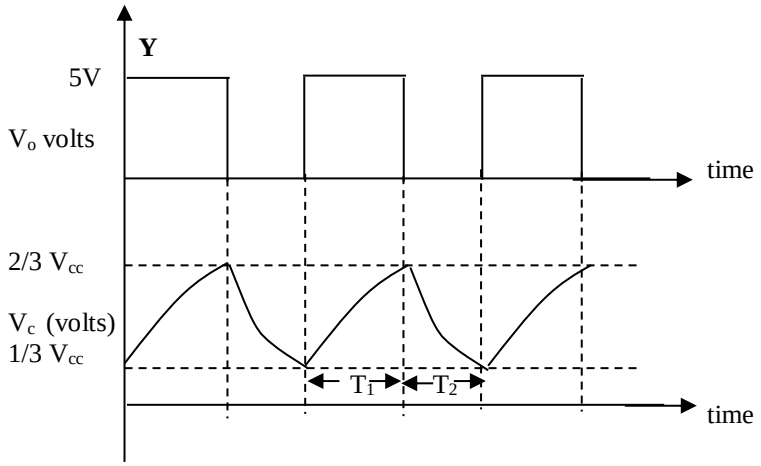


Fig (1a) : Waveforms in an Astable Multivibrator

Design Example 2 : To design an astable multivibrator circuit using 555 timer for a frequency of 1 KHz, duty cycle = 50 % & V_{out} =5 Volts.

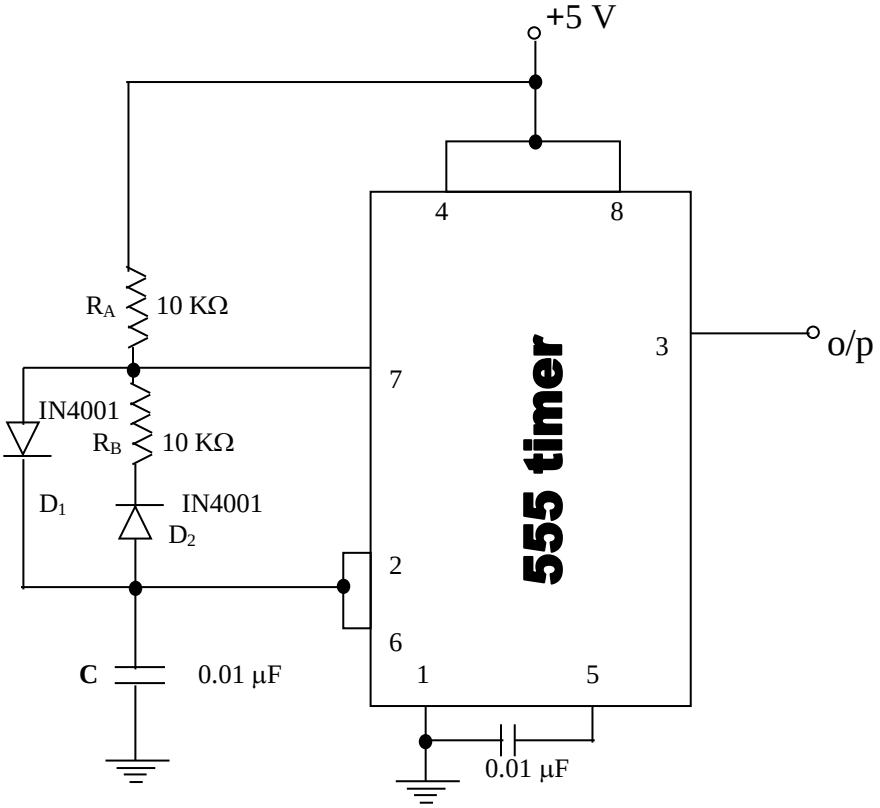
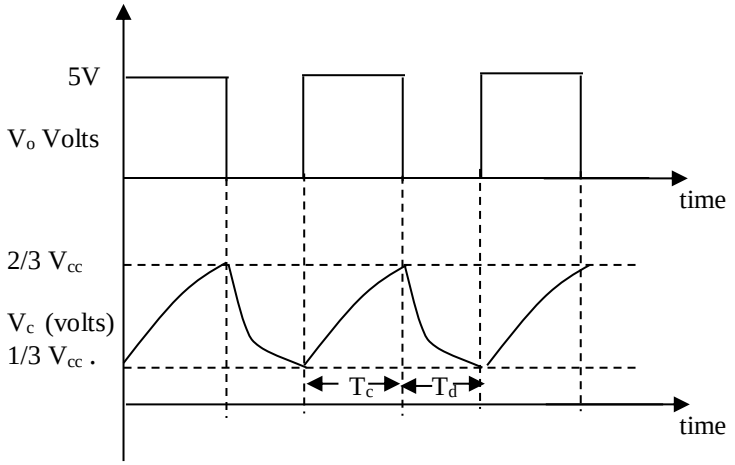


Fig (2) : Circuit diagram of AMV for any duty cycle



Fig(2a):

$T_1 = 0.69 (R_A + R_{f1}) C$ and $T_2 = 0.69 (R_B + R_{f2}) C$

Assuming that the diodes' on- resistances R_{f1} & R_{f2} are same and neglecting these, we get $T_1 = 0.69 (R_A) C$ and $T_2 = 0.69 (R_B) C$

If $R_A = R_B = 10$ k Ω, then duty cycle = $\{ R_A / (R_A + R_B) \} = 50$ %

Given f = 1 kHz, and therefore T = 1ms. Further, $T_1 = T_2 = 0.5$ msec

0.5ms = 0.69 x 10 k Ω x C ➔ C = 0.072 μF

Design Example 3: To design an AMV for 1 KHz, duty cycle = 0.8 & V_{out} =12 V

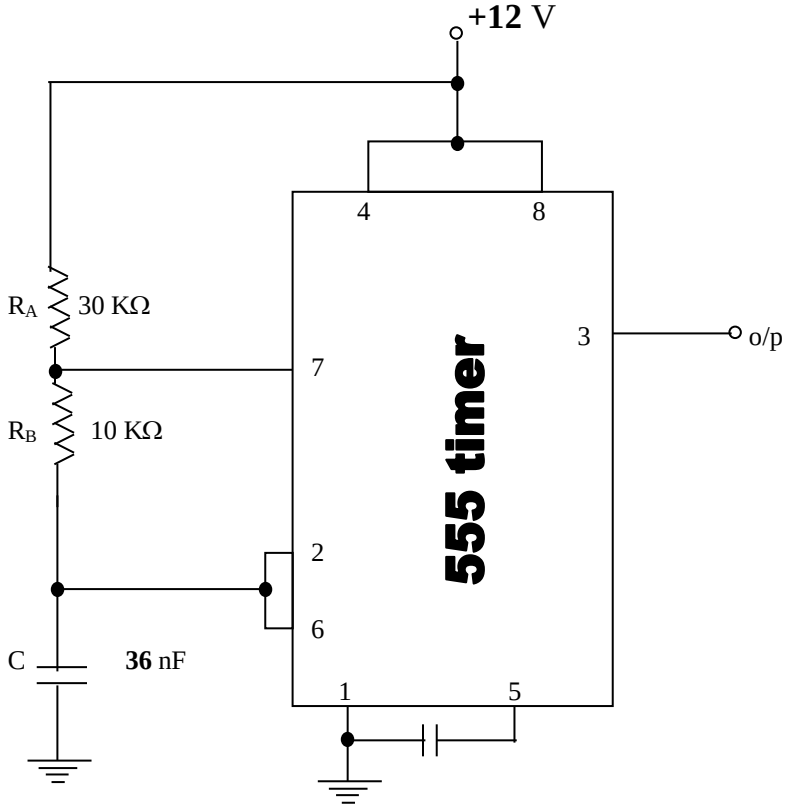


Fig (3) 0.01 μF

$T_1 = 0.69 (R_A + R_B) C$ and $T_2 = 0.69 R_B C$

Given., Duty cycle = 0.8

But Duty cycle $= \frac{T_1}{T_1 + T_2} = \frac{R_A + R_B}{R_A + 2R_B} = 0.8$

$\therefore R_A + R_B = 0.8 R_A + 1.6 R_B$

or $0.2 R_A = 0.6 R_B$

$R_A = 3 R_B$

If $R_B = 10$ K , then $R_A = 30$ K

$T = 0.69 (R_A + 2 R_B) C$

given f = 1 kHz, T = 1ms

Calculating., C = 36 nF.

Monostable Multivibrator (MMV):-

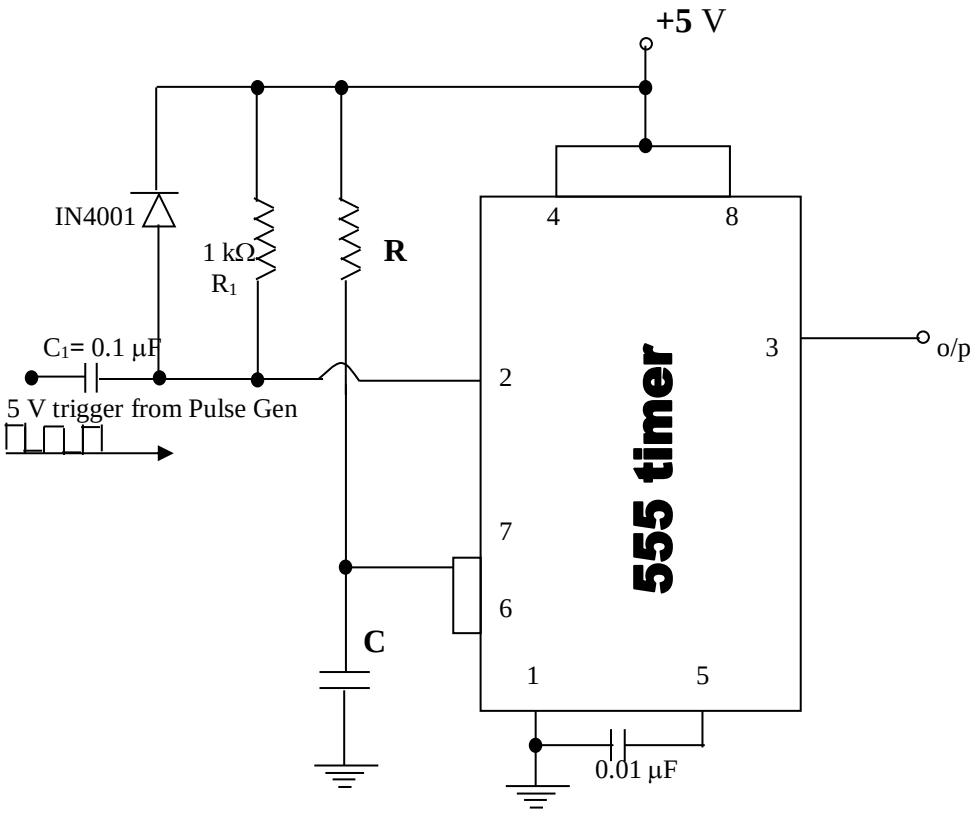


Fig (4) :- Monostable multivibrator circuit using 555 timer IC

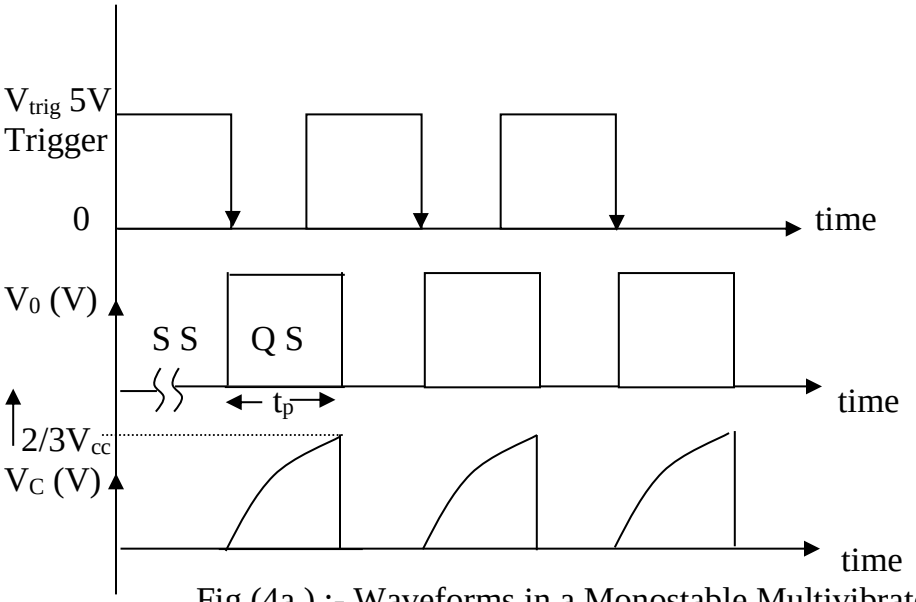


Fig (4a) :- Waveforms in a Monostable Multivibrator

NOTE : - SS : Stable State & QS : Quasi Stable State

Design Example 1 : To design a MMV for a pulse width of 1.25 msec

Pulse width = 1.11 RC

$$RC = \frac{t_p}{1.11}$$

Let C = 0.1 μF ; t_p = 1.25 ms

$$R = \frac{1.25\ ms}{1.11x\ 0.1\ \mu} = 11.267\ k\Omega$$ [Use a 10 K and 1 K resistors in series.]

Design Example 2 : To design a MMV for a pulse width of 3.0 msec

1) Let C = 0.1 μF

t_p = 3ms

$$R = \frac{t_p}{1.11 \times C}$$

$$R = \frac{3 \times 10^{-3}}{1.11 \times 0.1 \times 10^{-6}} = R = 27.02\ k\Omega$$ [Use 10 K + 10 K + 6.8 K in series]

Experiment No. 11 **Date:**

DAC USING R-2R LADDER NETWORK

Aim : To rig up and test a 4-bit R-2R ladder network DAC .

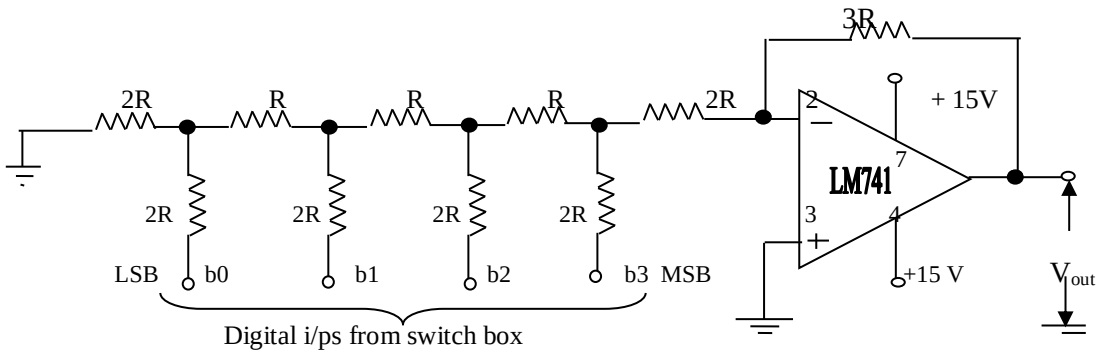
Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1	μA741 IC		1
2.	Resistors	2.2 kΩ	18
3.	Power supply	± 15 volts 0-5 volts	1 1
4.	Multimeter and probes	-	1 set
5.	Spring board, IC base board	-	1 1 set
6.	Connecting wires	-	1 set

PROCEDURE :

1) Connections are made as shown in fig (1) .
2) The digital inputs b_1-b_4 are connected to a switch box. The 4 bits are increased in steps from 0000 to 1111 and at each step V_{out} is measured using a multimeter.
3) The readings are tabulated.
4) A graph of digital i/p versus analog o/p voltage is plotted, and the different parameters as shown in figure(2) are determined and recorded.

Circuit Diagram:-



Fig(1): Circuit diagram of R-2R DAC

Design :

$V_{out} = -\frac{V_r}{2^n}\sum_{i=0}^{n-1} b_i 2^i$ Where, $b_i = 0 \, or \, 1$

When all the digital i/p bits are 1 and V_r = +5 volts.

$$V_{out} = -\frac{5}{2^4}\sum_{i=0}^{3} b_i 2^i$$

$$= -\frac{5}{2^4}\left[b_o 2^0 + b_1 2^1 + b_2 2^2 + b_3 2^3\right]$$

$$= -\frac{5}{2^4} x15 \longrightarrow$$ For a full scale input of 1111

$V_{out(\text{ full scale})}$ = -4.6875 Volts

Tabular Column : -

b_3	b_2	b_1	b_0	V_{out} (Theoretical) volts	V_{out} (Practical) Volts
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	1	1	1		
0	1	0	0		

0 0 1	1 1 1	0 1 1	1 0 1		

Typical Converter Relationship :-

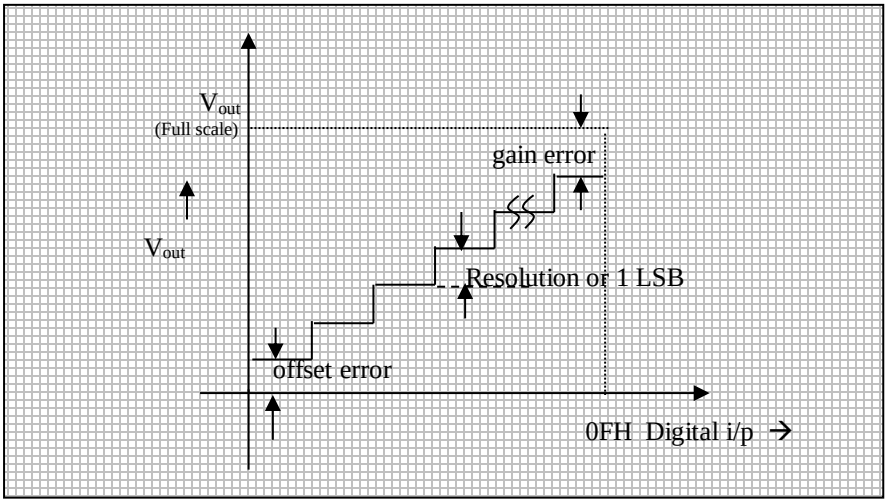


Fig (2): Typical Converter Relationship

Results:-

1) LSB or Resolution = _____ Volts
2) Offset error = _____ Volts
3) V_{out} (full scale) designed = _____ Volts
4) V_{out} (full scale) obtained = _____ Volts
5) Gain error = _____ Volts

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