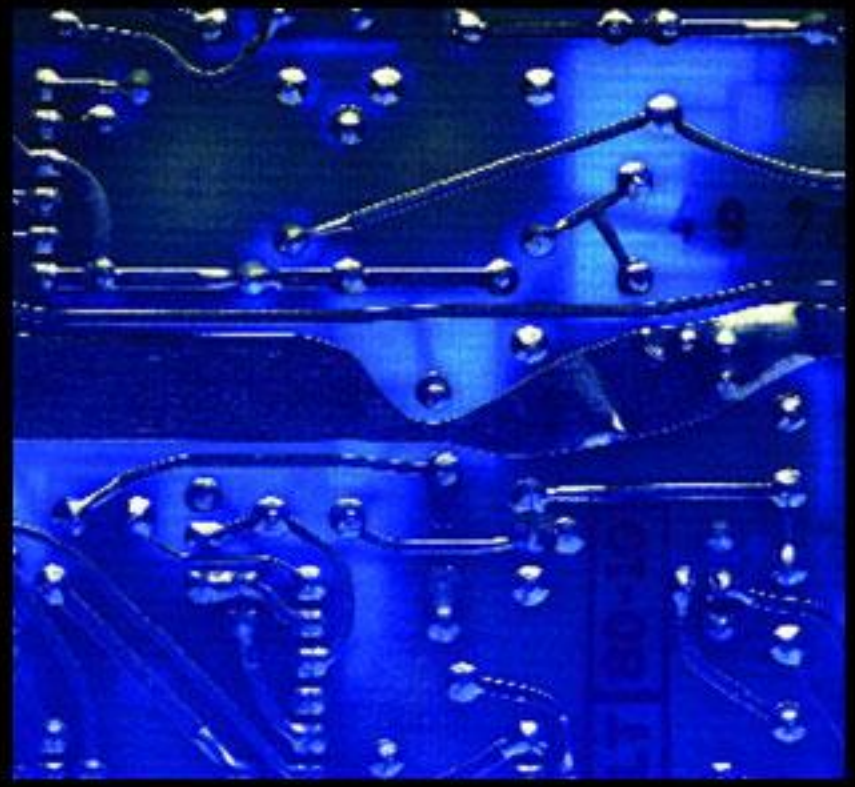
ELECTRONIC DEVICES AND CIRCUIT THEORY

TENTH EDITION



BOYLESTAD

PEARSON

PART-1 INTRODUCTION

Definitions

In small-signal amplifiers the main factors are:

- **Amplification**
- **Linearity**
- **Gain**

Since large-signal, or power, amplifiers handle relatively large voltage signals and current levels, the main factors are:

- **Efficiency**
- **Maximum power capability**
- **Impedance matching to the output device**

Introduction

Power amplifiers are used to deliver a relatively high amount of power, usually to a low resistance load.

Typical load values range from 300W (for transmission antennas) to 8W (for audio speaker).

Although these load values do not cover every possibility, they do illustrate the fact that power amplifiers usually drive low-resistance loads.

Amplifier Types

Class A

The amplifier conducts through the full 360° of the input. The Q-point is set near the middle of the load line.

Class B

The amplifier conducts through 180° of the input. The Q-point is set at the cutoff point.

Class AB

This is a compromise between the class A and B amplifiers. The amplifier conducts somewhere between 180 and 360° . The Q-point is located between the mid-point and cutoff.

Amplifier Types

Class C

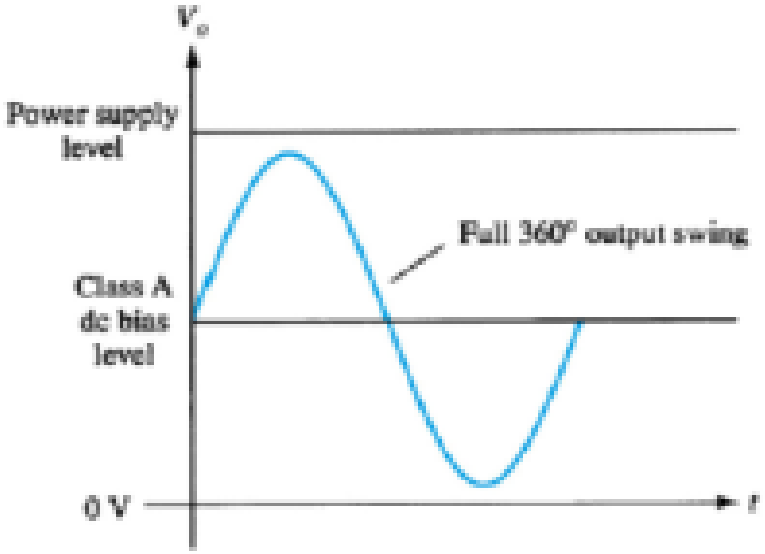
The amplifier conducts less than 180 ° of the input. The Q-point is located below the cutoff level.

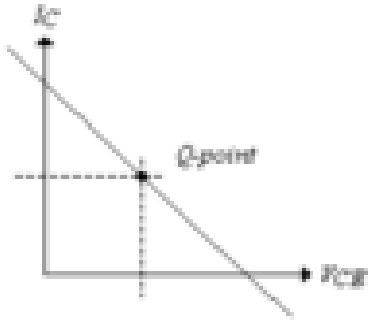
Class D

This is an amplifier that is biased especially for digital signals.

Class A Amplifier

The output of a class A amplifier conducts for the full 360° of the cycle.
The Q-point is set at the middle of the load line so that the AC signal can swing a full cycle.

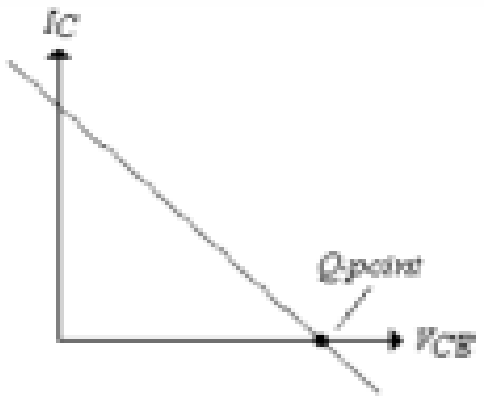


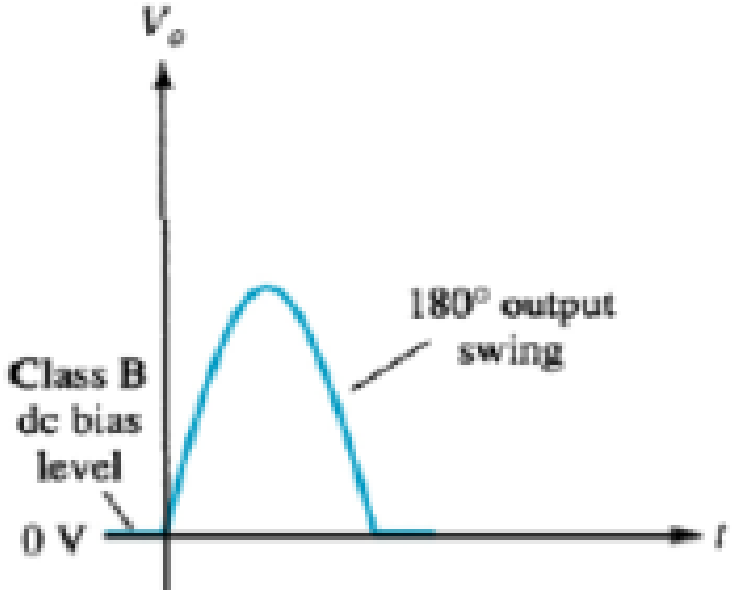


Remember that the DC load line indicates the maximum and minimum limits set by the DC power supply.

Class B Amplifier

A class B amplifier output only conducts for 180° or one-half of the AC input signal.



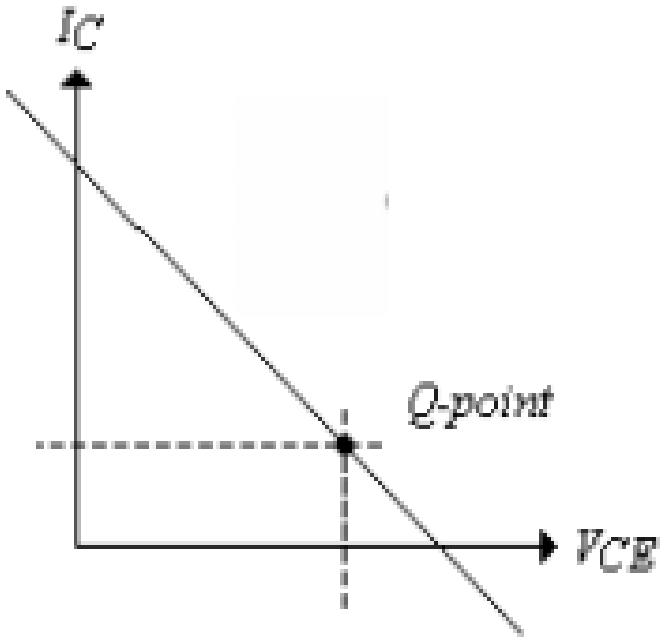


The Q-point is at 0V on the load line, so that the AC signal can only swing for one-half cycle.

Class AB Amplifier

This amplifier is a compromise between the class A and class B amplifier.

—The Q-point is above that of the Class B but below the class A. The output conducts between 180° and 360° of the AC input signal.



Amplifier Efficiency

TABLE 16.1 Comparison of Amplifier Classes

	Class A	Class AB	Class B	Class C*	Class D
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

*Class C is usually not used for delivering large amounts of power, thus the efficiency is not given here.

Efficiency refers to the ratio of output to input power. The lower the amount of conduction of the amplifier the higher the efficiency.

SERIES-FED CLASS A AMPLIFIER

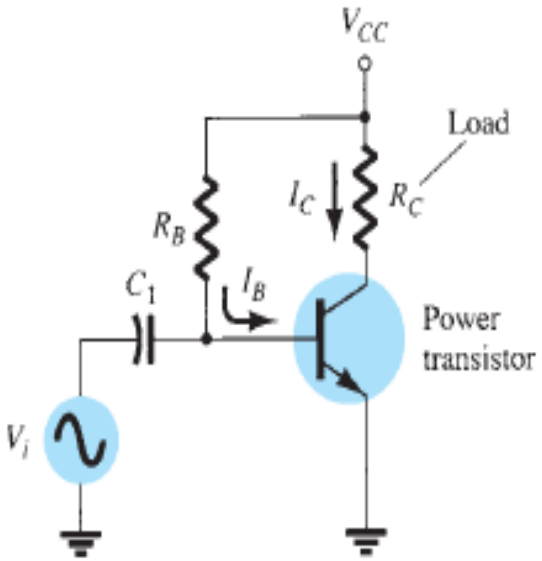


FIG. 12.2
Series-fed class A large-signal amplifier.

DC Bias Operation

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7\,\text{V}}{R_B} \tag{12.1}$$

with the collector current then being

$$I_C = \beta I_B \tag{12.2}$$

with the collector–emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C \tag{12.3}$$

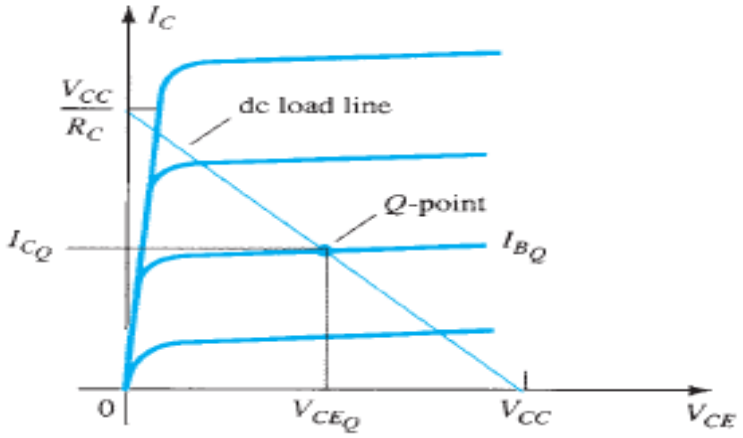


FIG. 12.3
Transistor characteristic showing load line and Q-point.

AC Operation

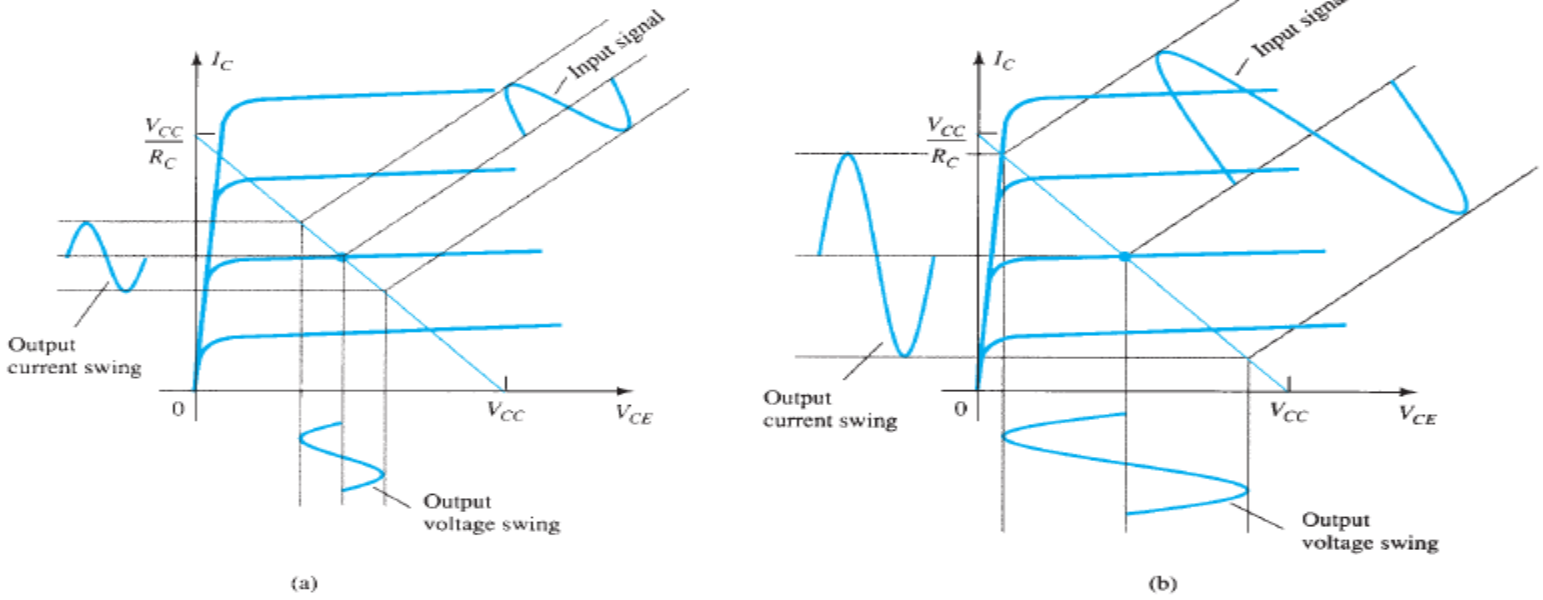


FIG. 12.4
Amplifier input and output signal variation.

Power Considerations

The power into an amplifier is provided by the supply voltage. With no input signal, the dc current drawn is the collector bias current I_{C_Q}. The power then drawn from the supply is

$$P_i(\text{dc}) = V_{CC}I_{C_Q} \tag{12.4}$$

Output Power The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load R_C in the circuit of Fig. 12.2. The ac signal V_i causes the base current to vary around the dc bias current and the collector current around its quiescent level I_{C_Q}. As shown in Fig. 12.4, the ac input signal results in ac current and ac voltage signals. The larger the input signal, the larger is the output swing, up to the maximum set by the circuit. The ac power delivered to the load (R_C) can be expressed in a number of ways.

Using RMS signals. The ac power delivered to the load (R_C) may be expressed using

$$P_o(\text{ac}) = V_{CE}(\text{rms})I_C(\text{rms}) \tag{12.5}$$

$$P_o(\text{ac}) = I_C^2(\text{rms})R_C \tag{12.6}$$

$$P_o(\text{ac}) = \frac{V_C^2(\text{rms})}{R_C} \tag{12.7}$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% \qquad \textbf{(12.8)}$$

Maximum Efficiency For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is

$$\text{maximum } V_{CE}(\text{p-p}) = V_{CC}$$

For the current swing it is

$$\text{maximum } I_C(\text{p-p}) = \frac{V_{CC}}{R_C}$$

Using the maximum voltage swing in Eq. (12.7) yields

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}(V_{CC}/R_C)}{8}$$

$$= \frac{V_{CC}^2}{8R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_C) = V_{CC}\frac{V_{CC}/R_C}{2}$$

$$= \frac{V_{CC}^2}{2R_C}$$

We can then use Eq. (12.8) to calculate the maximum efficiency:

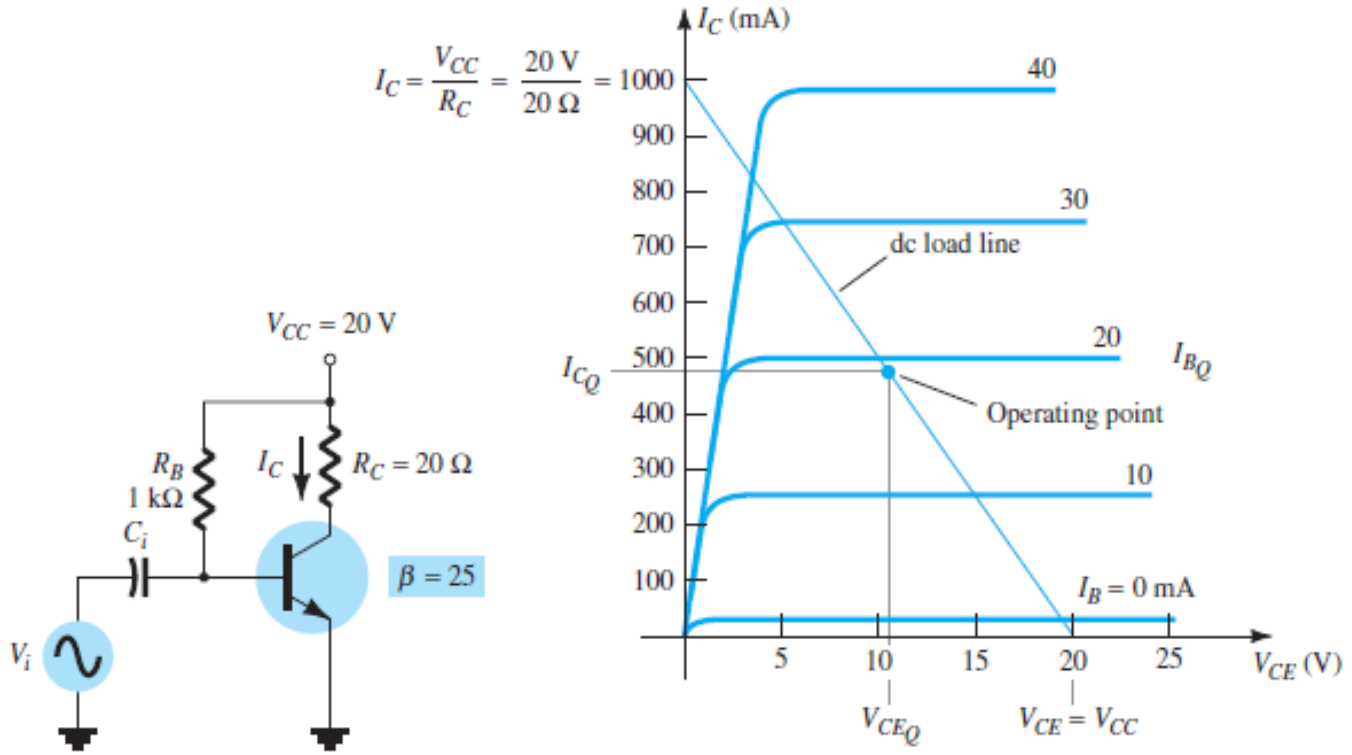
$$\text{maximum } \%\,\eta = \frac{\text{maximum } P_o(\text{ac})}{\text{maximum } P_i(\text{dc})} \times 100\%$$

$$= \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\%$$

$$= 25\%$$

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%. Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%.

EXAMPLE 12.1 Calculate the input power, output power, and efficiency of the amplifier circuit in Fig. 12.5 for an input voltage that results in a base current of 10 mA peak.



Solution: Using Eqs. (12.1) through (12.3), we can determine the Q-point to be

$$I_{B_Q} = \frac{V_{CC} - 0.7\,\text{V}}{R_B} = \frac{20\,\text{V} - 0.7\,\text{V}}{1\,\text{k}\Omega} = 19.3\,\text{mA}$$

$$I_{C_Q} = \beta I_B = 25(19.3\,\text{mA}) = 482.5\,\text{mA} \cong 0.48\,\text{A}$$

$$V_{CE_Q} = V_{CC} - I_C R_C = 20\,\text{V} - (0.48\,\Omega)(20\,\Omega) = 10.4\,\text{V}$$

This bias point is marked on the transistor collector characteristic of Fig. 12.5b. The ac variation of the output signal can be obtained graphically using the dc load line drawn on Fig. 12.5b by connecting $V_{CE} = V_{CC} = 20\,\text{V}$ with $I_C = V_{CC}/R_C = 1000\,\text{mA} = 1\,\text{A}$, as shown. When the input ac base current increases from its dc bias level, the collector current rises by

$$I_C(\text{p}) = \beta I_B(\text{p}) = 25(10\,\text{mA peak}) = 250\,\text{mA peak}$$

Using Eq. (12.6) yields

$$P_o(\text{ac}) = I_C^2(rms)R_C = \frac{I_C^2(\text{p})}{2}R_C = \frac{(250 \times 10^{-3}\,\text{A})^2}{2}(20\,\Omega) = \mathbf{0.625\,W}$$

Using Eq. (12.4) results in

$$P_i(\text{dc}) = V_{CC}I_{C_Q} = (20\,\text{V})(0.48\,\text{A}) = \mathbf{9.6\,W}$$

The amplifier's power efficiency can then be calculated using Eq. (12.8):

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.625\,\text{W}}{9.6\,\text{W}} \times 100\% = \mathbf{6.5\%}$$

TRANSFORMER-COUPLED CLASS A AMPLIFIER

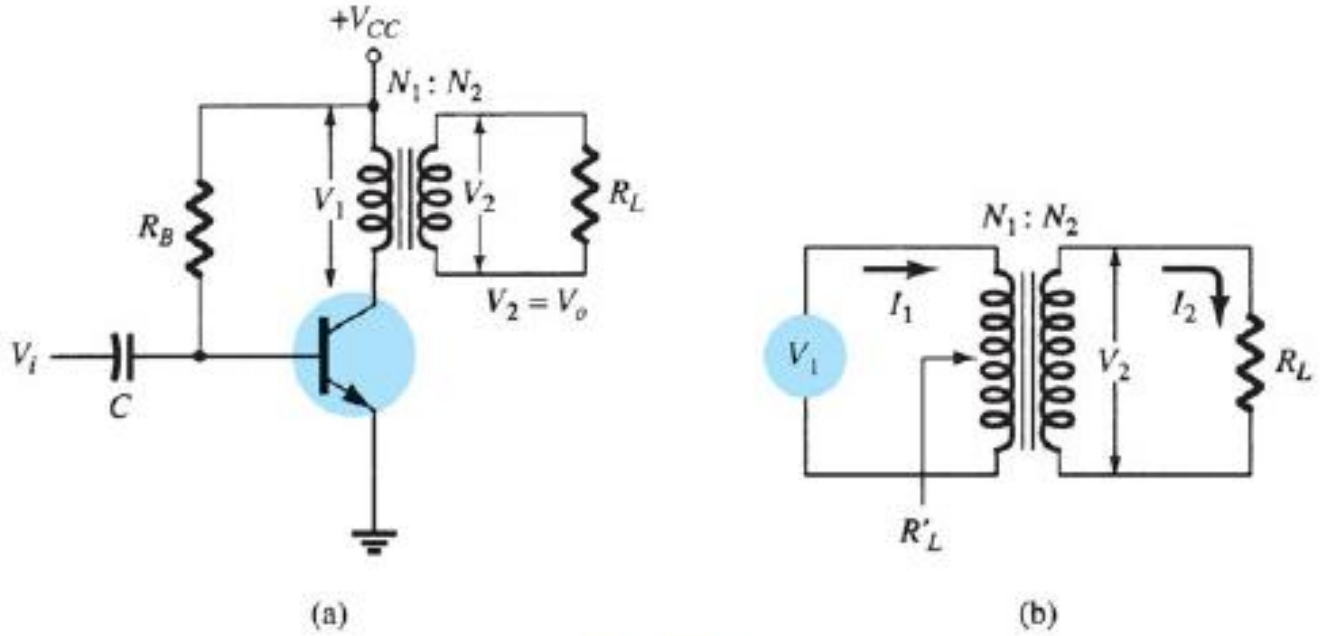


FIG. 12.6
Transformer-coupled audio power amplifier.

Transformer Action

A transformer can increase or decrease voltage or current levels according to the turns ratio, as explained below. In addition, the impedance connected to one side of a transformer can be made to appear either larger or smaller (step up or step down) at the other side of the transformer, depending on the square of the transformer winding turns ratio. The following discussion assumes ideal (100%) power transfer from primary to secondary, that is, no power losses are considered.

Voltage Transformation As shown in Fig. 12.7a, the transformer can step up or step down a voltage applied to one side directly as the ratio of the turns (or number of windings) on each side. The voltage transformation is given by

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} \tag{12.9}$$

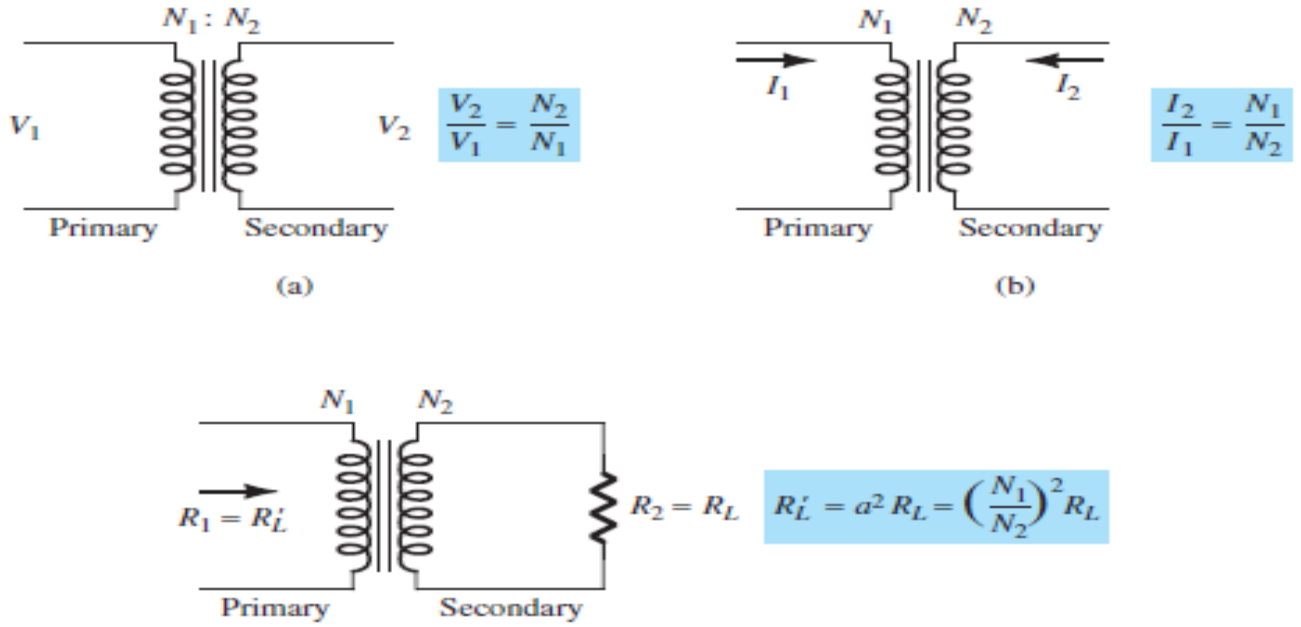
Equation (12.9) shows that if the number of turns of wire on the secondary side is larger than the number on the primary, the voltage at the secondary side is larger than the voltage at the primary side.

Current Transformation The current in the secondary winding is inversely proportional to the number of turns in the windings. The current transformation is given by

$$\frac{I_2}{I_1} = \frac{N_1}{N_2} \tag{12.10}$$

Impedance Transformation Since the voltage and current can be changed by a transformer, an impedance "seen" from either side (primary or secondary) can also be changed. As shown in Fig. 12.7c, an impedance R_L is connected across the transformer secondary. This impedance is changed by the transformer when viewed at the primary side (R'_L). This can be shown as follows:

$$\frac{R_L}{R'_L} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2\,I_1}{I_2\,V_1} = \frac{V_2 I_1}{V_1 I_2} = \frac{N_2 N_2}{N_1 N_1} = \left(\frac{N_2}{N_1}\right)^2$$



$\frac{V_2}{V_1} = \frac{N_2}{N_1}$

$\frac{I_2}{I_1} = \frac{N_1}{N_2}$

$R'_L = a^2 R_L = \left(\frac{N_1}{N_2}\right)^2 R_L$

FIG. 12.7

Transformer operation: (a) voltage transformation; (b) current transformation; (c) impedance transformation.

If we define $a = N_1/N_2$, where a is the turns ratio of the transformer, the above equation becomes

$$\boxed{\frac{R'_L}{R_L} = \frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2 = a^2} \qquad \textbf{(12.11)}$$

We can express the load resistance reflected to the primary side as

$$\boxed{R_1 = a^2 R_2} \quad \text{or} \quad \boxed{R'_L = a^2 R_L} \qquad \textbf{(12.12)}$$

where R'_L is the reflected impedance. As shown in Eq. (12.12), the reflected impedance is related directly to the square of the turns ratio. If the number of turns of the secondary is smaller than that of the primary, the impedance seen looking into the primary is larger than that of the secondary by the square of the turns ratio.

Operation of Amplifier Stage

TR

DC Load Line The transformer (dc) winding resistance determines the dc load line for the circuit of Fig. 12.6. Typically, this dc resistance is small (ideally 0 Ω) and, as shown in Fig. 12.8, a 0-Ω dc load line is a straight vertical line. A practical transformer winding resistance would be a few ohms, but only the ideal case will be considered in this discussion. There is no dc voltage drop across the 0-Ω dc load resistance, and the load line is drawn straight vertically from the voltage point, $V_{CE_Q} = V_{CC}$.

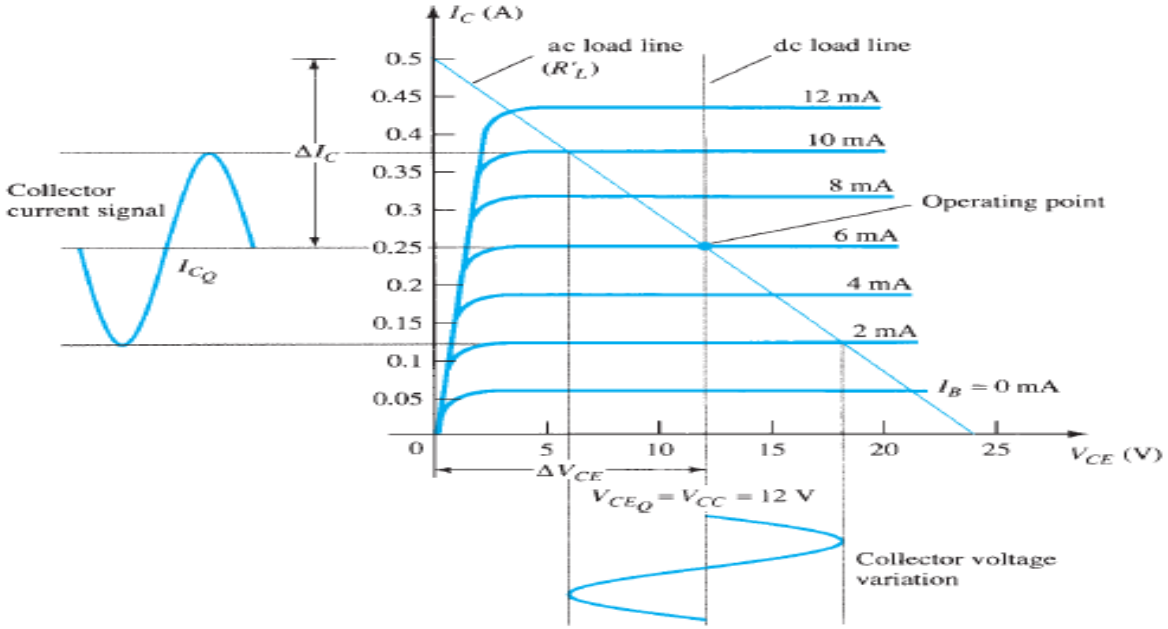


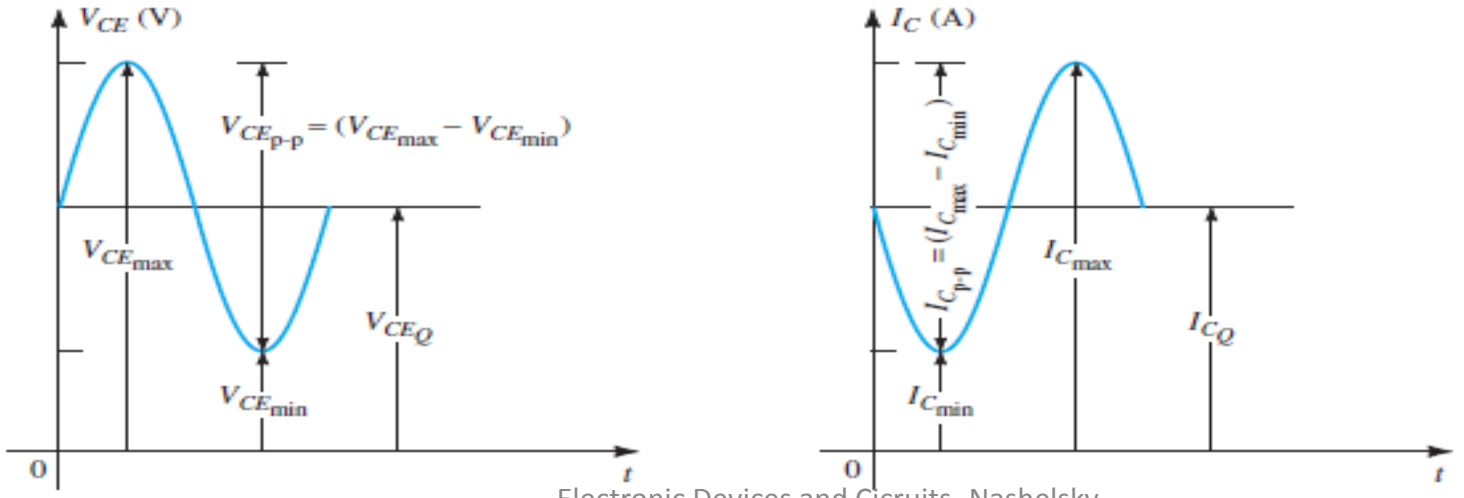
FIG. 12.8
Load lines for class A transformer-coupled amplifier.

Quiescent Operating Point The operating point in the characteristic curve of Fig.12.8 can be obtained graphically at the point of intersection of the dc load line and the base current set by the circuit. The collector quiescent current can then be obtained from the operating point. In class A operation, keep in mind that the dc bias point sets the conditions for the maximum undistorted signal swing for both collector current and collector–emitter voltage. If the input signal produces a voltage swing less than the maximum possible, the efficiency of the circuit at that time will be less than the maximum of 50%. The dc bias point is therefore important in setting the operation of a class A series-fed amplifier.

AC Load Line To carry out ac analysis, it is necessary to calculate the ac load resistance "seen" looking into the primary side of the transformer, then draw the ac load line on the collector characteristic. The reflected load resistance (R_L') is calculated using Eq. (12.12) using the value of the load connected across the secondary (R_L) and the turns ratio of the transformer. The graphical analysis technique then proceeds as follows. Draw the ac load line so that it passes through the operating point and has a slope equal to $-1/R_L'$ (the reflected load resistance), the load line slope being the negative reciprocal of the ac load resistance. Notice that the ac load line shows that the output signal swing can exceed the value of V_{CC}. In fact, the voltage developed across the transformer primary can be quite large. It is therefore necessary after obtaining the ac load line to check that the possible voltage swing does not exceed transistor maximum ratings.

Signal Swing and Output AC Power Figure 12.9 shows the voltage and current signal swings from the circuit of Fig. 12.6. From the signal variations shown in Fig. 12.9, the values of the peak-to-peak signal swings are

$$V_{CE}(\text{p-p}) = V_{CE_{max}} - V_{CE_{min}}$$
$$I_C(\text{p-p}) = I_{C_{max}} - I_{C_{min}}$$



The ac power developed across the transformer primary can then be calculated using

$$P_o(\text{ac}) = \frac{(V_{CE_{\max}} - V_{CE_{\min}})(I_{C_{\max}} - I_{C_{\min}})}{8} \tag{12.13}$$

The ac power calculated is that developed across the primary of the transformer. Assuming an ideal transformer (a highly efficient transformer has an efficiency of well over 90%), we find that the power delivered by the secondary to the load is approximately that calculated using Eq. (12.13). The output ac power can also be determined using the voltage delivered to the load.

For the ideal transformer, the voltage delivered to the load can be calculated using Eq. (12.9):

$$V_L = V_2 = \frac{N_2}{N_1} V_1$$

The power across the load can then be expressed as

$$P_L = \frac{V_L^2(\text{rms})}{R_L}$$

and equals the power calculated using Eq. (12.5c).

Using Eq. (12.10) to calculate the load current yields

$$I_L = I_2 = \frac{N_1}{N_2} I_C$$

with the output ac power then calculated using

$$P_L = I_L^2(\text{rms}) R_L$$

Efficiency

The input (dc) power obtained from the supply is calculated from the supply dc voltage and the average power drawn from the supply:

$$P_i(\text{dc}) = V_{CC}I_{C_Q} \tag{12.14}$$

Thus the only power loss considered here is that dissipated by the power transistor and calculated using

$$P_Q = P_i(\text{dc}) - P_o(\text{ac}) \tag{12.15}$$

EXAMPLE 12.5 For the circuit of Fig. 12.10 and results of Example 12.4, calculate the dc input power, power dissipated by the transistor, and efficiency of the circuit for the input signal of Example 12.4.

Solution: Eq. (12.14):

$$P_i(\text{dc}) = V_{CC}I_{C_Q} = (10\text{ V})(140\text{ mA}) = \mathbf{1.4\text{ W}}$$

Eq. (12.15):

$$P_Q = P_i(\text{dc}) - P_o(\text{ac}) = 1.4\text{ W} - 0.477\text{ W} = \mathbf{0.92\text{ W}}$$

The efficiency of the amplifier is then

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.477\text{ W}}{1.4\text{ W}} \times 100\% = \mathbf{34.1\%}$$

Maximum Theoretical Efficiency For a class A transformer-coupled amplifier, the maximum theoretical efficiency goes up to 50%. Based on the signals obtained using the amplifier, the efficiency can be expressed as

$$\%\,\eta = 50\left(\frac{V_{CE_{max}} - V_{CE_{min}}}{V_{CE_{max}} + V_{CE_{min}}}\right)^2\% \qquad \textbf{(12.16)}$$

The larger the value of $V_{CE_{max}}$ and the smaller the value of $V_{CE_{min}}$, the closer the efficiency approaches the theoretical limit of 50%.

EXAMPLE 12.6 Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 12 V and outputs of:

a. $V(\text{p}) = 12\text{ V}$.
b. $V(\text{p}) = 6\text{ V}$.
c. $V(\text{p}) = 2\text{ V}$.

Solution:

a. Since $V_{CE_Q} = V_{CC} = 12\text{ V}$, the maximum and minimum of the voltage swing are, respectively,

$$V_{CE_{max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 12\text{ V} = 24\text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 12\text{ V} = 0\text{ V}$$

resulting in

$$\%\,\eta = 50\left(\frac{24\text{ V} - 0\text{ V}}{24\text{ V} + 0\text{ V}}\right)^2\% = \mathbf{50\%}$$

b.

$$V_{CE_{max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 6\text{ V} = 18\text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 6\text{ V} = 6\text{ V}$$

resulting in

$$\%\,\eta = 50\left(\frac{18\text{ V} - 6\text{ V}}{18\text{ V} + 6\text{ V}}\right)^2\% = \mathbf{12.5\%}$$

c.

$$V_{CE_{max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 2\text{ V} = 14\text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 2\text{ V} = 10\text{ V}$$

Poac = $\frac{Vcc^2}{2R'_L}$ (2)

Similarly, Pindc = Vcc × Icq

Since Q-point is located in middle of ac load line , Icq = Iop

Pindc = $\frac{Vcc^2}{R'_L}$ (3)

Hence efficiency is given by,

From equation (2) & (3),

$\eta(max)\% = \frac{Poac}{Pindc} \times 100$

$\eta(max)\% = \frac{Vcc^2}{2R'_L} \times \frac{R'_L}{Vcc^2} \times 100$

η(max) = 50%

$$\%\,\eta = 50\left(\frac{14\,\text{V} - 10\,\text{V}}{14\,\text{V} + 10\,\text{V}}\right)^2\% = 1.39\%$$

CLASS B AMPLIFIER OPERATION

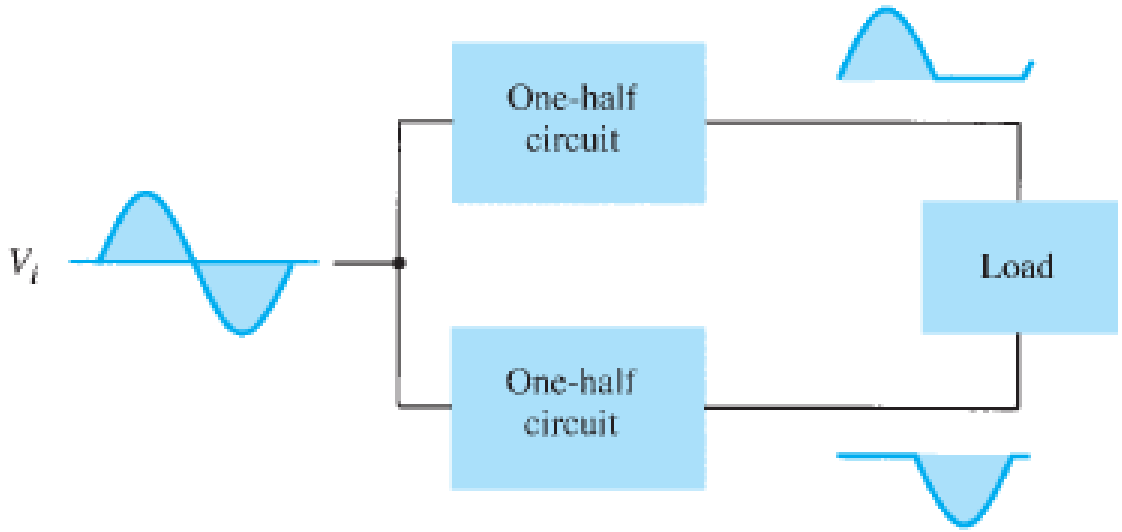


FIG. 12.12
Block representation of push–pull operation.

Input (DC) Power

The power supplied to the load by an amplifier is drawn from the power supply (or power supplies; see Fig. 12.13) that provides the input or dc power. The amount of this input power can be calculated using

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} \tag{12.17}$$

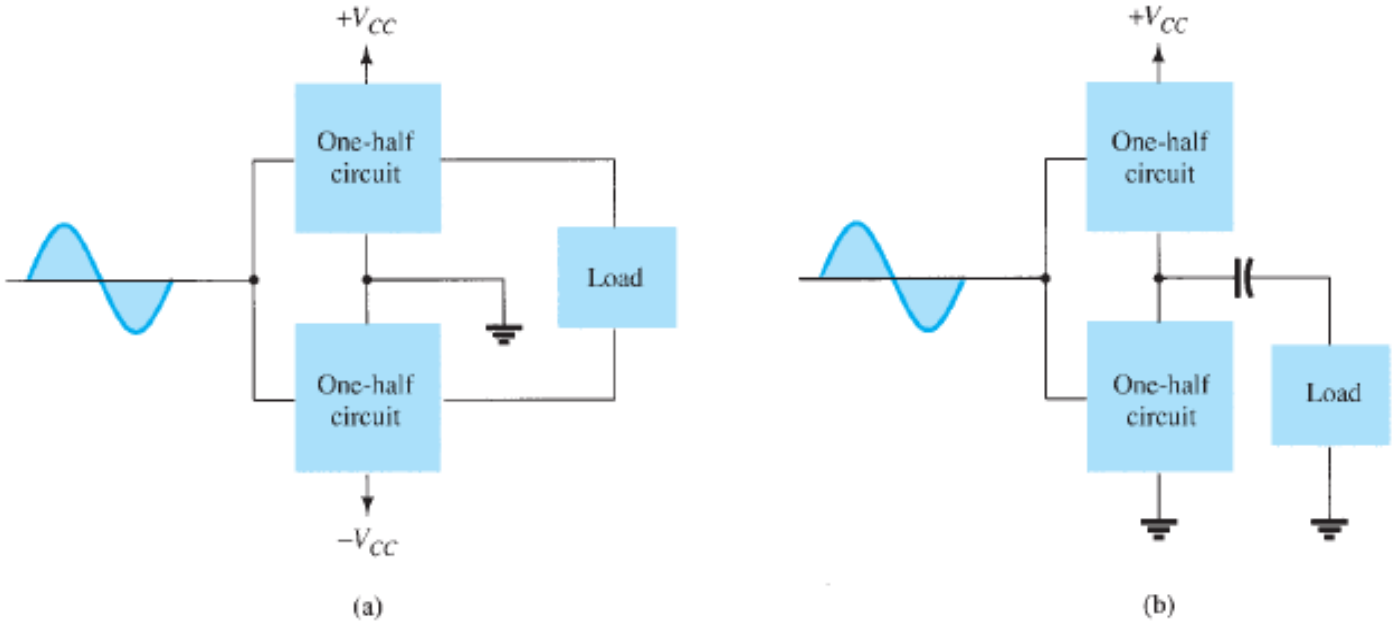


FIG. 12.13

Connection of push–pull amplifier to load: (a) using two voltage supplies; (b) using one voltage supply.

$$I_{dc} = \frac{2}{\pi} I(\text{p})$$

where $I(\text{p})$ is the peak value of the output current waveform. Using Eq. (12.18) in the power input equation (12.17) results in

$$P_i(\text{dc}) = V_{CC}\left(\frac{2}{\pi} I(\text{p})\right) \tag{12.19}$$

Output (AC) Power

The power delivered to the load (usually referred to as a resistance R_L) can be calculated using any one of a number of equations. If one is using an rms meter to measure the voltage across the load, the output power can be calculated as

$$P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L} \tag{12.20}$$

If one is using an oscilloscope, the measured peak or peak-to-peak output voltage can be used:

$$P_o(\text{ac}) = \frac{V_L^2(\text{p-p})}{8R_L} = \frac{V_L^2(\text{p})}{2R_L} \tag{12.21}$$

The larger the rms or peak output voltage, the larger is the power delivered to the load.

Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation

$$\% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Using Eqs. (12.19) and (12.21) in the efficiency equation above results in

$$\% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)I(\text{p})]} \times 100\% = \frac{\pi}{4}\frac{V_L(\text{p})}{V_{CC}} \times 100\% \quad \textbf{(12.22)}$$

[using $I(\text{p}) = V_L(\text{p})/R_L$]. Equation (12.22) shows that the larger the peak voltage, the higher is the circuit efficiency, up to a maximum value when $V_L(\text{p}) = V_{CC}$, this maximum efficiency then being

$$\text{maximum efficiency} = \frac{\pi}{4} \times 100\% = 78.5\%$$

Power Dissipated by Output Transistors The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load,

$$P_{2Q} = P_i(\text{dc}) - P_o(\text{ac}) \quad \textbf{(12.23)}$$

where P_{2Q} is the power dissipated by the two output power transistors. The dissipated power handled by each transistor is then

$$P_Q = \frac{P_{2Q}}{2} \tag{12.24}$$

EXAMPLE 12.7 For a class B amplifier providing a 20-V peak signal to a 16-Ω load (speaker) and a power supply of $V_{CC} = 30$ V, determine the input power, output power, and circuit efficiency.

Solution: A 20-V peak signal across a 16-Ω load provides a peak load current of

$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{20\text{ V}}{16\ \Omega} = 1.25\text{ A}$$

The dc value of the current drawn from the power supply is then

$$I_{\text{dc}} = \frac{2}{\pi} I_L(\text{p}) = \frac{2}{\pi}(1.25\text{ A}) = 0.796\text{ A}$$

and the input power delivered by the supply voltage is

$$P_i(\text{dc}) = V_{CC} I_{\text{dc}} = (30\text{ V})(0.796\text{ A}) = \mathbf{23.9\text{ W}}$$

The output power delivered to the load is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(20\text{ V})^2}{2(16\ \Omega)} = \mathbf{12.5\text{ W}}$$

for a resulting efficiency of

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{12.5\text{ W}}{23.9\text{ W}} \times 100\% = \mathbf{52.3\%}$$

Maximum Power Considerations

For class B operation, the maximum output power is delivered to the load when $V_L(\text{p}) = V_{CC}$:

$$\boxed{\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L}} \tag{12.25}$$

The corresponding peak ac current $I(\text{p})$ is then

$$I(\text{p}) = \frac{V_{CC}}{R_L}$$

so that the maximum value of average current from the power supply is

$$\text{maximum } I_{\text{dc}} = \frac{2}{\pi} I(\text{p}) = \frac{2V_{CC}}{\pi R_L}$$

Using this current to calculate the maximum value of input power results in

$$\boxed{\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_{\text{dc}}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L}} \tag{12.26}$$

The maximum circuit efficiency for class B operation is then

$$\text{maximum } \%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_{CC}^2/2R_L}{V_{CC}[(2/\pi)(V_{CC}/R_L)]} \times 100\%$$

$$= \frac{\pi}{4} \times 100\% = \mathbf{78.54\%} \tag{12.27}$$

For class B operation, the maximum power dissipated by the output transistors does not occur at the maximum power input or output condition. The maximum power dissipated by the two output transistors occurs when the output voltage across the load is

$$V_L(\text{p}) = 0.636V_{CC} \qquad \left(= \frac{2}{\pi}V_{CC}\right)$$

for a maximum transistor power dissipation of

$$\boxed{\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}} \tag{12.28}$$

The maximum efficiency of a class B amplifier can also be expressed as follows:

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L}$$

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} = V_{CC}\left[\frac{2V_L(\text{p})}{\pi R_L}\right]$$

so that

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)(V_L(\text{p})/R_L)]} \times 100\%$$

$$\%\,\eta = 78.54\frac{V_L(\text{p})}{V_{CC}}\% \tag{12.29}$$

EXAMPLE 12.9 Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 24$ V with peak output voltages of:

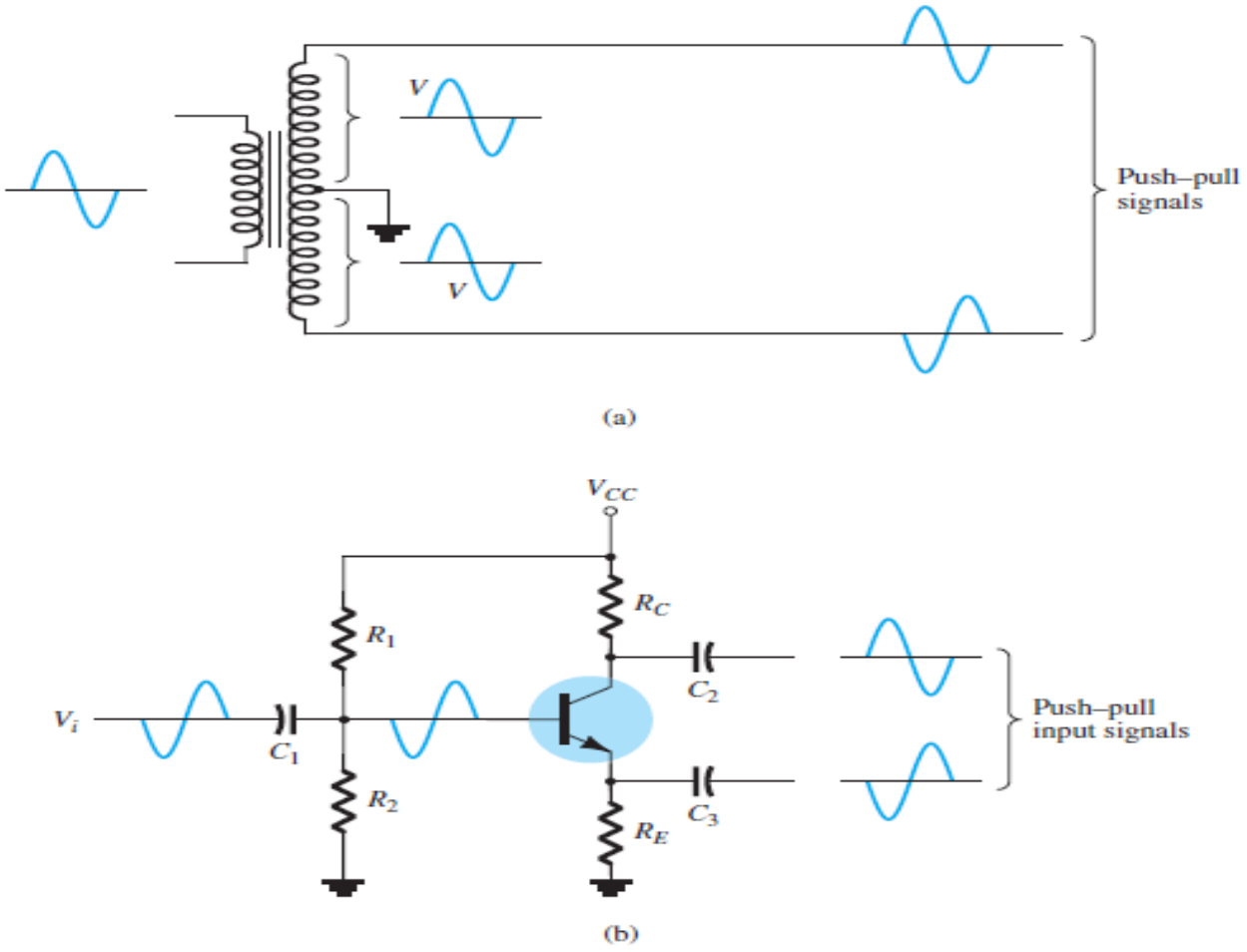
a. $V_L(\text{p}) = 22$ V.
b. $V_L(\text{p}) = 6$ V.

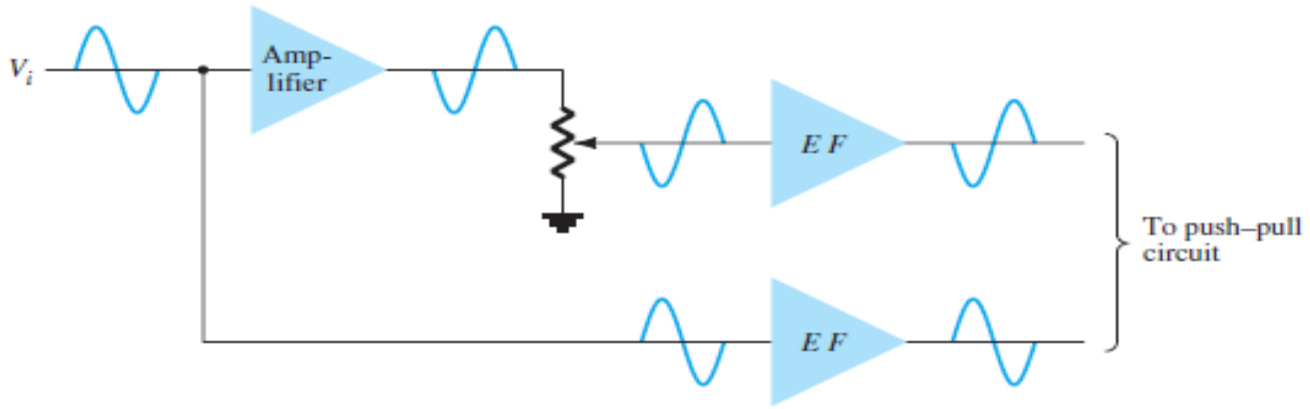
Solution: Using Eq. (12.29) gives

a. $\%\,\eta = 78.54\frac{V_L(\text{p})}{V_{CC}}\% = 78.54\left(\frac{22\text{ V}}{24\text{ V}}\right) = \mathbf{72\%}$

b. $\%\,\eta = 78.54\left(\frac{6\text{ V}}{24\text{ V}}\right)\% = \mathbf{19.6\%}$

CLASS B AMPLIFIER CIRCUITS



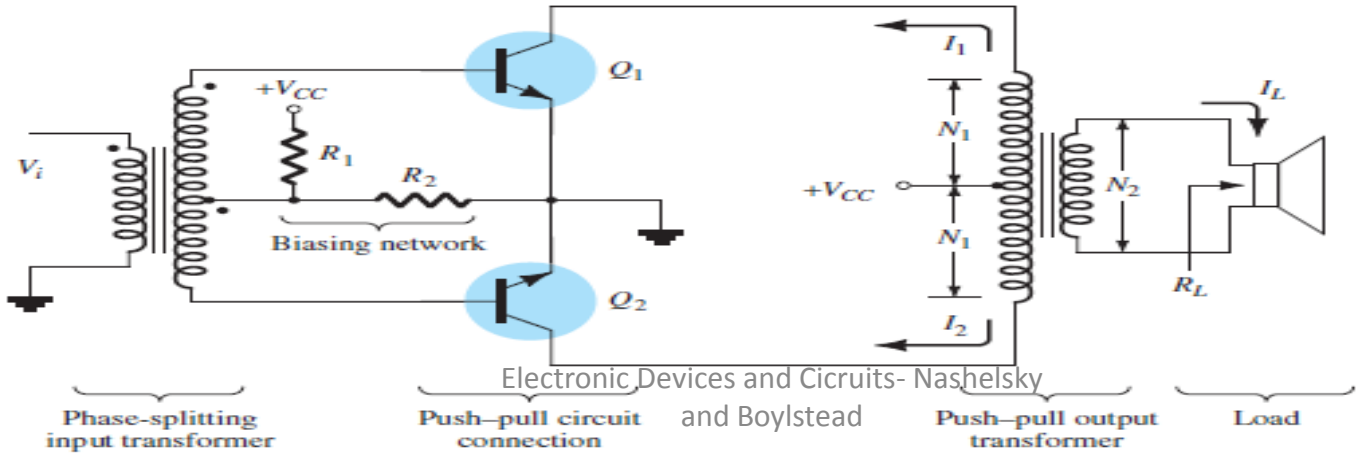


(c)

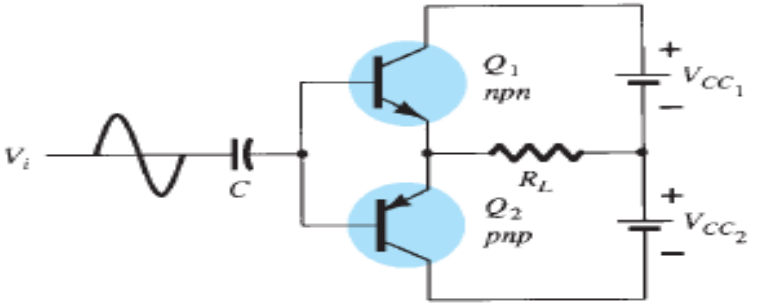
Transformer-Coupled Push–Pull Circuits

The circuit of Fig. 12.15 uses a center-tapped input transformer to produce opposite-polarity signals to the two transistor inputs and an output transformer to drive the load in a push–pull mode of operation described next.

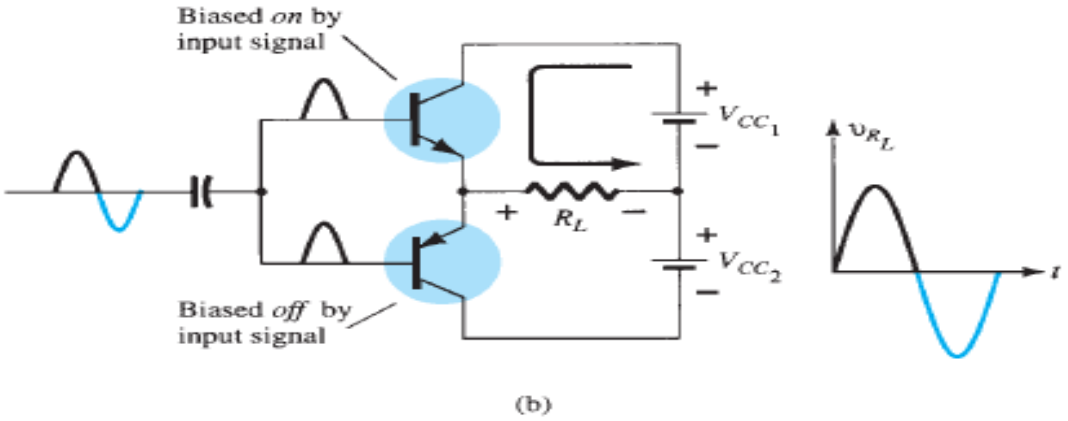
During the first half-cycle of operation, transistor Q_1 is driven into conduction, whereas transistor Q_2 is driven off. The current I_1 through the transformer results in the first half-cycle of signal to the load. During the second half-cycle of the input signal, Q_2 conducts, whereas Q_1 stays off, the current I_2 through the transformer resulting in the second half-cycle to the load. The overall signal developed across the load then varies over the full cycle of signal operation.



Complementary-Symmetry Circuits



(a)



(b)

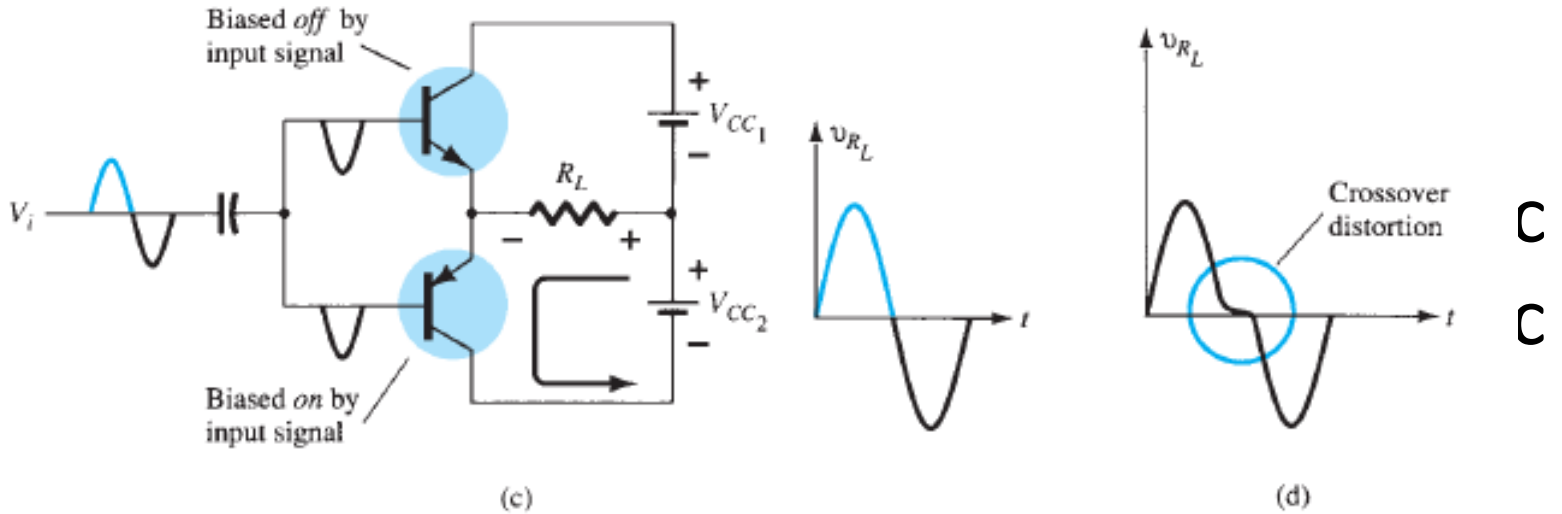


FIG. 12.16
Complementary-symmetry push–pull circuit.

Quasi-Complementary Push–Pull Amplifier

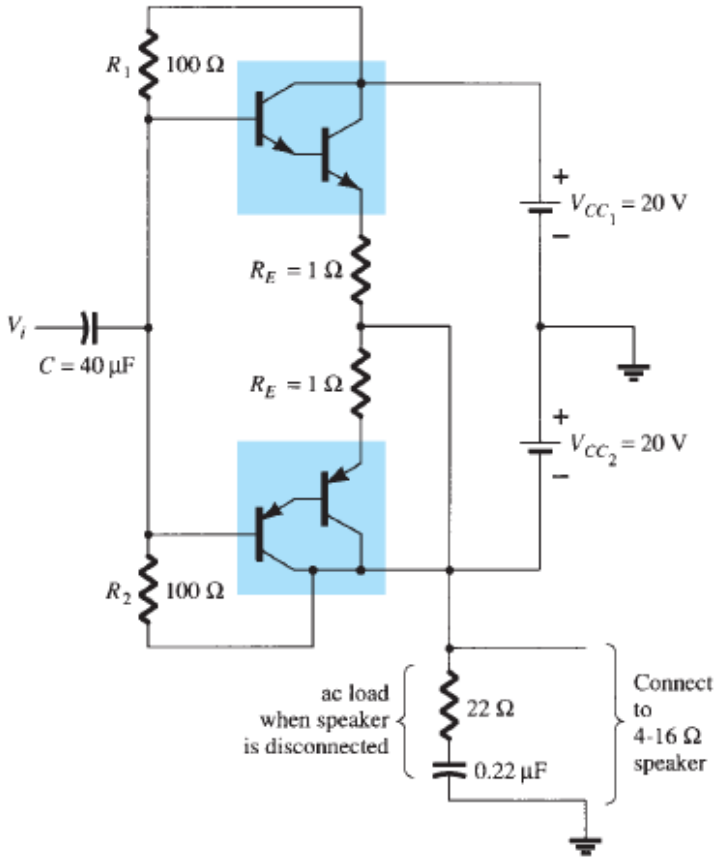


FIG. 12.17
Complementary-symmetry push–pull circuit using Darlington transistors.

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quasi-complementary circuit, as shown in Fig. 12.18. The push–pull operation is achieved by using complementary transistors (Q_1 and Q_2) before the matched *npn* output transistors (Q_3 and Q_4). Notice that transistors Q_1 and Q_3 form a Darlington connection that provides output from a low-impedance emitter-follower. The connection of transistors Q_2 and Q_4 forms a feedback pair, which similarly provides a low-impedance drive to the load. Resistor

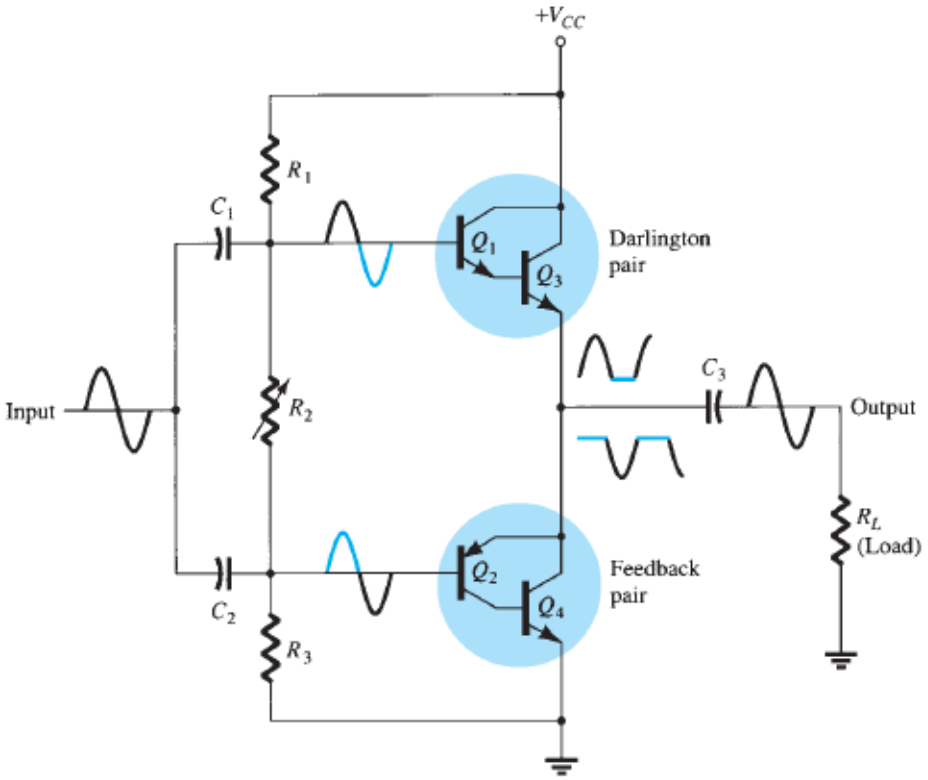


FIG. 12.18
Quasi-complementary push–pull transformerless power amplifier.

AMPLIFIER DISTORTION

A pure sinusoidal signal has a single frequency at which the voltage varies positive and negative by equal amounts. Any signal varying over less than the full 360° cycle is considered to have distortion. An ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version, the resulting waveform being a pure single-frequency sinusoidal signal. When distortion occurs, the output will not be an exact duplicate (except for magnitude) of the input signal.

Distortion can occur because the device characteristic is not linear, in which case nonlinear or amplitude distortion occurs. This can occur with all classes of amplifier operation. Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

One technique for describing distorted but period waveforms uses Fourier analysis, a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples—these components are called *harmonic components* or *harmonics*. For example, a signal that is originally 1000 Hz could result, after distortion, in a frequency component at 1000 Hz (1 kHz) and harmonic components at 2 kHz (2 × 1 kHz), 3 kHz (3 × 1 kHz), 4 kHz (4 × 1 kHz), and so on. The original frequency of 1 kHz is called the *fundamental frequency*; those at integer multiples are the *harmonics*. The 2-kHz component is therefore called a *second harmonic*, that at 3 kHz is the *third harmonic*, and so on. The fundamental frequency is not considered a harmonic. Fourier analysis does not allow for fractional harmonic frequencies—only integer multiples of the fundamental.

Harmonic Distortion

A signal is considered to have harmonic distortion when there are harmonic frequency components (not just the fundamental component). If the fundamental frequency has an amplitude A_1 and the nth frequency component has an amplitude A_n, a harmonic distortion can be defined as

$$\%\ n\text{th harmonic distortion} = \%\ D_n = \frac{|A_n|}{|A_1|} \times 100\%$$

The fundamental component is typically larger than any harmonic component.

Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V, and fourth harmonic amplitude of 0.05 V.

Solution: Using Eq. (12.30) yields

$$\%\ D_2 = \frac{|A_2|}{|A_1|} \times 100\% = \frac{0.25\ \text{V}}{2.5\ \text{V}} \times 100\% = \mathbf{10\%}$$

$$\%\ D_3 = \frac{|A_3|}{|A_1|} \times 100\% = \frac{0.1\ \text{V}}{2.5\ \text{V}} \times 100\% = \mathbf{4\%}$$

$$\%\ D_4 = \frac{|A_4|}{|A_1|} \times 100\% = \frac{0.05\ \text{V}}{2.5\ \text{V}} \times 100\% = \mathbf{2\%}$$

Total Harmonic Distortion When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based on the individual elements as combined by the relationship of the following equation:

$$\%\,\text{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\%$$

where THD is total harmonic distortion.

Calculate the total harmonic distortion for the amplitude components given in Example 12.13.

Solution: Using the computed values of $D_2 = 0.10$, $D_3 = 0.04$, and $D_4 = 0.02$ in Eq. (12.31), we obtain

$$\begin{aligned}\%\,\text{THD} &= \sqrt{D_2^2 + D_3^2 + D_4^2} \times 100\% \\ &= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100\% = 0.1095 \times 100\% \\ &= \mathbf{10.95\%}\end{aligned}$$

An instrument such as a spectrum analyzer would allow measurement of the harmonics present in the signal by providing a display of the fundamental component of a signal and a number of its harmonics on a display screen. Similarly, a wave analyzer instrument allows more precise measurement of the harmonic components of a distorted signal by filtering out each of these components and providing a reading of these components. In any case, the technique of considering any distorted signal as containing a fundamental component and harmonic components is practical and useful. For a signal occurring in class AB or class B, the distortion may be mainly even harmonics, of which the second harmonic component is the largest. Thus, although the distorted signal theoretically contains all harmonic components from the second harmonic up, the most important in terms of the amount of distortion in the classes presented above is the second harmonic.

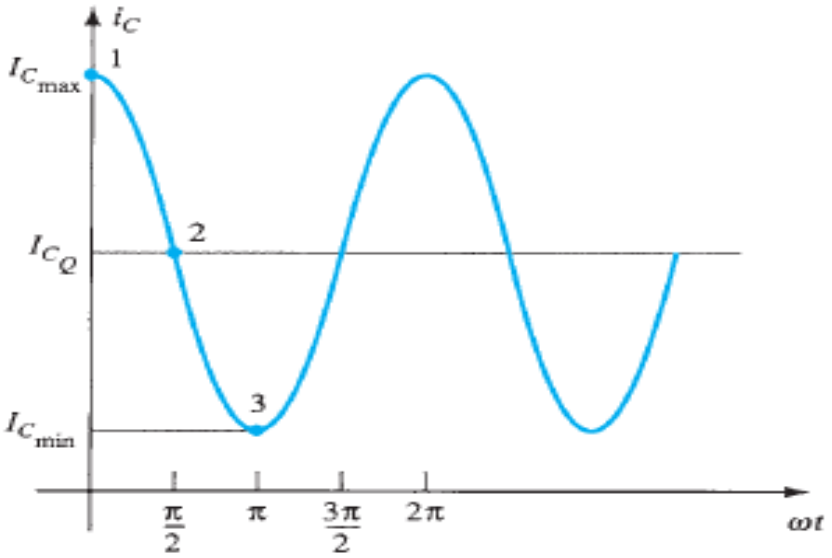


FIG. 12.20
Waveform for obtaining second harmonic distortion.

Second Harmonic Distortion Figure 12.20 shows a waveform to use for obtaining second harmonic distortion. A collector current waveform is shown with the quiescent, minimum, and maximum signal levels, and the time at which they occur is marked on the waveform. The signal shown indicates that some distortion is present. An equation that approximately describes the distorted signal waveform is

$$i_C \approx I_{C_Q} + I_0 + I_1 \cos \omega t + I_2 \cos \omega t \qquad \textbf{(12.32)}$$

The current waveform contains the original quiescent current I_{C_Q}, which occurs with zero input signal; an additional dc current I_0, due to the nonzero average of the distorted signal; the fundamental component of the distorted ac signal I_1; and a second harmonic component I_2, at twice the fundamental frequency. Although other harmonics are also present, only the second is considered here. Equating the resulting current from Eq. (12.32) at a few points in the cycle to that shown on the current waveform provides the following three relations:

At point 1 ($\omega t = 0$),

$$i_C = I_{C_{max}} = I_{C_Q} + I_0 + I_1 \cos 0 + I_2 \cos 0$$
$$I_{C_{max}} = I_{C_Q} + I_0 + I_1 + I_2$$

At point 2 ($\omega t = \pi/2$),

$$i_C = I_{C_Q} = I_{C_Q} + I_0 + I_1 \cos \frac{\pi}{2} + I_2 \cos \frac{2\pi}{2}$$
$$I_{C_Q} = I_{C_Q} + I_0 - I_2$$

At point 3 ($\omega t = \pi$),

$$i_C = I_{C_{min}} = I_{C_Q} + I_0 + I_1 \cos \pi + I_2 \cos 2\pi$$
$$I_{C_{min}} = I_{C_Q} + I_0 - I_1 + I_2$$

Solving the preceding three equations simultaneously gives the following results:

$$I_0 = I_2 = \frac{I_{C_{max}} + I_{C_{min}} - 2I_{C_Q}}{4}, \qquad I_1 = \frac{I_{C_{max}} - I_{C_{min}}}{2}$$

Referring to Eq. (12.30), we can express the definition of second harmonic distortion as

$$D_2 = \left|\frac{I_2}{I_1}\right| \times 100\%$$

Inserting the values of I_1 and I_2 determined above gives

$$D_2 = \left|\frac{\frac{1}{2}(I_{C_{max}} + I_{C_{min}}) - I_{C_Q}}{I_{C_{max}} - I_{C_{min}}}\right| \times 100\% \qquad \textbf{(12.33)}$$

In a similar manner, the second harmonic distortion can be expressed in terms of measured collector–emitter voltages:

$$D_2 = \left|\frac{\frac{1}{2}(V_{CE_{max}} + V_{CE_{min}}) - V_{CE_Q}}{V_{CE_{max}} - V_{CE_{min}}}\right| \times 100\% \qquad \textbf{(12.34)}$$

Calculate the second harmonic distortion if an output waveform displayed on an oscilloscope provides the following measurements:

a. $V_{CE_{min}} = 1\text{ V}, V_{CE_{max}} = 22\text{ V}, V_{CE_Q} = 12\text{ V}.$
b. $V_{CE_{min}} = 4\text{ V}, V_{CE_{max}} = 20\text{ V}, V_{CE_Q} = 12\text{ V}.$

Solution: Using Eq. (12.34), we get

a. $$D_2 = \left|\frac{\frac{1}{2}(22\text{ V} + 1\text{ V}) - 12\text{ V}}{22\text{ V} - 1\text{ V}}\right| \times 100\% = \mathbf{2.38\%}$$

b. $$D_2 = \left|\frac{\frac{1}{2}(20\text{ V} + 4\text{ V}) - 12\text{ V}}{20\text{ V} - 4\text{ V}}\right| \times 100\% = \mathbf{0\%} \qquad \text{(no distortion)}$$

Power of a Signal Having Distortion

When distortion does occur, the output power calculated for the undistorted signal is no longer correct. When distortion is present, the output power delivered to the load resistor R_C due to the fundamental component of the distorted signal is

$$P_1 = \frac{I_1^2 R_C}{2} \tag{12.35}$$

The total power due to all the harmonic components of the distorted signal can then be calculated using

$$P = (I_1^2 + I_2^2 + I_3^2 + \cdots)\frac{R_C}{2} \tag{12.36}$$

The total power can also be expressed in terms of the total harmonic distortion,

$$P = (1 + D_2^2 + D_3^2 + \cdots)I_1^2\frac{R_C}{2} = (1 + \text{THD}^2)P_1 \tag{12.37}$$

EXAMPLE 12.16 For a harmonic distortion reading of $D_2 = 0.1$, $D_3 = 0.02$, and $D_4 = 0.01$, with $I_1 = 4$ A and $R_C = 8\ \Omega$, calculate the total harmonic distortion, fundamental power component, and total power.

Solution: The total harmonic distortion is

$$\text{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2} = \sqrt{(0.1)^2 + (0.02)^2 + (0.01)^2} \approx \mathbf{0.1}$$

The fundamental power, using Eq. (12.35), is

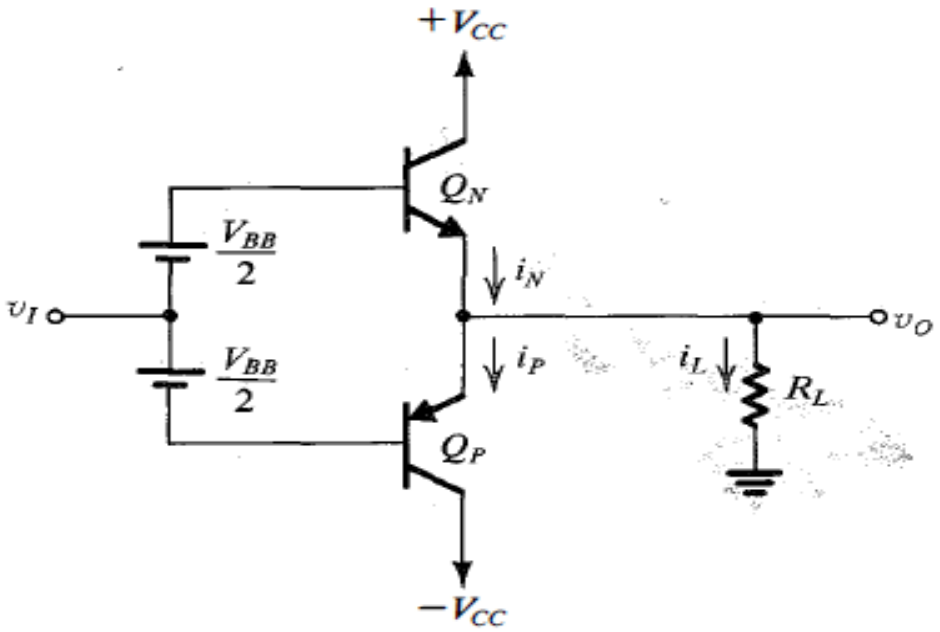
$$P_1 = \frac{I_1^2 R_C}{2} = \frac{(4\text{ A})^2(8\ \Omega)}{2} = \mathbf{64\text{ W}}$$

The total power calculated using Eq. (12.37) is then

$$P = (1 + \text{THD}^2)P_1 = [1 + (0.1)^2]64 = (1.01)64 = \mathbf{64.64\text{ W}}$$

CLASS AB OUTPUT STAGE

Crossover distortion can be virtually eliminated by biasing the complementary output transistors at a small nonzero current. The result is the class AB output stage shown in Fig. 14.11. A bias voltage V_{BB} is applied between the bases of Q_N and Q_P. For $v_I = 0$, $v_O = 0$, and a voltage $V_{BB}/2$ appears across the base–emitter junction of each of Q_N and Q_P. Assuming



matched devices,

$$i_N = i_P = I_Q = I_S e^{V_{BB}/2V_T}$$

The value of V_{BB} is selected to yield the required quiescent current I_Q.

Circuit Operation

When v_I goes positive by a certain amount, the voltage at the base of Q_N increases by the same amount and the output becomes positive at an almost equal value,

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN} \tag{14.24}$$

The positive v_O causes a current i_L to flow through R_L, and thus i_N must increase; that is,

$$i_N = i_P + i_L \tag{14.25}$$

The increase in i_N will be accompanied by a corresponding increase in v_{BEN} (above the quiescent value of $V_{BB}/2$). However, since the voltage between the two bases remains constant at V_{BB}, the increase in v_{BEN} will result in an equal decrease in v_{EBP} and hence in i_P. The relationship between i_N and i_P can be derived as follows:

$$v_{BEN} + v_{EBP} = V_{BB}$$

$$V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S}$$

$$i_N i_P = I_Q^2 \tag{14.26}$$

Thus, as i_N increases, i_P decreases by the same ratio while the product remains constant. Equations (14.25) and (14.26) can be combined to yield i_N for a given i_L as the solution to the quadratic equation

$$i_N^2 - i_L i_N - I_Q^2 = 0 \tag{14.27}$$

From the equations above, we can see that for positive output voltages, the load current is supplied by Q_N, which acts as the output emitter follower. Meanwhile, Q_P will be conducting a current that decreases as v_O increases; for large v_O the current in Q_P can be ignored altogether.

For negative input voltages the opposite occurs: The load current will be supplied by Q_P, which acts as the output emitter follower, while Q_N conducts a current that gets smaller as v_I becomes more negative. Equation (14.26), relating i_N and i_P, holds for negative inputs as well.

We conclude that the class AB stage operates in much the same manner as the class B circuit, with one important exception: For small v_I, both transistors conduct, and as v_I is increased or decreased, one of the two transistors takes over the operation. Since the transition is a smooth one, crossover distortion will be almost totally eliminated. Figure 14.12 shows the transfer characteristic of the class AB stage.

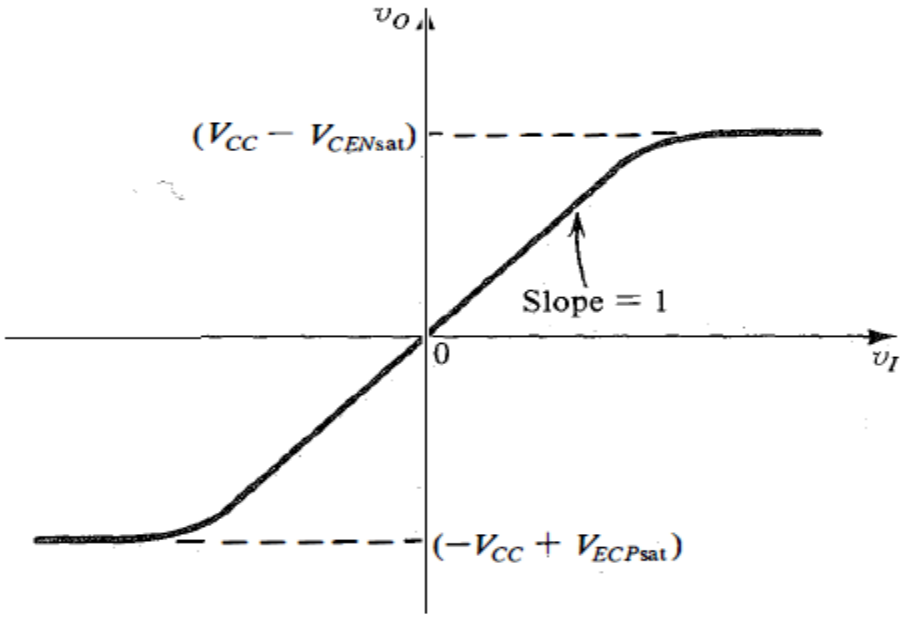


FIGURE 14.12 Transfer characteristic of the class AB stage in Fig. 14.11.

POWER BJTs

Transistors that are required to conduct currents in the ampere range and withstand power dissipation in the watts and tens-of-watts ranges differ in their physical structure, packaging, and specification from the small-signal transistors considered in earlier chapters. In this section we consider some of the important properties of power transistors, especially those aspects that pertain to the design of circuits of the type discussed earlier. There are, of course, other important applications of power transistors, such as their use as switching elements in power inverters and motor-control circuits. Such applications are not studied in this book.

14.6.1 Junction Temperature

Power transistors dissipate large amounts of power in their collector–base junctions. The dissipated power is converted into heat, which raises the junction temperature. However, the junction temperature T_J must not be allowed to exceed a specified maximum, T_{Jmax}; otherwise the transistor could suffer permanent damage. For silicon devices, T_{Jmax} is in the range of 150°C to 200°C.

14.6.2 Thermal Resistance

Consider first the situation of a transistor operating in free air—that is, with no special arrangements for cooling. The heat dissipated in the transistor junction will be conducted away from the junction to the transistor case, and from the case to the surrounding environment. In a steady state in which the transistor is dissipating P_D watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as

$$T_J - T_A = \theta_{JA} P_D \tag{14.36}$$

where θ_{JA} is the **thermal resistance** between junction and ambience, having the units of degrees Celsius per watt. Note that θ_{JA} simply gives the rise in junction temperature over the ambient temperature for each watt of dissipated power. Since we wish to be able to dissipate large amounts of power without raising the junction temperature above $T_{J\max}$, it is desirable to have, for the thermal resistance θ_{JA}, as small a value as possible. For operation in free air,

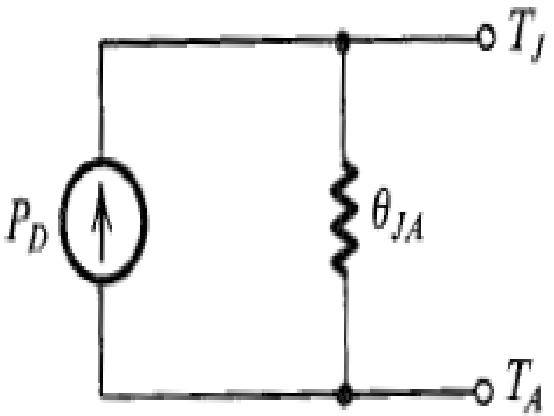


FIGURE 14.17 Electrical equivalent circuit of the thermal-conduction process; $T_J - T_A = P_D\theta_{JA}$.

θ_{JA} depends primarily on the type of case in which the transistor is packaged. The value of θ_{JA} is usually specified on the transistor data sheet.

Equation (14.36), which describes the thermal-conduction process, is analogous to Ohm's law, which describes the electrical-conduction process. In this analogy, power dissipation corresponds to current, temperature difference corresponds to voltage difference, and thermal resistance corresponds to electrical resistance. Thus, we may represent the thermal-conduction process by the electric circuit shown in Fig. 14.17.

14.6.3 Power Dissipation Versus Temperature

The transistor manufacturer usually specifies the maximum junction temperature $T_{J\max}$, the maximum power dissipation at a particular ambient temperature T_{A0} (usually, 25°C), and the thermal resistance θ_{JA}. In addition, a graph such as that shown in Fig. 14.18 is usually provided. The graph simply states that for operation at ambient temperatures below T_{A0}, the device can safely dissipate the rated value of P_{D0} watts. However, if the device is to be operated at higher ambient temperatures, the maximum allowable power dissipation must be **derated** according to the straight line shown in Fig. 14.18. The power-derating curve is a graphical representation of Eq. (14.36). Specifically, note that if the ambient temperature is T_{A0} and the power dissipation is at the maximum allowed (P_{D0}), then the junction temperature will be $T_{J\max}$. Substituting these quantities in Eq. (14.36) results in

$$\theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}} \tag{14.37}$$

which is the inverse of the slope of the power-derating straight line. At an ambient temperature T_A, higher than T_{A0}, the maximum allowable power dissipation $P_{D\max}$ can be obtained from Eq. (14.36) by substituting $T_J = T_{J\max}$; thus,

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} \tag{14.38}$$

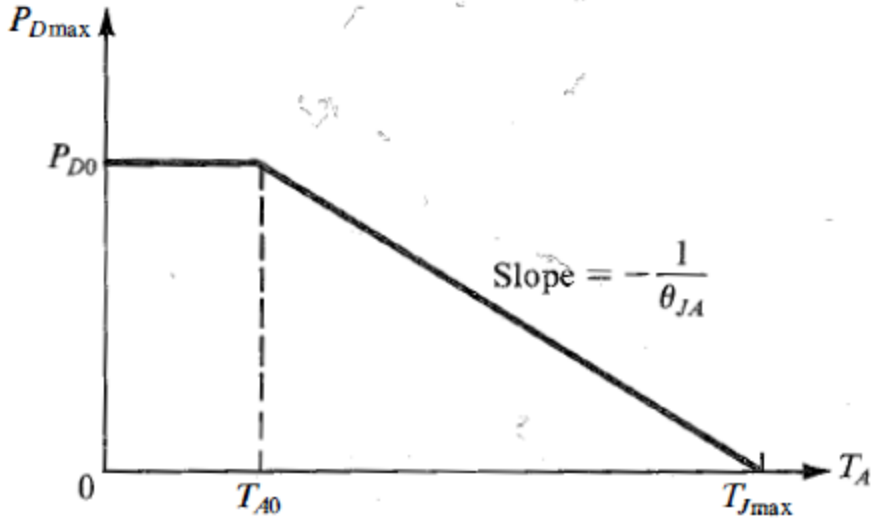


FIGURE 14.18 Maximum allowable power dissipation versus ambient temperature for a BJT operated in free air. This is known as a "power-derating" curve.

Observe that as T_A approaches $T_{J\max}$, the allowable power dissipation decreases; the lower thermal gradient limits the amount of heat that can be removed from the junction. In the extreme situation of $T_A = T_{J\max}$, no power can be dissipated because no heat can be removed from the junction.

A BJT is specified to have a maximum power dissipation P_{D0} of 2 W at an ambient temperature T_{A0} of 25°C, and a maximum junction temperature $T_{J\max}$ of 150°C. Find the following:

(a) The thermal resistance θ_{JA}.

(b) The maximum power that can be safely dissipated at an ambient temperature of 50°C.

(c) The junction temperature if the device is operating at $T_A = 25°C$ and is dissipating 1 W.

Solution

(a) $$\theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}} = \frac{150 - 25}{2} = 62.5°C/W$$

(b) $$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6\ W$$

(c) $$T_J = T_A + \theta_{JA} P_D = 25 + 62.5 \times 1 = 87.5°C$$

Transistor Case and Heat Sink

The thermal resistance between junction and ambience, θ_{JA}, can be expressed as

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \tag{14.39}$$

where θ_{JC} is the thermal resistance between junction and transistor case (package) and θ_{CA} is the thermal resistance between case and ambience. For a given transistor, θ_{JC} is fixed by the device design and packaging. The device manufacturer can reduce θ_{JC} by encapsulating the device in a relatively large metal case and placing the collector (where most of the heat is dissipated) in direct contact with the case. Most high-power transistors are packaged in this fashion. Figure 14.19 shows a sketch of a typical package.

Although the circuit designer has no control over θ_{JC} (once a particular transistor has been selected), the designer can considerably reduce θ_{CA} below its free-air value (specified by the manufacturer as part of θ_{JA}). Reduction of θ_{CA} can be effected by providing means to facilitate heat transfer from case to ambience. A popular approach is to bolt the transistor to the chassis or to an extended metal surface. Such a metal surface then functions as a **heat sink.** Heat is easily conducted from the transistor case to the heat sink; that is, the thermal resistance θ_{CS} is usually very small. Also, heat is efficiently transferred (by convection and

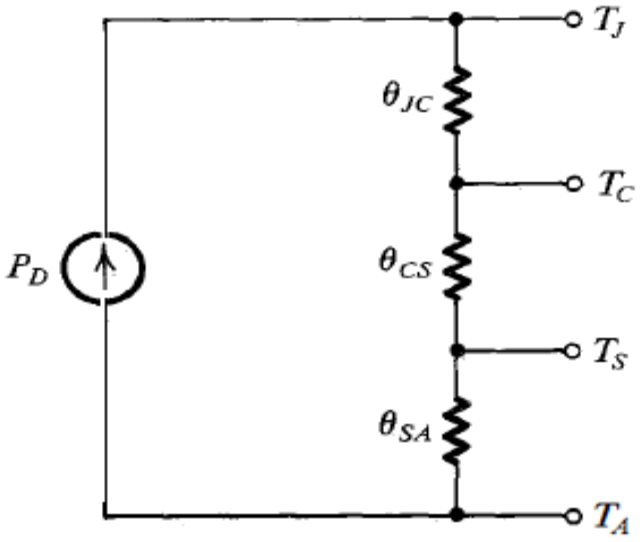


FIGURE 14.20 Electrical analog of the thermal conduction process when a heat sink is utilized.

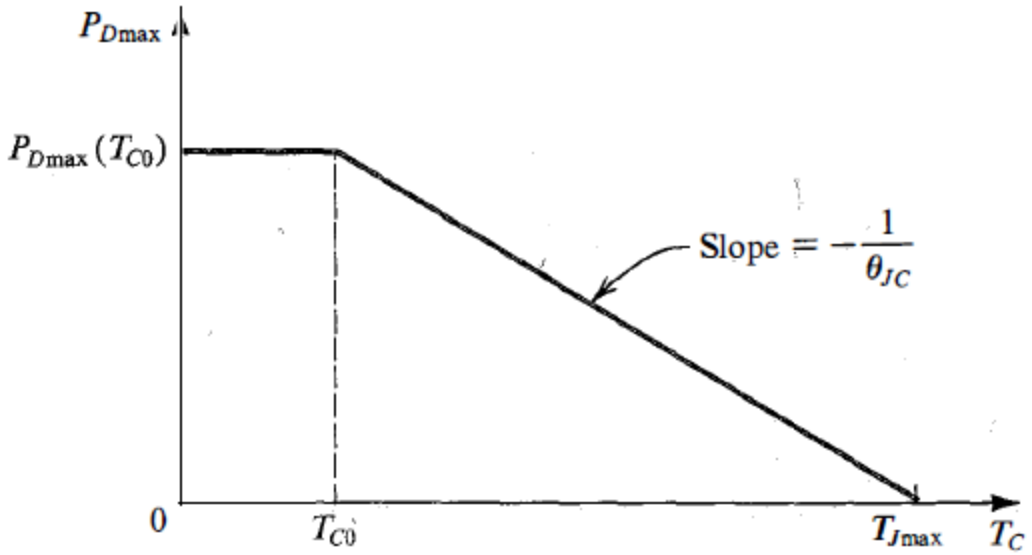


FIGURE 14.21 Maximum allowable power dissipation versus transistor-case temperature.

radiation) from the heat sink to the ambience, resulting in a low thermal resistance θ_{SA}. Thus, if a heat sink is utilized, the case-to-ambience thermal resistance given by

$$\theta_{CA} = \theta_{CS} + \theta_{SA} \tag{14.40}$$

can be small because its two components can be made small by the choice of an appropriate heat sink.[2] For example, in very high-power applications the heat sink is usually equipped with fins that further facilitate cooling by radiation and convection.

The electrical analog of the thermal-conduction process when a heat sink is employed is shown in Fig. 14.20, from which we can write

$$T_J - T_A = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA}) \tag{14.41}$$

As well as specifying θ_{JC}, the device manufacturer usually supplies a derating curve for $P_{D\max}$ versus the case temperature, T_C. Such a curve is shown in Fig. 14.21. Note that the slope of the power-derating straight line is $-1/\theta_{JC}$. For a given transistor, the maximum

power dissipation at a *case temperature* T_{C0} (usually 25°C) is much greater than that at an *ambient temperature* T_{A0} (usually 25°C). If the device can be maintained at a case temperature T_C, $T_{C0} \leq T_C \leq T_{Jmax}$, then the maximum safe power dissipation is obtained when $T_J = T_{Jmax}$,

$$P_{Dmax} = \frac{T_{Jmax} - T_C}{\theta_{JC}} \tag{14.42}$$

A BJT is specified to have $T_{Jmax} = 150°C$ and to be capable of dissipating maximum power as follows:

$$40 \text{ W at } T_C = 25°C$$
$$2 \text{ W at } T_A = 25°C$$

Above 25°C, the maximum power dissipation is to be derated linearly with $\theta_{JC} = 3.12°C/W$ and $\theta_{JA} = 62.5°C/W$. Find the following:

(a) The maximum power that can be dissipated safely by this transistor when operated in free air at $T_A = 50°C$.

(b) The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C, but with a heat sink for which $\theta_{CS} = 0.5°C/W$ and $\theta_{SA} = 4°C/W$. Find the temperature of the case and of the heat sink.

(c) The maximum power that can be dissipated safely if an *infinite heat sink* is used and $T_A = 50°C$.

(a)

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6 \text{ W}$$

(b) With a heat sink, θ_{JA} becomes

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$
$$= 3.12 + 0.5 + 4 = 7.62°\text{C/W}$$

Thus,

$$P_{D\max} = \frac{150 - 50}{7.62} = 13.1 \text{ W}$$

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JC}} = \frac{150 - 50}{3.12} \cong 32 \text{ W}$$

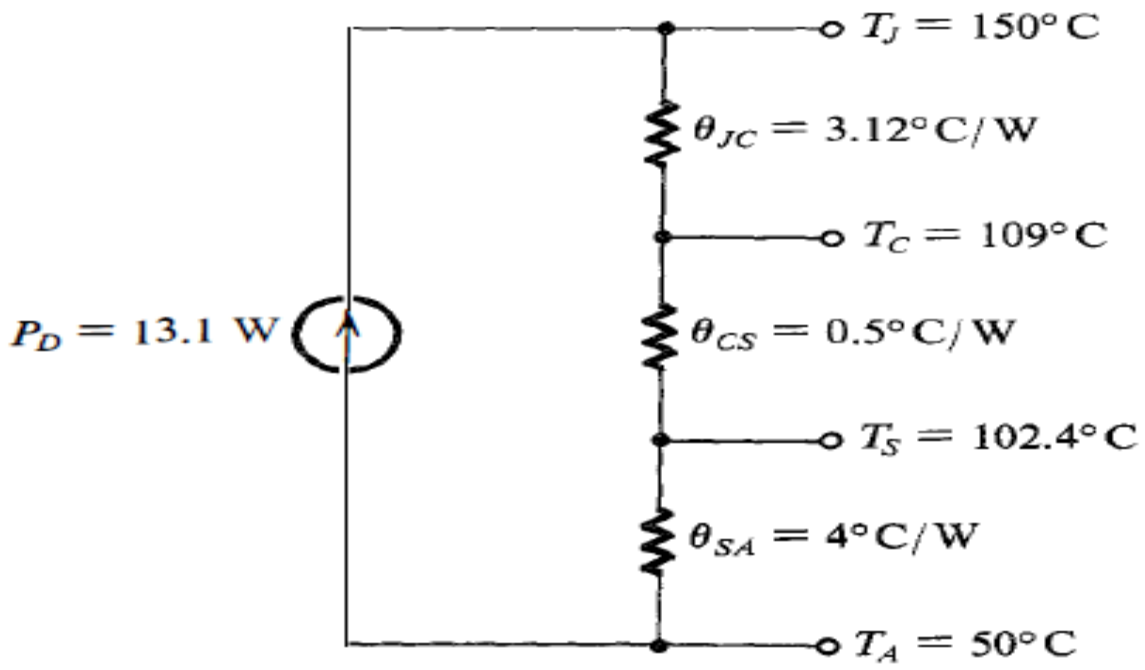


FIGURE 14.22 Thermal equivalent circuit for Example 14.5.