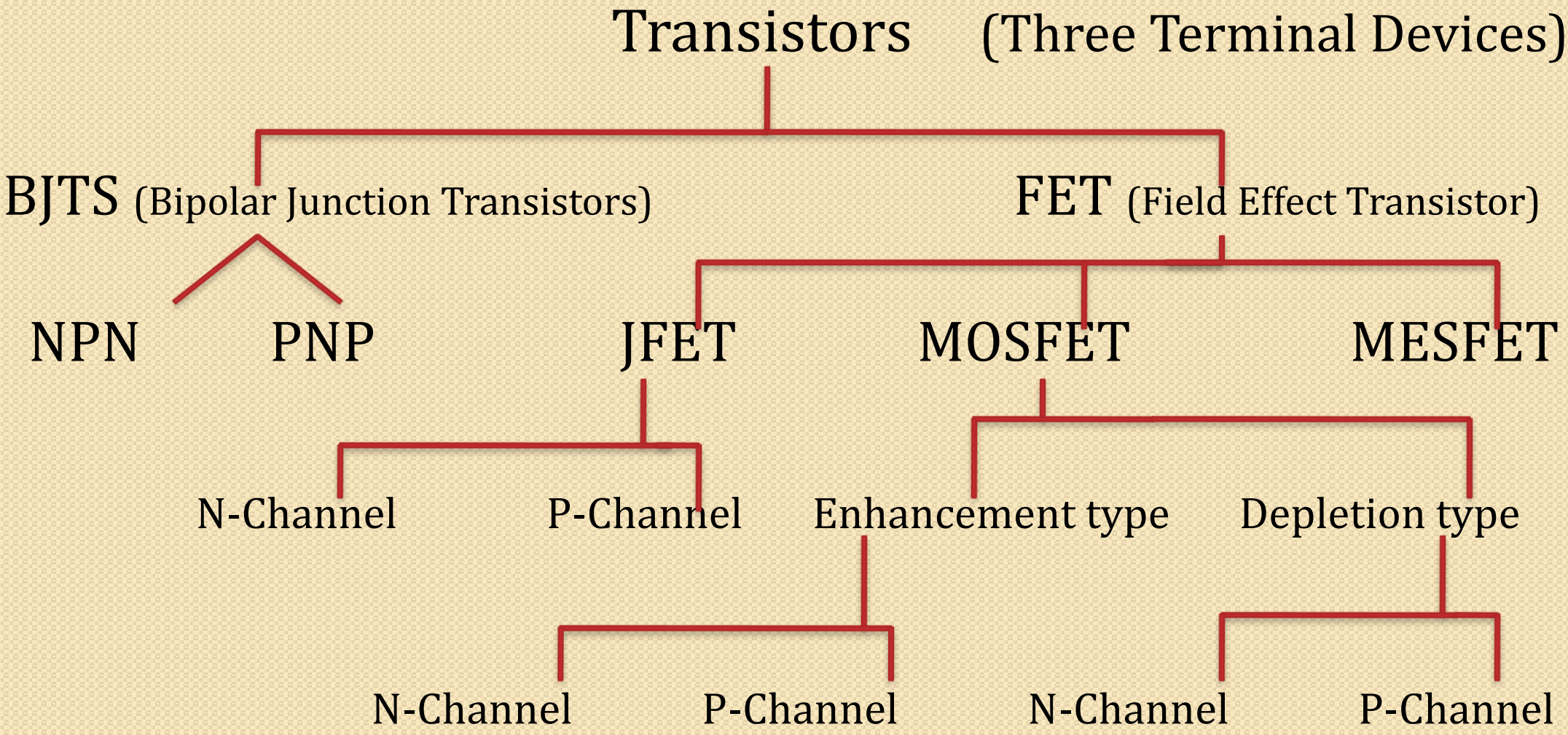
UNIT-4
MOS FIELD-EFFECT TRANSISTORS (MOSFETS)

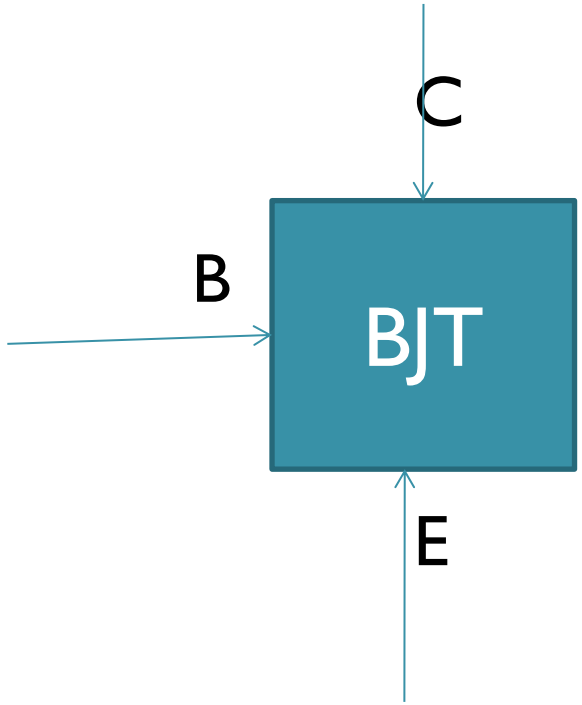
Introduction



Comparison Between BJTs & FETs

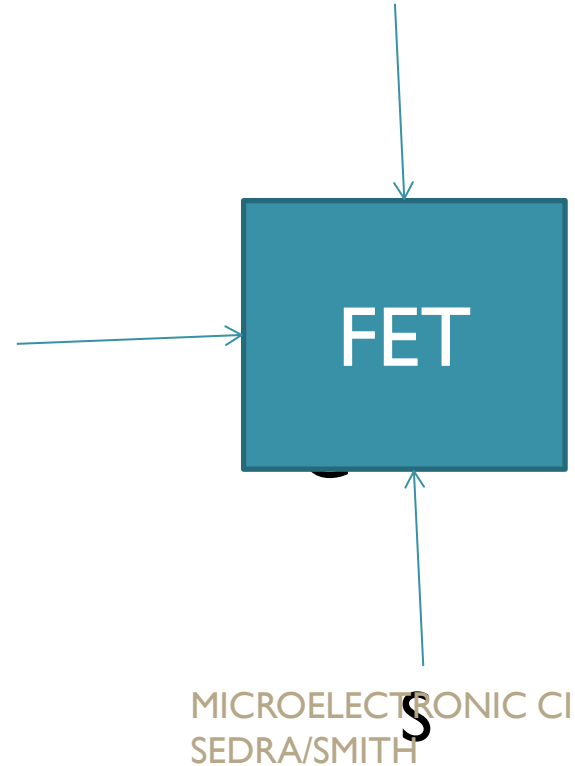
BJTs

1. Current Controlled Device



FETs

Voltage Controlled device



2.	Bipolar device	Unipolar device
3.	Has low I/P impedance	Has high I/P impedance
4.	Occupies more space	Occupies less space
5.	Stability against temperature is less	More temperature stable than BJT
6.	AC voltage gains for BJT amplifier is more	AC voltage gain for FET amplifier is less

7.	Highly susceptible to more noise.	Less susceptible to less noise.
8.	$I_C = \beta I_B$	$I_D = I_{Dss} \ (1-V_{GS}/V_p)$
	$I_C = I_E$	$I_D = I_S$
	$V_{BE} = 0.7V$ (starting point for analysis)	$I_G = 0A$ (starting point for analysis)

9.	Power dissipation is more.	Power dissipation is less.
10.	Used in amplifiers, switches, digital logic & memory.	Used in amplifiers, switches, filters , memory, digital logic Ics such as microprocessor, microcontrollers, signal processors, etc.

FIG 4.1 SHOWS THE PHYSICAL STRUCTURE OF ENHANCEMENT TYPE NMOS TRANSISTOR ; PERSPECTIVE VIEW. TYPICALLY *L=0.1 TO 3μm, W=0.2 TO 100μm,* AND THE THIC KNESS OF THE OXIDE LAYER *(t_{ox})* IS IN THE RANGE OF 2 TO 50 nm.

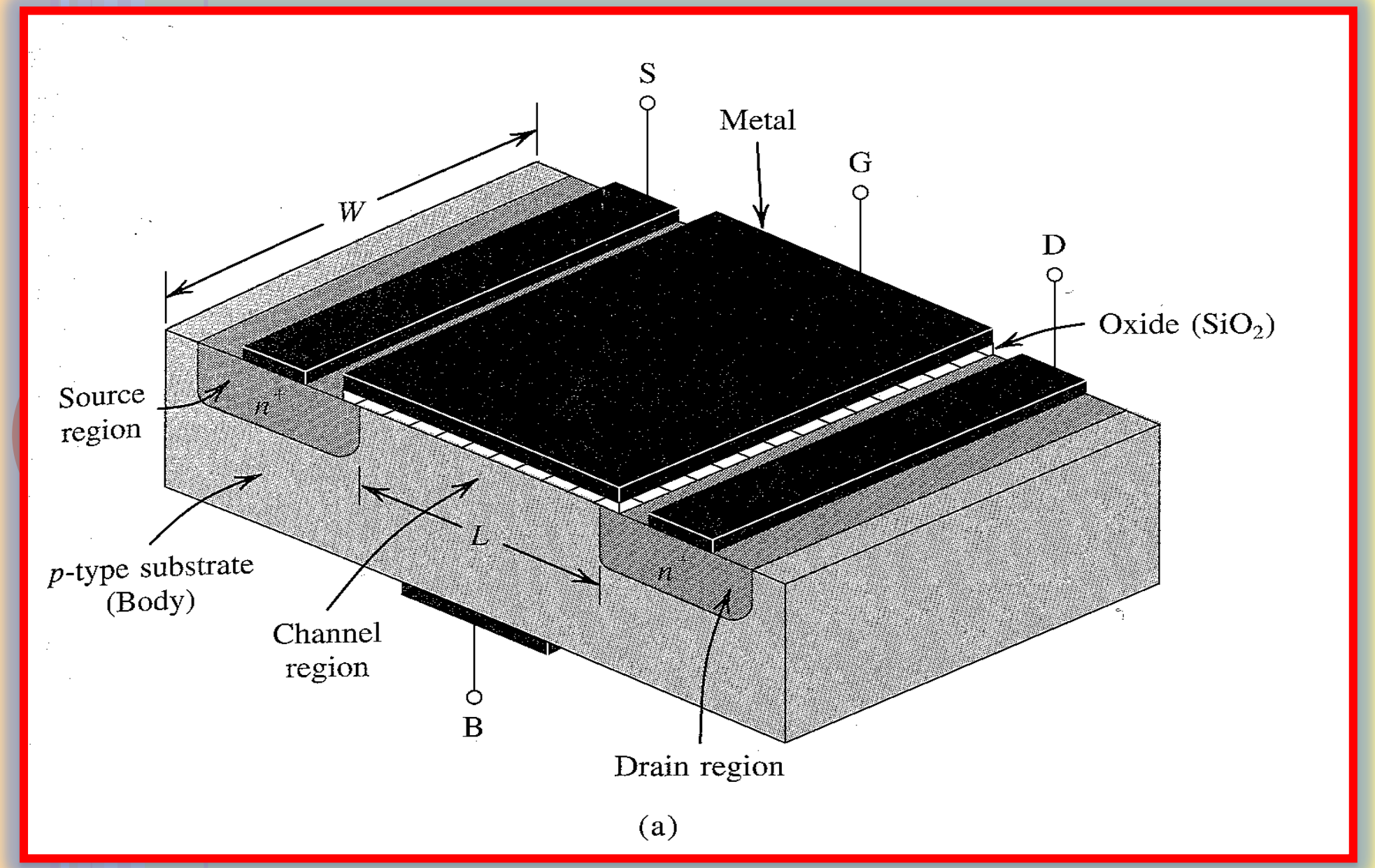
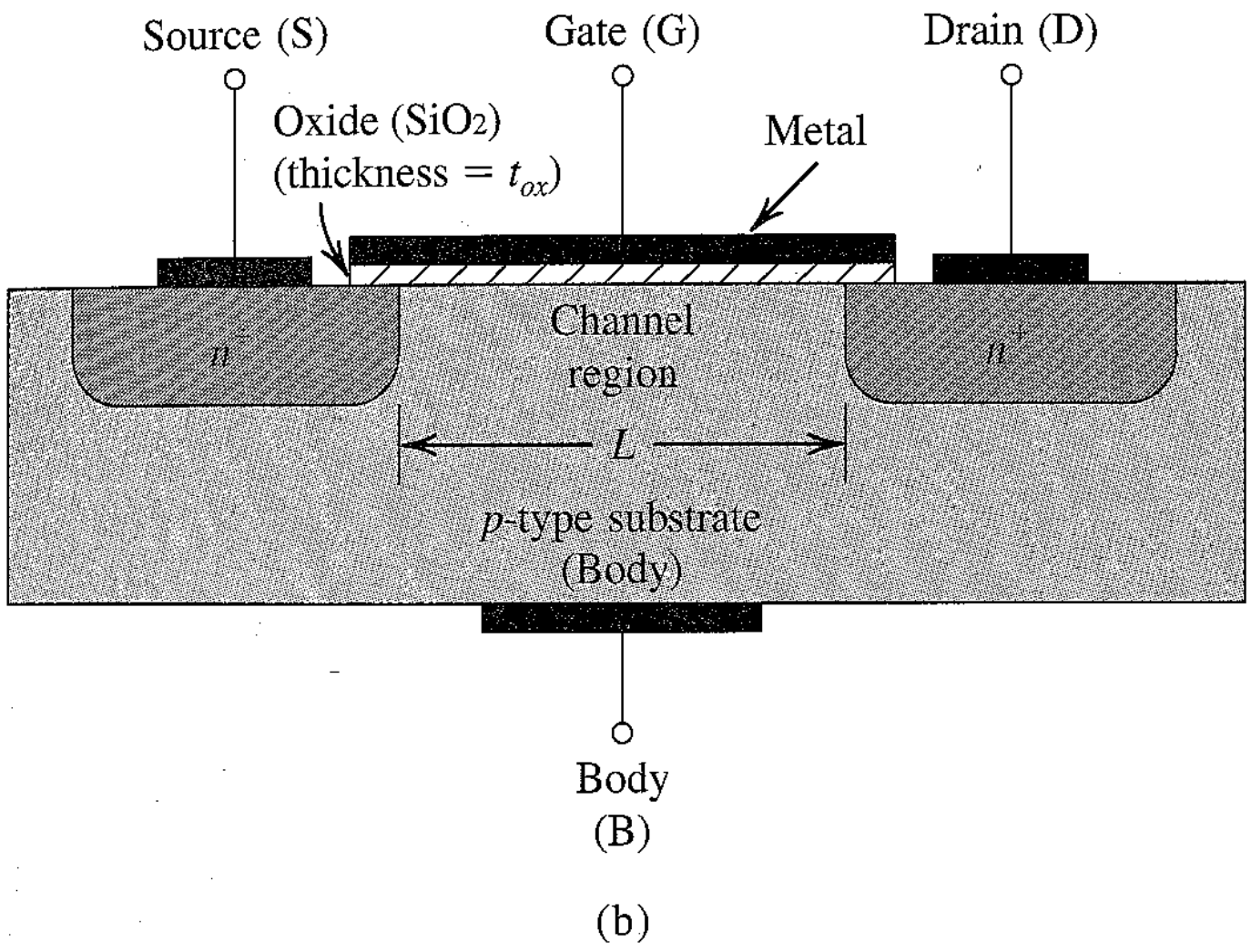


FIG 4.1 (B)PHYSICAL STRUCTURE OF ENHANCEMENT TYPE NMOS TRANSISTOR---- CROSS SECTIONAL VIEW.



Another name for the MOSFET is the insulated-gate FET or IGFET.

MOS FET FEATURES

- L is in the range of 0.1 μm to 3 μm, and
- W is in the range of 0.2 μm to 100μm.
- note that the MOSFET is a symmetrical device; thus its
- source and drain can be interchanged with no change in device characteristics
- Operation with No Gate Voltage
- These back -to-back diodes prevent current conduction from drain to source when a voltage VDS is applied
- In fact, the path between drain and
- source has a very high resistance (of the order of 10to power of 12 Ω).

FIG 4.2 SHOWS THE ENHANCEMENT TYPE NMOS TRANSISTOR WITH A POSITIVE VOLTAGE APPLIED TO THE GATE. AN N CHANNEL IS INDUCED AT THE TOP OF THE SUBSTRATE BENEATH THE GATE.

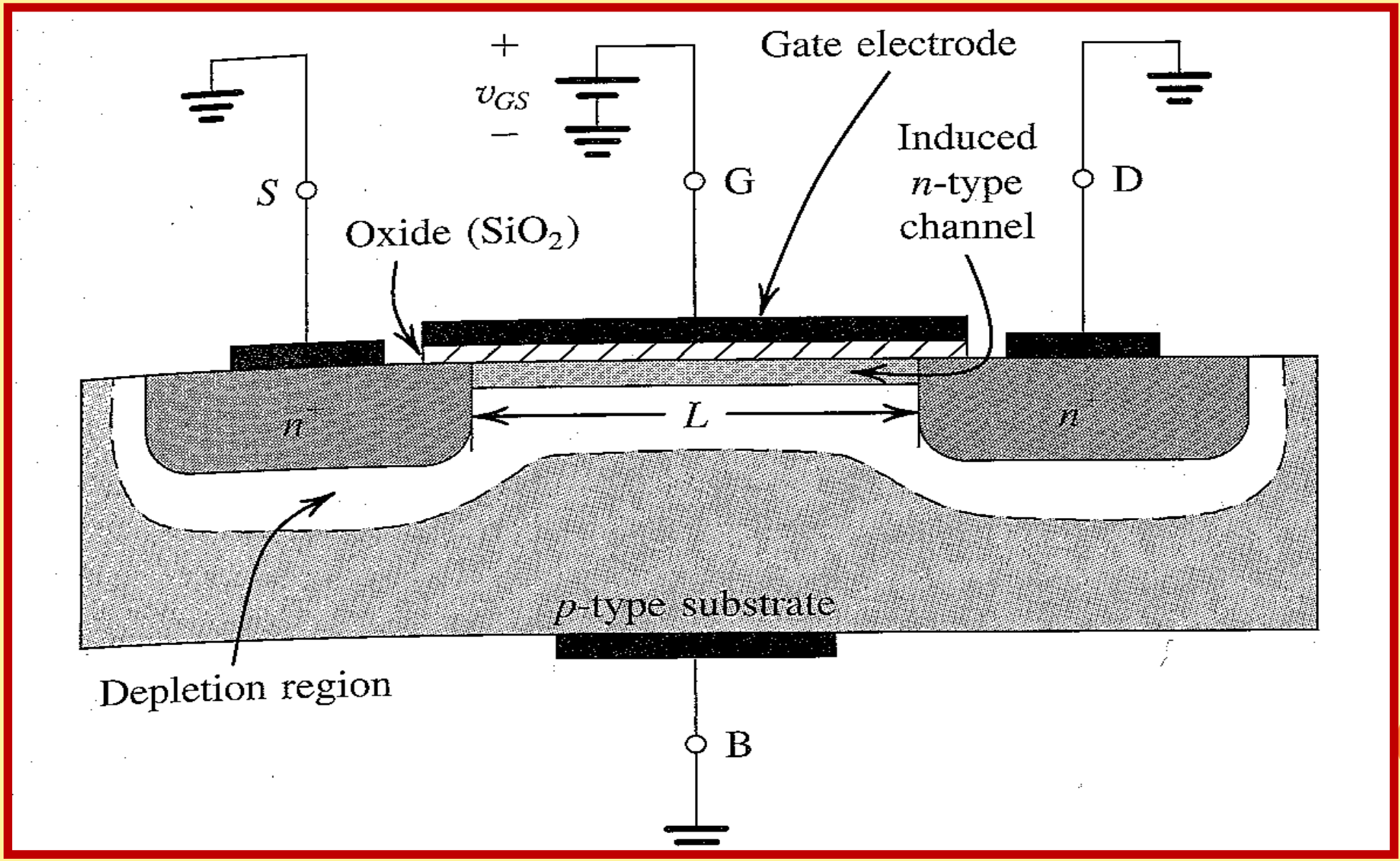


FIG 4.3 SHOWS AN NMOS TRANSISTOR WITH $V_{GS} > Vt$ AND WITH A SMALL V_{DS} APPLIED. THE DEVICE ACTS AS A RESISTANCE WHOSE VALUE IS DETERMINED BY VGS.

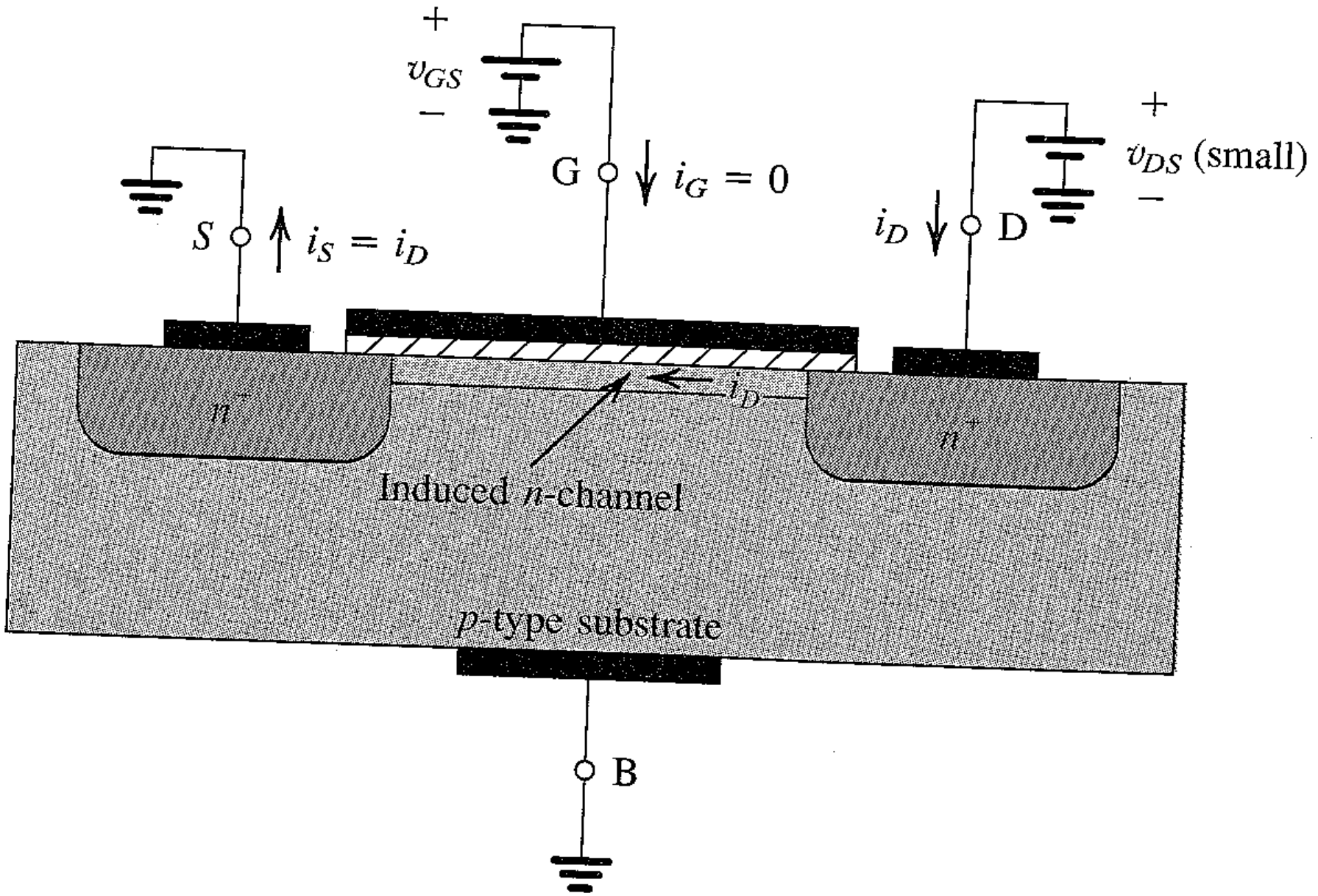


FIG 4.4 SHOWS THE I_D-V_{DS} CHARACTERISTICS OF THE MOSFET.

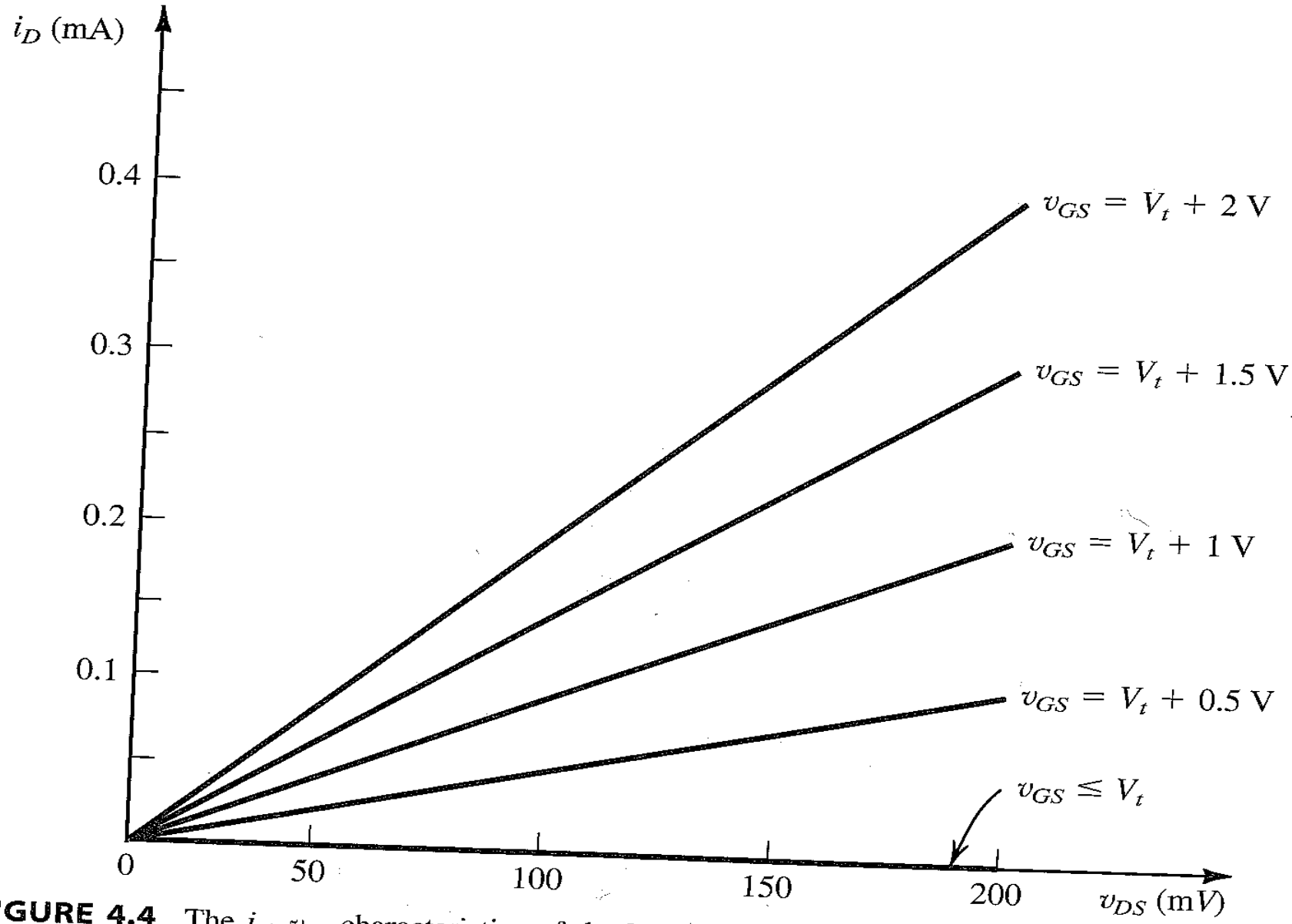


FIGURE 4.4 The i_D–v_{DS} characteristics of the

FIG 4.5 SHOWS THE OPERATION OF THE ENHANCEMENT NMOS TRANSISTOR AS V_{DS} IS INCREASED. THE INDUCED CHANNEL ACQUIRES A TAPERED SHAPE, AND ITS RESISTANCE INCREASES AS V_{DS} IS INCREASED. HERE V_{GS} IS KEPT CONSTANT AT VALUE > Vt

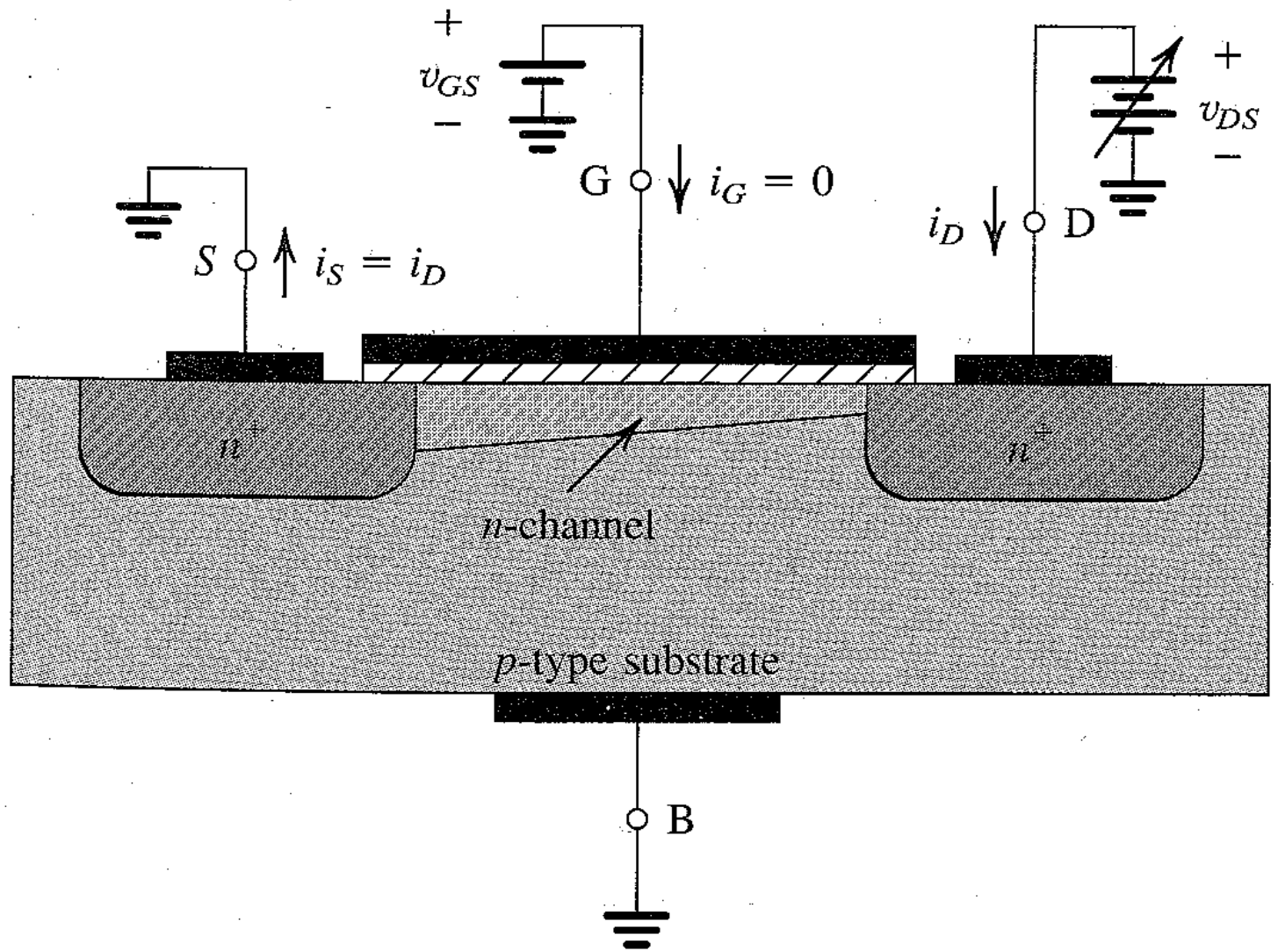


FIG 4.6 SHOWS THE DRAIN CURRENT I_D VERSUS THE DRAIN-TO-SOURCE VOLTAGE V_{DS} FOR AN ENHANCEMENT-TYPE NMOS TRANSISTOR OPERATED WITH $V_{GS}>Vt$.

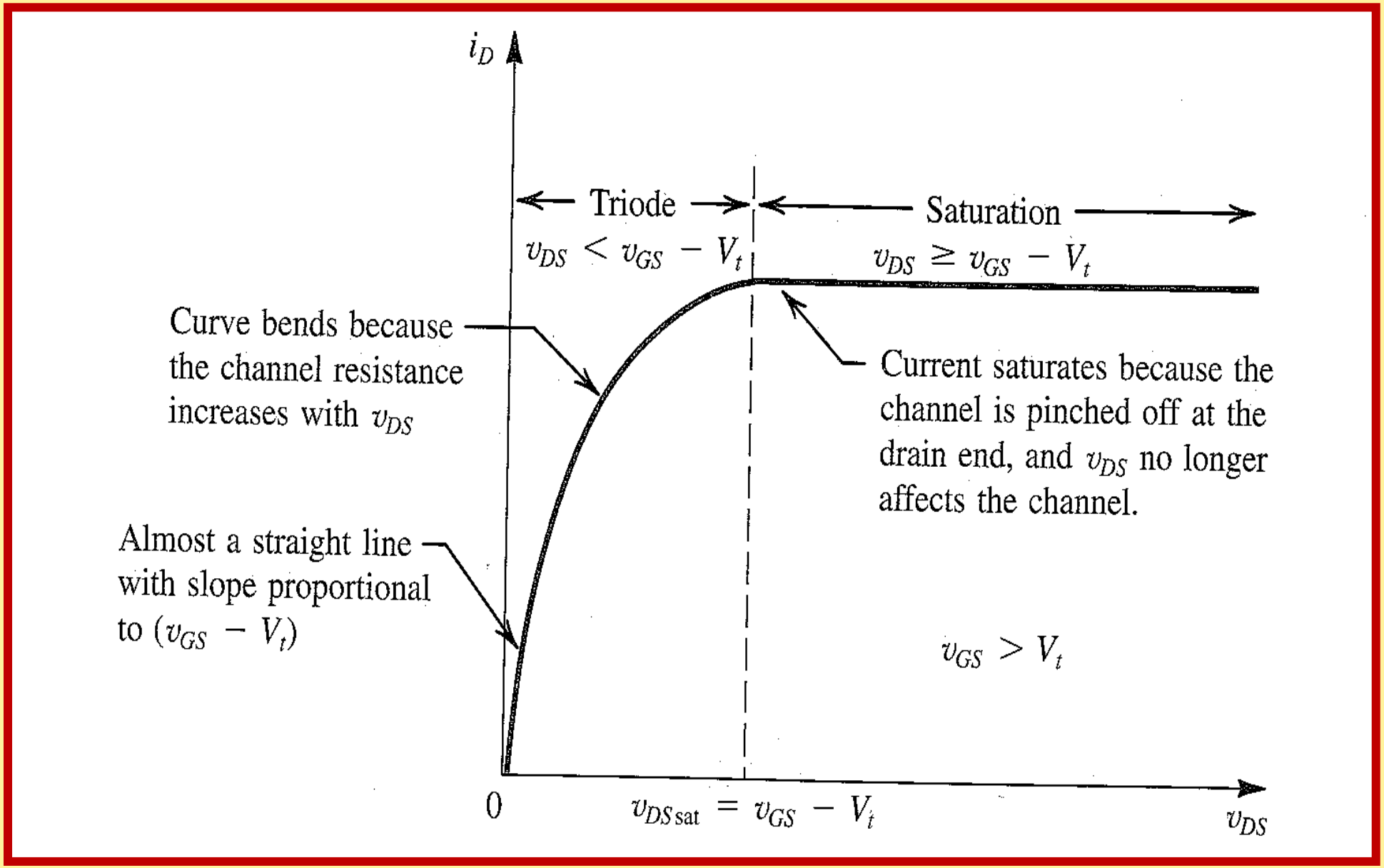


FIG 4.7 SHOWS INCREASING V_{DS} CAUSES THE CHANNEL TO ACQUIRE A TAPERED SHAPE. EVENTUALLY, AS V_{DS} REACHES V_{GS}-V_t, THE CHANNEL IS PINCHED OFF AT HE DRAIN END. INCREASING V_{DS}-V_t HAS LITTLE EFFECT(THEORETICALLY, NO EFFECT) ON THE CHANNEL'S SHAPE.

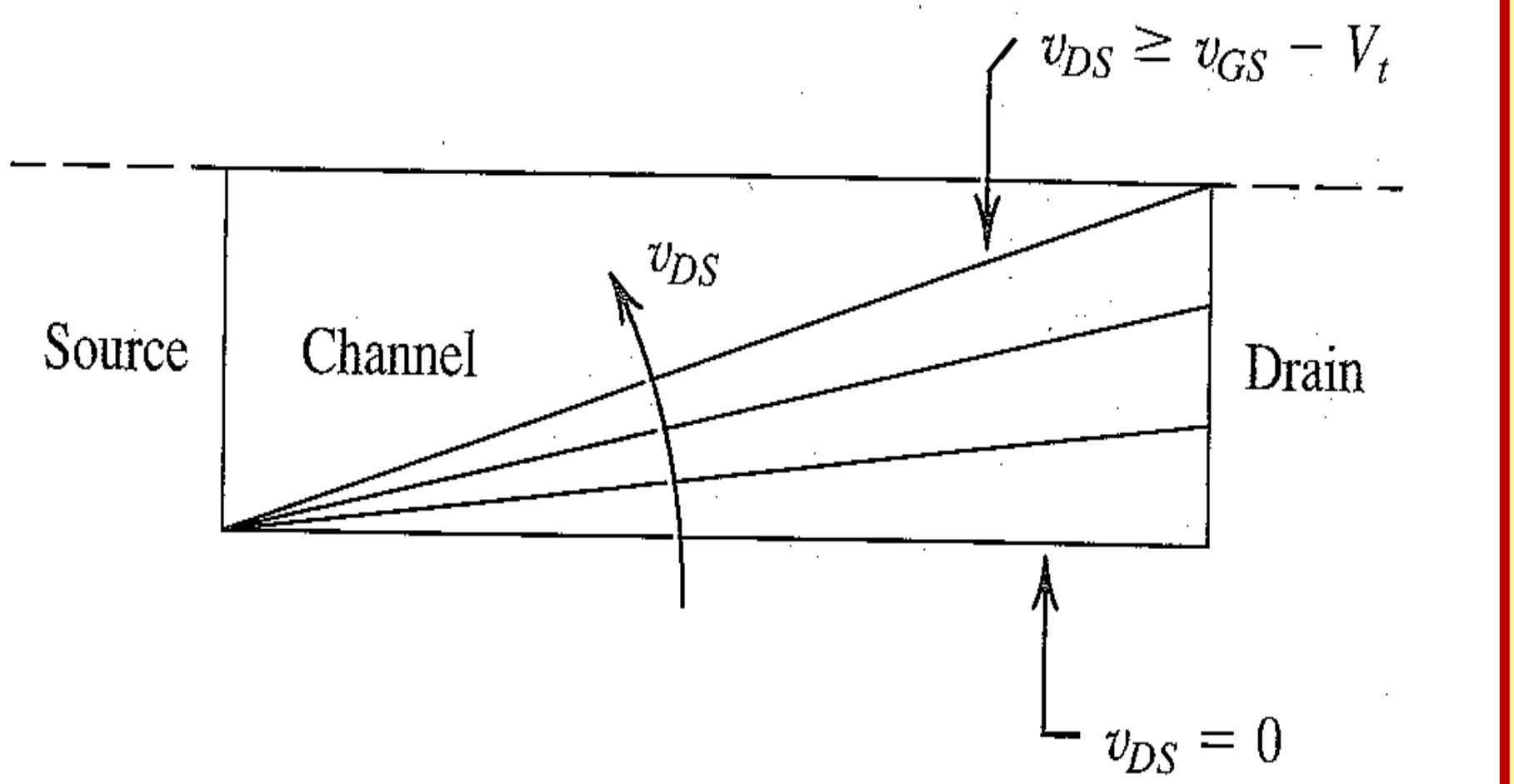
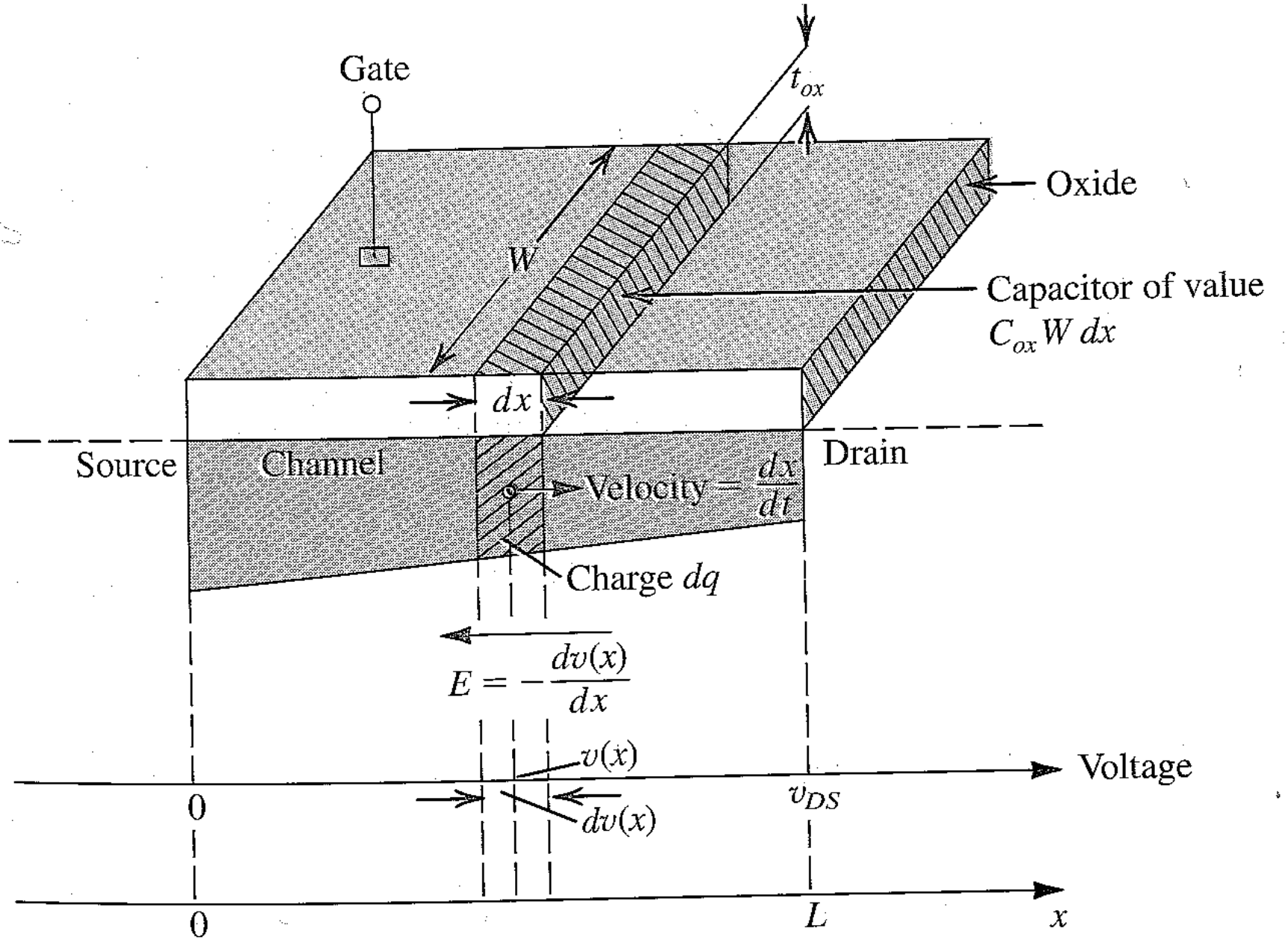


FIG 4.8 SHOWS THE DERIVATION OF THE I_D-V_{DS} CHARACTERISTICS OF THE NMOS TRANSISTOR.



The reader will recall that in the MOSFET, the gate and the channel region form a parallel-plate capacitor for which the oxide layer serves as a dielectric. If the capacitance per unit gate area is denoted C_{ox} and the thickness of the oxide layer is t_{ox}, then

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4.2}$$

where ε_{ox} is the permittivity of the silicon oxide,

$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

The oxide thickness t_{ox} is determined by the process technology used to fabricate the MOSFET. As an example, for $t_{ox} = 10$ nm, $C_{ox} = 3.45 \times 10^{-3}$ F/m^2, or 3.45 fF/μm^2 as it is usually expressed.

Now refer to Fig. 4.8 and consider the infinitesimal strip of the gate at distance x from the source. The capacitance of this strip is $C_{ox}W\,dx$. To find the charge stored on this infinitesimal strip of the gate capacitance, we multiply the capacitance by the *effective voltage*

between the gate and the channel at point x, where the effective voltage is the voltage that is responsible for inducing the channel at point x and is thus $[v_{GS} - v(x) - V_t]$ where $v(x)$ is the voltage in the channel at point x. It follows that the electron charge dq in the infinitesimal portion of the channel at point x is

$$dq = -C_{ox}(W\,dx)[v_{GS} - v(x) - V_t] \tag{4.3}$$

where the leading negative sign accounts for the fact that dq is a negative charge.

The voltage v_{DS} produces an electric field along the channel in the negative x direction. At point x this field can be expressed as

$$E(x) = -\frac{dv(x)}{dx}$$

The electric field $E(x)$ causes the electron charge dq to *drift* toward the drain with a velocity dx/dt,

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx} \tag{4.4}$$

where μ_n is the mobility of electrons in the channel (called surface mobility). It is a physical parameter whose value depends on the fabrication process technology. The resulting drift current i can be obtained as follows:

$$i = \frac{dq}{dt}$$

$$= \frac{dq}{dx}\frac{dx}{dt}$$

Substituting for the charge-per-unit-length dq/dx from Eq. (4.3), and for the electron drift velocity dx/dt from Eq. (4.4), results in

$$i = -\mu_n C_{ox} W [v_{GS} - v(x) - V_t] \frac{dv(x)}{dx}$$

Although evaluated at a particular point in the channel, the current i must be constant at all points along the channel. Thus i must be equal to the source-to-drain current. Since we are interested in the drain-to-source current i_D, we can find it as

$$i_D = -i = \mu_n C_{ox} W [v_{GS} - v(x) - V_t] \frac{dv(x)}{dx}$$

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Integrating both sides of this equation from $x = 0$ to $x = L$ and, correspondingly, for $v(0) = 0$ to $v(L) = v_{DS}$,

$$\int_0^L i_D\,dx = \int_0^{v_{DS}} \mu_n C_{ox} W[v_{GS} - V_t - v(x)]\,dv(x)$$

gives

$$i_D = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \tag{4.5}$$

This is the expression for the i_D–v_{DS} characteristic in the triode region. The value of the current at the edge of the triode region or, equivalently, at the beginning of the saturation region can be obtained by substituting $v_{DS} = v_{GS} - V_t$, resulting in

$$i_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \tag{4.6}$$

This is the expression for the i_D–v_{DS} characteristic in the saturation region; it simply gives the saturation value of i_D corresponding to the given v_{GS}. (Recall that in saturation i_D remains constant for a given v_{GS} as v_{DS} is varied.)

In the expressions in Eqs. (4.5) and (4.6), $\mu_n C_{ox}$ is a constant determined by the process technology used to fabricate the *n*-channel MOSFET. It is known as the **process transconductance parameter,** for as we shall see shortly, it determines the value of the MOSFET transconductance, is denoted k_n', and has the dimensions of A/V^2.

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$$k_n' = \mu_n C_{ox} \tag{4.7}$$

Of course, the i_D–v_{DS} expressions in Eqs. (4.5) and (4.6) can be written in terms of k_n' as follows:

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{(Triode region)} \tag{4.5a}$$

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \quad \text{(Saturation region)} \tag{4.6a}$$

In this book we will use the forms with $(\mu_n C_{ox})$ and with k_n' interchangeably.

From Eqs. (4.5) and (4.6) we see that the drain current is proportional to the ratio of the channel width W to the channel length L, known as the **aspect ratio** of the MOSFET. The

Consider a process technology for which $L_{min} = 0.4\ \mu m$, $t_{ox} = 8$ nm, $\mu_n = 450\ cm^2/V \cdot s$, and $V_t = 0.7$ V.

(a) Find C_{ox} and k_n'.

(b) For a MOSFET with $W/L = 8\ \mu m/0.8\ \mu m$, calculate the values of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\ \mu A$.

(c) For the device in (b), find the value of V_{GS} required to cause the device to operate as a 1000-Ω resistor for very small v_{DS}.

(a)
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.32 \times 10^{-3}\ F/m^2$$
$$= 4.32\ fF/\mu m^2$$
$$k_n' = \mu_n C_{ox} = 450\ (cm^2/V \cdot s) \times 4.32\ (fF/\mu m^2)$$
$$= 450 \times 10^8\ (\mu m^2/V \cdot s) \times 4.32 \times 10^{-15} (F/\mu m^2)$$
$$= 194 \times 10^{-6}\ (F/V \cdot s)$$
$$= 194\ \mu A/V^2$$

(b) For operation in the saturation region,

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$$

Thus,

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8} (V_{GS} - 0.7)^2$$

$$V_{GS} - 0.7 = 0.32 \text{ V}$$

or

$$V_{GS} = 1.02 \text{ V}$$

and

$$V_{DS\min} = V_{GS} - V_t = 0.32 \text{ V}$$

(c) For the MOSFET in the triode region with v_{DS} very small,

$$i_D \cong k_n' \frac{W}{L}(v_{GS} - V_t)v_{DS}$$

from which the drain-to-source resistance r_{DS} can be found as

$$r_{DS} \equiv \left.\frac{v_{DS}}{i_D}\right|_{\text{small } v_{DS}}$$

$$= 1\Big/\left[k_n' \frac{W}{L}(V_{GS} - V_t)\right]$$

Thus

$$1000 = \frac{1}{194 \times 10^{-6} \times 10(V_{GS} - 0.7)}$$

which yields

$$V_{GS} - 0.7 = 0.52 \text{ V}$$

Thus,

$$V_{GS} = 1.22 \text{ V}$$

FIG 4.9 SHOWS THE CROSS SECTION OF A CMOS INTEGRATED CIRCUIT. NOTE THAT THE PMOS TRANSISTOR IS FORMED IN A SEPERATE *n*-TYPE REGION, KNOWN AS AN *n*-WELL. ANOTHER ARRANGEMENT IS ALSO POSSIBLE IN WHICH AN *n*-TYPE BODY IS USED AND THE N DEVICE IS FORMED IN A *p*-WELL.

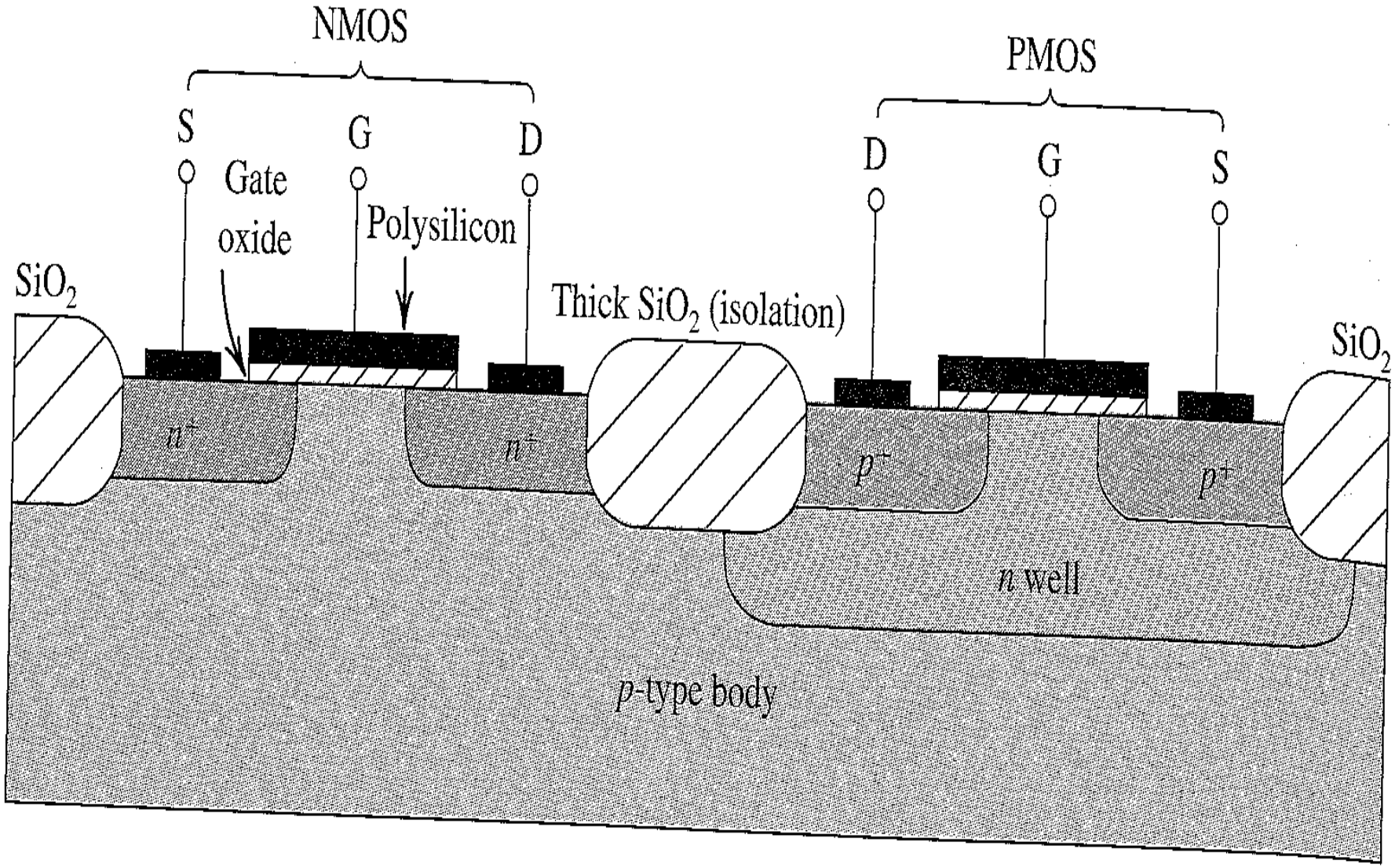
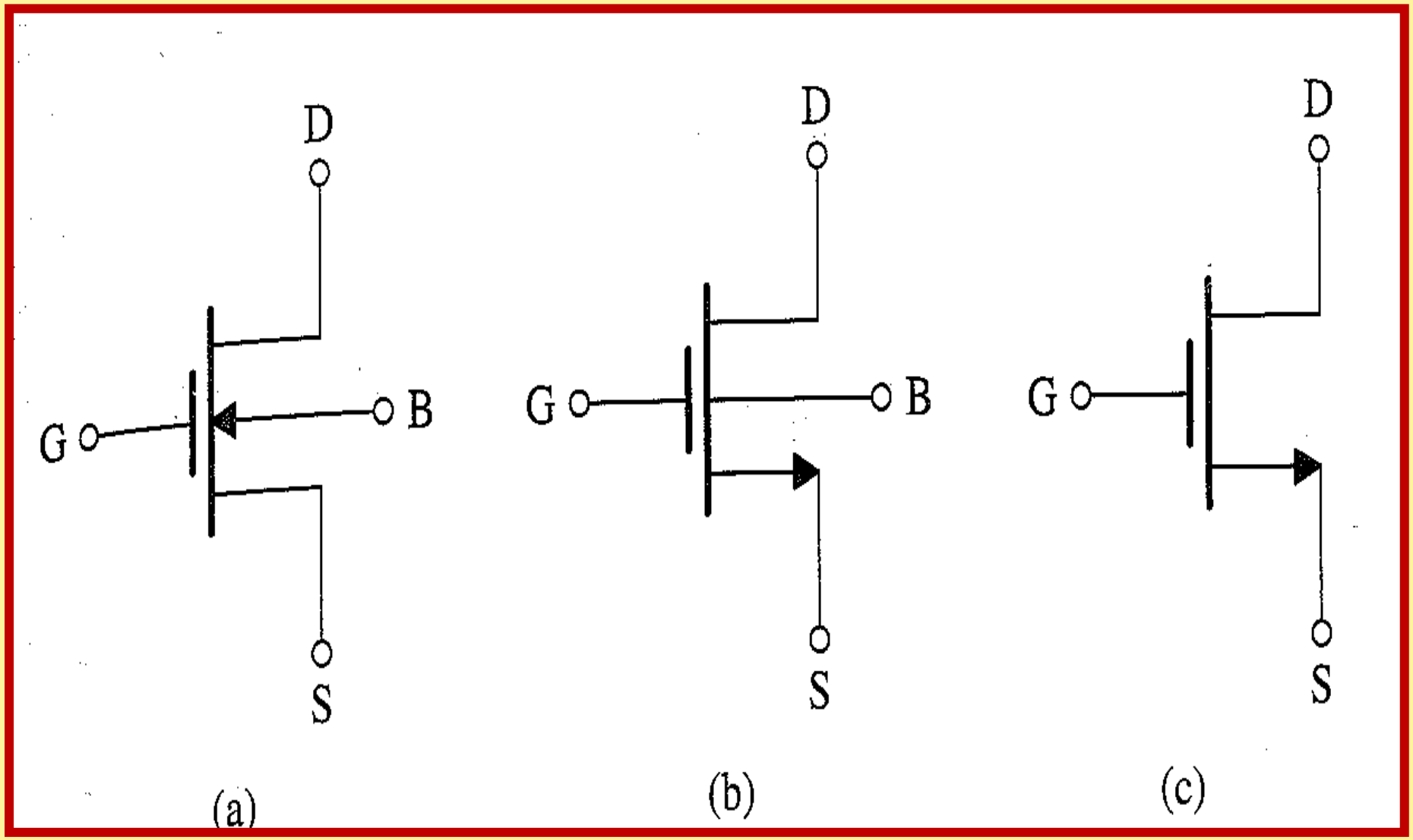


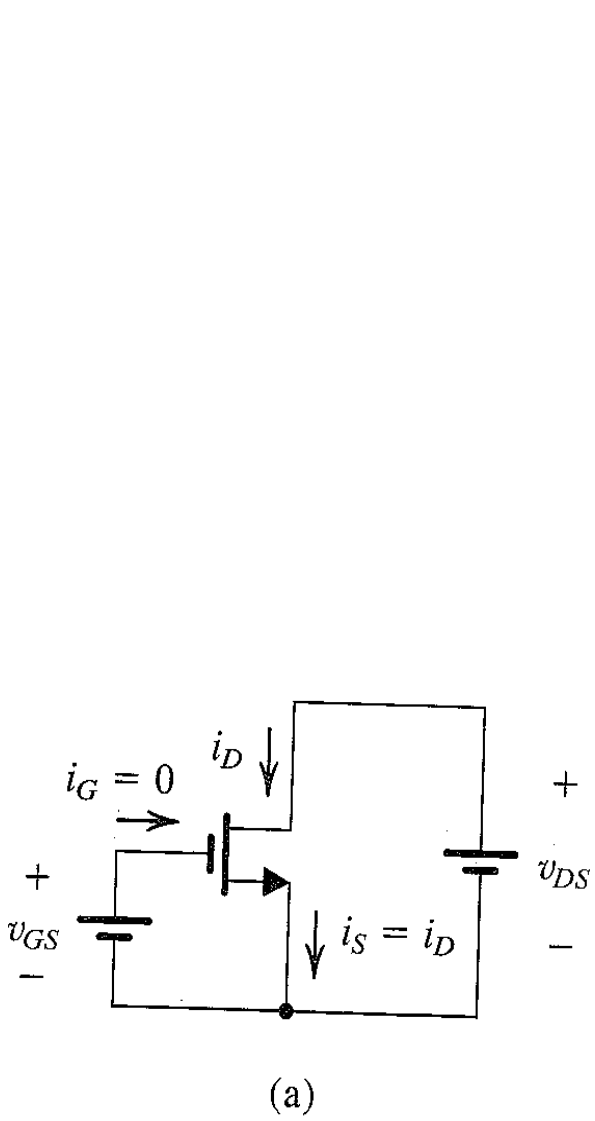
FIG4.10 (A) SHOWS THE CIRCUIT SYMBOL FOR THE *n*-CHANNEL ENHANCEMENT-TYPE MOSFET. FIG(B) SHOWS THE MODIFIED CIRCUIT SYMBOL WITH AN ARROWHEAD ON THE SOURCE TERMINAL TO DISTINGUISH IT FROM THE DRAIN AND TO INDICATE DEVICE POLARITY (*n*-CHANNEL). FIB(C) SHOWS THE SIMPLIFIED CIRCUIT SYMBOL TO BE USED WHEN THE SOURCE IS CONNECTED TO THE BODY OR WHEN THE EFFECT OF THE BODY ON DEVICE OPERATION IS UNIMPORANT.

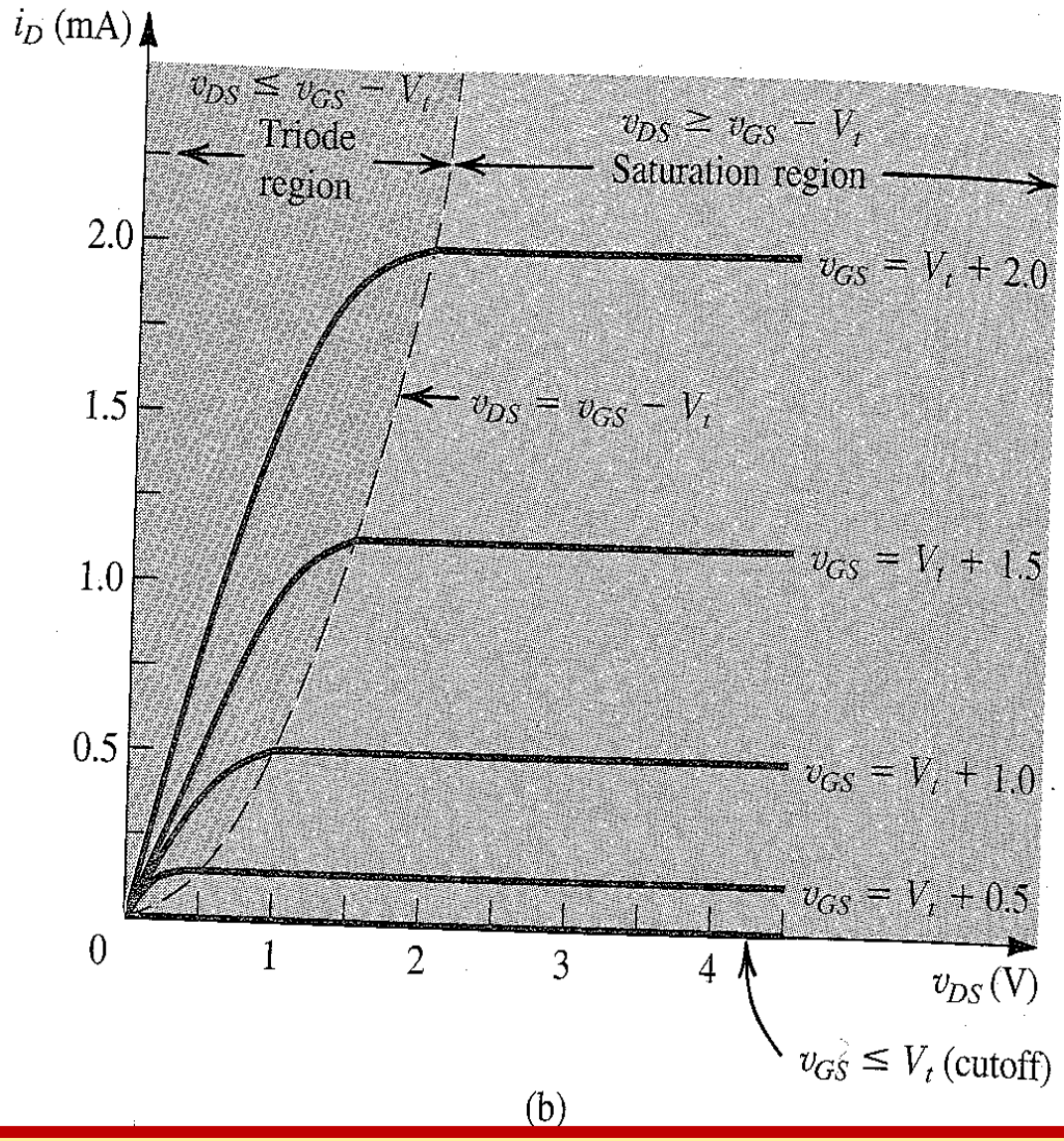


Operating the MOS TransistOr in the SubthreshOld RegiOn

- n-channel MOSFET, for $V_{GS} < V_t$, no current flows and the device is cut off.
- been found that for values of V_{GS} smaller than but close to V_t, a small drain current flows.
- In this subthreshold region of operation the drain current is exponentially related to V_{GS}
- there are special, but a growing number of, applications that make use of subthreshold operation

FIG 4.11 (A) SHOWS AN *n*-CHANNEL ENHANCEMENT-TYPE MOSFET WITH V_{GS} AND V_{DS} APPLIED AND WITH THE NORMAL DIRECTIONS OF CURRENT FLOW INDICATED. FIG (B) SHOWS THE I_D-V_{DS} CHARACTERISTICS FOR A DEVICE WITH $K'_n(W/L)=1.0$ mA/V^2.





The characteristic curves in Fig. 4.11(b) indicate that there are three distinct regions of operation: the **cutoff region,** the **triode region,** and the **saturation region.** The saturation region is used if the FET is to operate as an amplifier. For operation as a switch, the cutoff and triode regions are utilized. The device is cut off when $v_{GS} < V_t$. To operate the MOSFET in the triode region we must first induce a channel,

$$v_{GS} \geq V_t \quad \text{(Induced channel)} \tag{4.8}$$

and then keep v_{DS} small enough so that the channel remains continuous. This is achieved by ensuring that the gate-to-drain voltage is

$$v_{GD} > V_t \quad \text{(Continuous channel)} \tag{4.9}$$

This condition can be stated explicitly in terms of v_{DS} by writing $v_{GD} = v_{GS} + v_{SD} = v_{GS} - v_{DS}$; thus,

$$v_{GS} - v_{DS} > V_t$$

which can be rearranged to yield

$$v_{DS} < v_{GS} - V_t \quad \text{(Continuous channel)} \tag{4.10}$$

Either Eq. (4.9) or Eq. (4.10) can be used to ascertain triode-region operation. In words, *the n-channel enhancement-type MOSFET operates in the triode region when v_{GS} is greater than V_t and the drain voltage is lower than the gate voltage by at least V_t volts.*

In the triode region, the i_D–v_{DS} characteristics can be described by the relationship of Eq. (4.5), which we repeat here,

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right] \tag{4.11}$$

where $k_n' = \mu_n C_{ox}$ is the process transconductance parameter; its value is determined by the fabrication technology. If v_{DS} is sufficiently small so that we can neglect the v_{DS}^2 term in Eq. (4.11), we obtain for the i_D–v_{DS} characteristics near the origin the relationship

$$i_D \simeq k_n' \frac{W}{L} (v_{GS} - V_t) v_{DS} \tag{4.12}$$

This linear relationship represents the operation of the MOS transistor as a linear resistance r_{DS} whose value is controlled by v_{GS}. Specifically, for v_{GS} set to a value V_{GS}, r_{DS} is given by

$$r_{DS} \equiv \left.\frac{v_{DS}}{i_D}\right|_{\substack{v_{DS}\ \text{small} \\ v_{GS}=V_{GS}}} = \left[k_n' \frac{W}{L}(V_{GS}-V_t)\right]^{-1} \tag{4.13}$$

We discussed this region of operation in the previous section (refer to Fig. 4.4). It is also useful to express r_{DS} in terms of the **gate-to-source overdrive voltage,**

$$V_{OV} \equiv V_{GS} - V_t \tag{4.14}$$

as

$$r_{DS} = 1\Big/\left[k_n'\left(\frac{W}{L}\right)V_{OV}\right] \tag{4.15}$$

Finally, we urge the reader to show that the approximation involved in writing Eq. (4.12) is based on the assumption that $v_{DS} \ll 2V_{OV}$.

To operate the MOSFET in the saturation region, a channel must be induced,

$$v_{GS} \geq V_t \quad \text{(Induced channel)} \tag{4.16}$$

and pinched off at the drain end by raising v_{DS} to a value that results in the gate-to-drain voltage falling below V_t,

$$v_{GD} \leq V_t \quad \text{(Pinched-off channel)} \tag{4.17}$$

This condition can be expressed explicitly in terms of v_{DS} as

$$v_{DS} \geq v_{GS} - V_t \quad \text{(Pinched-off channel)} \tag{4.18}$$

FIG 4.12 THE I_D-V_{GS} CHARACTERISTICS FOR AN ENHANCEMENT-TYPE NMOS TRANSISTOR IN SATURATION(V_t=1V, K'N W/L=1.0mA/V^2)

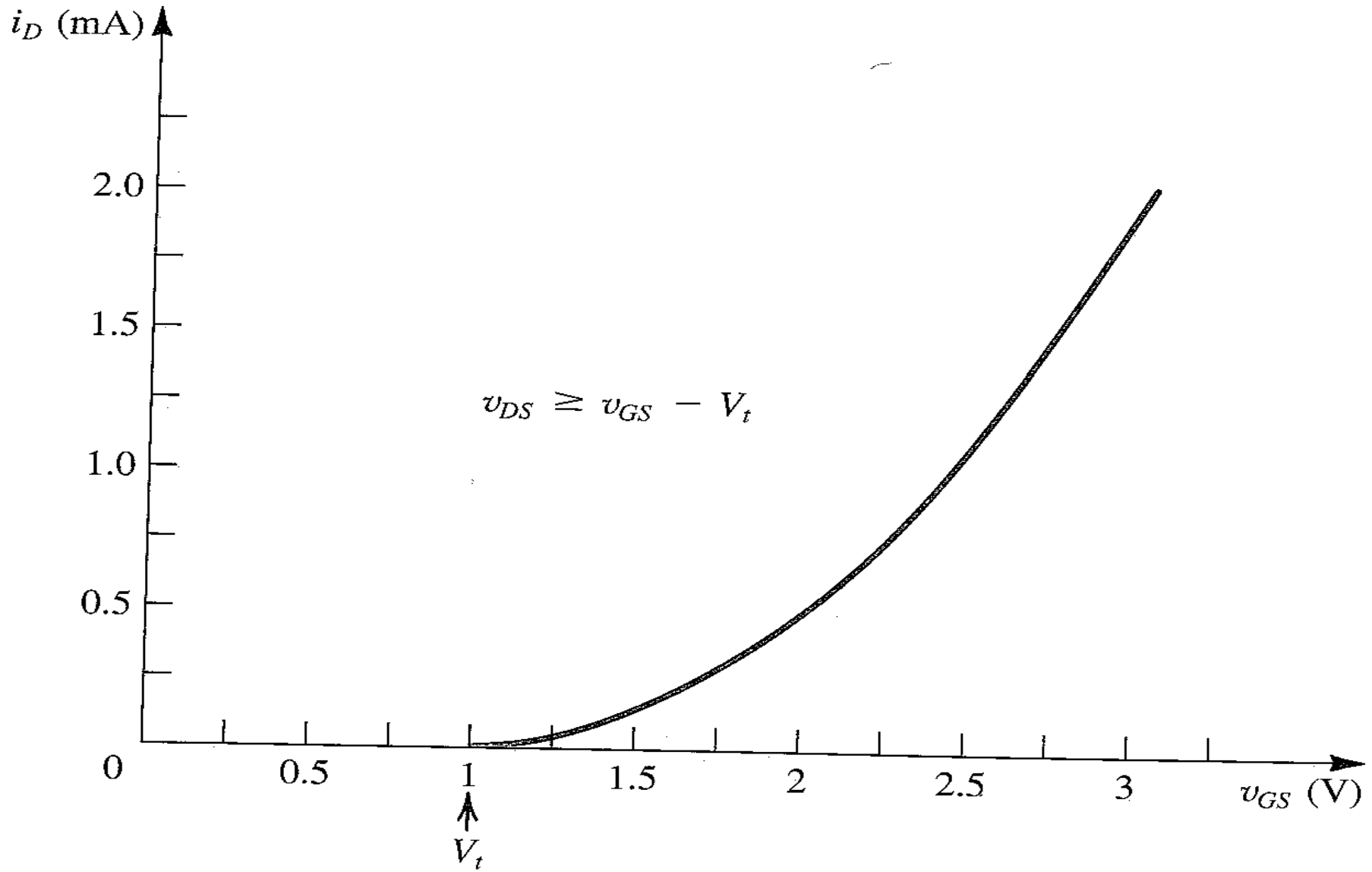


FIG 4.13 SHOWS THE LARGE SIGNAL EQUIVALENT – CIRCUIT MODEL OF AN *n*-CHANNEL MOSFET OPERATING IN THE SATURATION REGION.

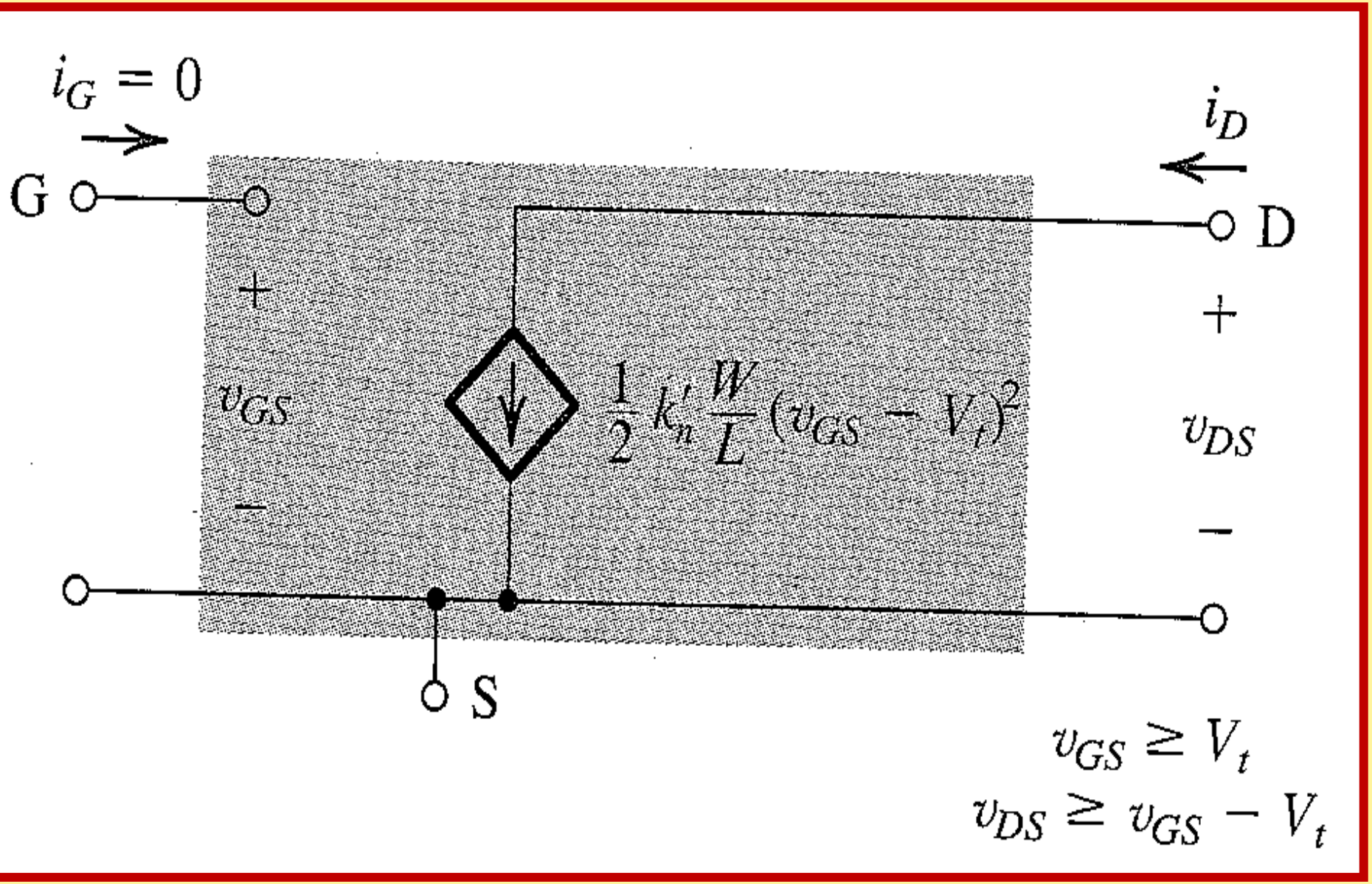
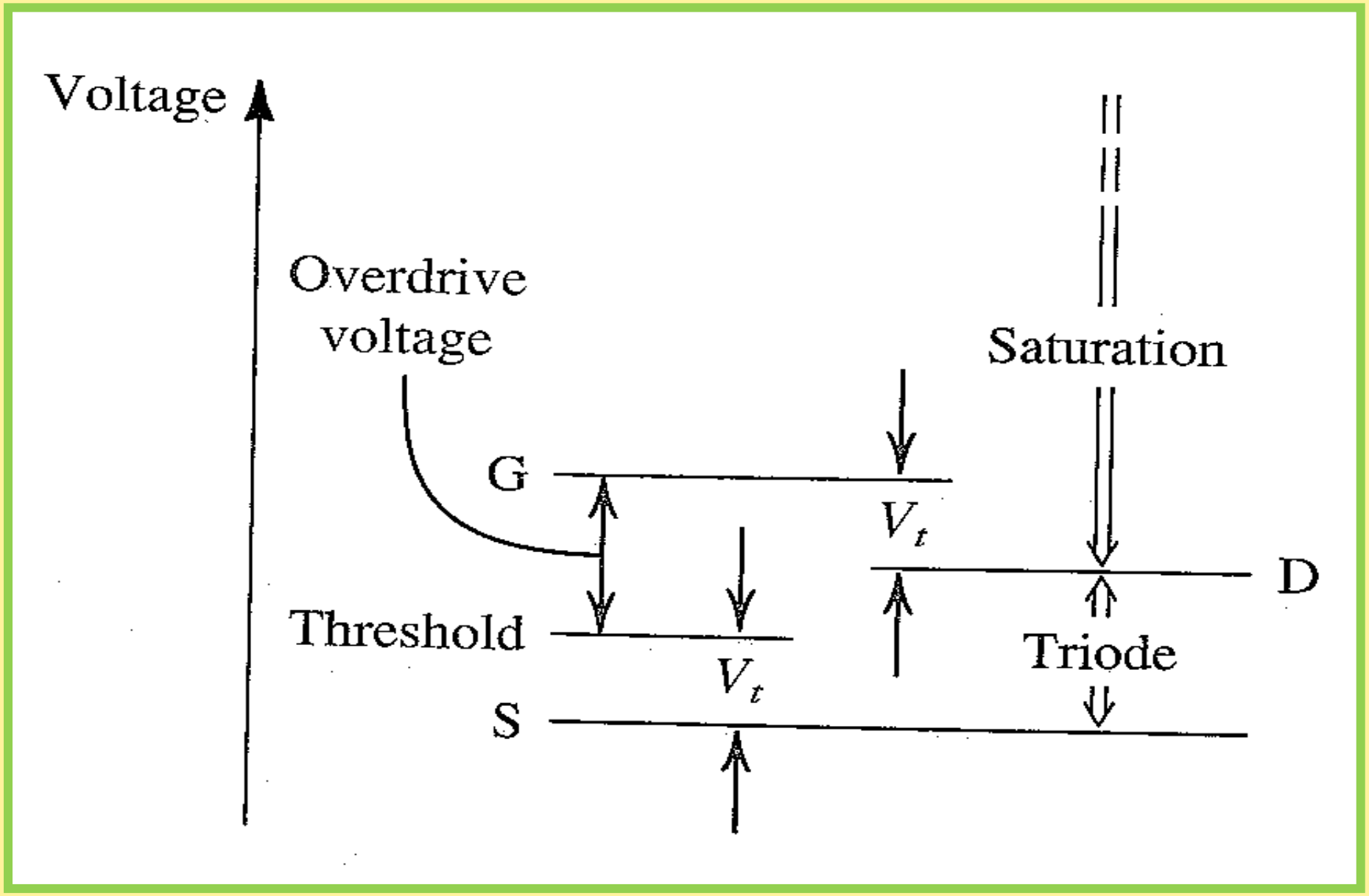


FIG 4.14 SHOWS THE RELATIVE LEVELS OF THE TERMINAL VOLTAGES OF THE ENHANCEMENT NMOS TRANSISTOR FOR OPERATION IN THE TRIODE REGION AND IN THE SATURATION REGION.



Finite Output Resistance in Saturation

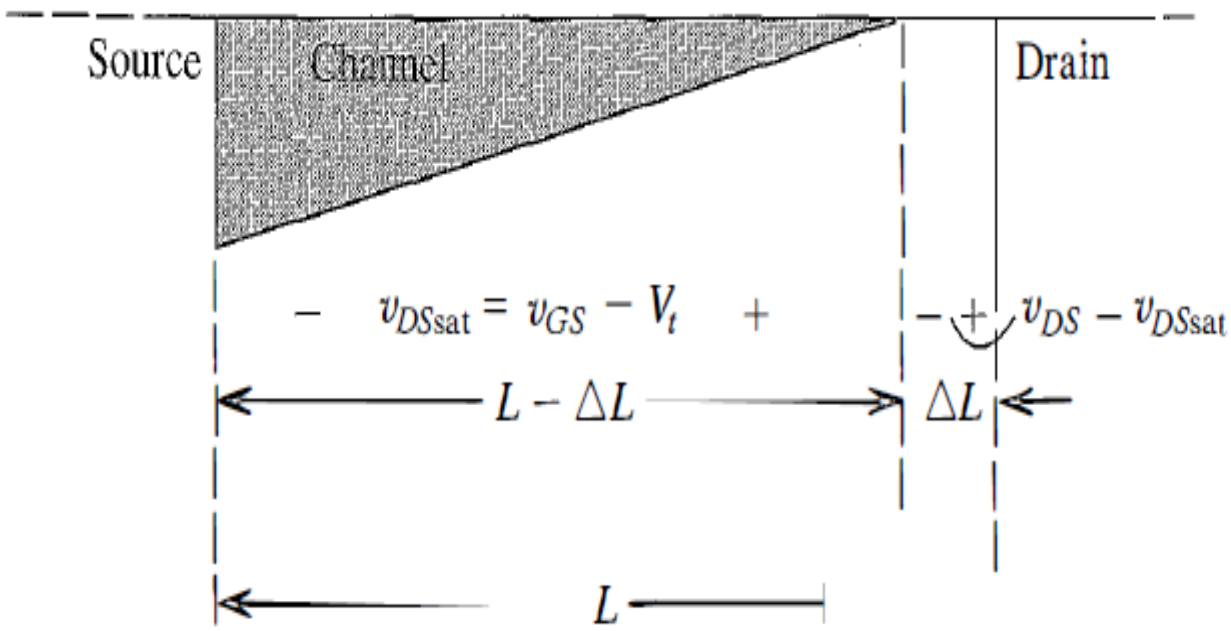


FIGURE 4.15 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

To account for the dependence of i_D on v_{DS} in saturation, we replace L in Eq. (4.20) with $L - \Delta L$ to obtain

$$i_D = \frac{1}{2}k_n' \frac{W}{L - \Delta L}(v_{GS} - V_t)^2$$

$$= \frac{1}{2}k_n' \frac{W}{L} \frac{1}{1 - (\Delta L / L)}(v_{GS} - V_t)^2$$

$$\cong \frac{1}{2}k_n' \frac{W}{L}\left(1 + \frac{\Delta L}{L}\right)(v_{GS} - V_t)^2$$

where we have assumed that $(\Delta L / L) \ll 1$. Now, if we assume that ΔL is proportional to v_{DS},

$$\Delta L = \lambda' v_{DS}$$

where λ' is a process-technology parameter with the dimensions of μm/V, we obtain for i_D,

$$i_D = \frac{1}{2}k_n' \frac{W}{L}\left(1 + \frac{\lambda'}{L} v_{DS}\right)(v_{GS} - V_t)^2$$

Usually, λ'/L is denoted λ,

$$\lambda = \frac{\lambda'}{L}$$

It follows that λ is a process-technology parameter with the dimensions of V^{-1} and that, for a given process, λ is inversely proportional to the length selected for the channel. In terms of λ, the expression for i_D becomes

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \qquad (4.22)$$

A typical set of i_D–v_{DS} characteristics showing the effect of channel-length modulation is displayed in Fig. 4.16. The observed linear dependence of i_D on v_{DS} in the saturation region is represented in Eq. (4.22) by the factor $(1 + \lambda v_{DS})$. From Fig. 4.16 we observe that when the straight-line i_D–v_{DS} characteristics are extrapolated they intercept the v_{DS}-axis at the point $v_{DS} = -V_A$, where V_A is a positive voltage. Equation (4.22), however, indicates that $i_D =$

at $v_{DS} = -1/\lambda$. It follows that

$$V_A = \frac{1}{\lambda}$$

and thus V_A is a process-technology parameter with the dimensions of V. For a given process, V_A is proportional to the channel length L that the designer selects for a MOSFET. Just as in the case of λ, we can isolate the dependence of V_A on L by expressing it as

$$V_A = V_A' L$$

where V_A' is entirely process-technology dependent with the dimensions of V/μm. Typically, V_A' falls in the range of 5 V/μm to 50 V/μm. The voltage V_A is usually referred to as the Early voltage, after J.M. Early, who discovered a similar phenomenon for the BJT (Chapter 5).

resistance r_o as

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\text{ constant}} \tag{4.23}$$

and using Eq. (4.22) results in

$$r_o = \left[\lambda \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_t)^2\right]^{-1} \tag{4.24}$$

which can be written as

$$r_o = \frac{1}{\lambda I_D} \tag{4.25}$$

or, equivalently,

$$r_o = \frac{V_A}{I_D} \tag{4.26}$$

where I_D is the drain current *without* channel-length modulation taken into account; that is,

$$I_D = \frac{1}{2} k_n' \frac{W}{L}(V_{GS} - V_t)^2$$

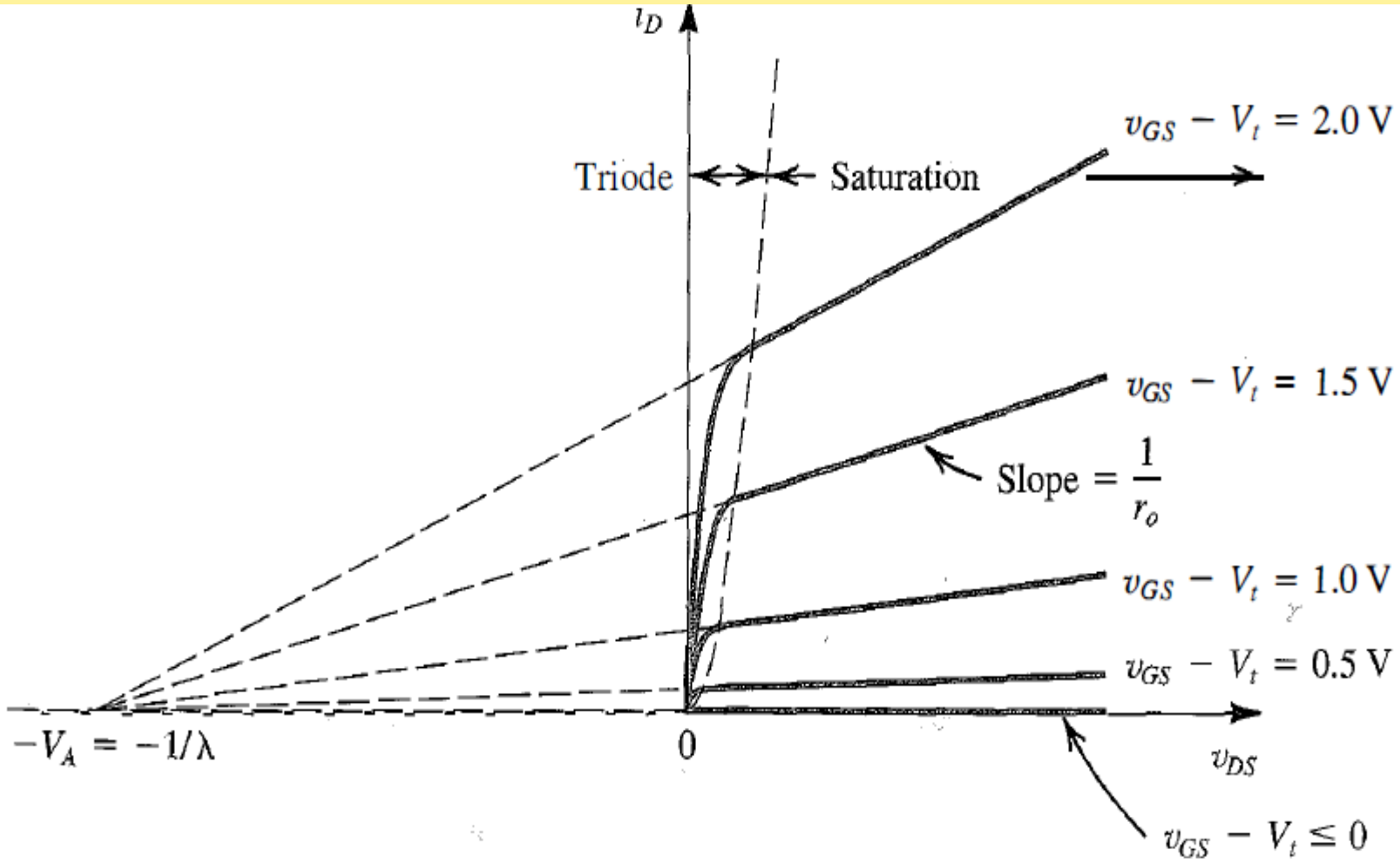


FIGURE 4.16 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

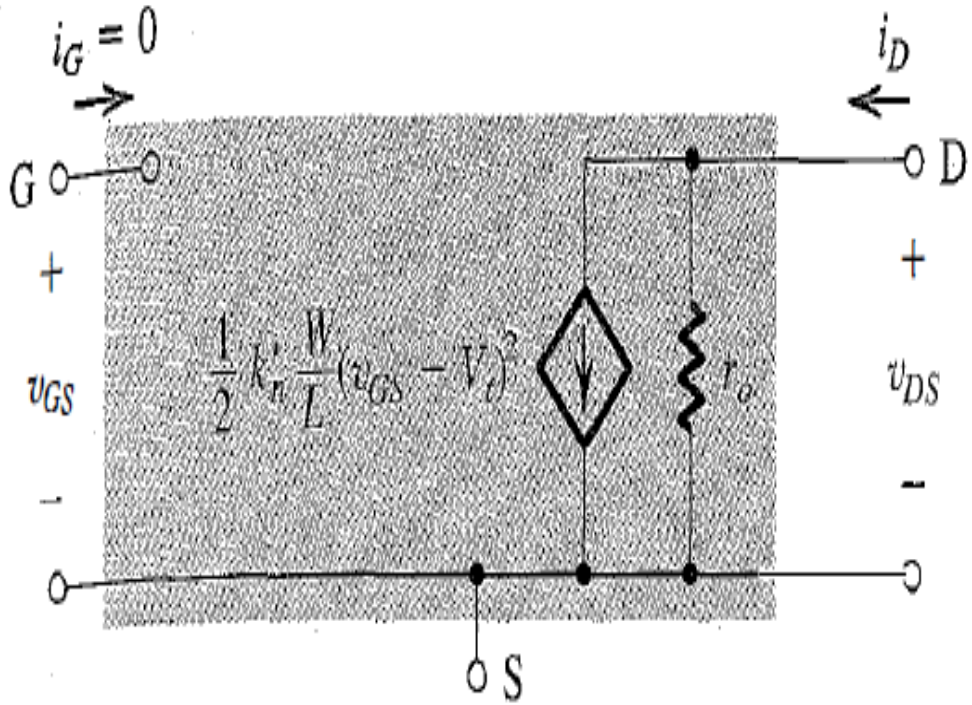
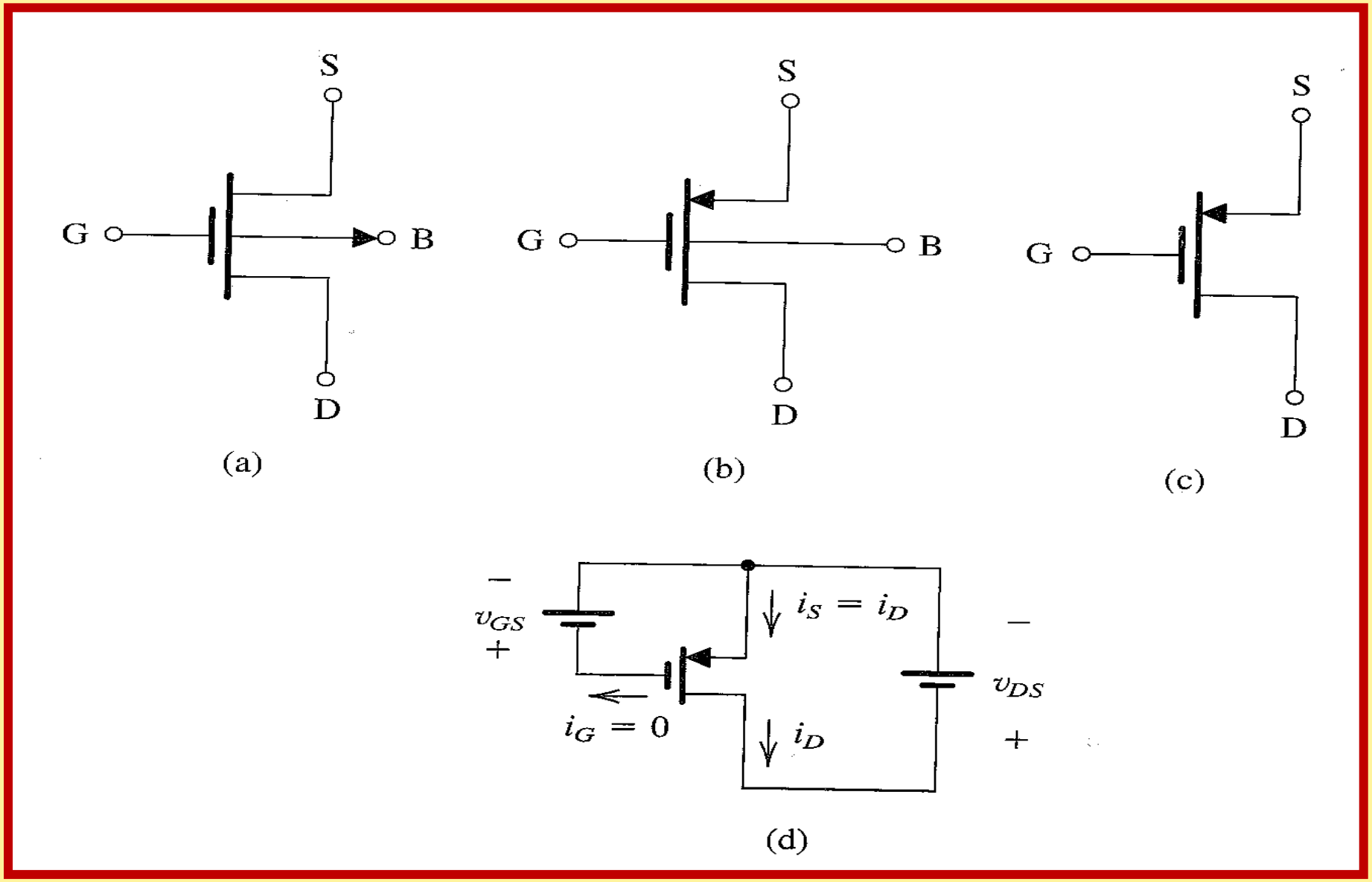


FIGURE 4.17 Large-signal equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (4.22).

FIG 4.18 (A) SHOWS THE CIRCUIT SYMBOL FOR THE P-CHANNEL ENHANCEMENT TYPE MOSFET.(B) MODIFIED SYMBOL WITH AN ARROWHEAD ON THE SOURCE LEAD. (C) SIMPLIFIED CIRCUIT SYMBOL FOR THE CASE WHERE THE SOURCE IS CONNECTED TO THE BODY . (D) THE MOSFET WITH VOLTAGES APPLIED AND THE DIRECTIONS OF THE CURRENT FLOW INDICATED. NOTE THAT VGS AND VDS ARE NEGATIVE AND ID FLOWS OUT OF THE DRAIN TERMINAL.



or, equivalently,

$$v_{SG} \geq |V_t|$$

and apply a drain voltage that is more negative than the source voltage (i.e., v_{DS} is negative or, equivalently, v_{SD} is positive). The current i_D flows out of the drain terminal, as indicated in the figure. To operate in the triode region v_{DS} must satisfy

$$v_{DS} \geq v_{GS} - V_t \quad \text{(Continuous channel)} \tag{4.28}$$

that is, the drain voltage must be higher than the gate voltage by at least $|V_t|$. The current i_D is given by the same equation as for NMOS, Eq. (4.11), except for replacing k_n' with k_p',

$$i_D = k_p' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \tag{4.29}$$

where v_{GS}, V_t, and v_{DS} are negative and the transconductance parameter k_p' is given by

$$k_p' = \mu_p C_{ox} \tag{4.30}$$

where μ_p is the mobility of holes in the induced p channel. Typically, $\mu_p = 0.25$ to $0.5\mu_n$ and is process-technology dependent.

To operate in saturation, v_{DS} must satisfy the relationship

$$v_{DS} \leq v_{GS} - V_t \quad \text{(Pinched-off channel)} \tag{4.31}$$

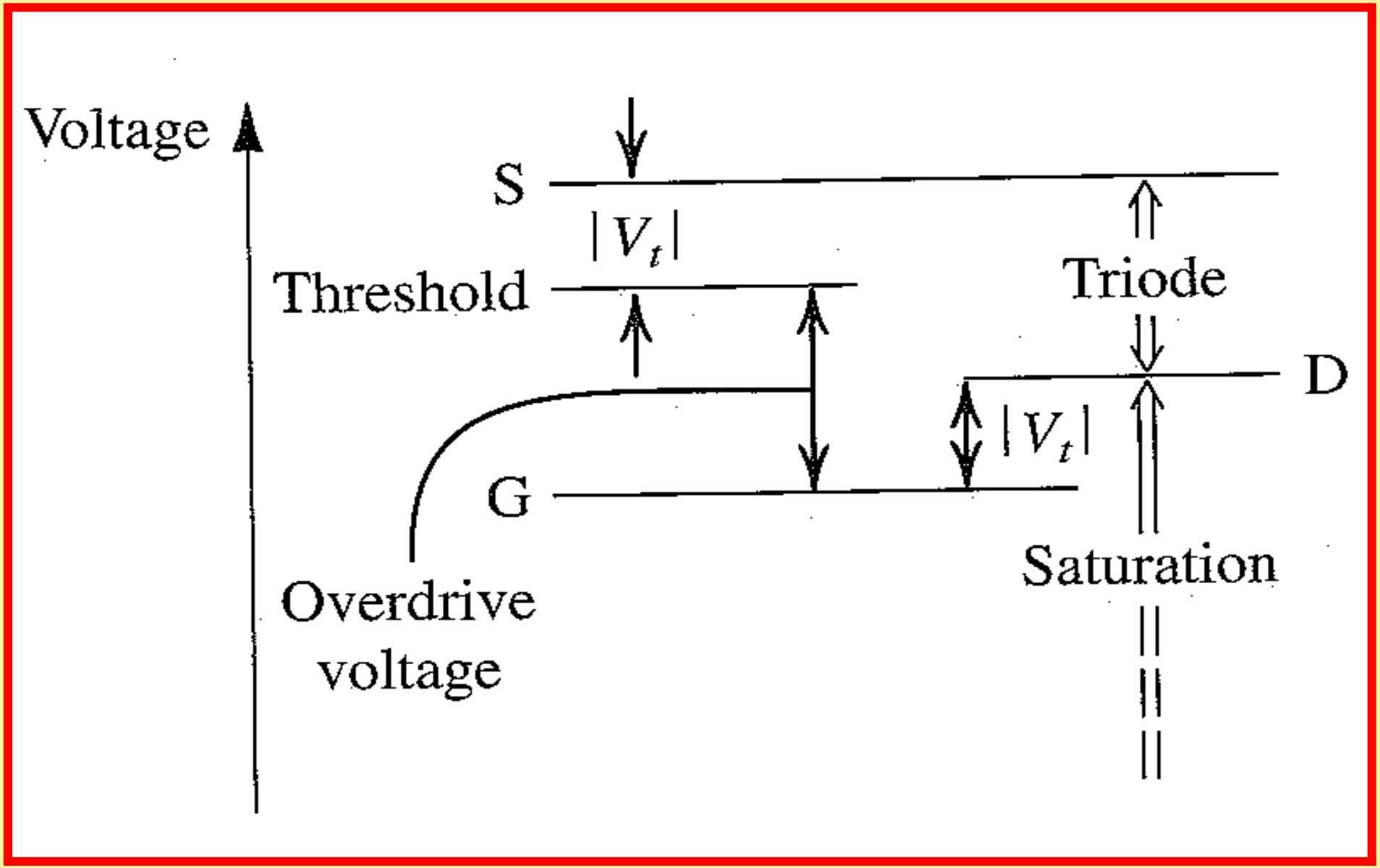
that is, the drain voltage must be lower than (gate voltage + $|V_t|$). The current i_D is given by the same equation used for NMOS, Eq. (4.22), again with k_n' replaced with k_p',

$$i_D = \frac{1}{2} k_p' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \tag{4.32}$$

where v_{GS}, V_t, λ, and v_{DS} are all negative. We should note, however, that in evaluating r_o using Eqs. (4.24) through (4.26), the magnitudes of λ and V_A should be used.

To recap, to turn a PMOS transistor on, the gate voltage has to be made lower than that of the source by at least $|V_t|$. To operate in the triode region, the drain voltage has to exceed that of the gate by at least $|V_t|$; otherwise, the PMOS operates in saturation.

FIG 4.19 SHOWS THE RELATIVE LEVELS OF THE TERMINAL VOLTAGES OF THE ENHANCEMENT TYPE PMOS TRANSISTOR FOR OPERATION IN THE TRIODE REGION AND IN THE SATURATION REGION.



4.4 An enhancement type NMOS transistor with V_t=0.7V has its source terminal grounded and a 1.5V dc applied to the gate. In what region does the device operate for

a) $V_{D=}$0.5V b) V_D= 0.9V c) $V_{D=}$3V

solution: The MOSFET operates in- triode region when $V_{DS}<V_{Ov}$ and in saturation region when $V_{DS}>V_{OV}$

here$V_{ov}=V_{GS}-V_t$= 1.5 - 0.7=0.8V

case a) when $V_D=V_{DS}$=0.5V is applied

$V_{DS}<V_{GS}-V_t$

Device operates in triode region.

Case b) when V_{DS}=0.9V

$V_{DS}> V_{GS} -V_t$

Device operates in saturation region.

Case c) when V_{DS}=3V

$V_{DS}> V_{GS}-V_t$

Device operates in saturation region.

MOSFET CIRCUITS AT DC
EXAMPLE 4.2

Design the circuit of Fig. 4.20 so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu$A/V^2, $L = 1\ \mu$m, and $W = 32\ \mu$m. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

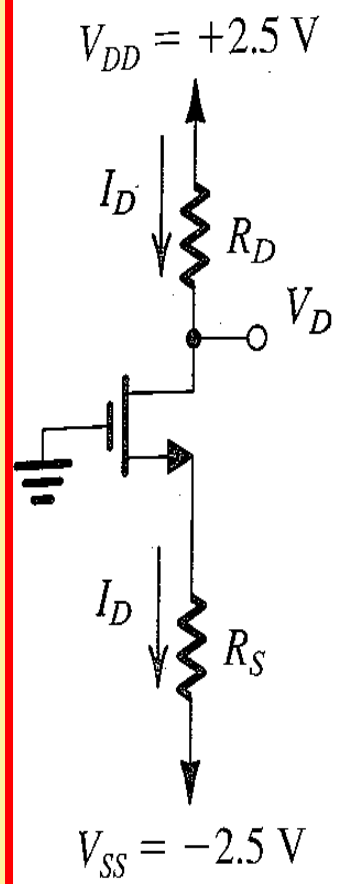


FIGURE 4.20 Circuit for Example 4.2.

Solution for Example 4.2

Solution

Since $V_D = 0.5$ V is greater than V_G, this means the NMOS transistor is operating in the saturation region, and we use the saturation-region expression of i_D to determine the required value of V_{GS},

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Substituting $V_{GS} - V_t = V_{OV}$, $I_D = 0.4$ mA $= 400$ μA, $\mu_n C_{ox} = 100$ μA/V^2, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 4.20, we note that the gate is at ground potential. Thus the source must be at -1.2 V, and the required value of R_S can be determined from

$$R_S = \frac{V_S - V_{SS}}{I_D}$$

$$= \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega$$

To establish a dc voltage of +0.5 V at the drain, we must select R_D as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega$$

EXAMPLE 4.3

Design the circuit in Fig. 4.21 to obtain a current I_D of 80 μA. Find the value required for R, and find the dc voltage V_D. Let the NMOS transistor have $V_t = 0.6$ V, $\mu_n C_{ox} = 200\ \mu\text{A/V}^2$, $L = 0.8\ \mu$m, and $W = 4\ \mu$m. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

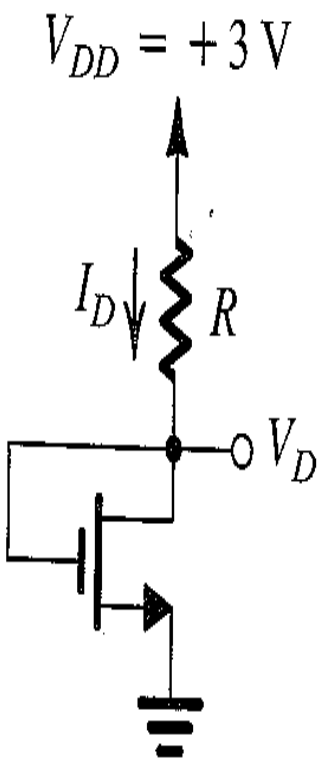


FIGURE 4.21 Circuit for Example 4.3.

SOLUTION FOR EXAMPLE 4.3

Solution

Because $V_{DG} = 0$, $V_D = V_G$ and the FET is operating in the saturation region. Thus,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

from which we obtain V_{OV} as

$$V_{OV} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$$

$$= \sqrt{\frac{2 \times 80}{200 \times (4/0.8)}} = 0.4 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.6 + 0.4 = 1 \text{ V}$$

and the drain voltage will be

$$V_D = V_G = +1 \text{ V}$$

The required value for R can be found as follows:

$$R = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{3 - 1}{0.080} = 25 \text{ k}\Omega$$

EXAMPLE 4.4

Design the circuit in Fig. 4.22 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2.

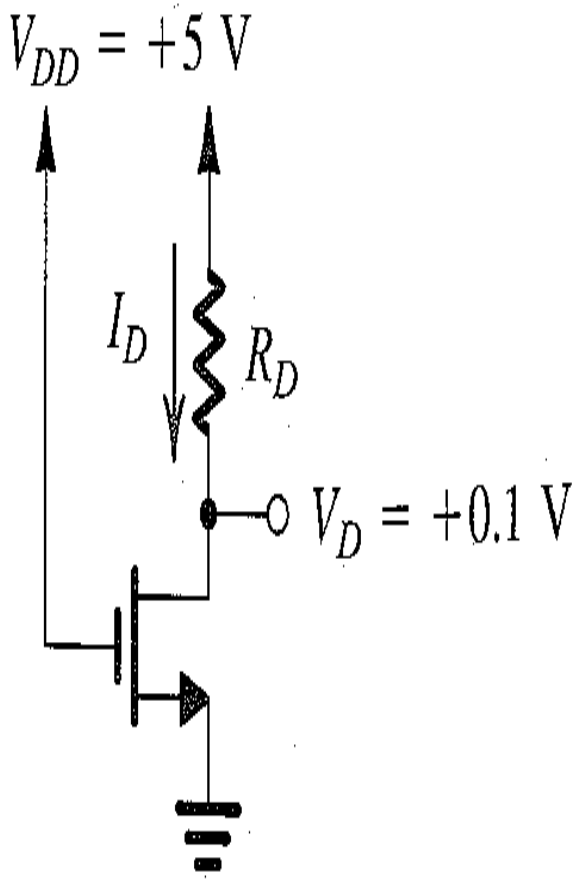


FIGURE 4.22 Circuit for Example 4.4.

Solution

Since the drain voltage is lower than the gate voltage by 4.9 V and $V_t = 1$ V, the MOSFET is operating in the triode region. Thus the current I_D is given by

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = 1 \times \left[(5-1)\times 0.1 - \frac{1}{2}\times 0.01\right]$$

$$= 0.395 \text{ mA}$$

The required value for R_D can be found as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega$$

In a practical discrete-circuit design problem one selects the closest standard value available for, say, 5% resistors—in this case, 12 kΩ; see Appendix G. Since the transistor is operating in the triode region with a small V_{DS}, the effective drain-to-source resistance can be determined as follows:

$$r_{DS} = \frac{V_{DS}}{I_D}$$

$$= \frac{0.1}{0.395} = 253 \ \Omega$$

EXAMPLE 4.5

EXAMPLE 4.5

Analyze the circuit shown in Fig. 4.23(a) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

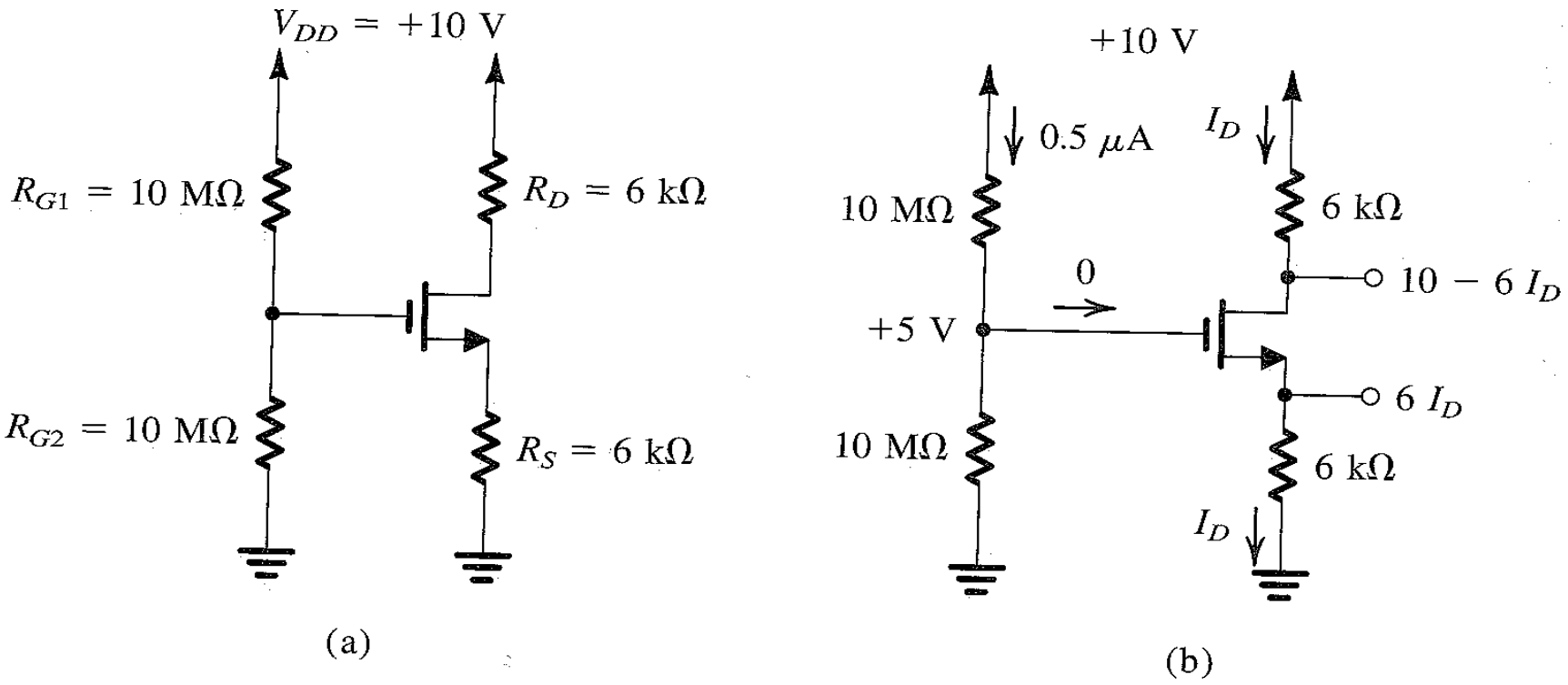


FIGURE 4.23 **(a)** Circuit for Example 4.5. **(b)** The circuit with some of the analysis details shown.

SOLUTION FOR EXAMPLE 4.5

Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 10-MΩ resistors,

$$V_G = V_{DD}\frac{R_{G2}}{R_{G2}+R_{G1}} = 10\times\frac{10}{10+10} = +5\text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 4.23(b). Since the voltage at the gate is 5 V and the voltage at the source is I_D (mA) × 6 (kΩ) = $6I_D$, we have

$$V_{GS} = 5 - 6I_D$$

Thus I_D is given by

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2$$

$$= \frac{1}{2}\times 1\times(5-6I_D-1)^2$$

which results in the following quadratic equation in I_D:

$$18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for I_D: 0.89 mA and 0.5 mA. The first value results in a source voltage of $6\times 0.89 = 5.34$, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5\text{ mA}$$
$$V_S = 0.5\times 6 = +3\text{ V}$$
$$V_{GS} = 5-3 = 2\text{ V}$$
$$V_D = 10-6\times 0.5 = +7\text{ V}$$

Since $V_D > V_G - V_t$, the transistor is operating in saturation, as initially assumed.

EXAMPLE 4.6

Design the circuit of Fig. 4.24 so that the transistor operates in saturation with $I_D = 0.5$ mA and $V_D = +3$ V. Let the enhancement-type PMOS transistor have $V_t = -1$ V and $k_p'(W/L) = 1$ mA/V^2. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?

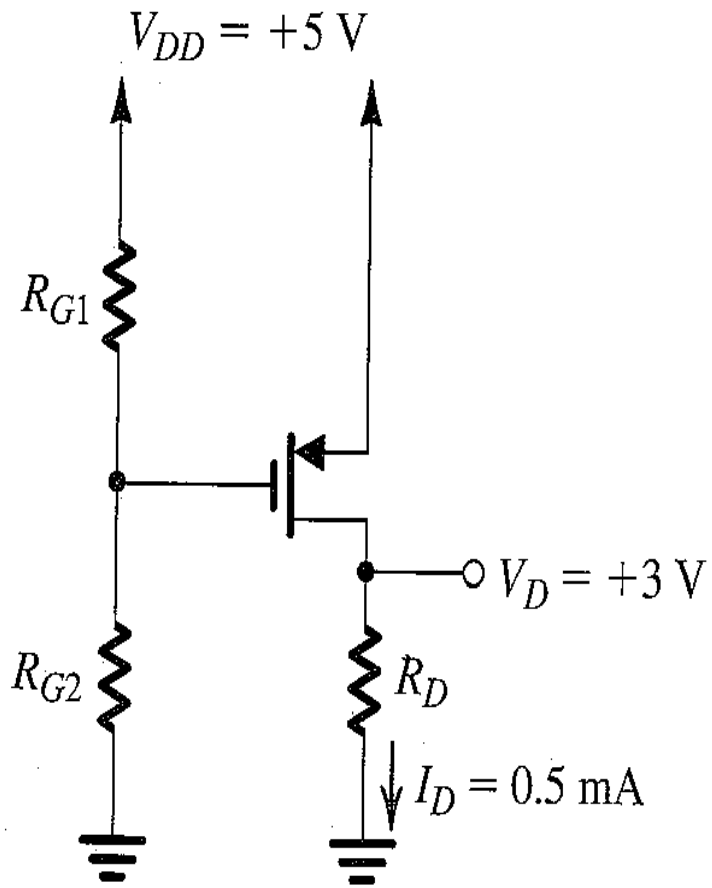


FIGURE 4.24 Circuit for Example 4.6.

SOLUTION FOR EXAMPLE 4.6

Solution

Since the MOSFET is to be in saturation, we can write

$$I_D = \frac{1}{2} k_p' \frac{W}{L} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} k_p' \frac{W}{L} V_{OV}^2$$

Substituting $I_D = 0.5$ mA and $k_p'W/L = 1$ mA/V^2 and recalling that for a PMOS transistor V_{OV} is negative, we obtain

$$V_{OV} = -1 \text{ V}$$

and

$$V_{GS} = V_t + V_{OV} = -1 - 1 = -2 \text{ V}$$

Since the source is at +5 V, the gate voltage must be set to +3 V. This can be achieved by the appropriate selection of the values of R_{G1} and R_{G2}. A possible selection is $R_{G1} = 2$ MΩ and $R_{G2} = 3$ MΩ.

The value of R_D can be found from

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6 \text{ kΩ}$$

Saturation-mode operation will be maintained up to the point that V_D exceeds V_G by $|V_t|$; that is, until

$$V_{D_{\max}} = 3 + 1 = 4 \text{ V}$$

This value of drain voltage is obtained with R_D given by

$$R_D = \frac{4}{0.5} = 8 \text{ kΩ}$$

FIG 4.26 (a) SHOWS THE BASIC STRUCTURE OF THE COMMON SOURCE AMPLIFIER. (b) SHOWS THE GRAPHICAL CONSTRUCTION TO DETERMINE THE TRANSFER CHARACTERISTIC OF THE AMPLIFIER IN (a).

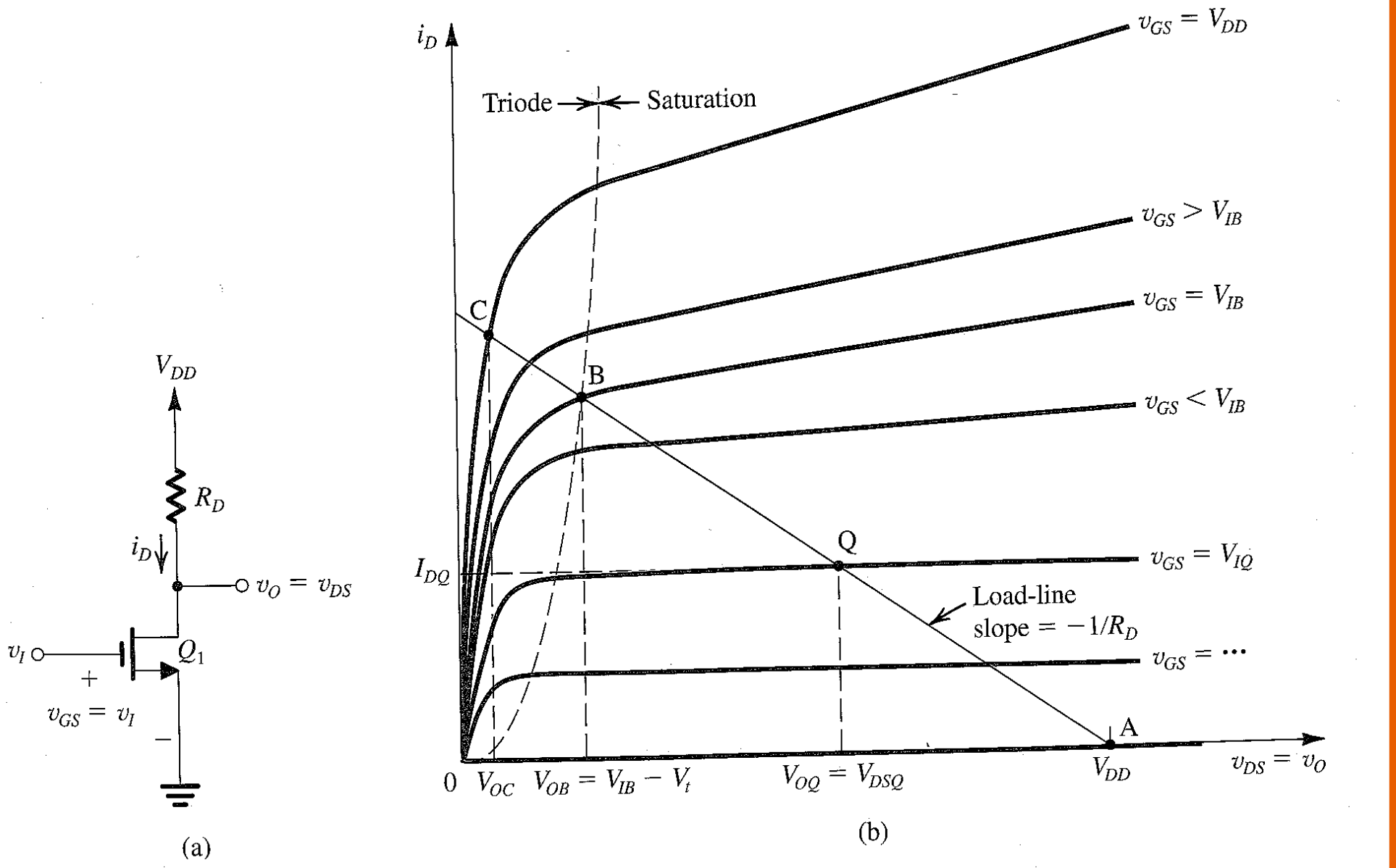
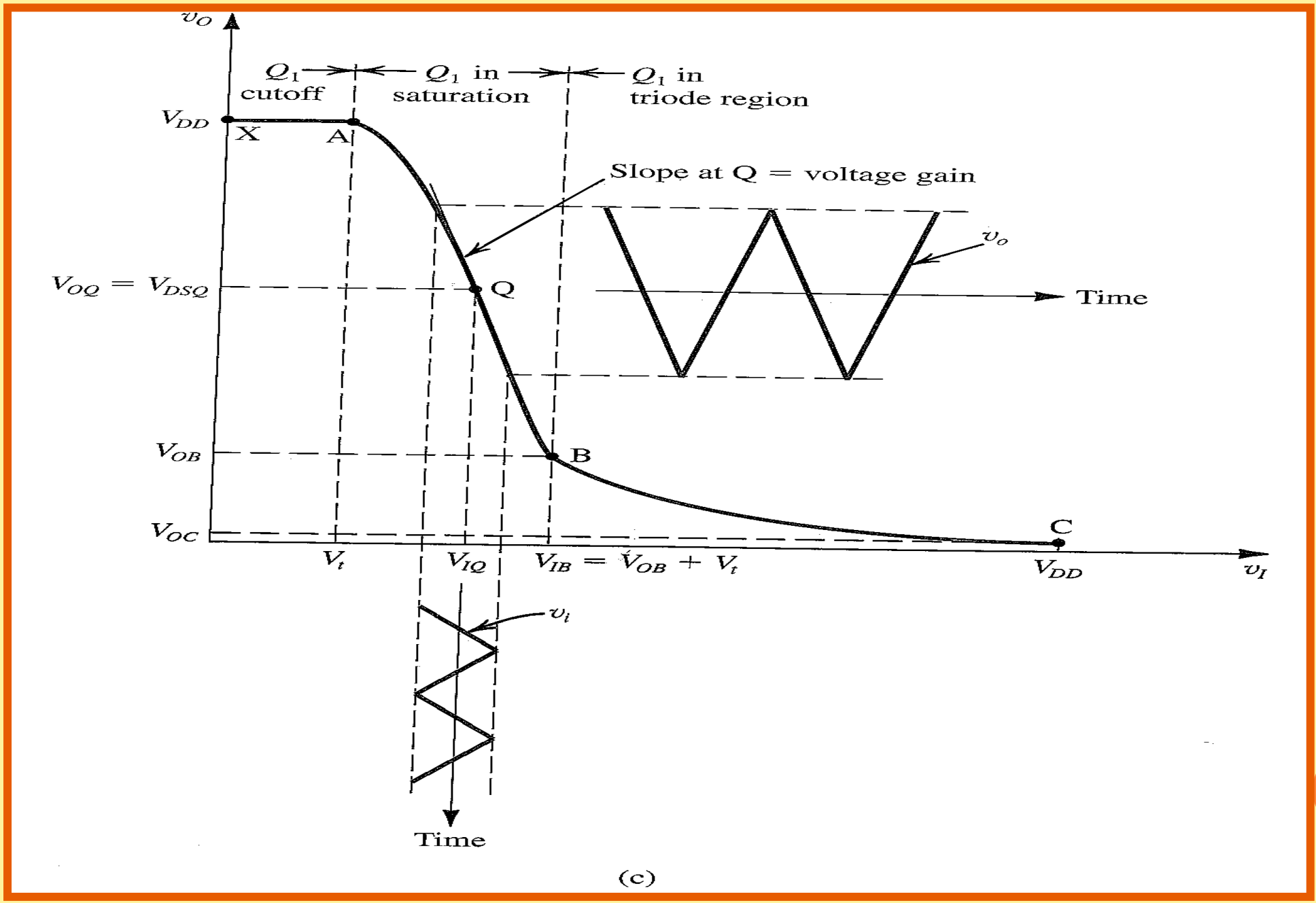


FIG4.26 (C) SHOWS THE TRANSFER CHARACTERISTICS SHOWING OPERATION AS AN AMPLIFIER BIASED AT POINT *Q*.



LARGE-SIGNAL OPERATION-THE TRANSFER CHARACTERISTIC

$$v_O = v_{DS} = V_{DD} - R_D i_D$$

4.4.2 Graphical Derivation of the Transfer Characteristic

The operation of the common-source circuit is governed by the MOSFET's i_D–v_{DS} characteristics and by the relationship between i_D and v_{DS} imposed by connecting the drain to the power supply V_{DD} via resistor R_D, namely

$$v_{DS} = V_{DD} - R_D i_D \tag{4.36}$$

or, equivalently,

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS} \tag{4.37}$$

Figure 4.26(b) shows a sketch of the MOSFET's i_D–v_{DS} characteristic curves superimposed on which is a straight line representing the i_D–v_{DS} relationship of Eq. (4.37). Observe that the straight line intersects the v_{DS}-axis at V_{DD} [since from Eq. (4.36) $v_{DS} = V_{DD}$ at $i_D = 0$] and has a slope of $-1/R_D$. Since R_D is usually thought of as the **load resistor** of the amplifier (i.e., the resistor across which the amplifier provides its output voltage), the straight line in Fig. 4.26(b) is known as the **load line.**

The graphical construction of Fig. 4.26(b) can now be used to determine v_O (equal to v_{DS}) for each given value of v_I ($v_{GS} = v_I$). Specifically, for any given value of v_I, we locate the corresponding i_D–v_{DS} curve and find v_O from the point of intersection of this curve with the load line.

The graphical construction of Fig. 4.26(b) can now be used to determine v_O (equal to v_{DS}) for each given value of v_I ($v_{GS} = v_I$). Specifically, for any given value of v_I, we locate the corresponding i_D–v_{DS} curve and find v_O from the point of intersection of this curve with the load line.

Qualitatively, the circuit works as follows: Since $v_{GS} = v_I$, we see that for $v_I < V_t$, the transistor will be cut off, i_D will be zero, and $v_O = v_{DS} = V_{DD}$. Operation will be at the point labeled A. As v_I exceeds V_t, the transistor turns on, i_D increases, and v_O decreases. Since v_O will initially be high, the transistor will be operating in the saturation region. This corresponds to points along the segment of the load line from A to B. We have identified a particular point in this region of operation and labeled it Q. It is obtained for $V_{GS} = V_{IQ}$ and has the coordinates $V_{OQ} = V_{DSQ}$ and I_{DQ}.

Saturation-region operation continues until v_O decreases to the point that it is below v_I by V_t volts. At this point, $v_{DS} = v_{GS} - V_t$, and the MOSFET enters its triode region of operation. This is indicated in Fig. 4.26(b) by point B, which is at the intersection of the load line and the broken-line curve that defines the boundary between the saturation and the triode regions. Point B is defined by

$$V_{OB} = V_{IB} - V_t$$

For $v_I > V_{IB}$, the transistor is driven deeper into the triode region. Note that because the characteristic curves in the triode region are bunched together, the output voltage decreases slowly towards zero. Here we have identified a particular operating point C obtained for $v_I = V_{DD}$. The corresponding output voltage V_{OC} will usually be very small. This point-by-point determination of the transfer characteristic results in the transfer curve shown in Fig. 4.26(c). Observe that we have delineated its three distinct segments, each corresponding to one of the three regions of operation of MOSFET Q_1. We have also labeled the critical points of the transfer curve in correspondence with the points in Fig. 4.26(b).

4.4.3 Operation as a Switch

When the MOSFET is used as a switch, it is operated at the extreme points of the transfer curve. Specifically, the device is turned off by keeping $v_I < V_t$ resulting in operation somewhere on the segment XA with $v_O = V_{DD}$. The switch is turned on by applying a voltage close to V_{DD}, resulting in operation close to point C with v_O very small (at C, $v_O = V_{OC}$). At this juncture we observe that the transfer curve of Fig. 4.26(c) is of the form presented in Section 1.7 for the digital logic inverter. Indeed, the common-source MOS circuit can be used as a logic inverter with the "low" voltage level close to 0 V and the "high" level close to V_{DD}. More elaborate MOS logic inverters are studied in Section 4.10.

4.4.4 Operation as a Linear Amplifier

To operate the MOSFET as an amplifier we make use of the saturation-mode segment of the transfer curve. The device is biased at a point located somewhere close to the middle of the curve; point Q is a good example of an appropriate bias point. The dc bias point is also called the **quiescent point,** which is the reason for labeling it Q. The voltage signal to be amplified v_i is then superimposed on the dc voltage V_{IQ} as shown in Fig. 4.26(c). By keeping v_i sufficiently small to restrict operation to an almost linear segment of the transfer curve, the resulting output voltage signal v_o will be proportional to v_i. That is, the amplifier will be very nearly linear, and v_o will have the same waveform as v_i except that it will be larger by a factor equal to the voltage gain of the amplifier at Q, A_v, where

$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{IQ}} \tag{4.38}$$

Thus the voltage gain is equal to the slope of the transfer curve at the bias point Q. Observe that the slope is negative, and thus the basic CS amplifier is inverting. This should be also evident from the waveforms of v_i and v_o shown in Fig. 4.26(c). It should be obvious that if the amplitude of the input signal v_i is increased, the output signal will become distorted since operation will no longer be restricted to an almost linear segment of the transfer curve.

We shall return to the small-signal operation of the MOSFET in Section 4.6. For the time being, however, we wish to make an important observation about selecting an appropriate location for the bias point Q. Since the output signal will be superimposed on the dc voltage at the drain V_{OQ} or V_{DSQ}, it is important that V_{DSQ} be of such value to allow for the required output signal swing. That is, V_{DSQ} should be lower than V_{DD} by a sufficient amount and higher than V_{OB} by a sufficient amount to allow for the required positive and negative output signal swing, respectively. If V_{DSQ} is too close to V_{DD}, the positive peaks of the output signals might "bump" into V_{DD} and would be clipped off, because the MOSFET would turn off for part of the cycle. We speak of this situation as the circuit not having sufficient "headroom." Similarly, if V_{DSQ} is too close to the boundary of the triode region, the MOSFET would enter the triode region for the part of the cycle near the negative peaks, resulting in a distorted output signal. We speak of this situation as the circuit not having sufficient "legroom." Finally, it is important to note that although we made our comments on the selection of bias-point location in the context of a given transfer curve, the circuit designer also has to decide on a value for R_D, which of course determines the transfer curve. It is therefore more appropriate when considering the location of the bias point Q to do so with reference to the i_D–v_{DS} plane. This point is further illustrated by the sketch in Fig. 4.27.

Analytical Expressions for the Transfer Characteristic

The i–v relationships that describe the MOSFET operation in the three regions—cutoff, saturation, and triode—can be easily used to derive analytical expressions for the three segments of the transfer characteristic in Fig. 4.26(a).

The Cutoff-Region Segment, XA Here, $v_I \leq V_t$, and $v_O = V_{DD}$.

The Saturation-Region Segment, AQB Here, $v_I \geq V_t$, and $v_O \geq v_I - V_t$. Neglecting channel-length modulation and substituting for i_D from

$$i_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_I - V_t)^2$$

into

$$v_O = V_{DD} - R_D i_D$$

gives

$$v_O = V_{DD} - \frac{1}{2}R_D \mu_n C_{ox}\frac{W}{L}(v_I - V_t)^2 \qquad (4.39)$$

We can use this relationship to derive an expression for the incremental voltage gain A_v at a bias point Q at which $v_I = V_{IQ}$ as follows:

$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{IQ}}$$

Thus,

$$A_v = -R_D \mu_n C_{ox} \frac{W}{L}(V_{IQ} - V_t) \tag{4.40}$$

Observe that the voltage gain is proportional to the values of R_D, the transconductance parameter $k_n' = \mu_n C_{ox}$, the transistor aspect ratio W/L, and the overdrive voltage at the bias point $V_{OV} = V_{IQ} - V_t$.

Another simple and very useful expression for the voltage gain can be obtained by substituting $v_I = V_{IQ}$ and $v_O = V_{OQ}$ in Eq. (4.39), utilizing Eq. (4.40), and substituting $V_{IQ} - V_t = V_{OV}$. The result is

$$A_v = -\frac{2(V_{DD} - V_{OQ})}{V_{OV}} \cong -\frac{2V_{RD}}{V_{OV}} \tag{4.41}$$

where V_{RD} is the dc voltage across the drain resistor R_D; that is, $V_{RD} = V_{DD} - V_{OQ}$.

The end point of the saturation-region segment is characterized by

$$V_{OB} = V_{IB} - V_t \tag{4.42}$$

The Triode-Region Segment, BC Here, $v_I \geq V_t$, and $v_O \leq v_I - V_t$. Substituting for i_D by the triode-region expression

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_I - V_t)v_O - \frac{1}{2}v_O^2\right]$$

into

$$v_O = V_{DD} - R_D i_D$$

gives

$$v_O = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}\left[(v_I - V_t)v_O - \frac{1}{2}v_O^2\right]$$

The portion of this segment for which v_O is small is given approximately by

$$v_O \cong V_{DD} - R_D \mu_n C_{ox} \frac{W}{L}(v_I - V_t)v_O$$

which reduces to

$$v_O = V_{DD} \Big/ \left[1 + R_D \mu_n C_{ox} \frac{W}{L}(v_I - V_t)\right] \tag{4.43}$$

We can use the expression for r_{DS}, the drain-to-source resistance near the origin of the i_D–v_{DS} plane (Eq. 4.13),

$$r_{DS} = 1 \Big/ \left[\mu_n C_{ox} \frac{W}{L}(v_I - V_t)\right]$$

together with Eq. (4.43) to obtain

$$v_O = V_{DD}\frac{r_{DS}}{r_{DS} + R_D} \tag{4.44}$$

which makes intuitive sense: For small v_O, the MOSFET operates as a resistance r_{DS} (whose value is determined by v_I), which forms with R_D a voltage divider across V_{DD}. Usually, $r_{DS} \ll R_D$, and Eq. (4.44) reduces to

$$v_O \cong V_{DD}\frac{r_{DS}}{R_D} \tag{4.45}$$

BIASING IN MOS AMPLIFIER CIRCUITS

An appropriate dc operating point or bias point is characterized by a stable and predictable dc drain current ID and by a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region for all expected input-signal levels

Biasing by Fixing V GS

FIG 4.27 SHOWS THE TWO LOAD LINES AND CORRESPONDING BIAS POINTS. BIAS POINT Q_1 DOES NOT LEAVE SUFFICIENT ROOM FOR POSITIVE SIGNAL SWING AT THE DRAIN (TOO CLOSE TO V_{DD}).BIAS POINT Q_2 IS TOO CLOSE TO THE BOUNDARY OF THE TRIODE REGION AND MIGHT NOT ALLOW FOR SUFFICIENT NEGATIVE SIGNAL SWING.

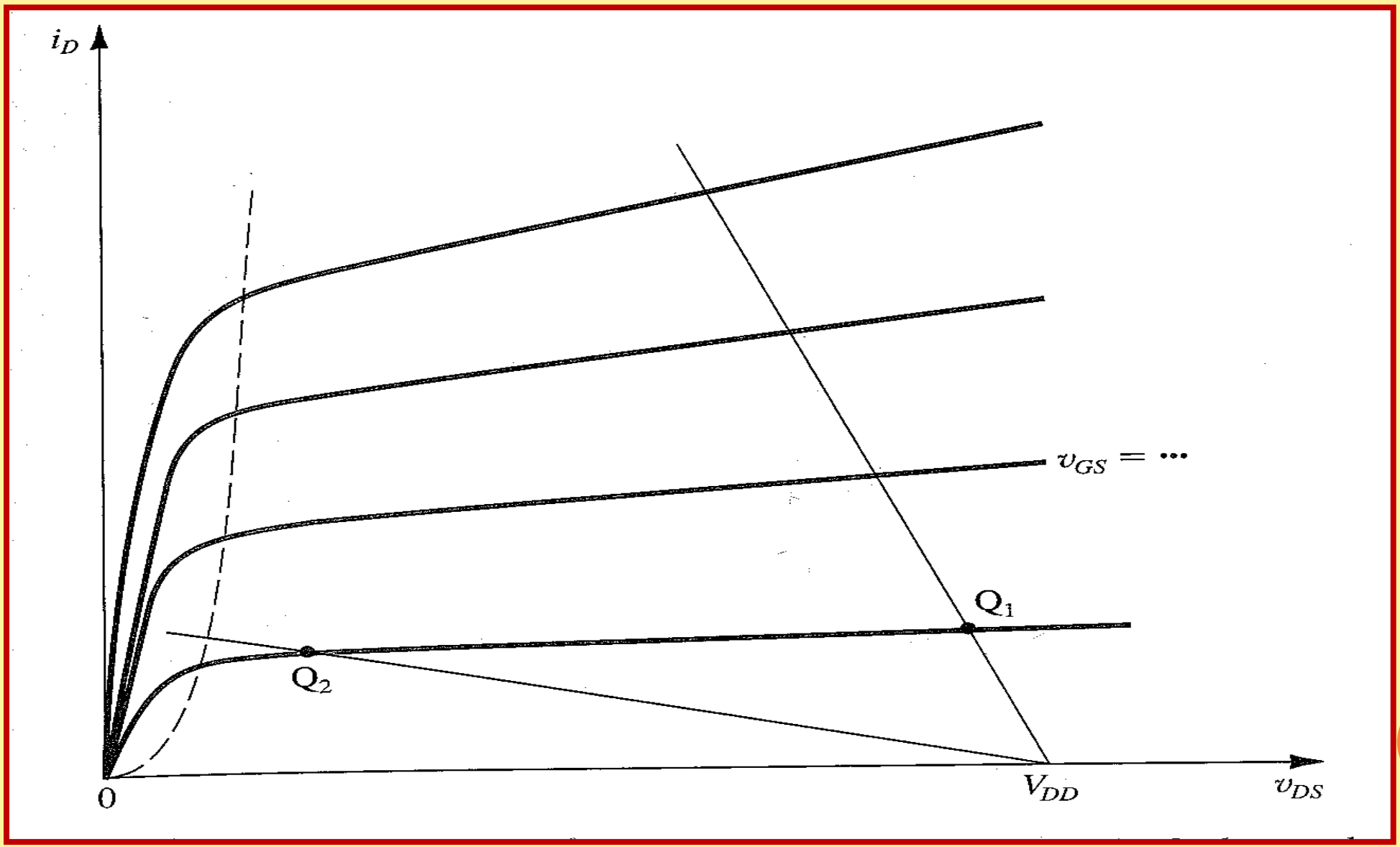


Fig 4.29 shows the use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and 2 represent extremes among units of the same type.

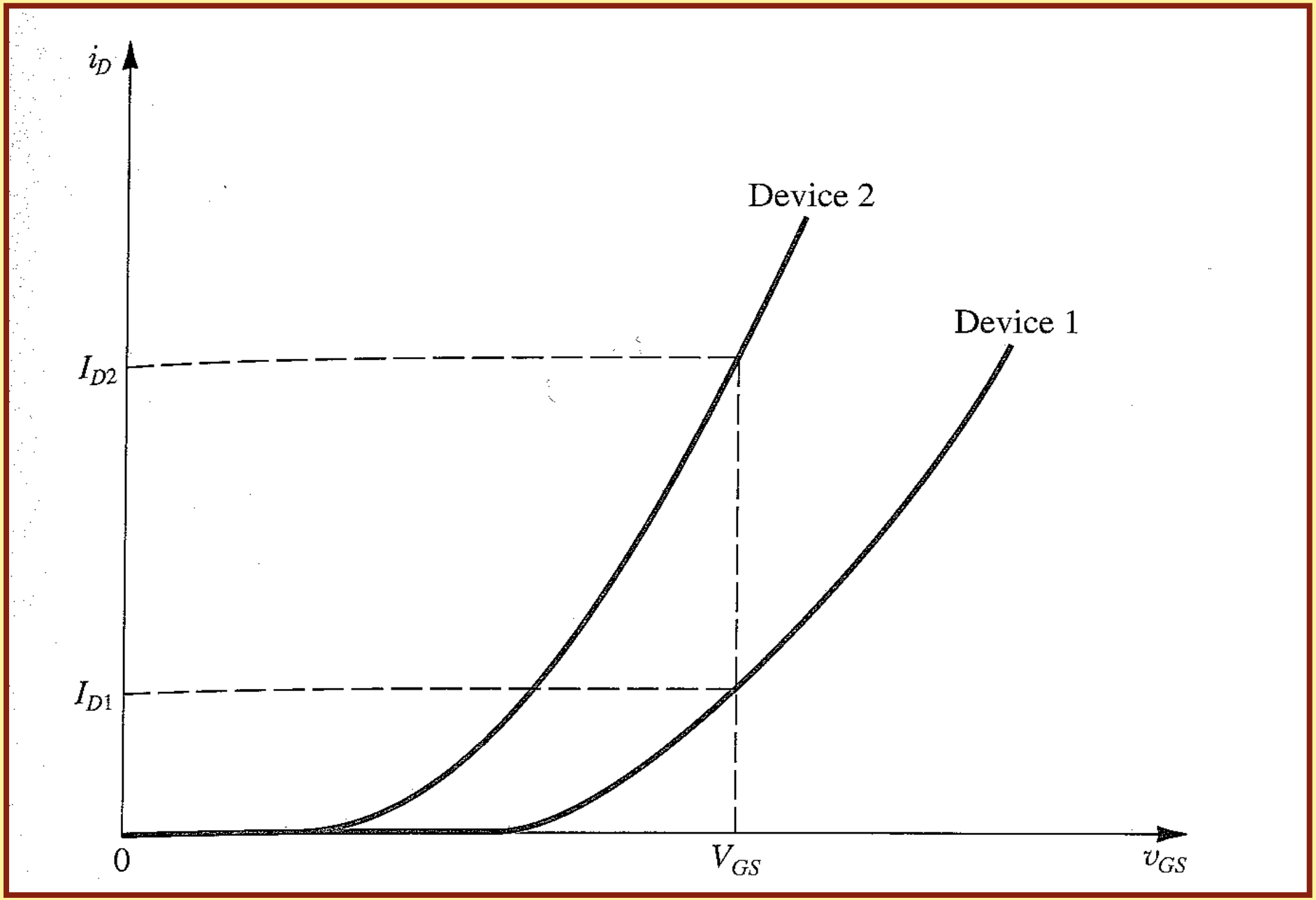
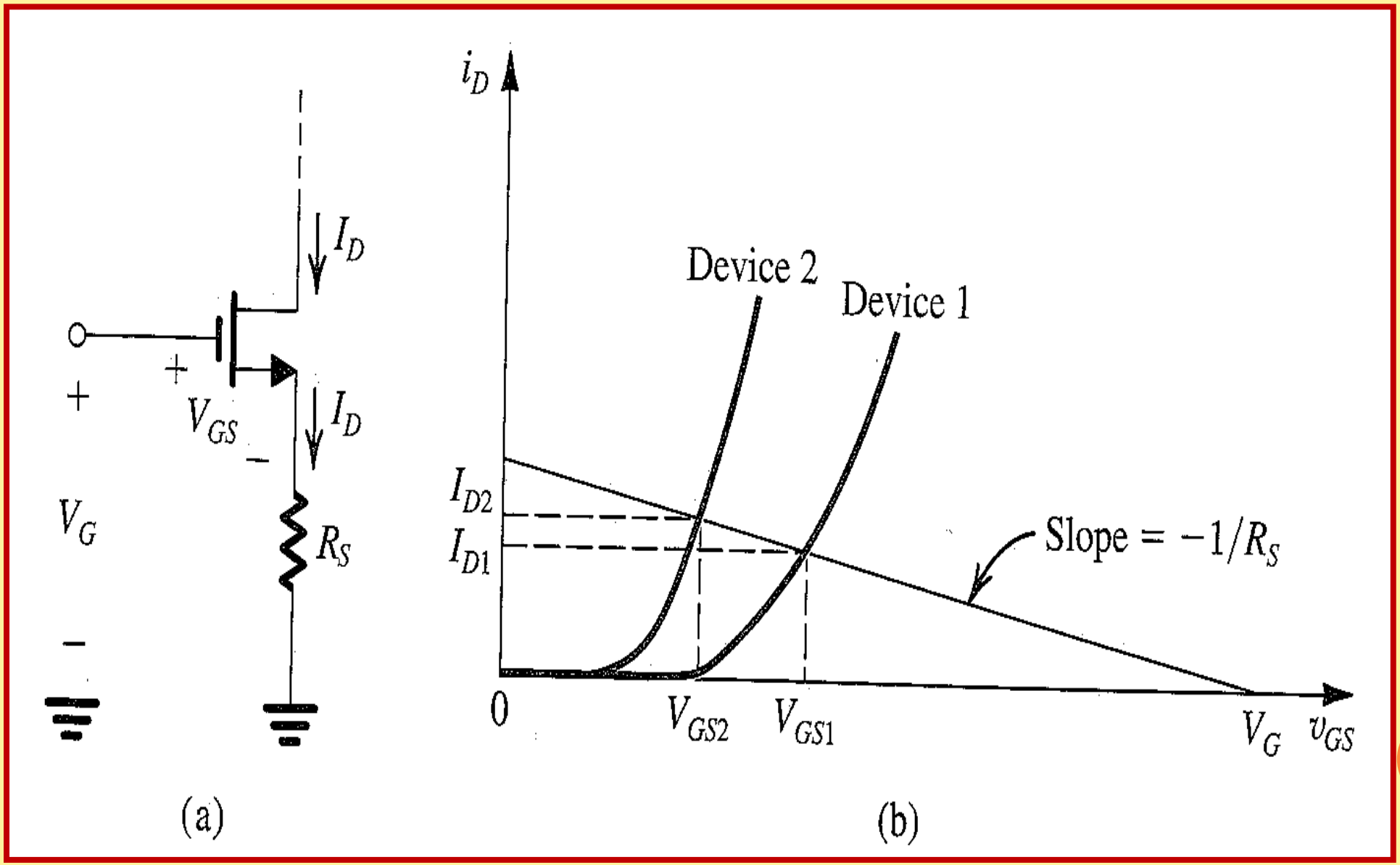


FIG 4.30 SHOWS BIASING USING A FIXED VOLTAGE AT THE GATE, V_G, AND A RESISTANCE IN THE SOURCE LEAD, R_S, (a) BASIC ARRANGEMENT; (b) REDUCED VARIABILITY IN I_D;



An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G, and connecting a resistance in the source lead, as shown in Fig. 4.30(a). For this circuit we can write

$$V_G = V_{GS} + R_S I_D \tag{4.46}$$

Now, if V_G is much greater than V_{GS}, I_D will be mostly determined by the values of V_G and R_S. However, even if V_G is not much larger than V_{GS}, resistor R_S provides *negative feedback*, which acts to stabilize the value of the bias current I_D. To see how this comes about consider the case when I_D increases for whatever reason. Equation (4.46) indicates that since V_G is constant, V_{GS} will have to decrease. This in turn results in a decrease in I_D, a change that is opposite to that initially assumed. Thus the action of R_S works to keep I_D as constant as possible. This negative feedback action of R_S gives it the name **degeneration resistance,** a name that we will appreciate much better at a later point in this text.

Figure 4.30(b) provides a graphical illustration of the effectiveness of this biasing scheme. Here we show the i_D–v_{GS} characteristics for two devices that represent the extremes of a batch of MOSFETs. Superimposed on the device characteristics is a straight line that represents the constraint imposed by the bias circuit—namely, Eq. (4.46). The intersection of this straight line with the i_D–v_{GS} characteristic curve provides the coordinates (I_D and V_{GS}) of the bias point. Observe that compared to the case of fixed V_{GS}, here the variability obtained in I_D is much smaller. Also, note that the variability decreases as V_G and R_S are made larger (providing a bias line that is less steep).

FIG 4.30 SHOWS BIASING USING A FIXED VOLTAGE AT THE GATE, VG, AND A RESISTANCE IN THE SOURCE LEAD, RS, (c) PRACTICAL IMPLEMENTATION USING A SINGLE SUPPLY; (d) COUPLING OF A SIGNAL SOURCE TO THE GATE USING A CAPACITOR CC1; (e) PRACTICAL IMPLEMENTATION USING TWO SUPPLIES.

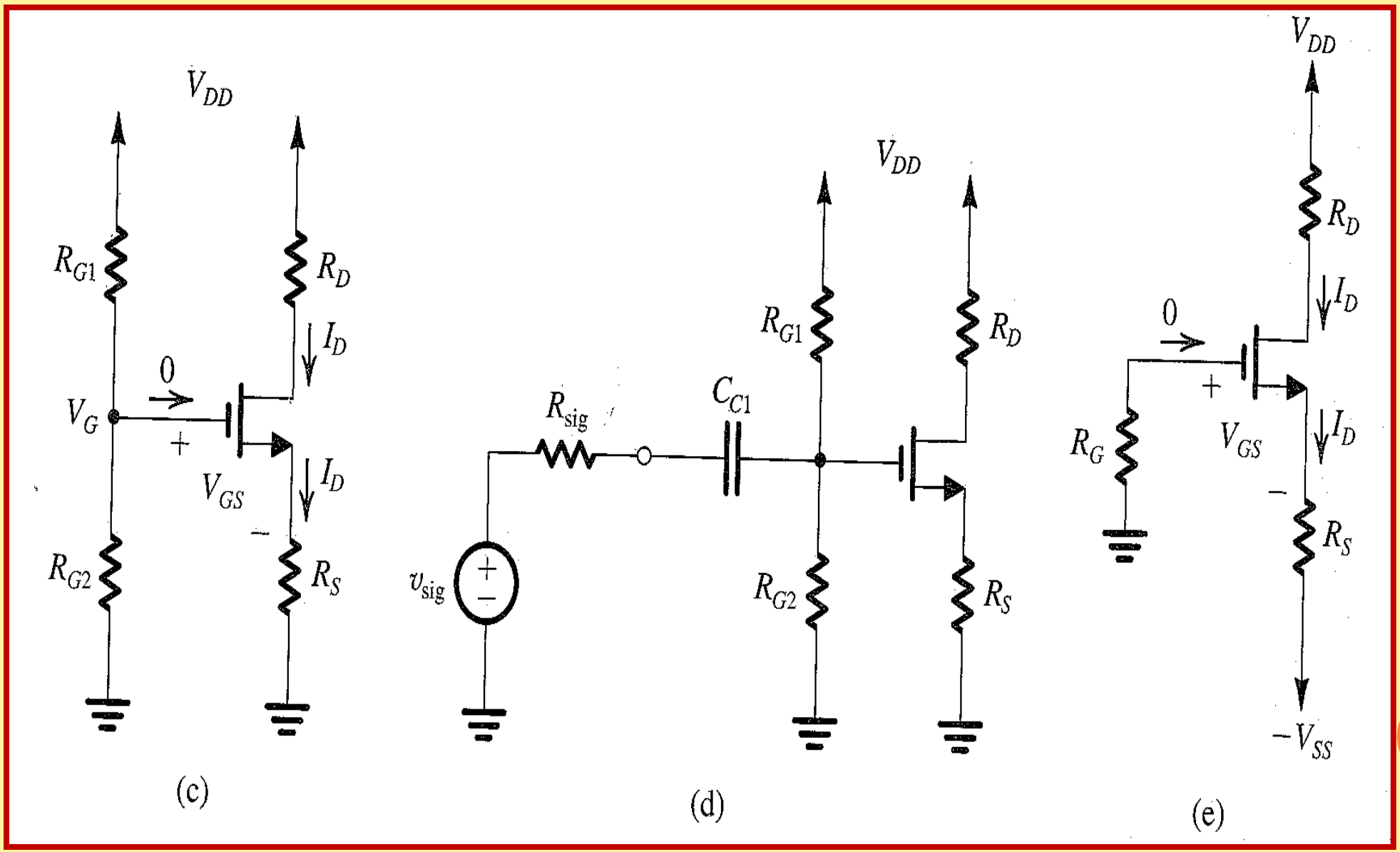
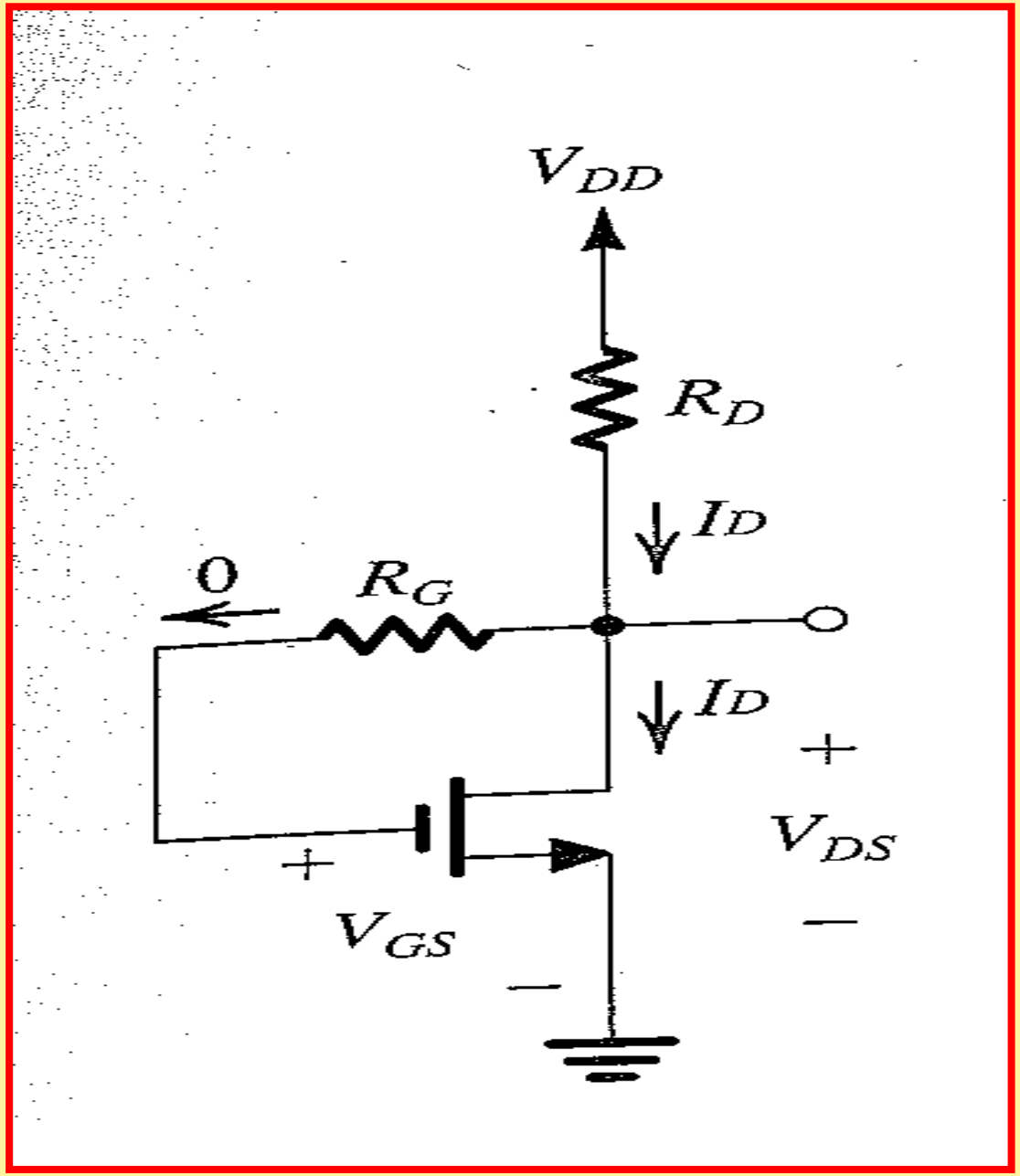


FIG 4.32 SHOWS THE BIASING OF THE MOSFET USING A LARGE DRAIN TO GATE FEEDBACK RESISTOR R_G.



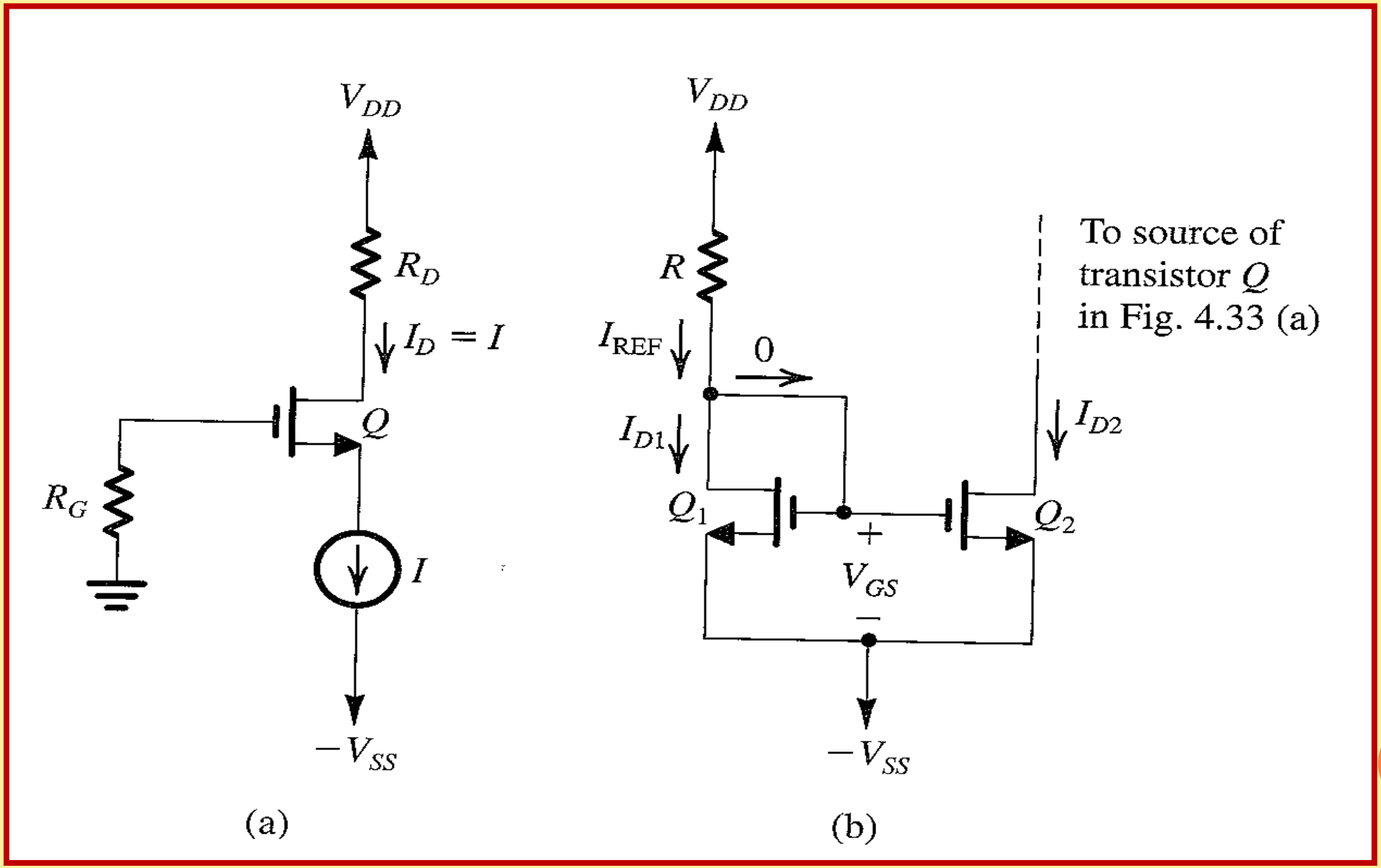
$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

$$V_{DD} = V_{GS} + R_D I_D$$

Thus the negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.

can be utilized as a CS amplifier by applying the input voltage signal to the gate via a coupling capacitor so as not to disturb the dc bias conditions already established. The amplified output signal at the drain can be coupled to another part of the circuit, again via a capacitor. We shall consider such a CS amplifier circuit in Section 4.6. There we will learn that this circuit has the drawback of a rather limited output voltage signal swing.

Fig 4.33(a) shows the biasing the MOSFET using a constant-current source *I*.(b) Implementation of the constant-current source *I* using a current mirror.



The most effective scheme for biasing a MOSFET amplifier is that using a constant-current source. Figure 4.33(a) shows such an arrangement applied to a discrete MOSFET. Here R_G (usually in the MΩ range) establishes a dc ground at the gate and presents a large resistance to an input signal source that can be capacitively coupled to the gate. Resistor R_D establishes an appropriate dc voltage at the drain to allow for the required output signal swing while ensuring that the transistor always remains in the saturation region.

A circuit for implementing the constant-current source I is shown in Fig. 4.33(b). The heart of the circuit is transistor Q_1, whose drain is shorted to its gate and thus is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2}k'_n\left(\frac{W}{L}\right)_1(V_{GS}-V_t)^2 \tag{4.50}$$

where we have neglected channel-length modulation (i.e., assumed $\lambda = 0$). The drain current of Q_1 is supplied by V_{DD} through resistor R. Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD}+V_{SS}-V_{GS}}{R} \tag{4.51}$$

where the current through R is considered to be the *reference current* of the current source and is denoted I_{REF}. Given the parameter values of Q_1 and a desired value for I_{REF}, Eqs. (4.50) and (4.51) can be used to determine the value of R. Now consider transistor Q_2: It has the same V_{GS} as Q_1; thus if we assume that it is operating in saturation, its drain current, which is the desired current I of the current source, will be

$$I = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2(V_{GS} - V_t)^2 \tag{4.52}$$

where we have neglected channel-length modulation. Equations (4.51) and (4.52) enable us to relate the current I to the reference current I_{REF},

$$I = I_{REF}\frac{(W/L)_2}{(W/L)_1} \tag{4.53}$$

Thus I is related to I_{REF} by the ratio of the aspect ratios of Q_1 and Q_2. This circuit, known as a **current mirror,** is very popular in the design of IC MOS amplifiers and will be studied in great detail in Chapter 6.