

BJT AC Analysis

AMPLIFICATION IN THE AC DOMAIN

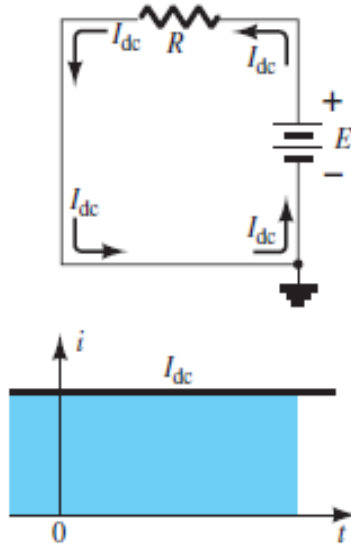


FIG. 5.1

Steady current established by a dc supply.

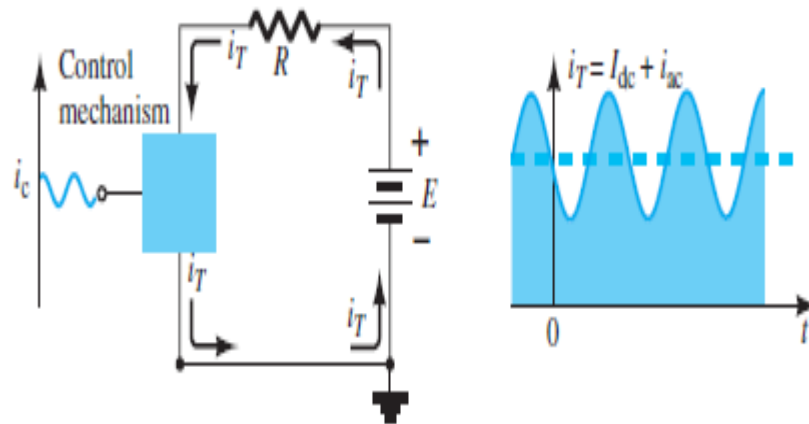


FIG. 5.2

Effect of a control element on the steady-state flow of the electrical system of Fig. 5.1.

$$i_{ac(p-p)} \gg i_c(p-p)$$

The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

BJT TRANSISTOR MODELING

A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

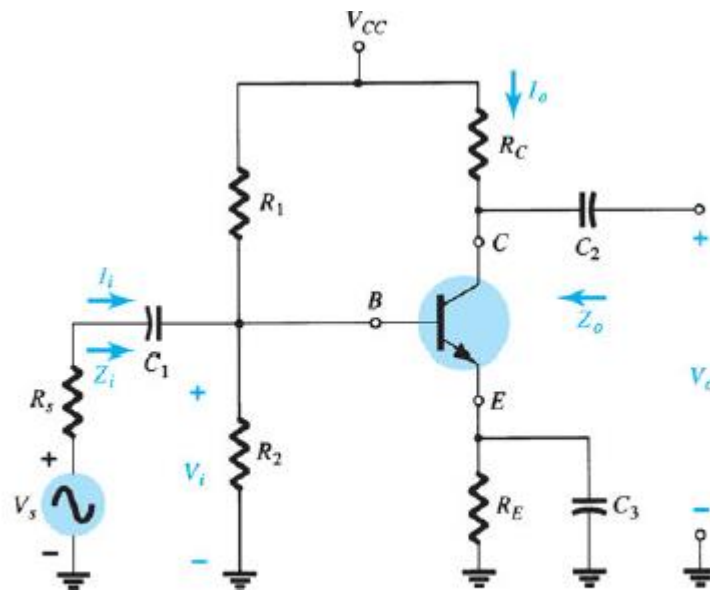


FIG. 5.3

Electronic Devices and circuits Nashelsky
and Boylestad

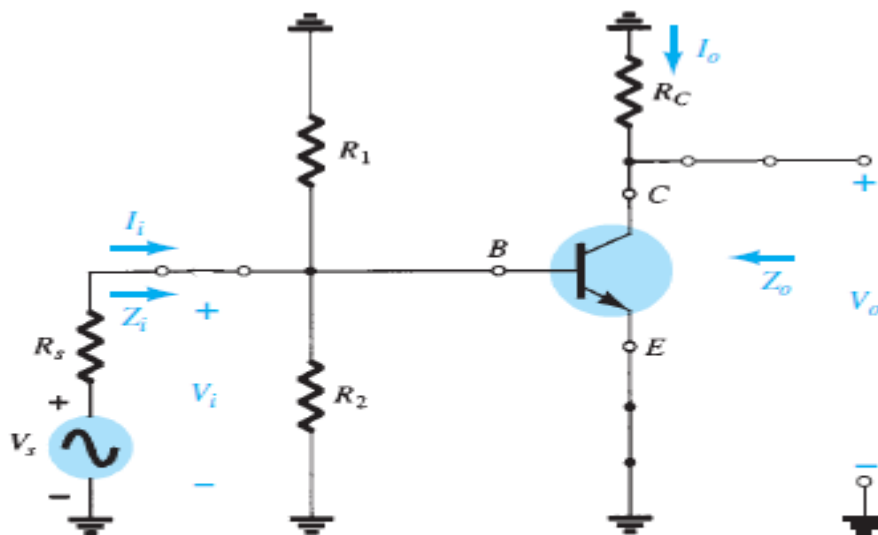


FIG. 5.4

The network of Fig. 5.3 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

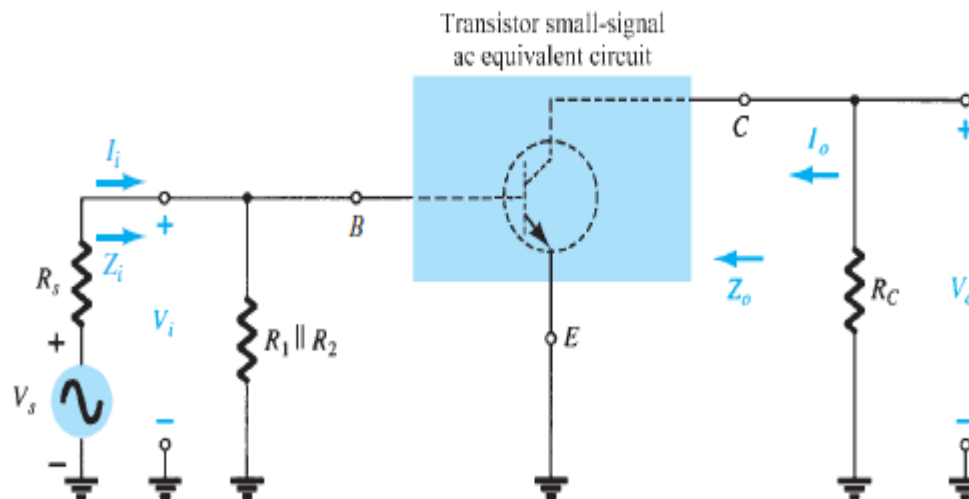


FIG. 5.7

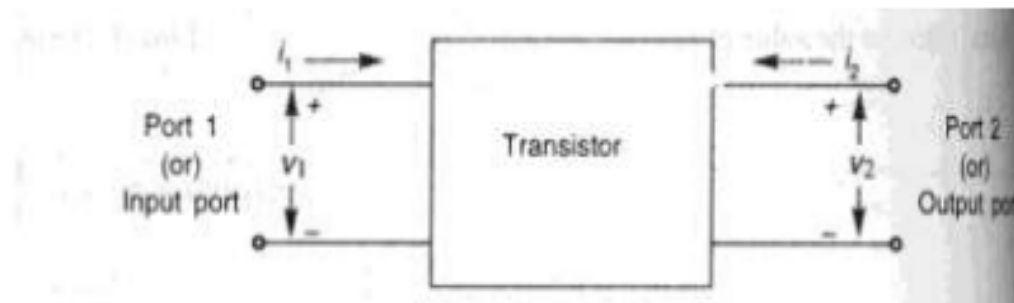
Circuit of Fig. 5.4 redrawn for small-signal ac analysis.

Electronic Devices and circuits Nashelsky and Boylestad

1. *Setting all dc sources to zero and replacing them by a short-circuit equivalent*
2. *Replacing all capacitors by a short-circuit equivalent*
3. *Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2*
4. *Redrawing the network in a more convenient and logical form*

Two port devices & Network Parameters:-

A transistor can be treated as a two part network. The terminal behavior of any two part network can be specified by the terminal voltages V_1 & V_2 at parts 1 & 2 respectively and current i_1 and i_2 , entering parts 1 & 2, respectively, as shown in figure.



Two port network

Of these four variables V_1 , V_2 , i_1 and i_2 , two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This leads to various two part parameters out of which the following three are more important.

Hybrid parameters (or) h – parameters:-

→ If the input current i_1 and output Voltage V_2 are taken as independent variables, the input voltage V_1 and output current i_2 can be written as

$$\begin{aligned} V_1 &= h_{11} i_1 + h_{12} V_2 \\ i_2 &= h_{21} i_1 + h_{22} V_2 \end{aligned}$$

The four hybrid parameters h_{11} , h_{12} , h_{21} and h_{22} are defined as follows.

$$h_{11} = [V_1 / i_1] \text{ with } V_2 = 0$$

= Input Impedance with output part short circuited.

$$h_{22} = [i_2 / V_2] \text{ with } i_1 = 0$$

= Output admittance with input part open circuited.

$$h_{12} = [V_1 / V_2] \text{ with } i_1 = 0$$

= reverse voltage transfer ratio with input part open circuited.

$$h_{21} = [i_2 / i_1] \text{ with } V_2 = 0$$

= Forward current gain with output part short circuited.

The dimensions of h – parameters are as follows:

h_{11} - Ω

h_{22} – mhos

h_{12} , h_{21} – dimension less.

→ as the dimensions are not alike, (ie) they are hybrid in nature, and these parameters are called as hybrid parameters.

$I = 11 = \text{input} ; 0 = 22 = \text{output} ;$

$F = 21 = \text{forward transfer} ; r = 12 = \text{Reverse transfer}.$

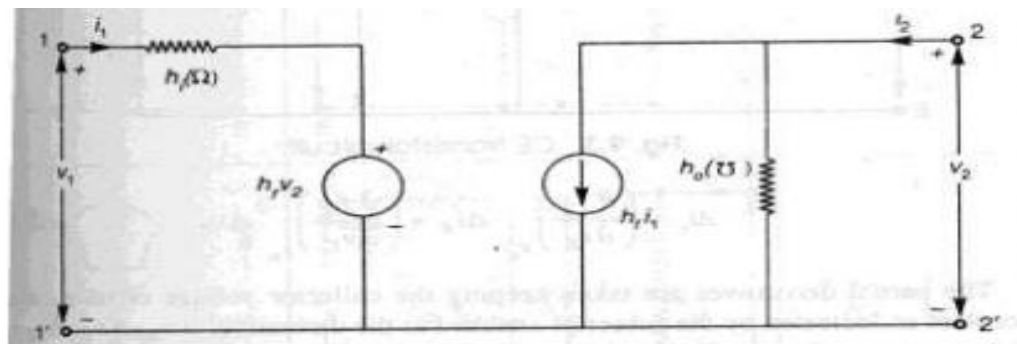
Notations used in transistor circuits:-

$h_{ie} = h_{11e} = \text{Short circuit input impedance}$

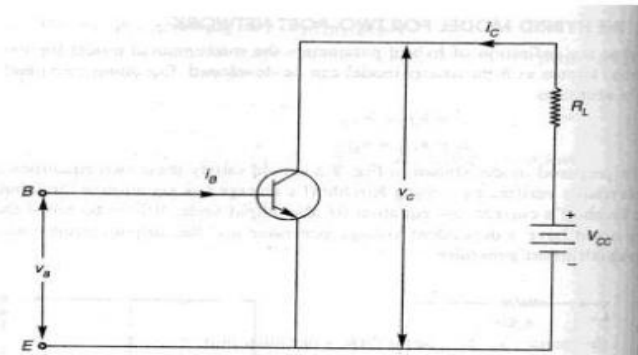
$h_{oe} = h_{22e} = \text{Open circuit output admittance}$

$h_{re} = h_{12e} = \text{Open circuit reverse voltage transfer ratio}$

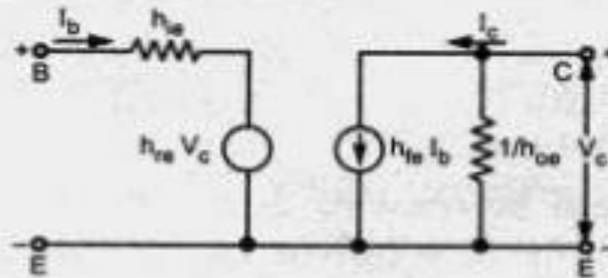
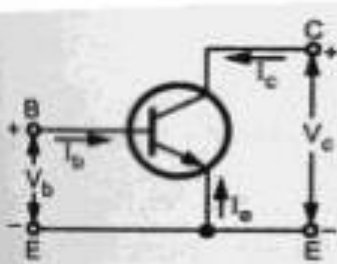
$h_{fe} = h_{21e} = \text{Short circuit forward current Gain}.$



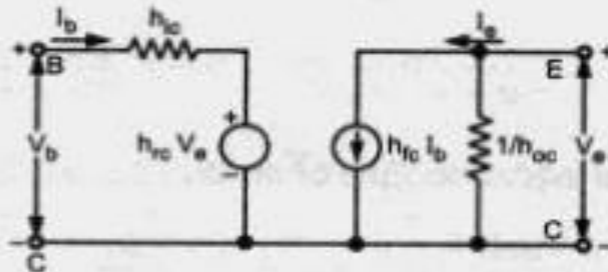
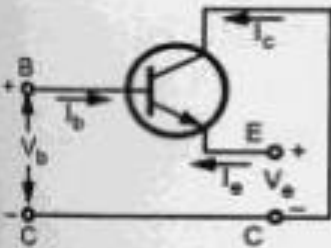
The Hybrid Model for Two-port Network



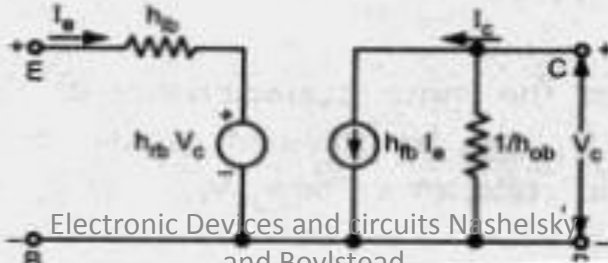
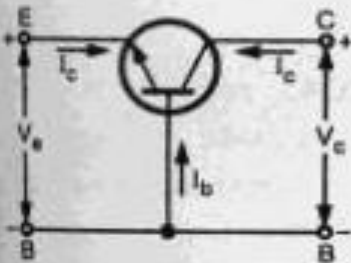
CE Transistor Circuit



CE
 $V_b = h_{ie} I_b + h_{re} V_c$
 $I_c = h_{fe} I_b + h_{oe} V_c$



CC
 $V_b = h_{ic} I_b + h_{rc} V_e$
 $I_e = h_{fc} I_b + h_{oc} V_e$



CB
 $V_e = h_{ib} I_e + h_{rb} V_c$
 $I_c = h_{fb} I_e + h_{ob} V_c$

THE r_e TRANSISTOR MODEL

Common-Emitter Configuration

The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage V_i is equal to the voltage V_{be} with the input current being the base current I_b as shown in Fig. 5.8.

Recall from Chapter 3 that because the current through the forward-biased junction of the transistor is I_E , the characteristics for the input side appear as shown in Fig. 5.9a for various levels of V_{BE} . Taking the average value for the curves of Fig. 5.9a will result in the single curve of Fig. 5.9b, which is simply that of a forward-biased diode.

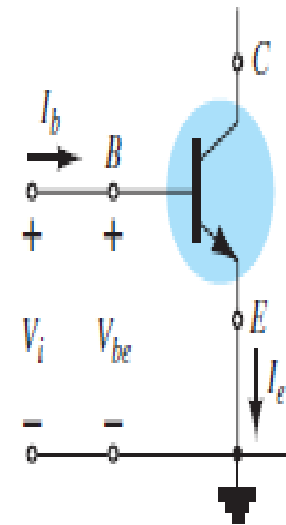


FIG. 5.8

Finding the input equivalent circuit for a BJT transistor.

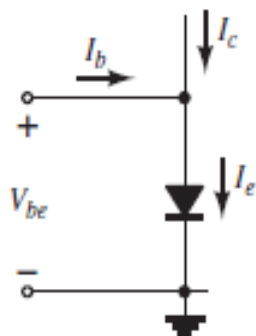


FIG. 5.10

Equivalent circuit for the input side of a BJT transistor.

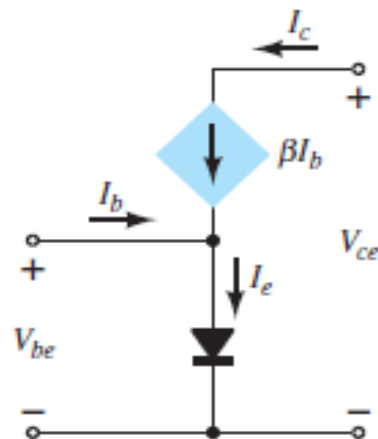


FIG. 5.12

BJT equivalent circuit.

$$r_D = 26 \text{ mV} / I_D.$$

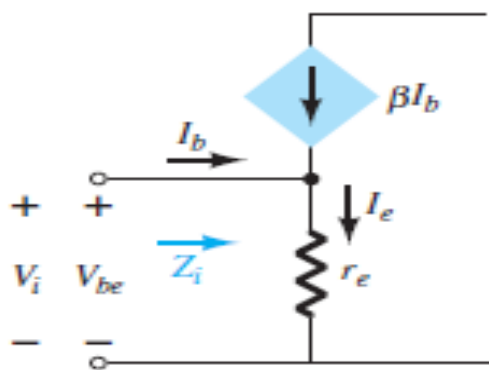


FIG. 5.13

Defining the level of Z_i .

$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

$$\begin{aligned} V_{be} &= I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e \\ &= (\beta + 1) I_b r_e \end{aligned}$$

$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b}$$

$$Z_i = (\beta + 1) r_e \cong \beta r_e$$

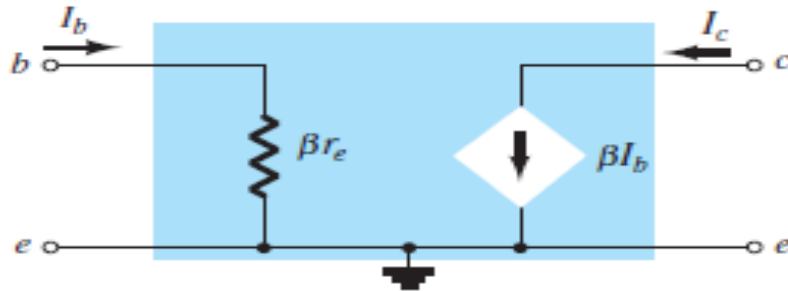


FIG. 5.14

Improved BJT equivalent circuit.

COMMON-EMITTER FIXED-BIAS CONFIGURATION

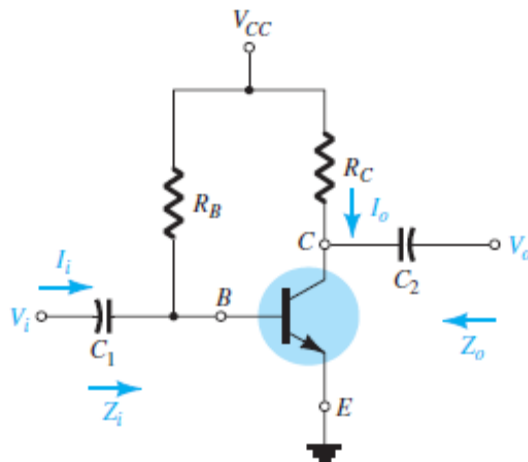


FIG. 5.20

Common-emitter fixed-bias configuration.

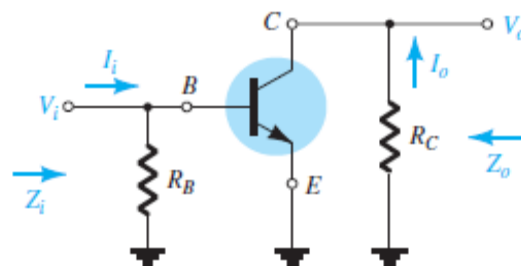


FIG. 5.21

Network of Fig. 5.20 following the removal of the effects of V_{CC} , C_1 , and C_2 .

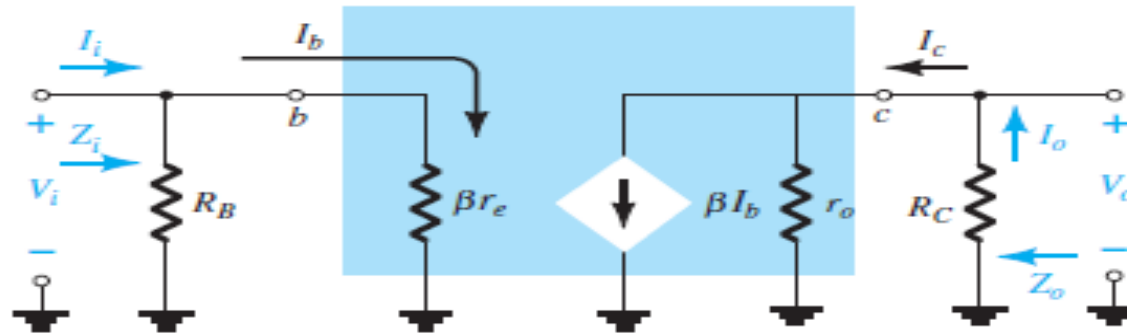


FIG. 5.22

Substituting the r_e model into the network of Fig. 5.21.

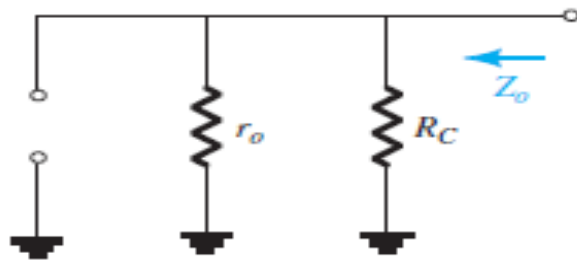
Z_i Figure 5.22 clearly shows that

$$Z_i = R_B \parallel \beta r_e \quad \text{ohms}$$

$$Z_i \cong \beta r_e \quad \text{ohms} \quad R_B \geq 10\beta r_e$$

Z_o Recall that the output impedance of any system is defined as the impedance Z_o determined when $V_i = 0$. For Fig. 5.22, when $V_i = 0$, $I_i = I_b = 0$, resulting in an open-circuit equivalence for the current source. The result is the configuration of Fig. 5.23. We have

$$Z_o = R_C \parallel r_o \quad \text{ohms} \quad (5.7)$$



$$Z_o = R_C \parallel r_o \text{ ohms}$$

FIG. 5.23

Determining Z_o for the network of Fig. 5.22.

If $r_o \geq 10R_C$, the approximation $R_C \parallel r_o \cong R_C$ is frequently applied, and

$$Z_o \cong R_C \quad r_o \geq 10R_C$$

A_v The resistors r_o and R_C are in parallel, and

$$V_o = -\beta I_b (R_C \parallel r_o)$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

so that

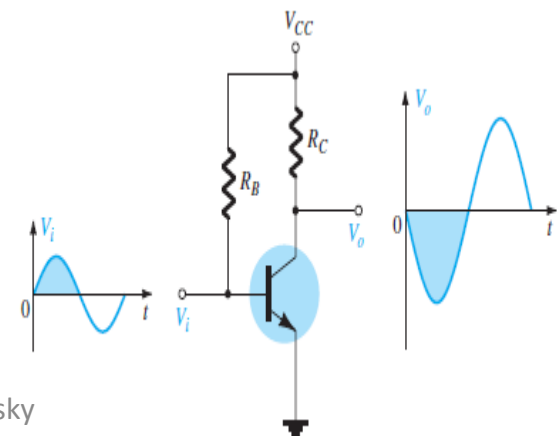
$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \parallel r_o)$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_o)}{r_e}$$

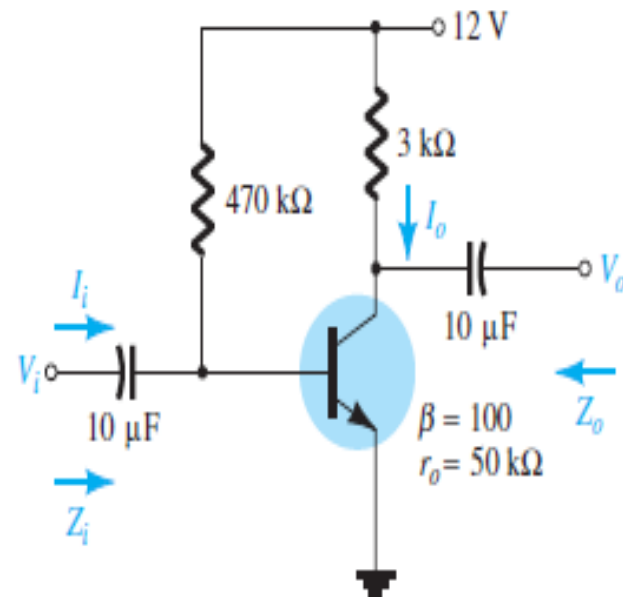
If $r_o \geq 10R_C$, so that the effect of r_o can be ignored,

$$A_v = -\frac{R_C}{r_e} \quad r_o \geq 10R_C$$



For the network of Fig. :

- Determine r_e .
- Find Z_i (with $r_o = \infty \Omega$).
- Calculate Z_o (with $r_o = \infty \Omega$).
- Determine A_v (with $r_o = \infty \Omega$).
- Repeat parts (c) and (d) including $r_o = 50 \text{ k}\Omega$ in all calculations and compare results.



a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega} = 24.04 \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04 \mu\text{A}) = 2.428 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.428 \text{ mA}} = \mathbf{10.71 \Omega}$$

b. $\beta r_e = (100)(10.71 \Omega) = 1.071 \text{ k}\Omega$

$$Z_i = R_B \parallel \beta r_e = 470 \text{ k}\Omega \parallel 1.071 \text{ k}\Omega = \mathbf{1.07 \text{ k}\Omega}$$

c. $Z_o = R_C = \mathbf{3 \text{ k}\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{3 \text{ k}\Omega}{10.71 \Omega} = \mathbf{-280.11}$

e. $Z_o = r_o \parallel R_C = 50 \text{ k}\Omega \parallel 3 \text{ k}\Omega = \mathbf{2.83 \text{ k}\Omega}$ vs. $3 \text{ k}\Omega$

$$A_v = -\frac{r_o \parallel R_C}{r_e} = \frac{2.83 \text{ k}\Omega}{10.71 \Omega} = \mathbf{-264.24}$$
 vs. -280.11

VOLTAGE-DIVIDER BIAS

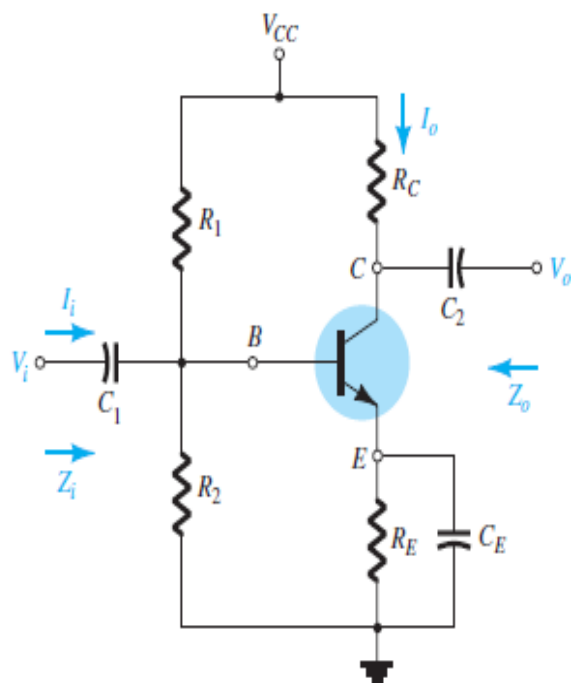


FIG. 5.26

Voltage-divider bias configuration.

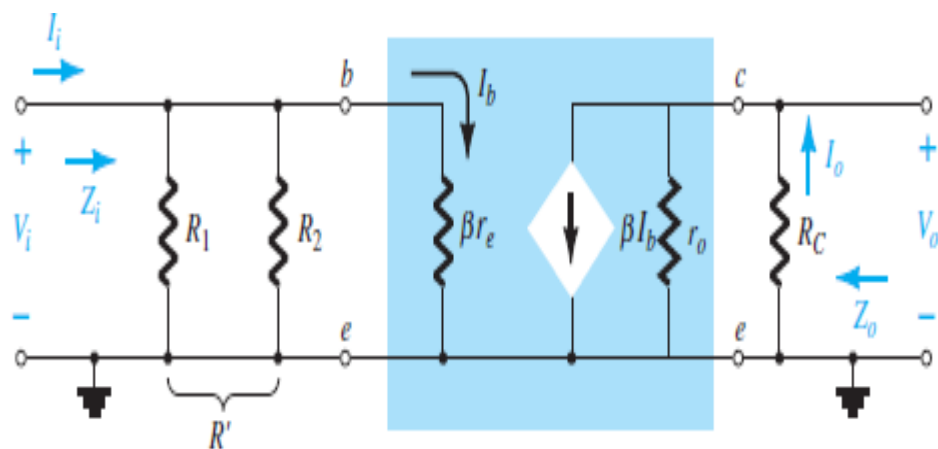


FIG. 5.27

Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.26.

$$R' = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Z_i From Fig. 5.27

$$Z_i = R' \parallel \beta r_e$$

Z_o From Fig. 5.27 with V_i set to 0 V, resulting in $I_b = 0 \mu\text{A}$ and $\beta I_b = 0 \text{ mA}$,

$$Z_o = R_C \parallel r_o \quad (5.13)$$

If $r_o \geq 10R_C$,

$$Z_o \cong R_C \quad r_o \geq 10R_C \quad (5.14)$$

A_v Because R_C and r_o are in parallel,

$$V_o = -(\beta I_b)(R_C \parallel r_o)$$

and

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \parallel r_o)$$

and

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \parallel r_o}{r_e} \quad (5.15)$$

which you will note is an exact duplicate of the equation obtained for the fixed-bias configuration.

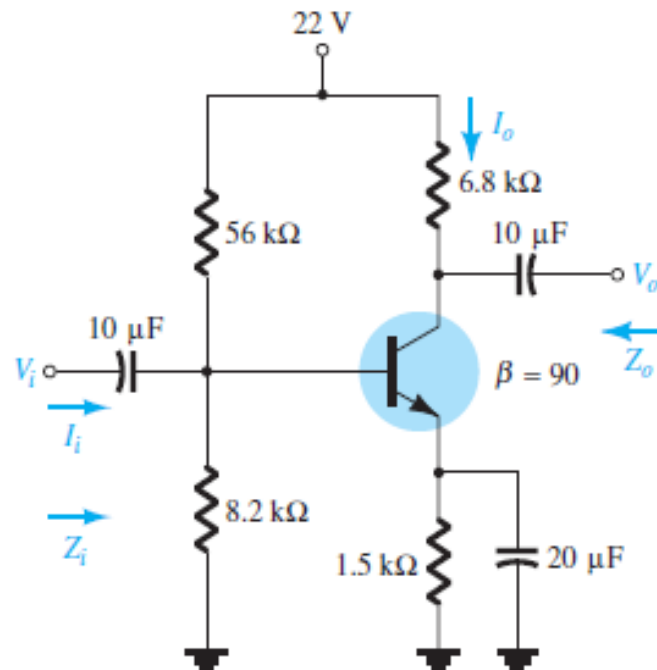
For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \quad r_o \geq 10R_C \quad (5.16)$$

Phase Relationship The negative sign of Eq. (5.15) reveals a 180° phase shift between V_o and V_i .

For the network of Fig. 4

- r_e .
- Z_i .
- Z_o ($r_o = \infty \Omega$).
- A_v ($r_o = \infty \Omega$).
- The parameters of parts (b) through (d) if $r_o = 50 \text{ k}\Omega$ and compare results.



a. DC: Testing $\beta R_E > 10R_2$,

$$(90)(1.5 \text{ k}\Omega) > 10(8.2 \text{ k}\Omega)$$

$$135 \text{ k}\Omega > 82 \text{ k}\Omega \text{ (satisfied)}$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2 \text{ k}\Omega)(22 \text{ V})}{56 \text{ k}\Omega + 8.2 \text{ k}\Omega} = 2.81 \text{ V}$$

$$V_E = V_B - V_{BE} = 2.81 \text{ V} - 0.7 \text{ V} = 2.11 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11 \text{ V}}{1.5 \text{ k}\Omega} = 1.41 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{1.41 \text{ mA}} = 18.44 \text{ }\Omega$$

b. $R' = R_1 \parallel R_2 = (56 \text{ k}\Omega) \parallel (8.2 \text{ k}\Omega) = 7.15 \text{ k}\Omega$

$$Z_i = R' \parallel \beta r_e = 7.15 \text{ k}\Omega \parallel (90)(18.44 \text{ }\Omega) = 7.15 \text{ k}\Omega \parallel 1.66 \text{ k}\Omega$$
$$= 1.35 \text{ k}\Omega$$

c. $Z_o = R_C = 6.8 \text{ k}\Omega$

d. $A_v = -\frac{R_C}{r_e} = -\frac{6.8 \text{ k}\Omega}{18.44 \text{ }\Omega} = -368.76$

e. $Z_i = 1.35 \text{ k}\Omega$

$$Z_o = R_C \parallel r_o = 6.8 \text{ k}\Omega \parallel 50 \text{ k}\Omega = 5.98 \text{ k}\Omega \text{ vs. } 6.8 \text{ k}\Omega$$

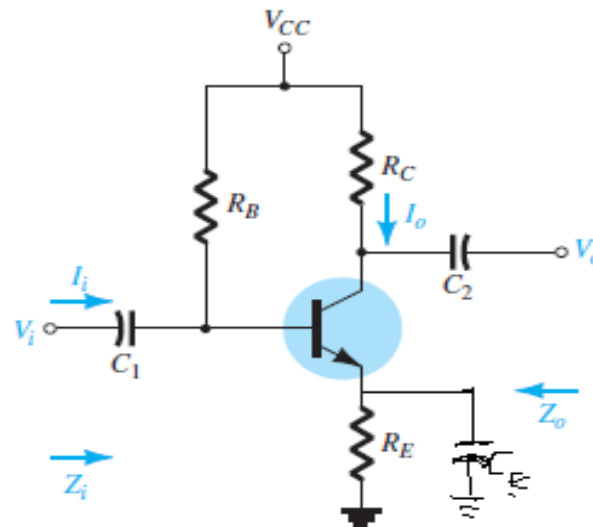
$$A_v = -\frac{R_C \parallel r_o}{r_e} = -\frac{5.98 \text{ k}\Omega}{18.44 \text{ }\Omega} = -324.3 \text{ vs. } -368.76$$

There was a measurable difference in the results for Z_o and A_v , because the condition $r_o \geq 10R_C$ was *not* satisfied.

CE EMITTER-BIAS CONFIGURATION

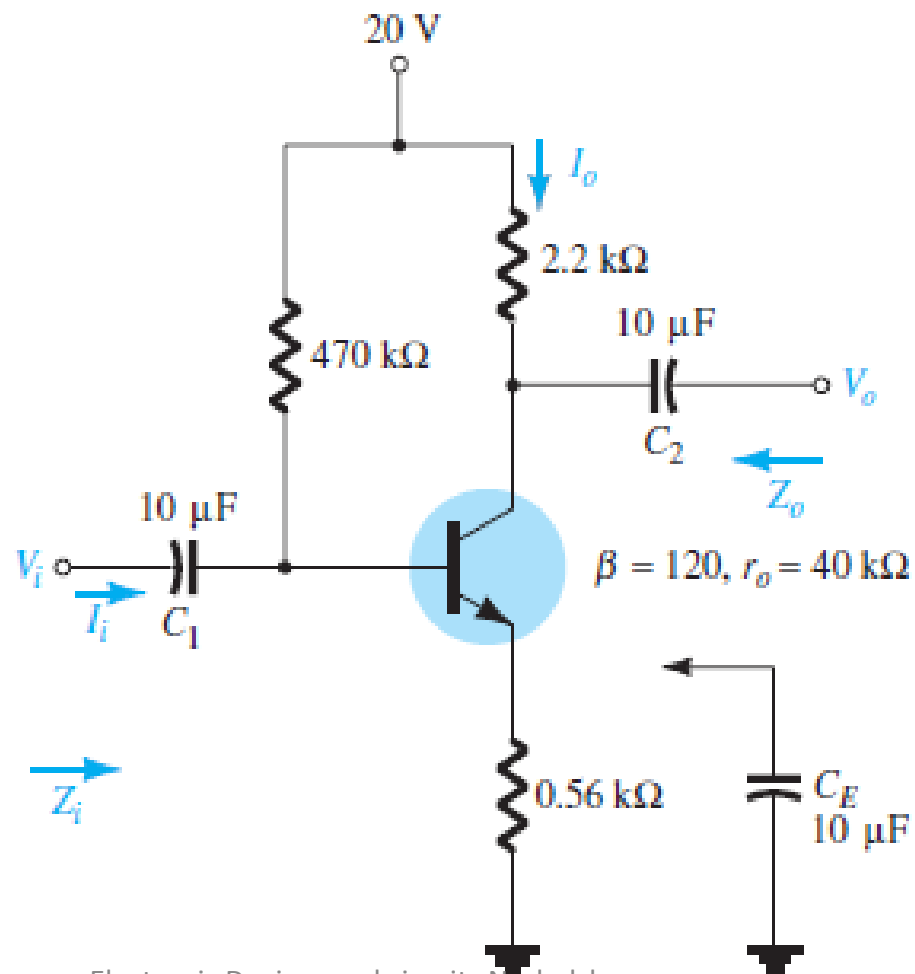
Bypassed

If R_E of Fig. 5.29 is bypassed by an emitter capacitor C_E , the complete r_e equivalent model can be substituted, resulting in the same equivalent network as Fig. 5.22. Equations (5.5) to (5.10) are therefore applicable.



For the network of Fig. :

- a. r_e .
- b. Z_i .
- c. Z_o .
- d. A_v .



a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega + (121)0.56 \text{ k}\Omega} = 35.89 \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89 \mu\text{A}) = 4.34 \text{ mA}$$

and $r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{4.34 \text{ mA}} = 5.99 \Omega$

b. R_E is “shorted out” by C_E for the ac analysis. Therefore,

$$\begin{aligned} Z_i &= R_B \parallel Z_b = R_B \parallel \beta r_e = 470 \text{ k}\Omega \parallel (120)(5.99 \Omega) \\ &= 470 \text{ k}\Omega \parallel 718.8 \Omega \cong 717.70 \Omega \end{aligned}$$

c. $Z_o = R_C = 2.2 \text{ k}\Omega$

$$\begin{aligned} \text{d. } A_v &= -\frac{R_C}{r_e} \\ &= -\frac{2.2 \text{ k}\Omega}{5.99 \Omega} = -367.28 \text{ (a significant increase)} \end{aligned}$$